

NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE01P13K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

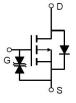
General Features

- V_{DS} =-100V, I_{D} =-13A $R_{DS(ON)}$ <200mΩ @ V_{GS} =-10V (Typ:170mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density celldesign for ultra low on-resistance

Application

- Power switch
- DC/DC converters

100% UIS TESTED! 100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|----------------|-----------|----------------|-----------|------------|------------|
| NCE01P13K | NCE01P13K | TO-252-2L | Ø330mm | 16mm | 2500 units |

Absolute Maximum Ratings (T_c=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|-----------------------|------------|------------|
| Drain-Source Voltage | V _{DS} | -100 | V |
| Gate-Source Voltage | V _G s | ±20 | V |
| Drain Current-Continuous | I _D | -13 | А |
| Drain Current-Continuous(Tc=100℃) | I _D (100℃) | -9.2 | А |
| Pulsed Drain Current | I _{DM} | -52 | Α |
| Maximum Power Dissipation | P _D | 40 | W |
| Derating factor | | 0.27 | W/℃ |
| Single pulse avalanche energy (Note 5) | E _{AS} | 80 | mJ |
| Operating Junction and Storage Temperature Range | T_{J}, T_{STG} | -55 To 175 | $^{\circ}$ |

Thermal Characteristic

| Thermal Resistance,Junction-to-Case (Note 2) | R _{θJc} | 3.75 | °C/W |
|--|------------------|------|------|
|--|------------------|------|------|



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Electrical Characteristics (T_c=25°C unless otherwise noted)

| Parameter | Symbol | Condition | Min | Тур | Max | Unit |
|------------------------------------|---|--|----------|------|------|------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | Source Breakdown Voltage BV _{DSS} V _{GS} =0V I _D =-250µA | | -100 | - | - | V |
| Zero Gate Voltage Drain Current | te Voltage Drain Current I _{DSS} V _{DS} =-100V,V _{GS} =0V | | - | - | 1 | μA |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} =±20V,V _{DS} =0V | - | - | ±10 | μA |
| On Characteristics (Note 3) | | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} ,I _D =-250μA | -1 | -1.9 | -3 | V |
| Drain-Source On-State Resistance | R _{DS(ON)} | V _{GS} =-10V, I _D =-10A | - | 170 | 200 | mΩ |
| Forward Transconductance | g FS | V _{DS} =-20V,I _D =-10A | - | 19 | - | S |
| Dynamic Characteristics (Note4) | | | • | • | | |
| Input Capacitance | C _{lss} | \/ 50\/\/ 0\/ | - | 1491 | - | PF |
| Output Capacitance | Coss | V _{DS} =-50V,V _{GS} =0V, | - | 47.5 | - | PF |
| Reverse Transfer Capacitance | C _{rss} | F=1.0MHz | - | 41.8 | - | PF |
| Switching Characteristics (Note 4) | | | ' | • | | |
| Turn-on Delay Time | t _{d(on)} | | - | 12 | - | nS |
| Turn-on Rise Time | t _r | V _{DD} =-50V,I _D =-10A | - | 52 | - | nS |
| Turn-Off Delay Time | t _{d(off)} | V _{GS} =-10V,R _{GEN} =9.1Ω | - | 28 | - | nS |
| Turn-Off Fall Time | t _f | | - | 38 | - | nS |
| Total Gate Charge | Qg |)/ 50)/I 40A | - | 32.5 | - | nC |
| Gate-Source Charge | Q _{gs} | V _{DS} =-50V,I _D =-10A, V _{GS} =-10V | - | 5.2 | - | nC |
| Gate-Drain Charge | Q _{gd} | V _{GS} 10V | - | 6.5 | - | nC |
| Drain-Source Diode Characteristics | | | | • | | |
| Diode Forward Voltage (Note 3) | V _{SD} | V _{GS} =0V,I _S =-10A | - | - | -1.2 | V |
| Diode Forward Current (Note 2) | Is | - | - | - | -13 | Α |
| Reverse Recovery Time | t _{rr} | TJ = 25°C, IF =-10A | - | 35 | - | nS |
| Reverse Recovery Charge | Qrr | di/dt = 100A/µs ^(Note3) | - | 46 | - | nC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

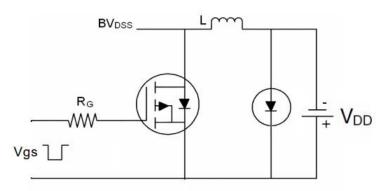
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300μ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E_{AS} condition: Tj=25 $^{\circ}$ C,V_{DD}=-50V,V_G=-10V,L=0.5mH,Rg=25 Ω

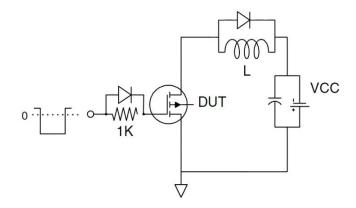


Test Circuit

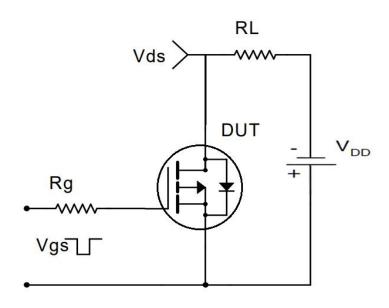
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

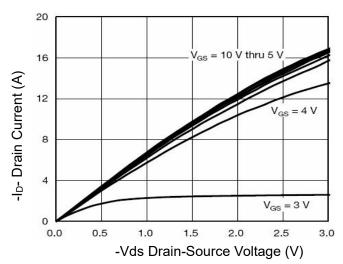


Figure 1 Output Characteristics

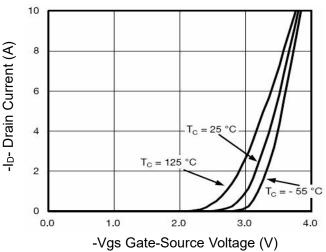


Figure 2 Transfer Characteristics

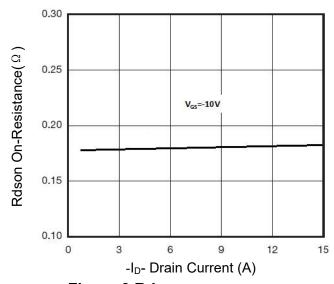


Figure 3 Rdson- Drain Current

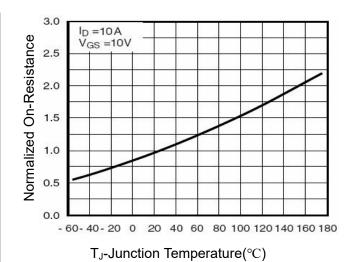


Figure 4 Rdson-JunctionTemperature

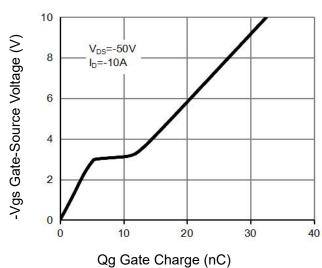


Figure 5 Gate Charge

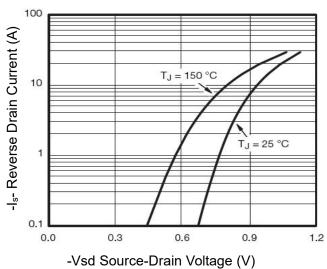


Figure 6 Source- Drain Diode Forward



C Capacitance (nF)

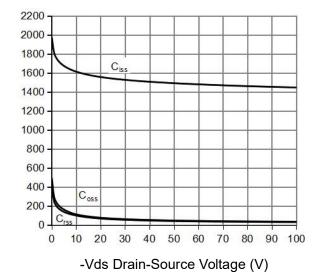


Figure 7 Capacitance vs Vds

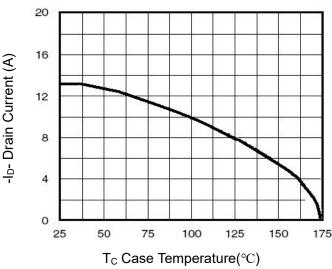


Figure 9 Drain Current vs Case Temperature

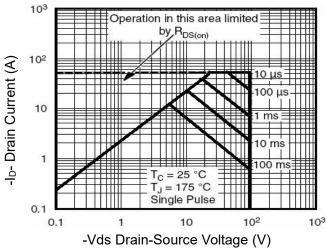


Figure 8 Safe Operation Area

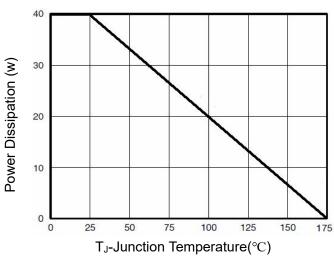


Figure 10 Power De-rating

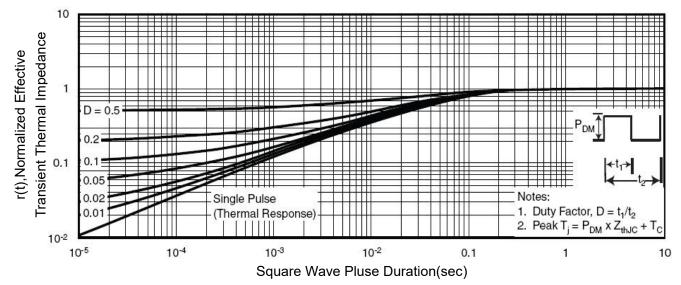
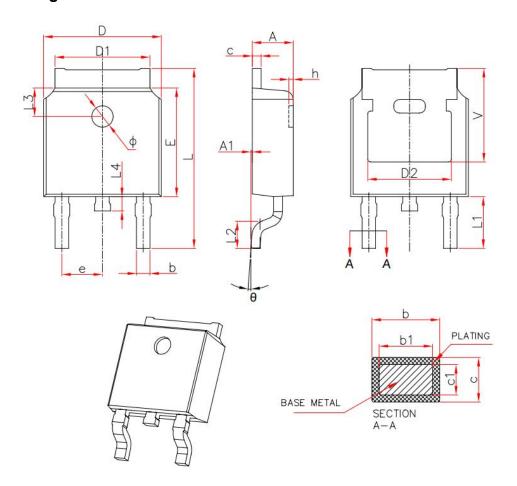


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252-2L Package Information



| Symbol | Millimeters | | | |
|--------|-------------|-------|--|--|
| | Min. | Max. | | |
| Α | 2.20 | 2.40 | | |
| A1 | 0.00 | 0.13 | | |
| b | 0.66 | 0.86 | | |
| b1 | 0.73 | 0.79 | | |
| С | 0.46 | 0.58 | | |
| c1 | 0.50 | 0.52 | | |
| D | 6.50 | 6.70 | | |
| D1 | 5.10 | 5.46 | | |
| D2 | 4.83 REF. | | | |
| E | 6.00 | 6.20 | | |
| е | 2.19 | 2.39 | | |
| L | 9.80 | 10.40 | | |
| L1 | 2.90 REF. | | | |
| L2 | 1.40 | 1.70 | | |
| L3 | 1.60 REF. | | | |
| L4 | 0.60 | 1.00 | | |
| Ф | 1.10 | 1.30 | | |
| θ | 0° | 8° | | |
| h | 0.00 | 0.30 | | |
| V | 5.35 REF. | | | |

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NCE01P13K

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