

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP01T13AD uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

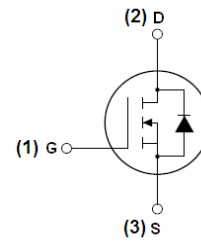
- $V_{DS} = 100V, I_D = 130A$
 $R_{DS(ON)} < 4.6m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP01T13AD	NCEP01T13AD	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	143	A
Drain Current-Continuous (Package Limited)	I_D	135	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	102	A
Pulsed Drain Current	I_{DM}	500	A
Maximum Power Dissipation	P_D	210	W
Derating factor		1.4	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1050	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.71	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

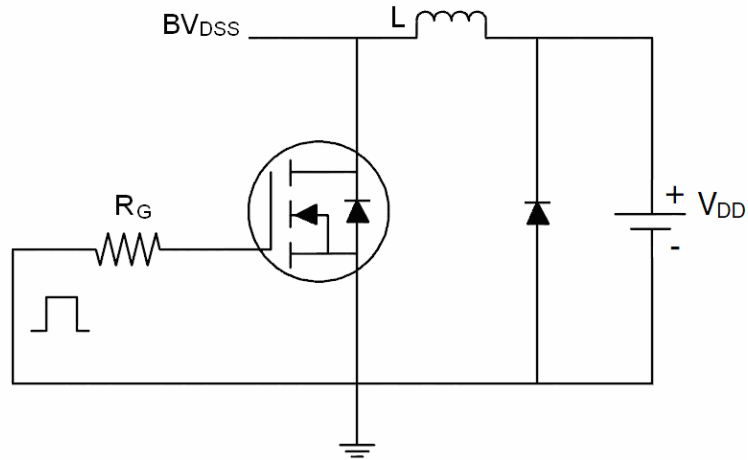
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5		4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=60A$	-	3.8	4.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=60A$	-	60	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	6400	-	PF
Output Capacitance	C_{oss}		-	731	-	PF
Reverse Transfer Capacitance	C_{rss}		-	35	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=60A$ $V_{GS}=10V, R_G=4.7\Omega$	-	19	-	nS
Turn-on Rise Time	t_r		-	76	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	nS
Turn-Off Fall Time	t_f		-	14	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=60A,$ $V_{GS}=10V$	-	92		nC
Gate-Source Charge	Q_{gs}		-	35.4		nC
Gate-Drain Charge	Q_{gd}		-	18.8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=135A$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	135	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu S$ ^(Note 3)	-	63		nS
Reverse Recovery Charge	Q_{rr}		-	142		nC

Notes:

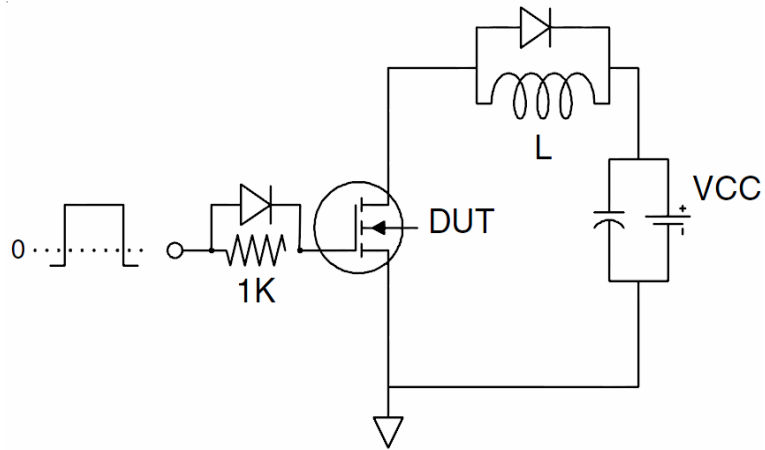
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

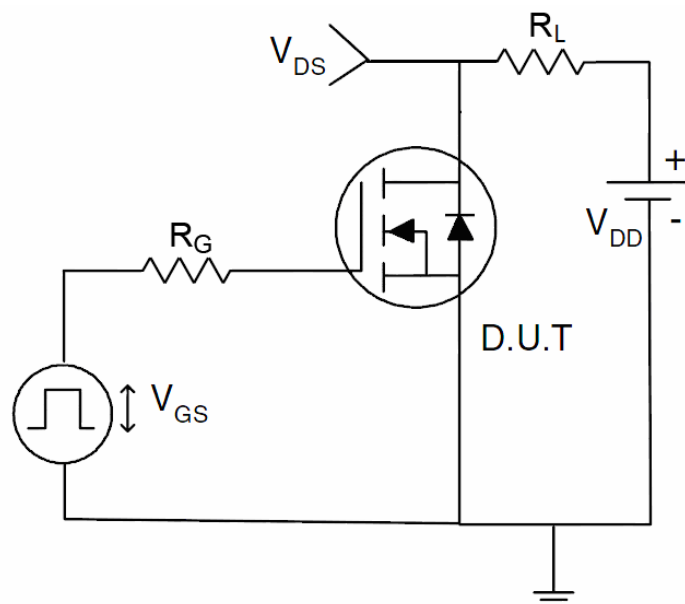
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

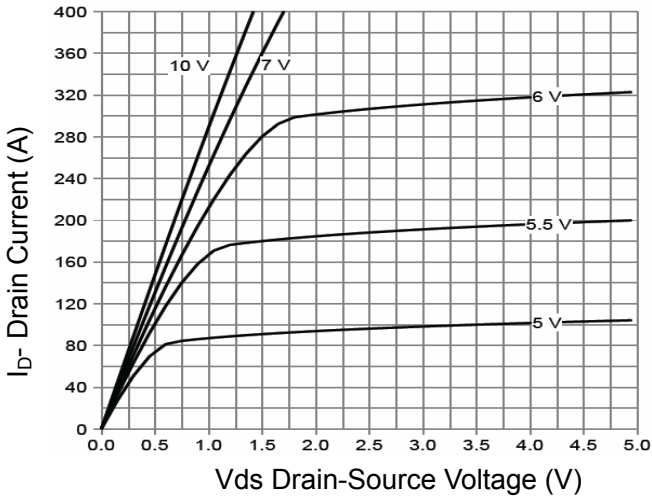


Figure 1 Output Characteristics

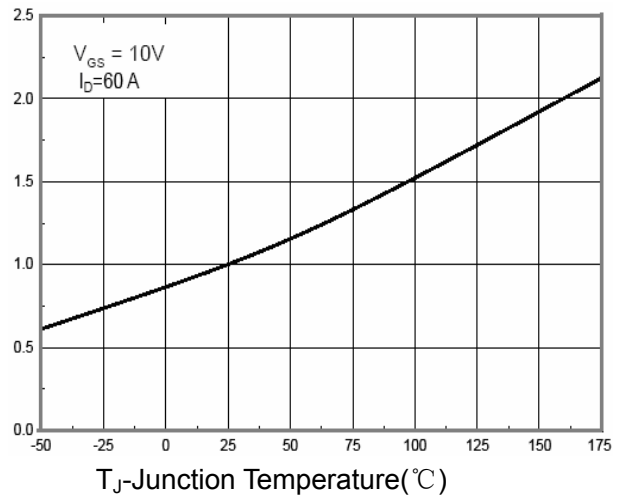


Figure 4 $R_{DS(on)}$ -Junction Temperature

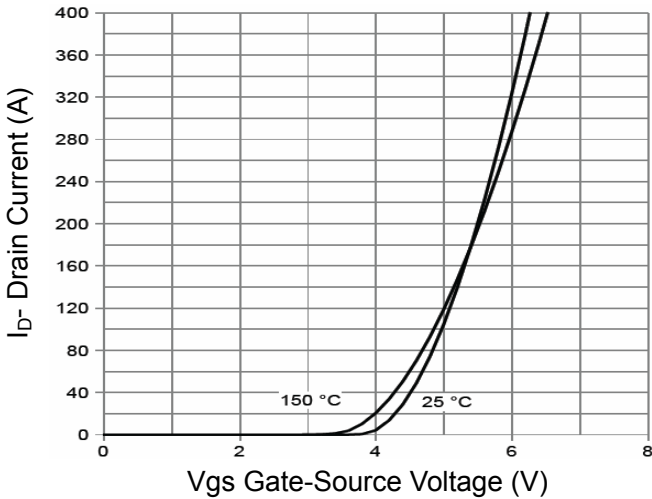


Figure 2 Transfer Characteristics

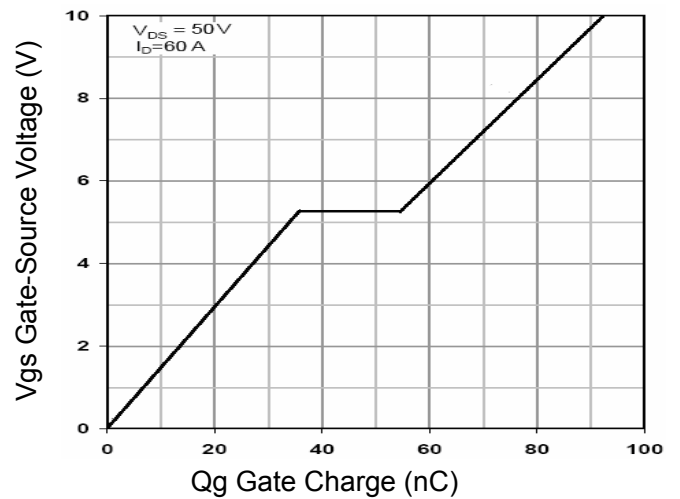


Figure 5 Gate Charge

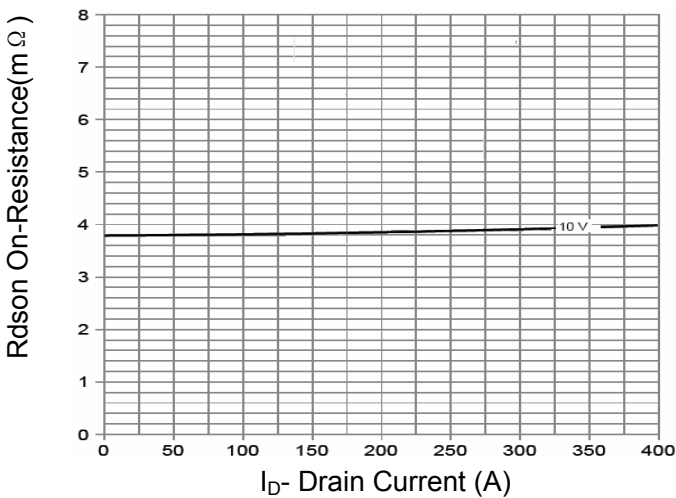


Figure 3 $R_{DS(on)}$ - Drain Current

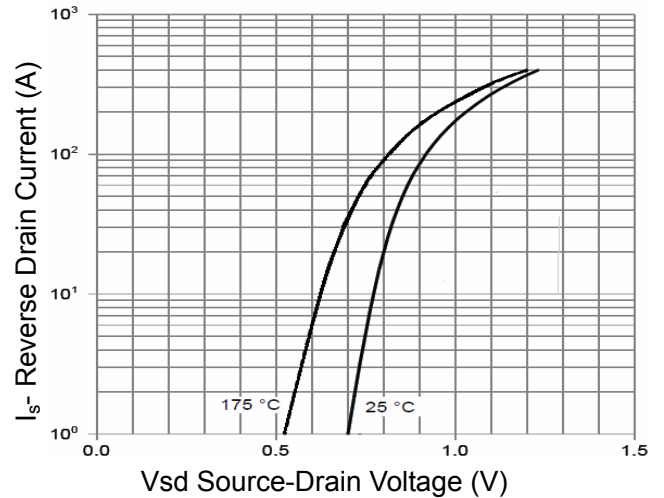


Figure 6 Source- Drain Diode Forward

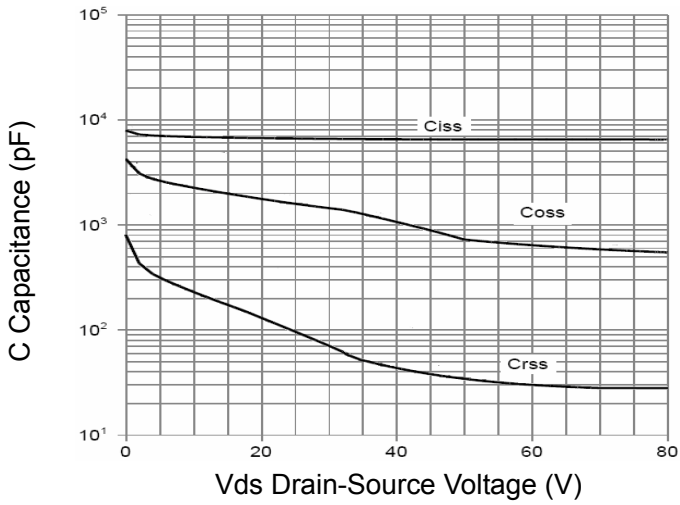


Figure 7 Capacitance vs Vds

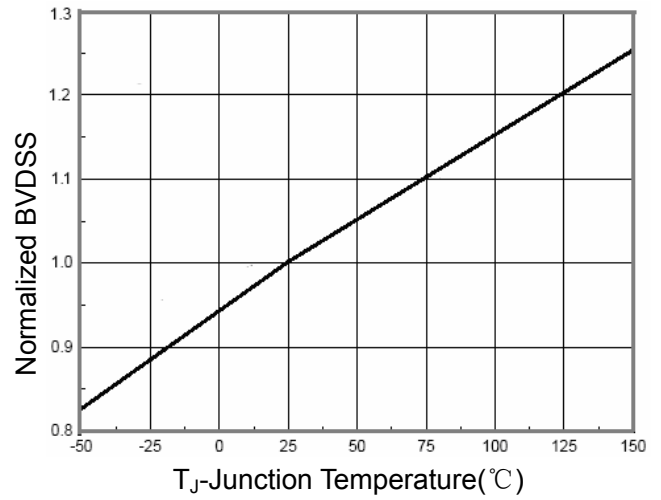


Figure 9 BV_{DSS} vs Junction Temperature

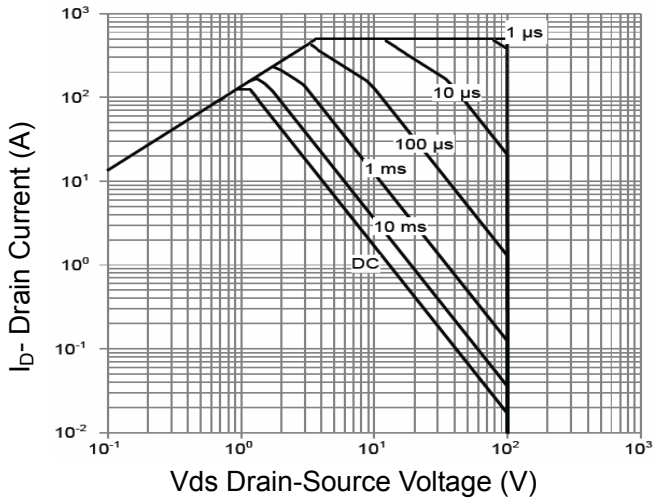


Figure 8 Safe Operation Area

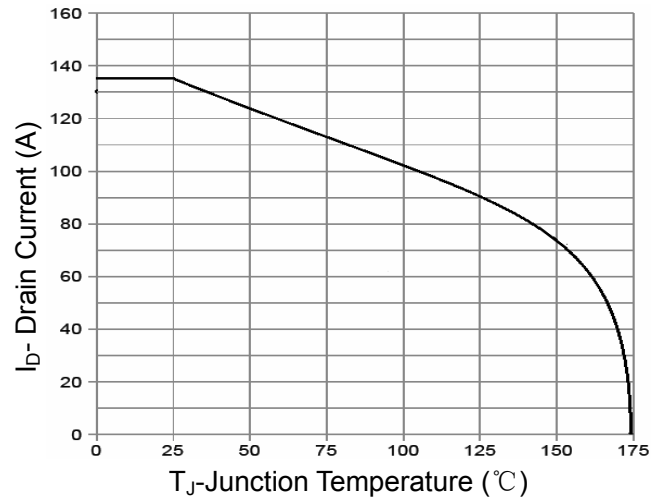


Figure 10 Current De-rating

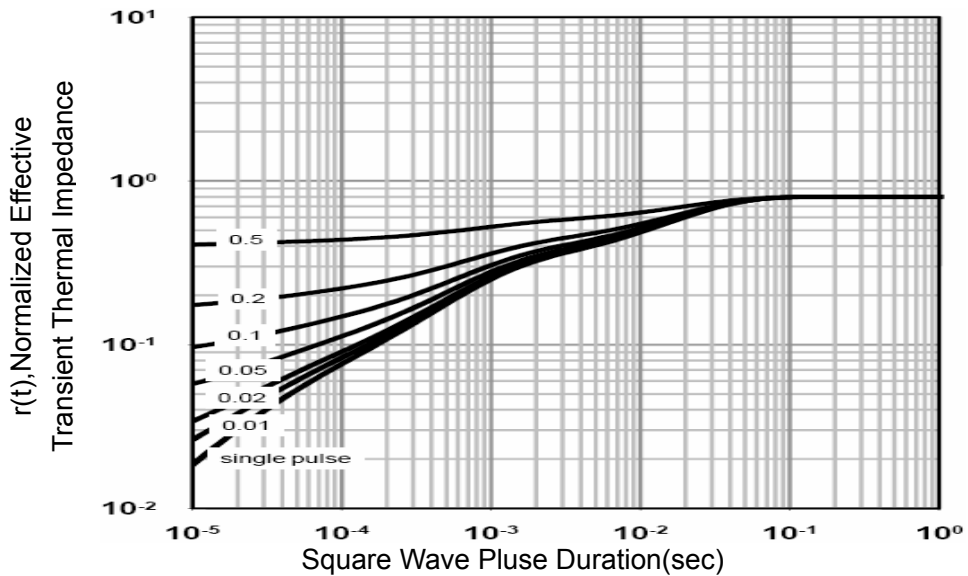
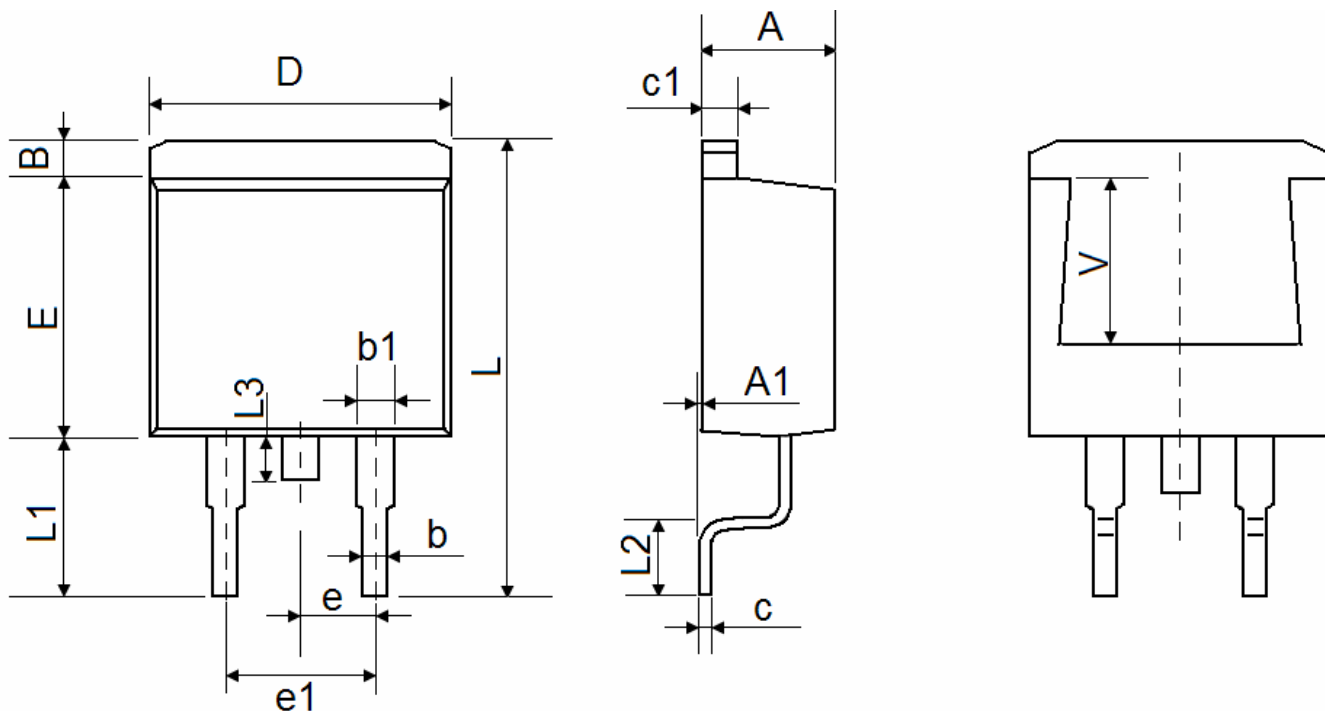


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF		0.220 REF	

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