NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE0140I2 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

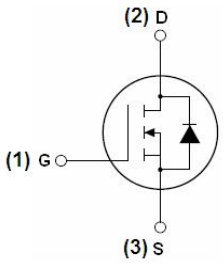
- V_{DS} = 100V,I_D =40A
  $R_{DS(ON)}$ < 15mΩ @ V_{GS}=10V (Typ:13mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

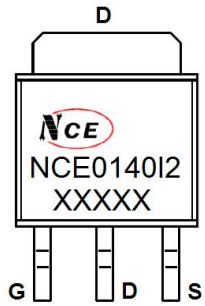
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

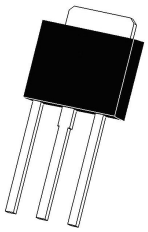
100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-251 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0140I2	NCE0140I2	TO-251	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	40	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	28	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	140	W
Derating factor	-	0.94	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	520	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.07	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

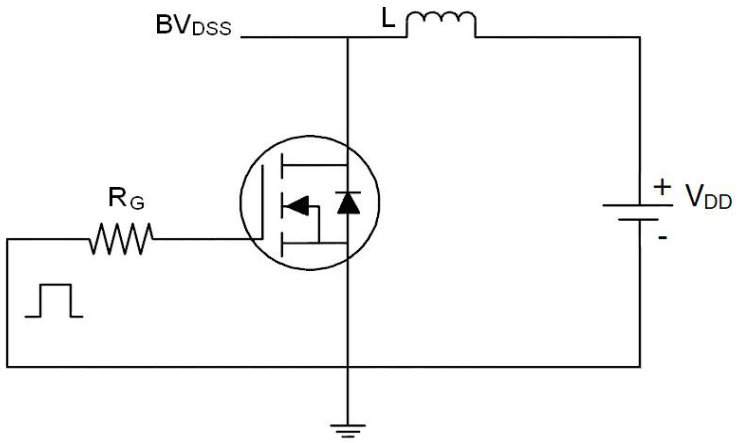
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=28A	-	13	15	mΩ
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=28A	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	3400	-	PF
Output Capacitance	C_{oss}		-	290	-	PF
Reverse Transfer Capacitance	C_{rss}		-	221	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	VDD=30V,ID=2A,RL=15Ω, RG=2.5Ω,VGS=10V	-	15	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g	ID=30A,VDD=30V,VGS=10V	-	94	-	nC
Gate-Source Charge	Q_{gs}		-	16	-	nC
Gate-Drain Charge	Q_{gd}		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=28A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	40	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 28A di/dt = 100A/μs (Note3)	-	33		nS
Reverse Recovery Charge	Qrr		-	54		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

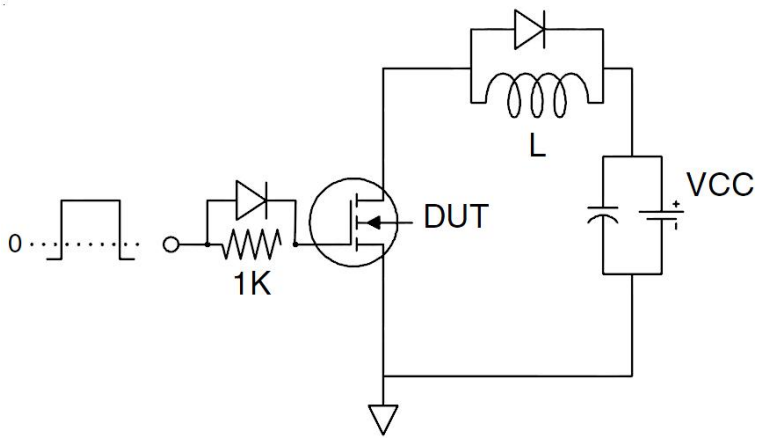
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

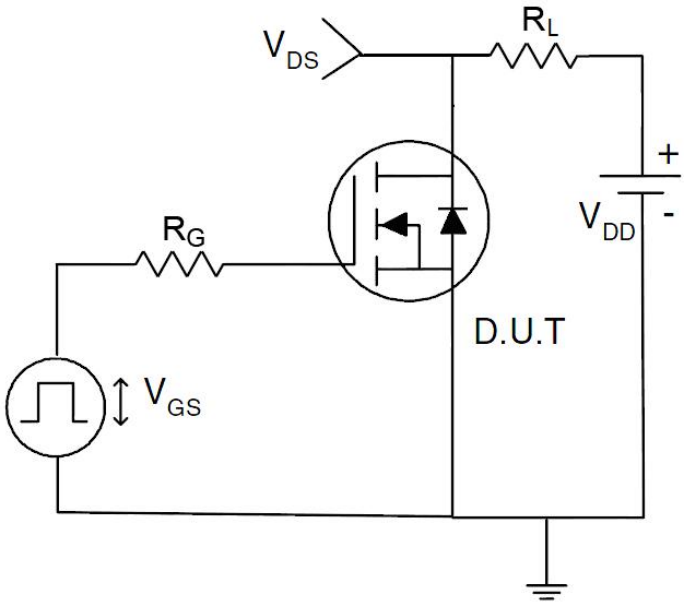
1）E_{AS} test Circuit



2）Gate charge test Circuit



3）Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

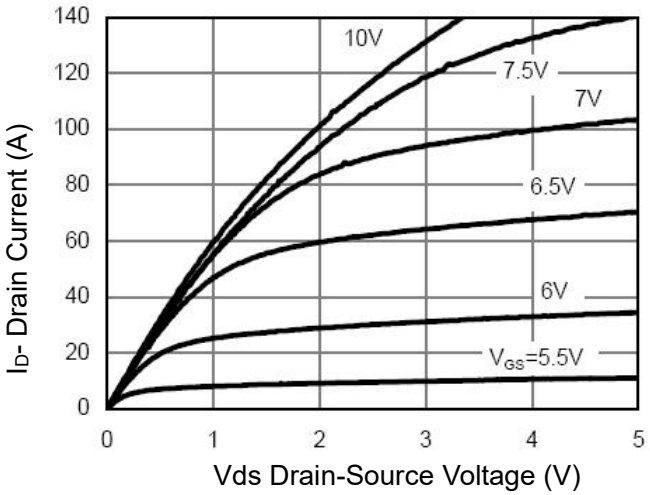


Figure 1 Output Characteristics

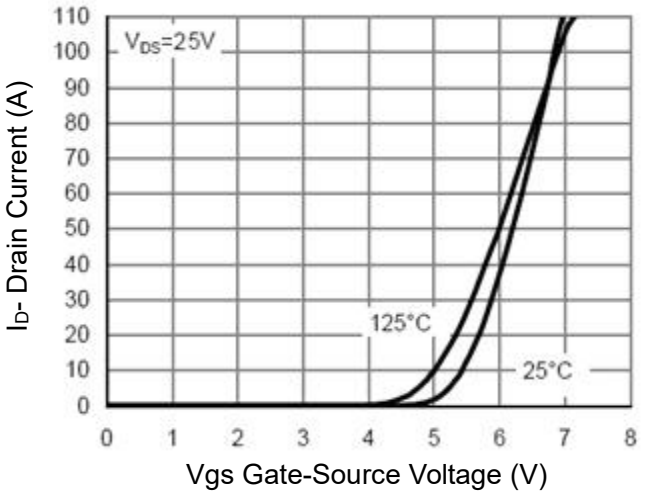


Figure 2 Transfer Characteristics

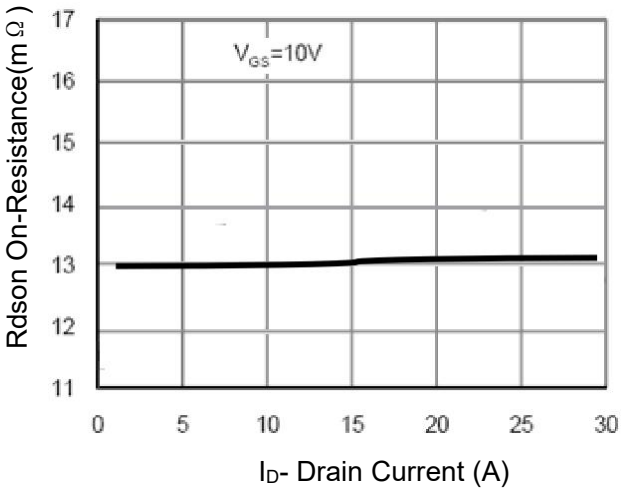


Figure 3 Rdson- Drain Current

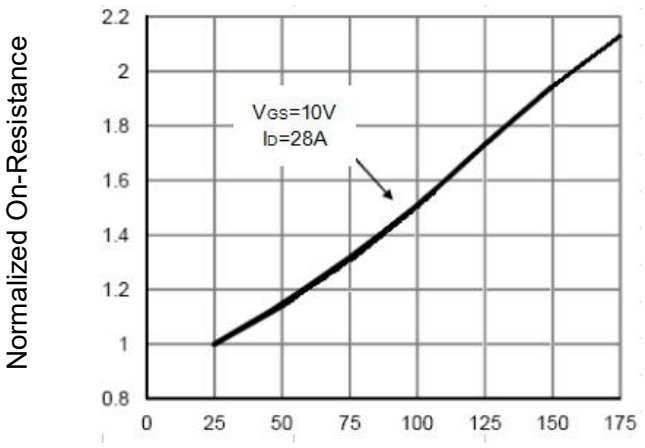


Figure 4 Rdson-JunctionTemperature

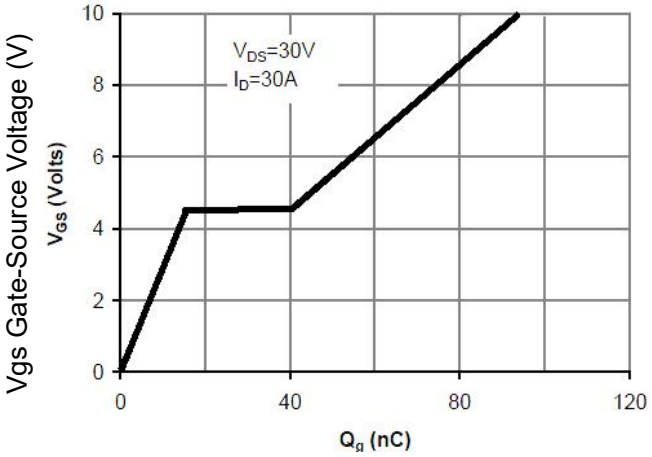


Figure 5 Gate Charge

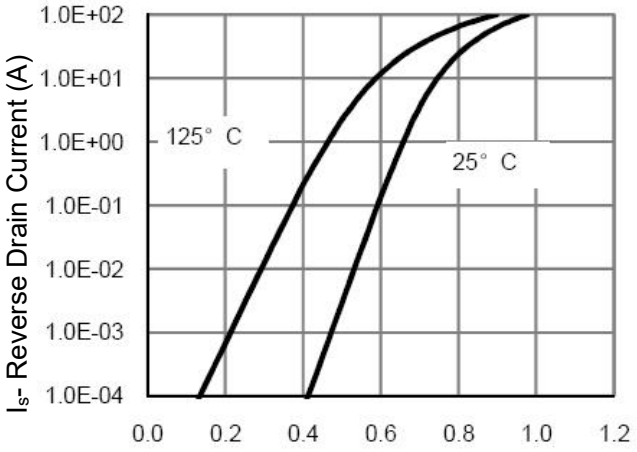


Figure 6 Source- Drain Diode Forward

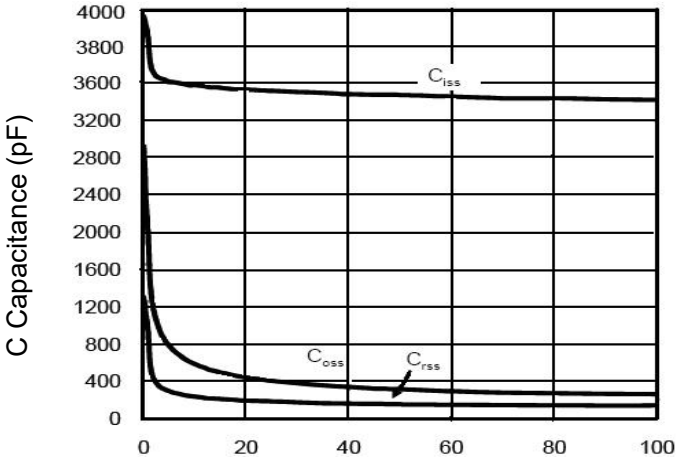


Figure 7 Capacitance vs Vds

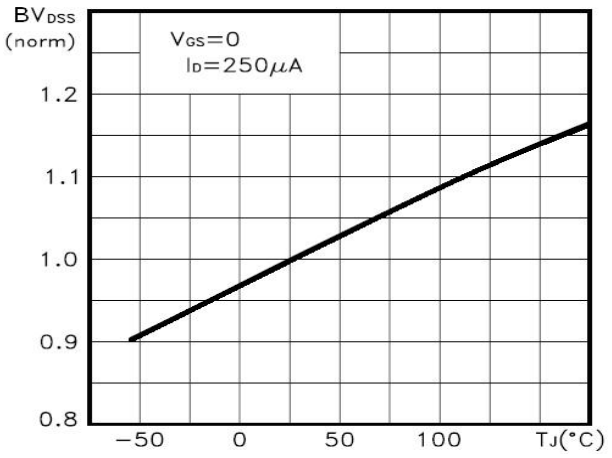


Figure 9 BV_{DSS} vs Junction Temperature

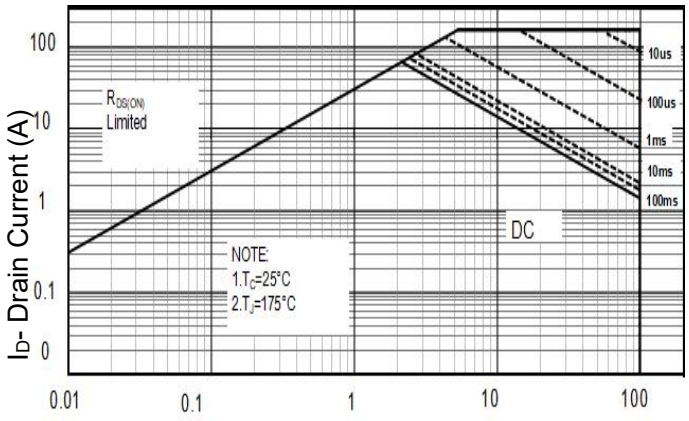


Figure 8 Safe Operation Area

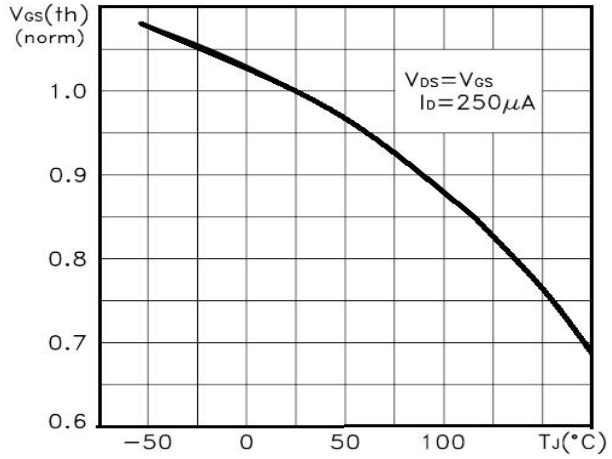


Figure 10 $V_{GS(th)}$ vs Junction Temperature

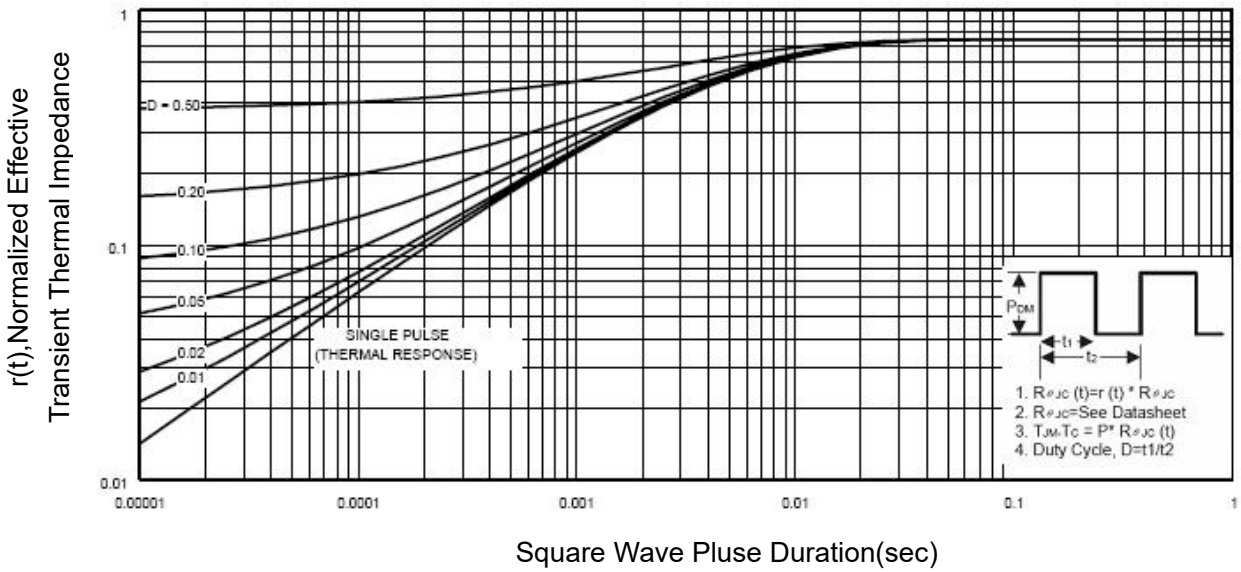
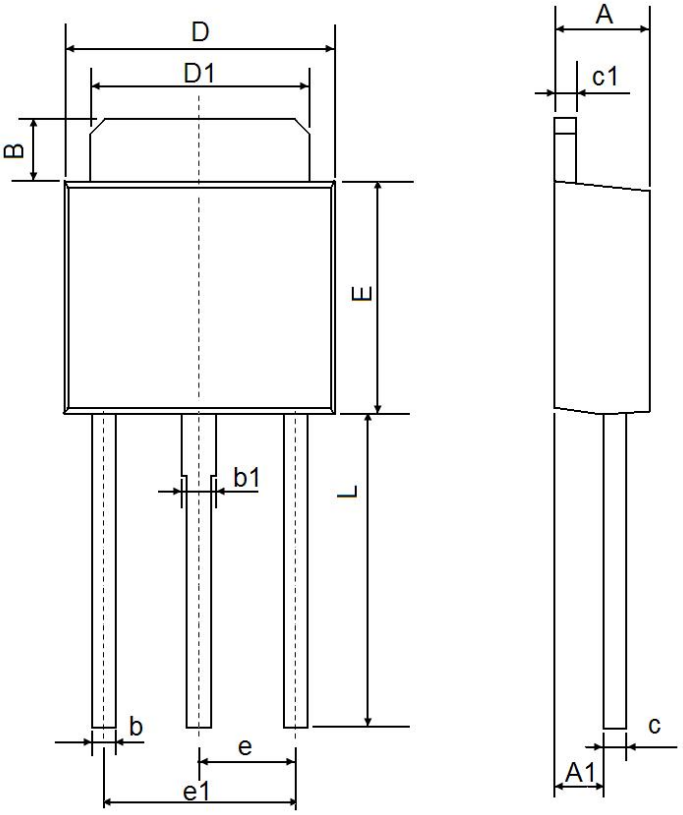


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-251(C) Package Information

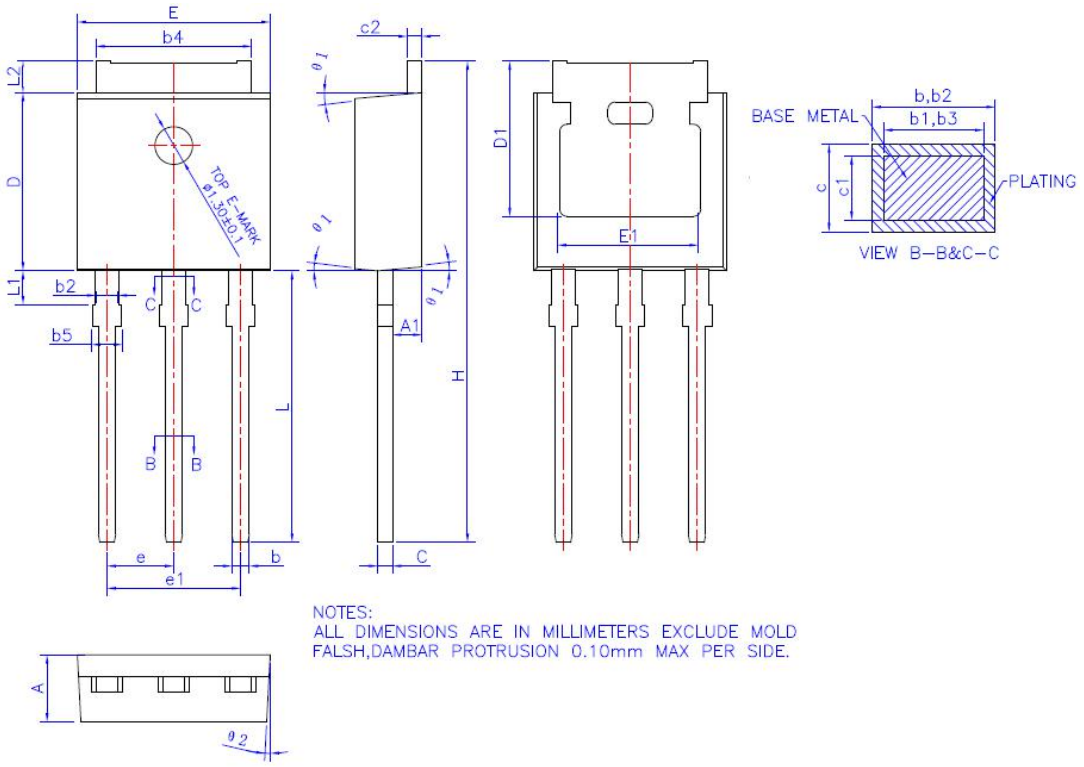


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact

TO-251 (J) Package Information



NOTES:
ALL DIMENSIONS ARE IN MILLIMETERS EXCLUDE MOLD FALSH,DAMBAR PROTRUSION 0.10mm MAX PER SIDE.

COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.35
A1	0.90	1.01	1.10
b	0.56	--	0.69
b1	0.55	0.60	0.65
b2	0.77	--	0.90
b3	0.76	0.81	0.86
b4	5.23	5.33	5.43
b5	—	--	1.05
c	0.46	--	0.59
c1	0.45	0.51	0.55
c2	0.46	--	0.59
D	6.00	6.10	6.20
D1	5.20	--	—
E	6.50	6.60	6.70
E1	4.60	4.83	5.00
e	2.24	2.29	2.34
e1	4.47	4.57	4.67
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.95	1.16	1.35
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

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