

NCE N-Channel Enhancement Mode Power MOSFET

DESCRIPTION

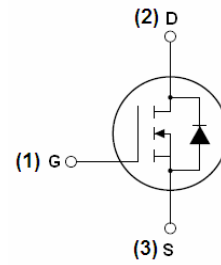
The NCE7580D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

GENERAL FEATURES

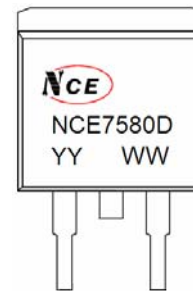
- $V_{DS} = 75V, I_D = 80A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS} = 10V$ (Typ: $6.5m\Omega$)
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

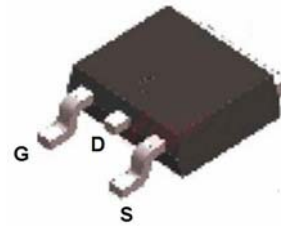
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin Assignment



TO-263-2L top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE7580D	NCE7580D	TO-263-2L	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	78	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	30	W
Peak diode recovery voltage	dv/dt	170	V/ns
Derating factor		1.13	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to- Case (Note 2)	$R_{\theta jc}$	0.88	$^{\circ}\text{C/W}$
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Electrical Characteristics (TA=25 $^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	75			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$			± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	2.85	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$		6.5	8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=30A$		60		S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$		3050		PF
Output Capacitance	C_{oss}			280		PF
Reverse Transfer Capacitance	C_{rss}			130		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		15		nS
Turn-on Rise Time	t_r			90		nS
Turn-Off Delay Time	$t_{d(off)}$			40		nS
Turn-Off Fall Time	t_f			95		nS
Total Gate Charge	Q_g	$V_{DS}=24V, I_D=40A,$ $V_{GS}=10V$		56		nC
Gate-Source Charge	Q_{gs}			12		nC
Gate-Drain Charge	Q_{gd}			16		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$			1.2	V
Diode Forward Current (Note 2)	I_S				80	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 75A$ $di/dt = 100A/\mu s(\text{Note 3})$			50	nS
Reverse Recovery Charge	Q_{rr}				48	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

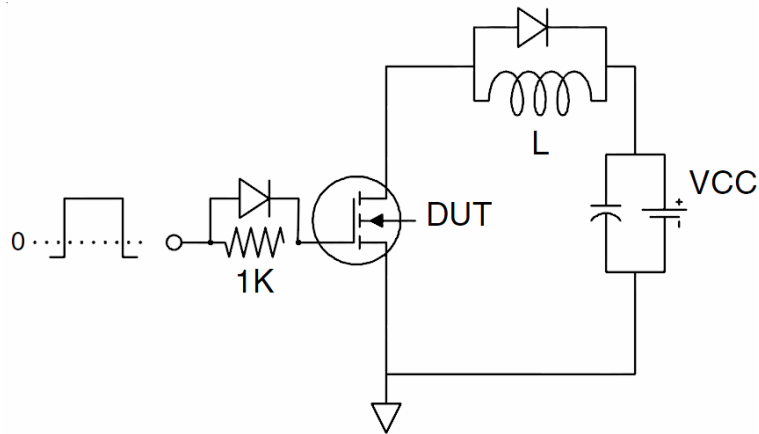
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.3\text{mH}, R_g=62\Omega$

Test circuit

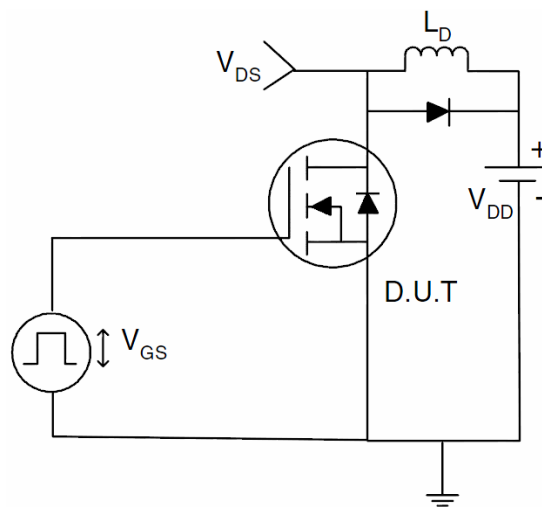
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

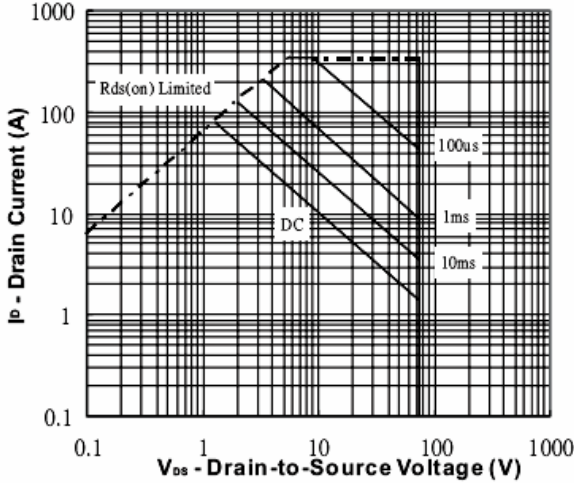


Figure2. Source-Drain Diode Forward Voltage

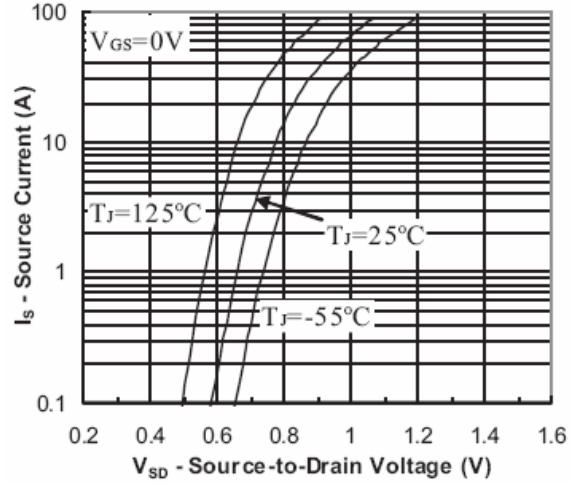


Figure3. Output characteristics

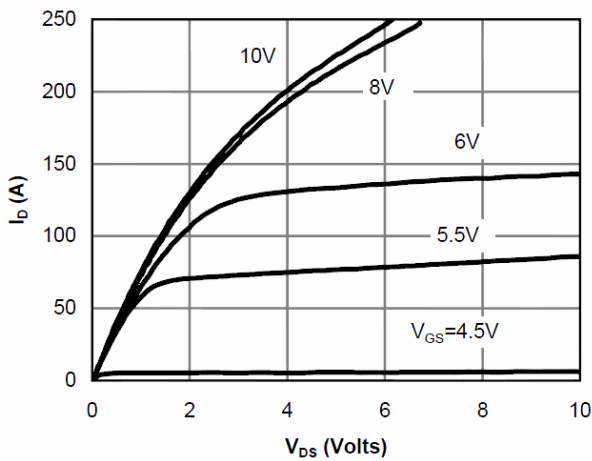


Figure4. Transfer characteristics

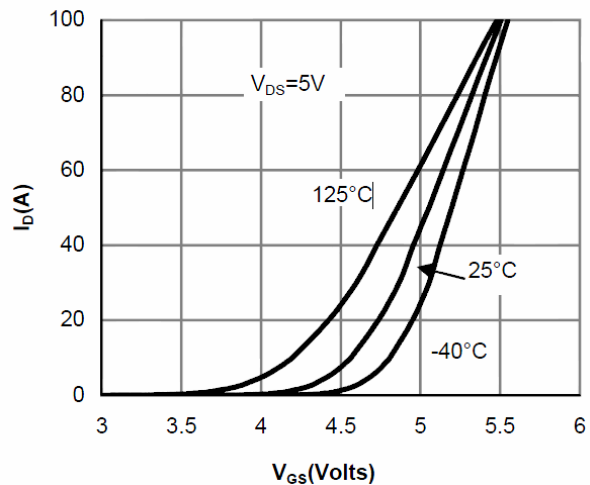


Figure5. Static drain-source on resistance

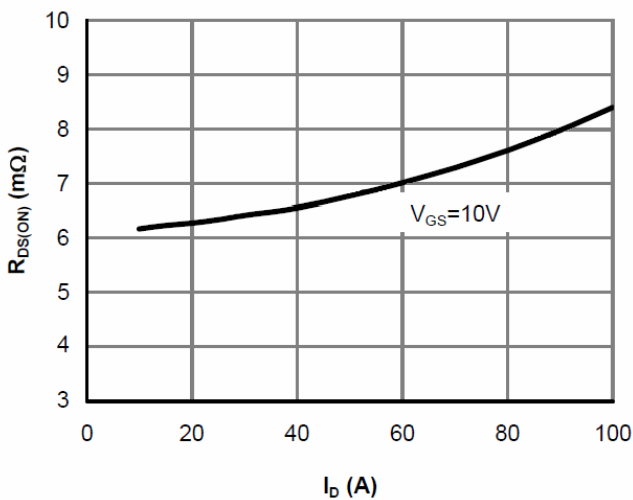


Figure6. R_{DS(ON)} vs Junction Temperature

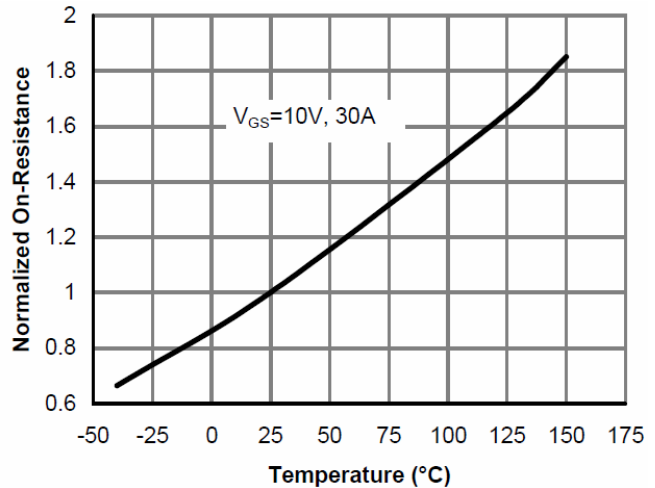


Figure7. BV_{DSS} vs Junction Temperature

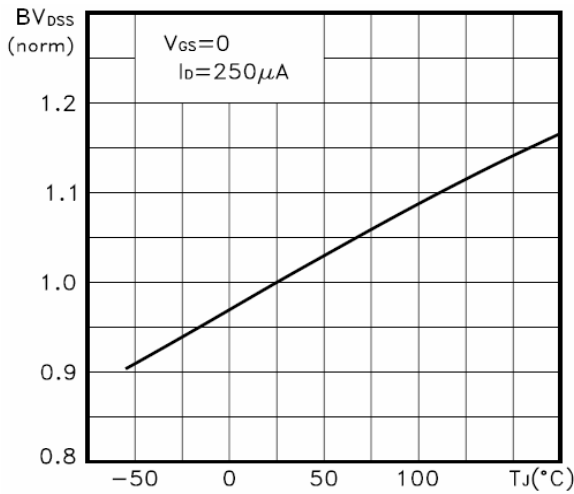


Figure8. $V_{GS(th)}$ vs Junction Temperature

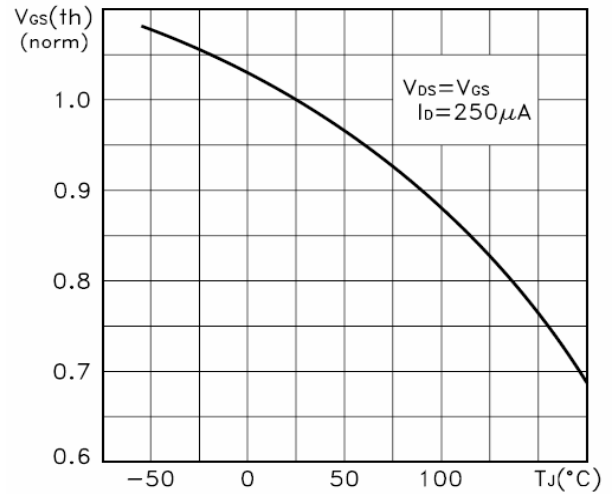


Figure9. Gate charge waveforms

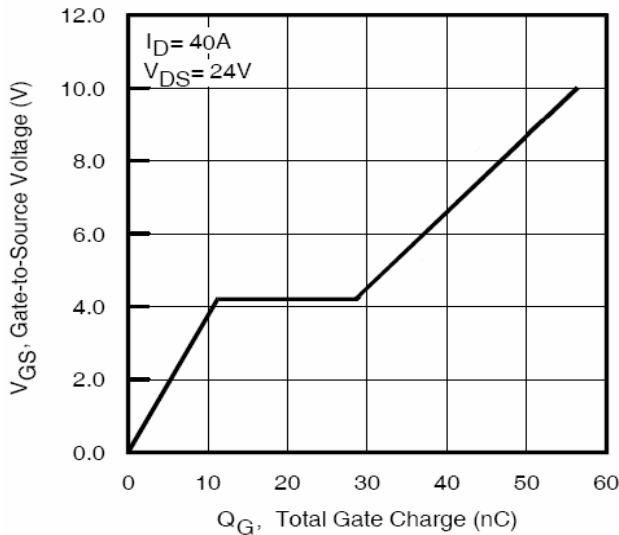


Figure10. Capacitance

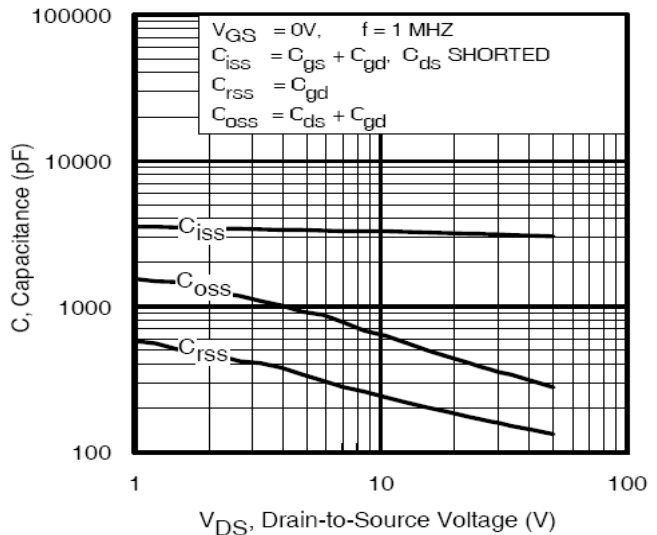
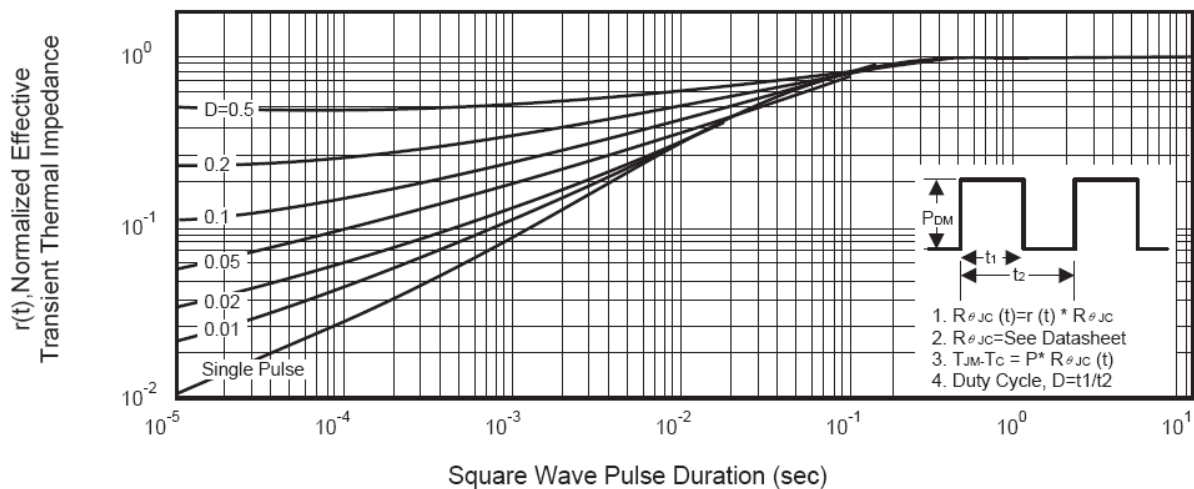
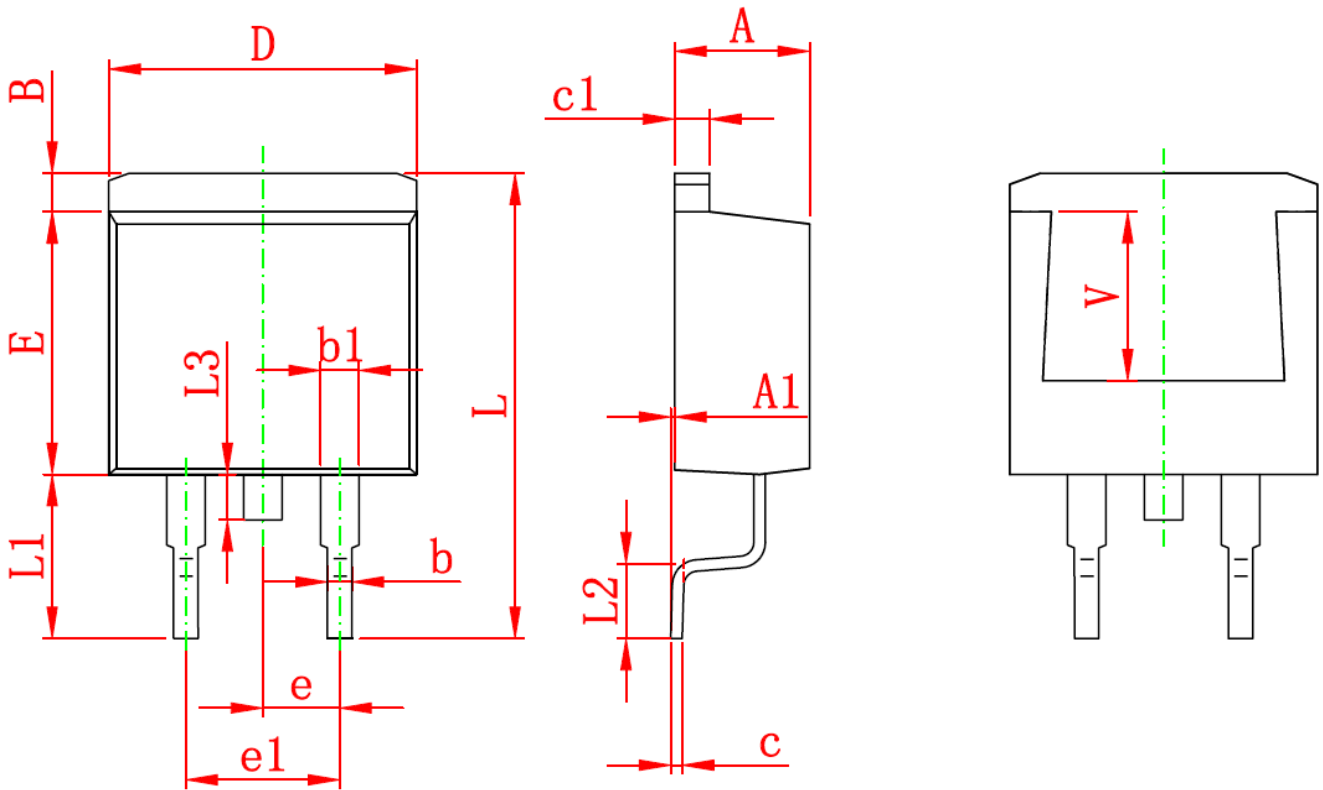


Figure11. Normalized Maximum Transient Thermal Impedance



TO-263-2L PACKAGE INFORMATION


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 (TYP.)		0.100 (TYP.)	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF.		0.220 REF.	

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