Description

Microsemi's PD69012 Power over Ethernet (PoE) Manager chip integrates power, analog and state of the art embedded core logic into a single 80-pin, plastic QFP package. The device is used in Ethernet switches and Midspans to enable network devices to share power and data over the same cable.

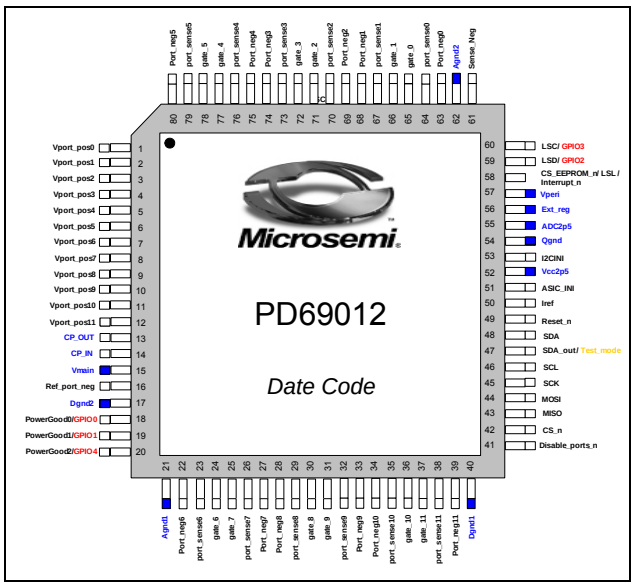
PD69012 device is a 12-port, mixed-signal, high-voltage Power over Ethernet driver. It enables detection of IEEE802.3af-2003 compliant PDs (Powered Devices) and IEEE802.3AT High Power Devices, thus, ensuring safe power feeding and disconnection of ports. With full digital control via a serial communication interface and a minimum of external components, the device integrates into multi-port and highly populated Ethernet switches and routers.

The PD69012 executes all real time functions as specified in the IEEE802.3af-2003 ("AF") standard and IEEE802.3at High Power ("AT") functionality, including load detection, "AF" and "AT" classification and port status monitoring. In addition it performs system level activities such as: power management and MIB support for system management. The PoE device is designed to detect and disable disconnected ports utilizing both DC and AC disconnection methods, as specified in the IEEE 802.3af-2003 standard.

The PD69012 is designed to support 2 main configurations:

- Auto mode: For Basic "AF" and "AT" PSE equipment
- Enhanced mode: For High End, Extended features set of AF and AT PSE equipment

Pin Configuration



Supported Features

PD69012 Auto Mode Features:

- Fully IEEE802.3af-2003 compliant
- Designed to support IEEE802.3at including two-event classification
- Supports Pre-standard PD detection
- Supports Cisco devices detection
- IETF Power Ethernet MIB (RFC 3621) compliant
- Single DC voltage input (44v-57v)
- Wide temperature range: -40° C to +85° C
- Low thermal dissipation (0.5Ω sense resistor)
- Drives 12 independent 2-pairs power ports or 6 independent 4-pairs ports
- Can cascade up to 8 PoE devices (96 ports)
- EEPROM interface for software patching and parameter configuration
- I^2C Host interface
- Supports Interrupt out pin
- Dynamic Power management
- Emergency power management supporting 3 Configurable Power Bank I/Os
- Direct register communication
- Direct LED drive
- Continuous monitoring per port and system data
- Parameter setting per port and per system
- Power soft start algorithm
- Thermal monitoring/protection
- Voltage monitoring/protection
- H/W disable ports input
- Built in 3.3 V regulator
- Internal power on reset
- Enhanced SPI bus for internal communication
- External EEPROM for system parameters update
- SW ROM patch option
- RoHS compliant

Enhanced Modes Additional Features:

- I^2C or UART host interface
- Serial Communication Protocol backwards compatible with PD63000 and PDIC66000
- Additional monitoring
- Extended parameter setting
- Port matrix for flexible PCB layout
- Field upgradeable software
- Emergency Power Management with 4 power supplies

Ordering Information

Part number	Temperature range	Package
PART	**TEMP. RANGE**	**PIN PACKAGE**
PD69012	-40 to +85 °C	LQFP 80 pin

This datasheet refers to ICs with date code "XAA0843" or later.
Date code: See the bottom line (XAA0843) in the Pin Configuration drawing. Where "*0*843" is the date code, "*08*" is the year (2008), and "*43*" is the week.

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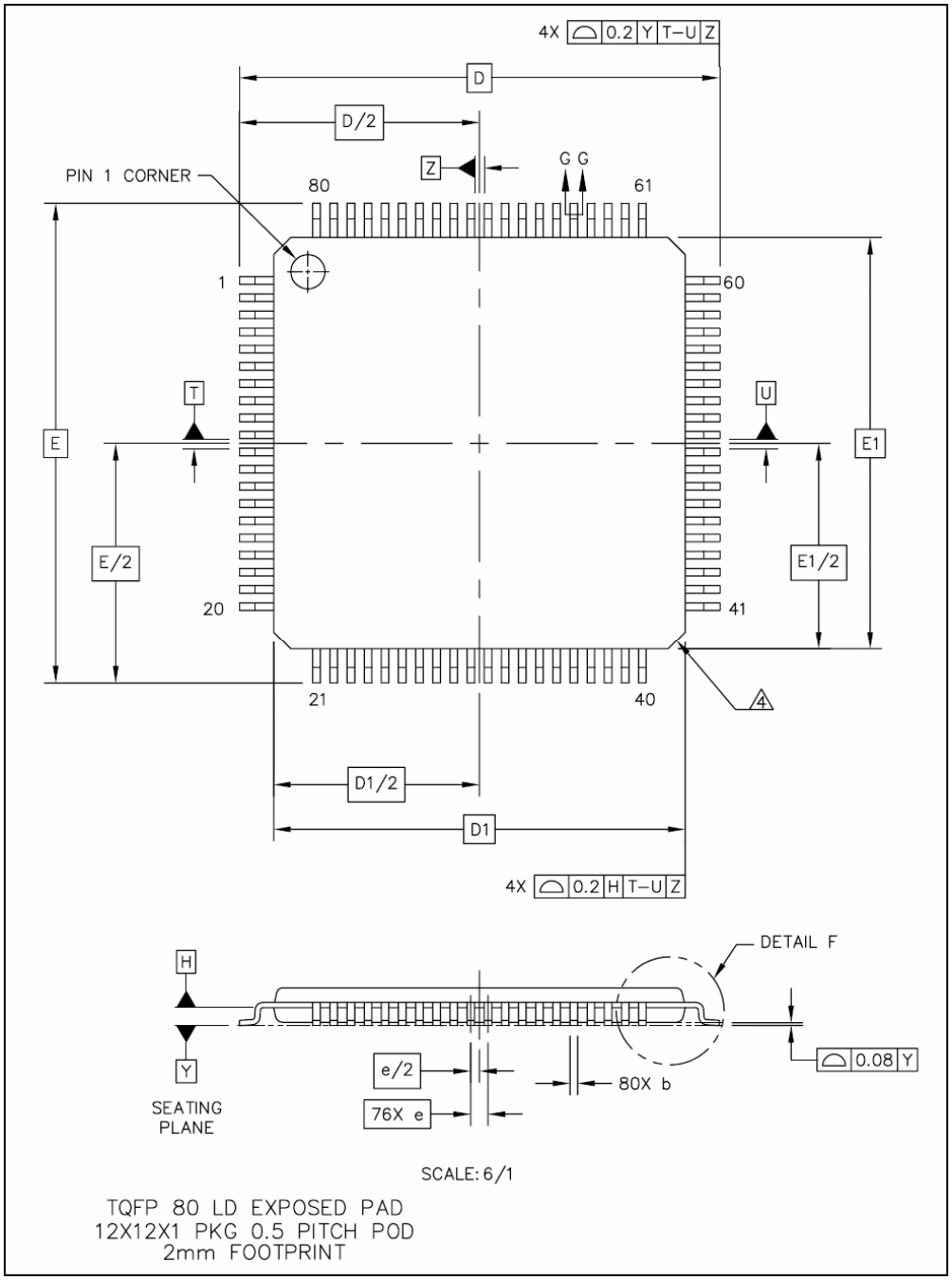
Package Information

The PD69012 is packed in an 80-pin LQFP plastic package, 12 x 12 x 1.4 mm with exposed pad.



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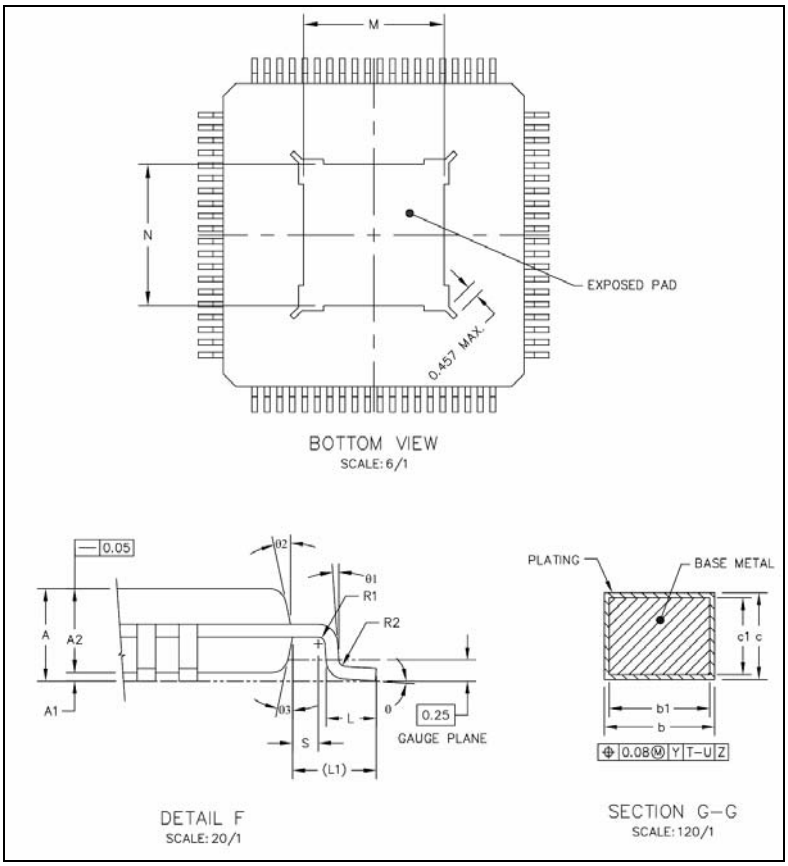

NOTES:

1. DATUMS T, U AND Z TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
2. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D AND E ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAM BAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

4 EXACT SHAPE OF EACH CORNER IS OPTION.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.2	L1		1 REF	
A1	0.05		0.15	R1	0.08		---
A2	0.95	1	1.05	R2	0.08		0.2
b	0.17	0.22	0.27	S	0.2		---
b1	0.17	0.2	0.23	θ	0°		7°
c	0.09		0.2	θ1	0°		---
c1	0.09		0.16	θ2	11°		13°
D		14 BSC		θ3	11°		13°
D1		12 BSC		M	5.5	5.6	5.7
e		0.5 BSC		N	5.5	5.6	5.7
E		14 BSC					
E1		12 BSC					
L	0.45	0.6	0.75				

UNIT	DIMENSION AND TOLERANCES
MM	ASME Y14.5M

Figure 1: PD69012 Package Description

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Maximum Ratings

V_{main} ..... -0.3 to 80 V(1)
DGND, AGND, QGND, SENSE_NEG..... -0.3 to 0.3 V(2)

V_{PORT_POSx} ..... -0.3 to 80 V(1)
V_{PORT_NEGx}, REF_PORT_NEG..... -8.4 to 80V(1)
V_{PORT_POSx} - V_{PORT_NEGx}..... -0.3 to 80 V(1)

PORT_SENSEx ..... -7.2 to 25 V (1)
Gate_x..... -0.3 to 18 V
VCC_{2p5}, ADC_{2p5}..... -0.3 to 3 V
V_{PERI}..... 4 V
EXT_REG..... -0.3 to 6 V
I2CINI, ASICINI..... -0.3 to 3 V
MISO, MOSI, SCK, SCL, SDA, CLK, RESETN, CS_N, INTERRUPT, POWER_BANK[2..0], LSD, LSC, LSL, SDA_OUT..... -0.3 to (V_{PERI} + 0.3) V

ESD (Human Body Model)..... -2 to 2 kV(3)
Max junction temperature (T_{junc})..... +150° C
Junction-ambient thermal resistance (θ_{JA})..... 30° C/W(4)
Junction-case thermal resistance (θ_{JC})..... 10° C/W
Lead temperature (soldering, 10 s)..... 260° C
Storage temperature..... -40 to +125 °C

Notes: "x" defines port numbers, 0 thru 3, inclusive.
(1) 80 V is the transient voltage that can be applied for 1 min max.
(2) Maximum value between grounds.
(3) ESD testing is performed in accordance with the Human Body Model (CZap = 100 pF, RZap = 1500 Ω).
(4) with 4ML PCB – no air flow

Stress beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating temperature At full load ambient	-40		+85	°C
Operational limitations (1)	15 to 44	44 to 55	55 to 57	V

(1) Operating functions depend on the input voltage, as shown in Figure 2.

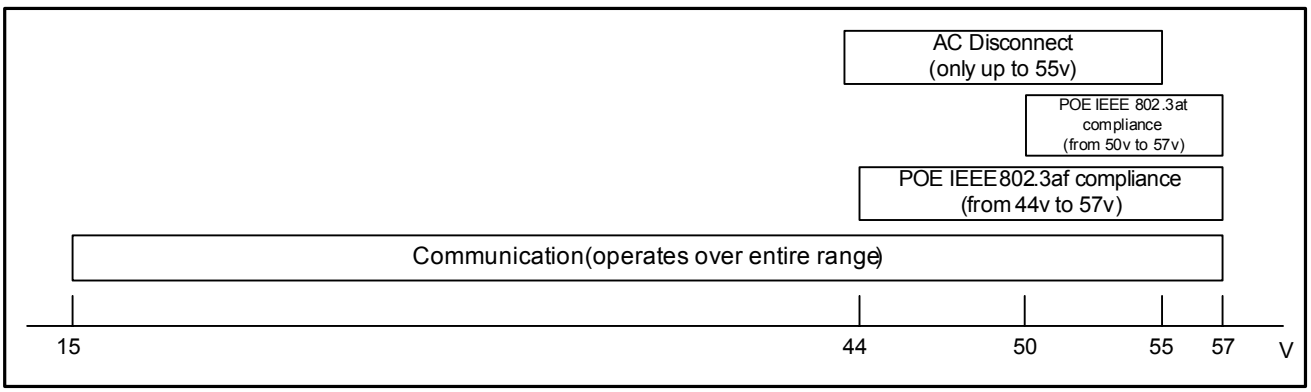

Figure 2: Operational Ranges

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Electrical Characteristics

PIN NAME:	• SCL • DISABLE_PORTS_N					
PAD TYPE:	Schmitt Trigger CMOS input, TTL Level with no internal Res.					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		1	µA	
Input Low Current	I_{IL}	-1		1	µA	

PIN NAME:	• LSD Multiplexed with GPIO_2 • LSC Multiplexed with GPIO_3 • POWER_GOOD0 Multiplexed with GPIO_0 • POWER_GOOD1 Multiplexed with GPIO_1 • POWER_GOOD2 Multiplexed with GPIO_4					
PAD TYPE:	CMOS I/O, TTL Level with no internal pull up / pull down resistor, with Schmitt trigger Input					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	
Input Low Current	I_{IL}	-1		+1	µA	
High Level Output Voltage		VPERI-0.4 V			V	Iout = -2 mA
Low Level Output Voltage				0.4	V	Iout = 2 mA

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PIN NAME:	• SCK • CS_N • MOSI					
PAD TYPE:	CMOS I/O, TTL Level with internal pull up current source, with Schmitt trigger Input					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	
Input Low Current	I_{IL}	-1		+1	µA	
High Level Output Voltage		VPERI-0.4 V			V	Iout = -2 mA
Low Level Output Voltage				0.4	V	Iout = 2 mA
Pull Up Current		10	20	50	uA	

PIN NAME:	• MISO					
PAD TYPE:	CMOS I/O, TTL Level with internal pull up current source, with Schmitt trigger Input					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
Input High Current	I_{IH}	-1		+1	µA	
Input Low Current	I_{IL}	-1		+1	µA	
High Level Output Voltage		VPERI-0.4 V			V	Iout = -2 mA
Low Level Output Voltage				0.4	V	Iout = 2 mA
Pull Down Current		10	20	50	uA	

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PIN NAME:	• **RESET_N** • **SDA** • **SDA_OUT Multiplexed with TEST_MODE**					
PAD TYPE:	Digital I/O – input/output open drain CMOS Open Drain Output with Schmitt Trigger Input, TTL Level (external pull up resistor Only))					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Output Voltage	V_{OL}			0.4	V	Iout = 6 mA
Low Level Input Voltage	V_{IL}			0.8	V	
Input Voltage Hysteresis		0.3			V	
OFF State Output Current		-1		+1	uA	

PIN NAME:	• **CS_EEPROM & LSL Multiplexed with INTERRUPT_N**					
PAD TYPE:	CMOS Open Drain Output (**external** pull up res. Only))					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Low Level Output Voltage				0.4	V	Iout = 6mA
OFF State Output Current		-1		+1	uA	

PIN NAME:	• **VPORT_NEGx** • **REF_PORT_NEG**					
PAD TYPE:	High Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Pin Current Consumption		-10		+10	uA	Port driver OFF, Vport differential measurement OFF, AC generator OFF

PIN NAME:	• **PORT_SENSEx**					
PAD TYPE:	Low Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		0		0.5	V	With external 0.5 ohm 2% to GND
Internal Current Consumption				20	uA	

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PIN NAME:	• VPORT_POSx • VPORT_NEGx					
PAD TYPE:	High Voltage Analog Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage (to GND)		0		62	V	

PIN NAME:	• VMAIN					
PAD TYPE:	High Voltage Supply Pad					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		44		57	V	
VMAIN Current Consumption			13.6	16	mA	Total on VMAIN

PIN NAME:	• CP_OUT					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		44		68	V	
Pin Internal Current Consumption				5	mA	

PIN NAME:	• CP_IN					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		34		57	V	

PIN NAME:	• ADC2p5 • VCC2p5 • VPERI • EXT_REG					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
ADC2p5 Output voltage		2.45		2.55	V	
ADC2p5 Internal Current Consumption				6	mA	Recommended external cap. = 47 nF to 135 nF
VCC2p5 Output Voltage		2.37		2.62	V	Recommended external cap. = 47 nF to 135 nF
VPERI Output Voltage		3.10		3.5	V	Recommended external cap. = 1 uF to 4.7 uF
VPERI External Current Load				6	mA	Without external NPN
EXT_REG Output Current				6	mA	

PIN NAME:	• ASICINI • I2CINI **(max. capacitance between mode input to GND should NOT exceed 1nF)**					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Operating Voltage		0		ADC2p5	V	
Current Consumption		-1		+1	uA	

PIN NAME:	• IREF					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Output Voltage		1.21		1.34	V	With external 24.9 K resistor to GND

PIN NAME:	• FET_Gx					
PAD TYPE:	Analog					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**NOTE**
Output Voltage		12		15	V	

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Dynamic Characteristics

The PD69012 utilizes three programmable current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}). Loads that dissipate more than I_{cut} for longer than T_{cut} are classified as 'overloads' and are automatically shutdown. Loads that consume I_{lim} current for more than T_{lim} are shutdown and classified as 'short circuits'. If the PD69012 is configured to operate in DC-Disconnect mode and the output power is below I_{min} for more than $T_{min,}$ the PD is classified as 'no-load' and is shutdown. If the PD69012 is configured to operate in AC-Disconnect mode, then if the load's impedance is above a pre-defined impedance for more than $T_{min,}$ the PD is classified as 'no-load' and is shutdown.

Automatic recovery from overload and no-load conditions is attempted every period of T_{OVLREC} and T_{UDLREC} (typically 5 and 1 seconds respectively). Output power is limited to $I_{lim,}$ which is a maximum peak current allowed at the port.

AF PORTS PARAMETERS

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown (can be modified through control port)			5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown (can be modified through control port)			1		s
Cutoff timers accuracy	Typical accuracy of T_{cut}		4	2	0	ms
Inrush current	I_{Inrsh}	For t=50 ms, C_{load}=180 uF max.	400		450	mA
Output current operating range	I_{port}	Continuous operation after startup period.	10		375	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		15.4	W
Off mode current	I_{min1}	Must disconnect for t greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over load current detection range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	T_{MPS}	DC modulation time for dc disconnect		49		ms
AC disconnect impedance	Zac		27	600	2000	KΩ

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AT PORTS PARAMETERS

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown (can be modified through control port)			5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown (can be modified through control port)			1		s
Cutoff timers accuracy	Typical accuracy of T_{cut}		4	2	0	ms
Inrush current	I_{Inrsh}	For t=50 ms, C_{load}=180 uF max.	400		450	mA
Output current operating range	I_{port}	Continuous operation after startup period.	10		643	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		36	W
Off mode current	I_{min1}	Must disconnect for t greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over load current detection range	I_{cut}	Time limited to T_{OVL}	686	728	771	mA
Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 2.8 Vdc			500	ms
Time Maintain Power Signature	TMPS	DC modulation time for dc disconnect		49		ms
AC disconnect impedance	Zac		27	600	2000	KΩ

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Pin Description

Pin	Pin Name	Pin Type	Description
0	PAD	Gnd	Exposed pad connected to underside of die
1	VPORT_POS0	Analog I/O	Port 0 positive input
2	VPORT_POS1	Analog I/O	Port 1 positive input
3	VPORT_POS2	Analog I/O	Port 2 positive input
4	VPORT_POS3	Analog I/O	Port 3 positive input
5	VPORT_POS4	Analog I/O	Port 4 positive input
6	VPORT_POS5	Analog I/O	Port 5 positive input
7	VPORT_POS6	Analog I/O	Port 6 positive input
8	VPORT_POS7	Analog I/O	Port 7 positive input
9	VPORT_POS8	Analog I/O	Port 8 positive input
10	VPORT_POS9	Analog I/O	Port 9 positive input
11	VPORT_POS10	Analog I/O	Port 10 positive input
12	VPORT_POS11	Analog I/O	Port 11 positive input
13	CP_OUT	Analog I/O	Charge pump output pulse
14	CP_IN	Supply	Charge pump input
15	VMAIN	Supply	Main Voltage supply
16	REF_PORT_NEG	Analog I/O	Port negative reference
17	DGND2	GND	Digital ground
18	POWER_GOOD0 MULTIPLEXED WITH GPIO_0	Digital I/O	Power supply monitoring multiplexed with general purpose I/O
19	POWER_GOOD1 MULTIPLEXED WITH GPIO_1	Digital I/O	Power supply monitoring multiplexed with general purpose I/O
20	POWER_GOOD2 MULTIPLEXED WITH GPIO_4	Digital I/O	Power supply monitoring multiplexed with general purpose I/O
21	AGND1	GND	Analog ground
22	VPORT_NEG6	Analog I/O	Port 6 negative voltage feeding
23	PORT_SENSE6	Analog I/O	Channel current monitoring
24	FET_G6	Analog I/O	Port 6 – Gate control
25	FET_G7	Analog I/O	Port 7 – Gate control
26	PORT_SENSE7	Analog I/O	Channel current monitoring
27	VPORT_NEG7	Analog I/O	Port 7 negative voltage feeding
28	VPORT_NEG8	Analog I/O	Port 8 negative voltage feeding

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Pin	Pin Name	Pin Type	Description
29	PORT_SENSE8	Analog I/O	Channel current monitoring
30	FET_G8	Analog I/O	Port 8 – Gate control
31	FET_G9	Analog I/O	Port 9 – Gate control
32	PORT_SENSE9	Analog I/O	Channel current monitoring
33	VPORT_NEG9	Analog I/O	Port 9 negative voltage feeding
34	VPORT_NEG10	Analog I/O	Port 10 negative voltage feeding
35	PORT_SENSE10	Analog I/O	Channel current monitoring
36	FET_G10	Analog I/O	Port 10 – Gate control
37	FET_G11	Analog I/O	Port 11 – Gate control
38	PORT_SENSE11	Analog I/O	Channel current monitoring
39	VPORT_NEG11	Analog I/O	Port 11 negative voltage feeding
40	DGND1	GND	Digital ground
41	DISABLE_PORTS_N	Digital Input	Disable All Ports Power – Active Low
42	CS_N	Digital I/O	SPI bus, Chip Select
43	MISO	Digital I/O	SPI bus, Master Data in/slave out
44	MOSI	Digital I/O	SPI bus, Master Data out/slave in
45	SCK	Digital I/O	SPI bus, Serial clock I/O
46	SCL	Digital Input	I2C bus, Serial Clock Input
47	SDA_OUT MULTIPLEXED WITH TEST_MODE	Digital I/O	Third pin in I²C protocol Test Mode Pin – Must be tied to VPERI with pull-up resistor if not used
48	SDA	Digital I/O	I2C bus, open drain
49	RESET_N	Digital I/O	Active Low Reset I/O
50	IREF	Analog I/O	Current reference
51	ASICINI	Analog Input	Analog input for chip initialization
52	VCC2P5	Internal Regulator	Internal 2.5 v source – not to be used for external devices
53	I2CINI	Analog Input	Analog input for I2C initialization
54	QGND	GND	Quiet analog ground
55	ADC2P5	Internal reference	ADC reference – not to be used for external devices
56	EXT_REG	Analog Out	External regulation
57	VPERI	Analog Out	Regulated 3.3 v output voltage source for external devices
58	CS_EEPROM_N & LSL MULTIPLEXED WITH INTERRUPT_N	Digital Output Open drain	SPI bus, EEPROM Chip Select & Led Stream Latch (if set) Multiplexed with interrupt out

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Pin	Pin Name	Pin Type	Description
59	LSD MULTIPLEXED WITH GPIO_2	Digital I/O	LED Stream Data – data out Multiplexed with General purpose I/O
60	LSC MULTIPLEXED WITH GPIO_3	Digital I/O	Led Stream CLK– CLK out Multiplexed with General purpose I/O
61	SENSE_NEG	Analog I/O	Port sense reference
62	AGND2	GND	Analog ground
63	VPORT_NEG0	Analog I/O	Port 0 negative voltage feeding
64	PORT_SENSE0	Analog I/O	Channel current monitoring
65	FET_G0	Analog I/O	Port 0 – Gate control
66	FET_G1	Analog I/O	Port 1 – Gate control
67	PORT_SENSE1	Analog I/O	Channel current monitoring
68	VPORT_NEG1	Analog I/O	Port 1 negative voltage feeding
69	VPORT_NEG2	Analog I/O	Port 2 negative voltage feeding
70	PORT_SENSE2	Analog I/O	Channel current monitoring
71	FET_G2	Analog I/O	Port 2 – Gate control
72	FET_G3	Analog I/O	Port 3 – Gate control
73	PORT_SENSE3	Analog I/O	Channel current monitoring
74	VPORT_NEG3	Analog I/O	Port 3 negative voltage feeding
75	VPORT_NEG4	Analog I/O	Port 4 negative voltage feeding
76	PORT_SENSE4	Analog I/O	Channel current monitoring
77	FET_G4	Analog I/O	Port 4 – Gate control
78	FET_G5	Analog I/O	Port 5 – Gate control
79	PORT_SENSE5	Analog I/O	Channel current monitoring
80	VPORT_NEG5	Analog I/O	Port 5 negative voltage feeding

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Configuration Pins

There are two main configuration pins (see Figure 3) utilized in the PD69012. These pins configure the operation mode of the chip and the communication addresses (SPI and I^2C)

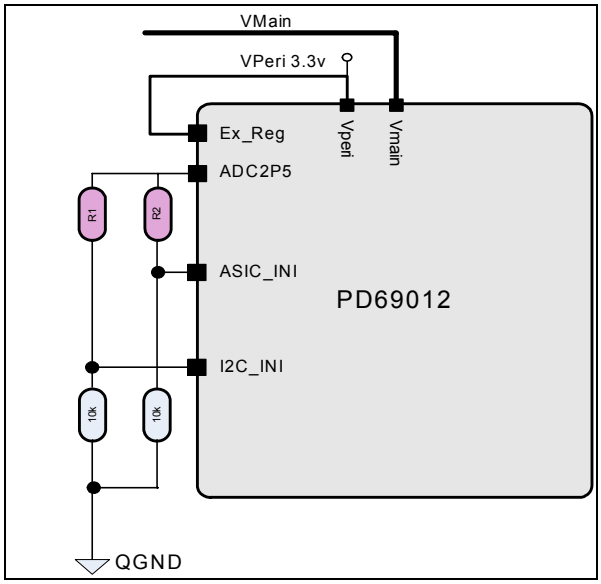

Figure 3: Electronic Connection of Configuration Pins

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Application Information

The PD69012 can be integrated into a number of applications such as daughter boards, Ethernet switches or routers. Examples of such applications are described below:

Integrated directly into a switch: Facilitates entire PoE concept by including the IC(s) on the main switch's PCB.

Daughter board add-on: The IC is integrated into a small PCB dedicated for PoE, mounted on top of the switch's main PCB or in the DIMM module

Integrated into an RJ45 connector: Saves space on the main board and creates small differences between the PoE and non-PoE versions of a switch

Midspans: Stand alone devices, installed between the Ethernet switch and PDs (Powered Devices) such as telephones, cameras, wireless LANs, etc.

These Midspans include the PD69012 IC as a PoE control element, destined to inject power over the communication lines.

Figure 4 and Figure 5 illustrate an example of basic applications of the PD69012 in an AC Disconnect Mode and the DC Disconnect Mode:

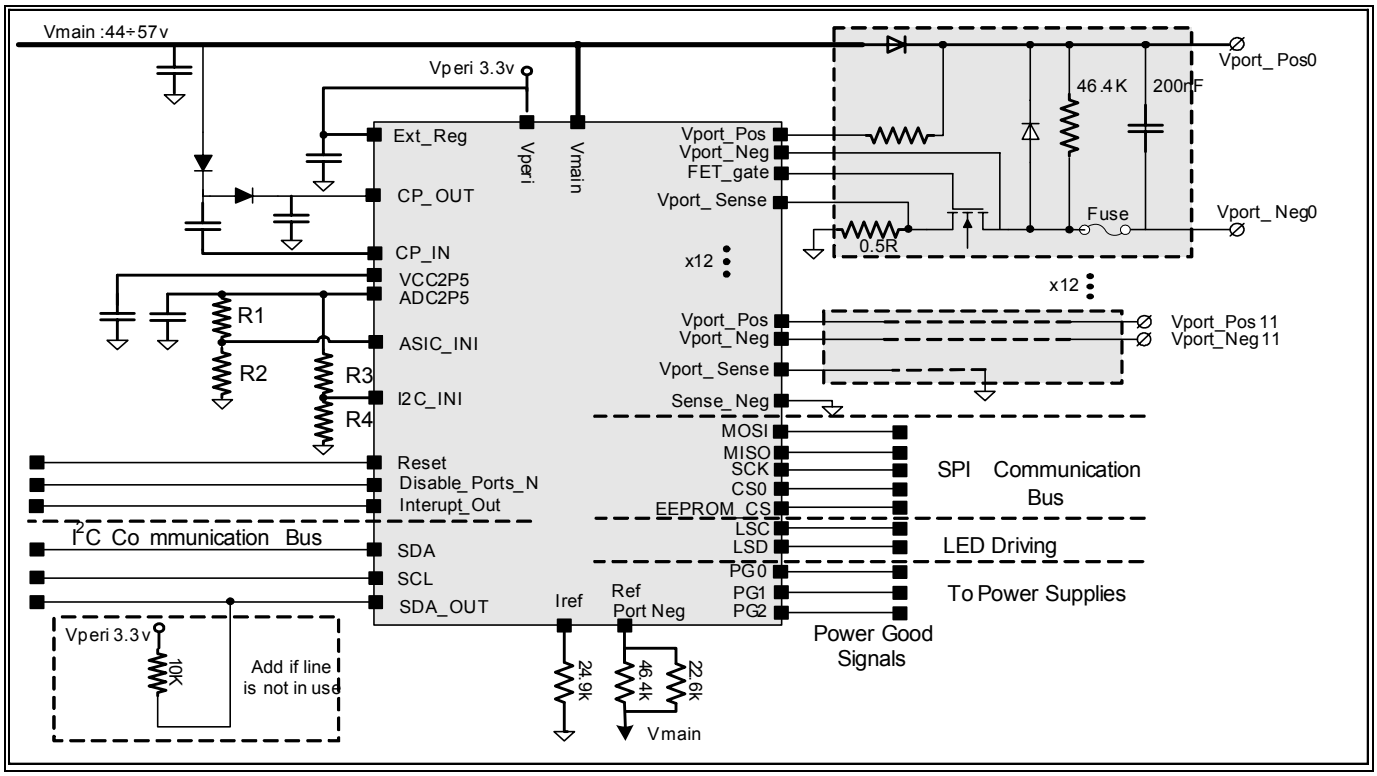

Figure 4: Basic Application with AC Disconnect Support

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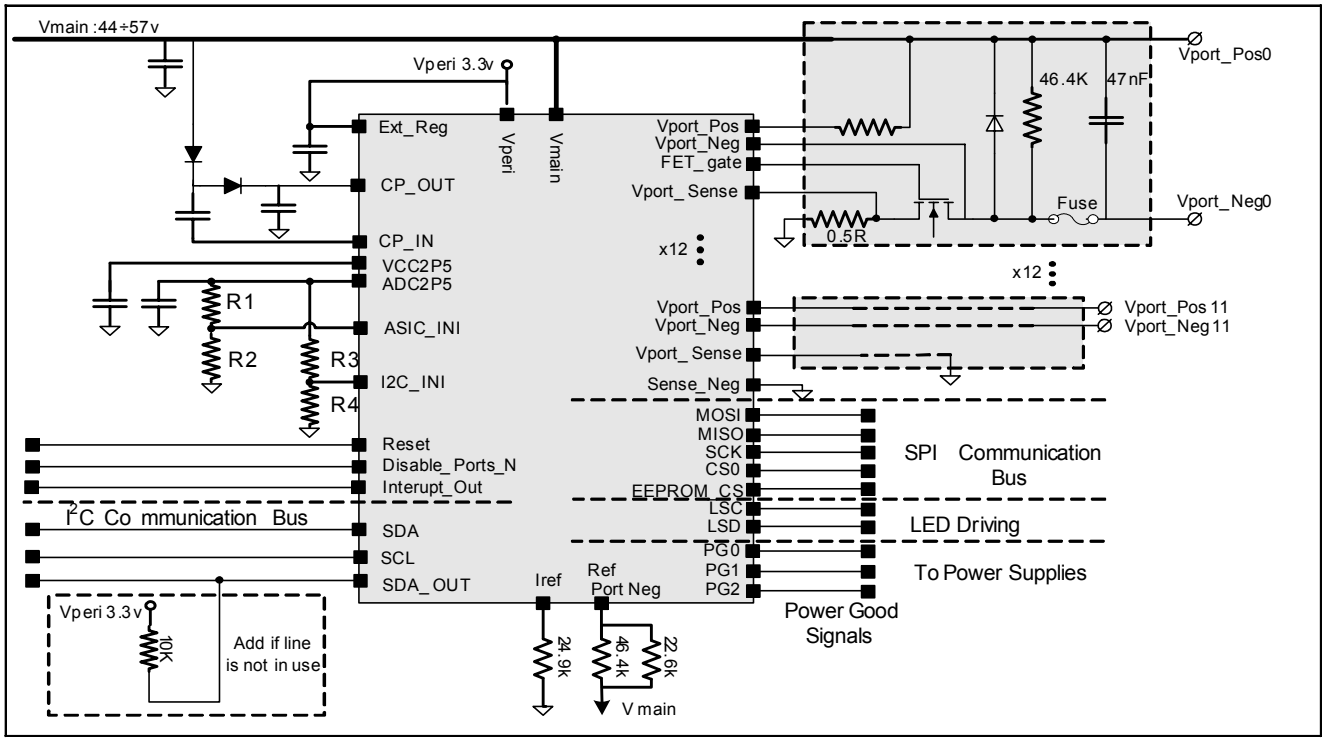

Figure 5: Basic Application with DC Disconnect Support

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 03 March 2009	-	Initial preliminary release
1.0 / 25-Aug-09		Release

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