MMFT2955E

Preferred Device

Power MOSFET
1 Amp, 60 Volts

P−Channel SOT−223

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient device also offers a drain−to−source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

Features

- Silicon Gate for Fast Switching Speeds
- The SOT−223 Package can be Soldered Using Wave or Reflow
- The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Pb−Free Package is Available

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DS}	60	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±15	
Drain Current − Continuous − Pulsed	I_D I_{DM}	1.2 4.8	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D (Note 1)	0.8 6.4	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, Peak I_L = 1.2 A, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	108	mJ

THERMAL CHARACTERISTICS

Thermal Resistance, Junction−to−Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C S

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

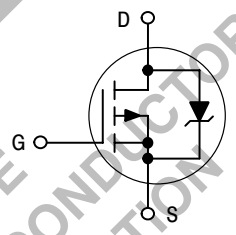
1. Power rating when mounted on FR−4 glass epoxy printed circuit board using recommended footprint.

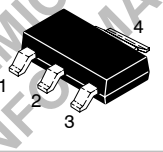
ON Semiconductor®

http://onsemi.com

1 AMPERE, 60 VOLTS
$R_{DS(on)}$ = 300 mΩ

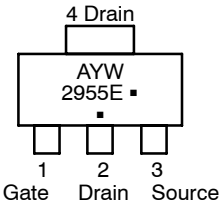
P−Channel





TO−261AA
CASE 318E
STYLE 3

MARKING DIAGRAM AND PIN ASSIGNMENT



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
2955E = Device Code
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MMFT2955ET1	SOT−223	1000 Tape & Reel
MMFT2955ET1G	SOT−223 (Pb−Free)	1000 Tape & Reel
MMFT2955ET3	SOT−223	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	60	–	–	Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 – –	 – –	 1.0 50	μAdc
Gate−Body Leakage Current, (V_{GS} = 15 V, V_{DS} = 0)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2.0	–	4.5	Vdc
Static Drain−to−Source On−Resistance, (V_{GS} = 10 V, I_D = 0.6 A)		$R_{DS(on)}$	–	–	0.3	Ω
Drain−to−Source On−Voltage, (V_{GS} = 10 V, I_D = 1.2 A)		$V_{DS(on)}$	–	–	0.48	Vdc
Forward Transconductance, (V_{DS} = 15 V, I_D = 0.6 A)		g_{FS}	–	7.5	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	460	–	pF
Output Capacitance		C_{oss}	–	210	–	
Reverse Transfer Capacitance		C_{rss}	–	84	–	
SWITCHING CHARACTERISTICS (Note 2)						
Turn−On Delay Time	(V_{DD} = 25 V, I_D = 1.6 A V_{GS} = 10 V, R_G = 50 Ω, R_{GS} = 25 Ω)	$t_{d(on)}$	–	18	–	ns
Rise Time		t_r	–	29	–	
Turn−Off Delay Time		$t_{d(off)}$	–	44	–	
Fall Time		t_f	–	32	–	
Total Gate Charge	(V_{DS} = 48 V, I_D = 1.2 A, V_{GS} = 10 Vdc) See Figures 15 and 16	Q_g	–	18	–	nC
Gate−Source Charge		Q_{gs}	–	2.8	–	
Gate−Drain Charge		Q_{gd}	–	7.5	–	
SOURCE DRAIN DIODE CHARACTERISTICS (Note 3)						
Forward On−Voltage	I_S = 1.2 A, V_{GS} = 0	V_{SD}	–	1.0	–	Vdc
Forward Turn−On Time	I_S = 1.2 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	–	90	–	ns

2. Switching characteristics are independent of operating junction temperature.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

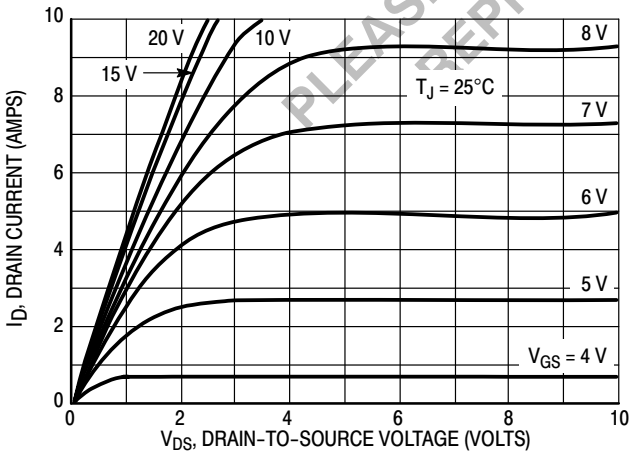


Figure 1. On Region Characteristics

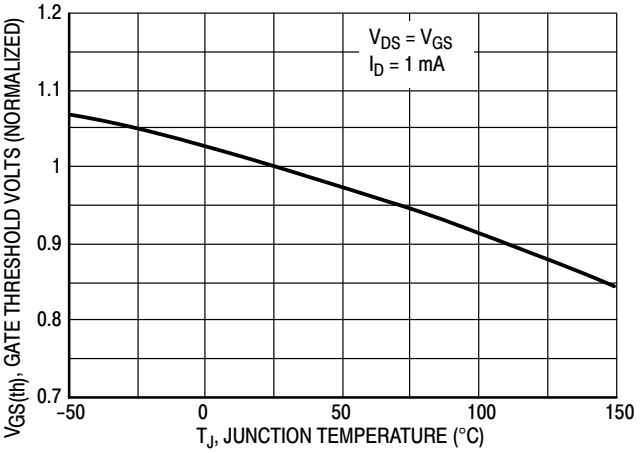


Figure 2. Gate−Threshold Voltage Variation With Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

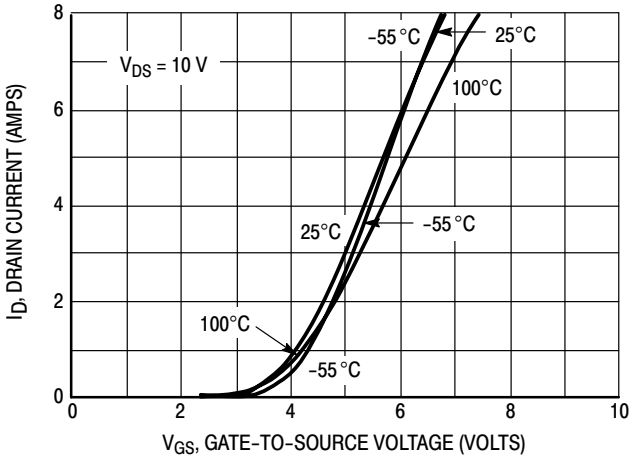


Figure 3. Transfer Characteristics

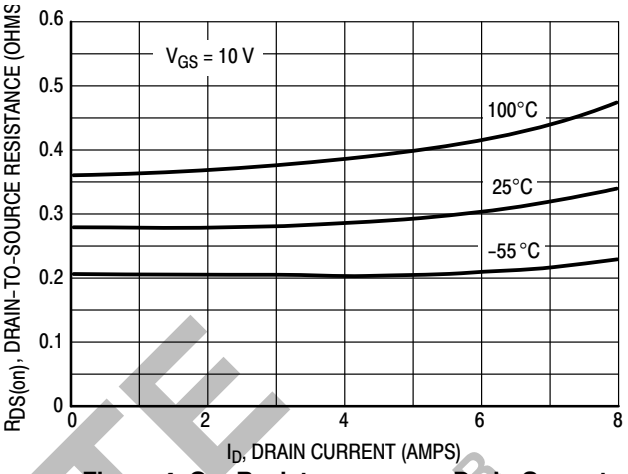


Figure 4. On−Resistance versus Drain Current

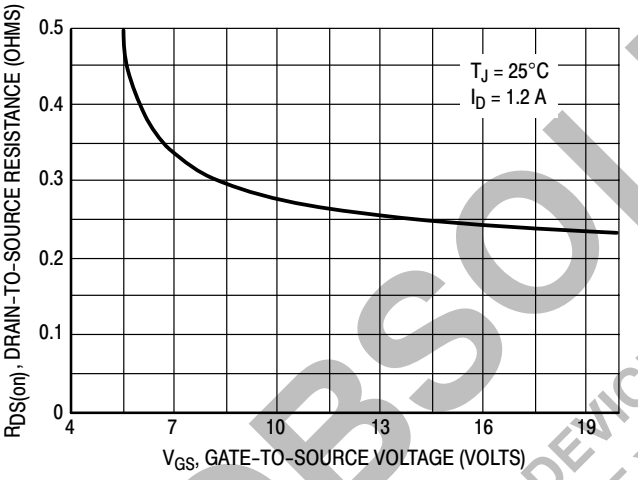


Figure 5. On−Resistance versus Gate−to−Source Voltage

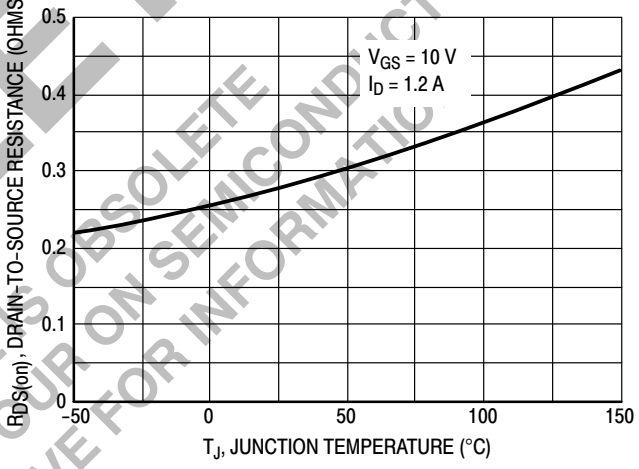


Figure 6. On−Resistance versus Junction Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance−General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, BVDSS. The switching SOA is applicable for both turn−on and turn−off of the devices for switching times less than one microsecond.

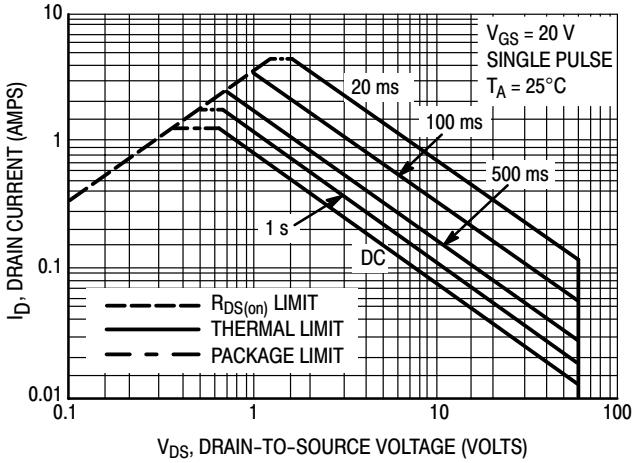


Figure 7. Maximum Rated Forward Biased Safe Operating Area

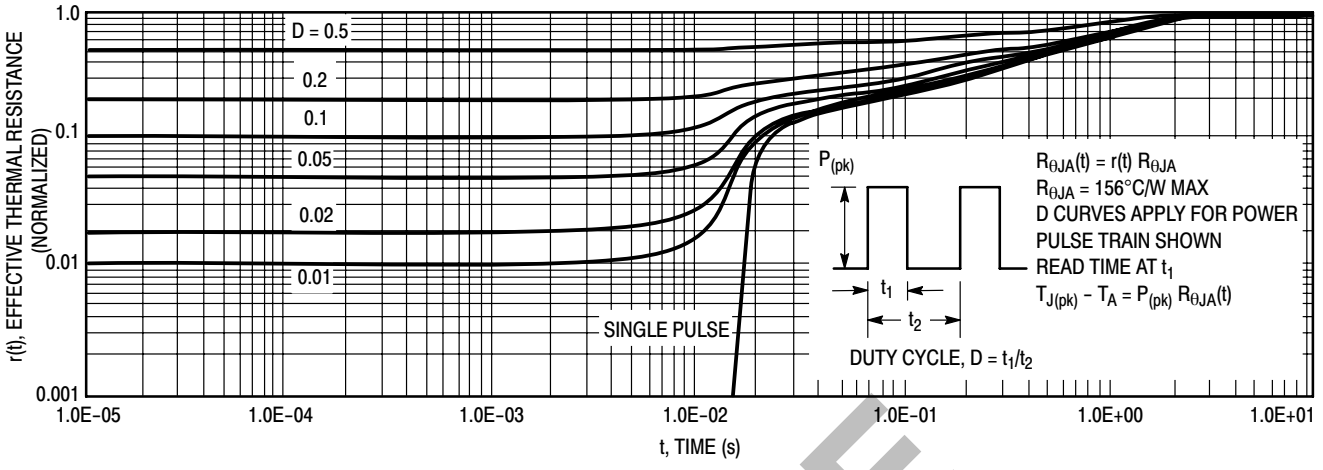


Figure 8. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source−drain current versus re−applied drain voltage when the source−drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half−bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain−to−source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source−drain diode current just prior to the onset of commutation.

V_R is specified at 80% rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in ON Semiconductor's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

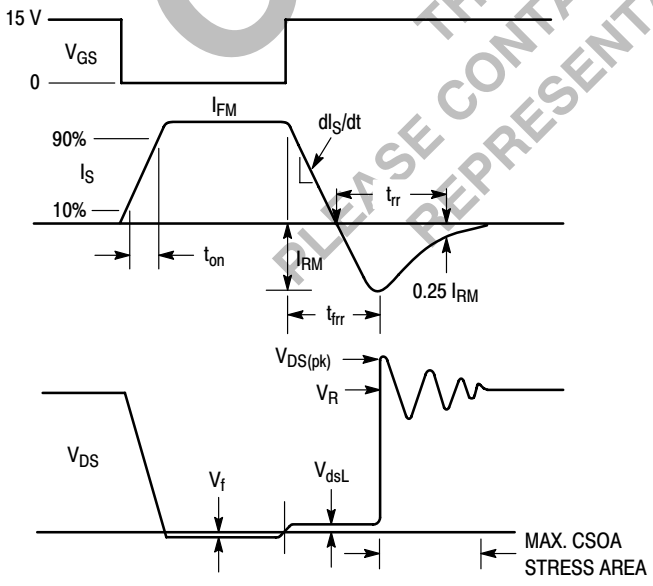


Figure 9. Commutating Waveforms

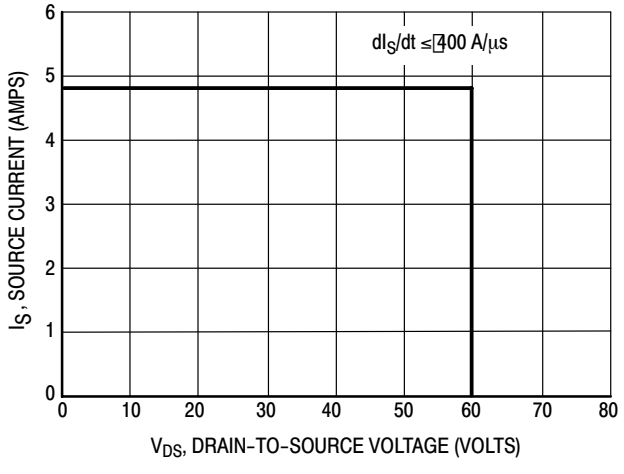


Figure 10. Commutating Safe Operating Area (CSOA)

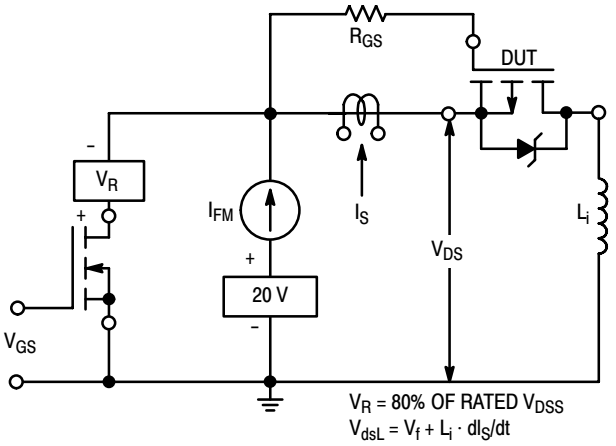


Figure 11. Commutating Safe Operating Area Test Circuit

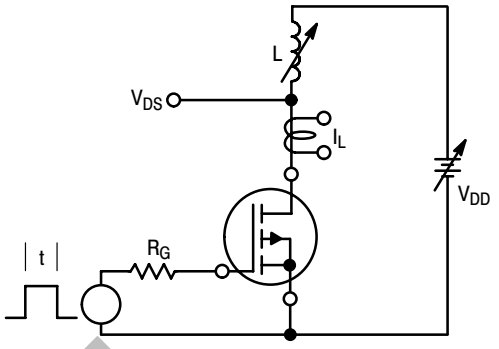


Figure 12. Unclamped Inductive Switching Test Circuit

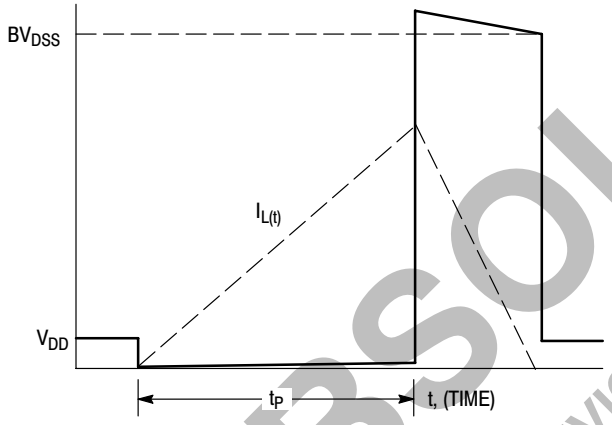


Figure 13. Unclamped Inductive Switching Waveforms

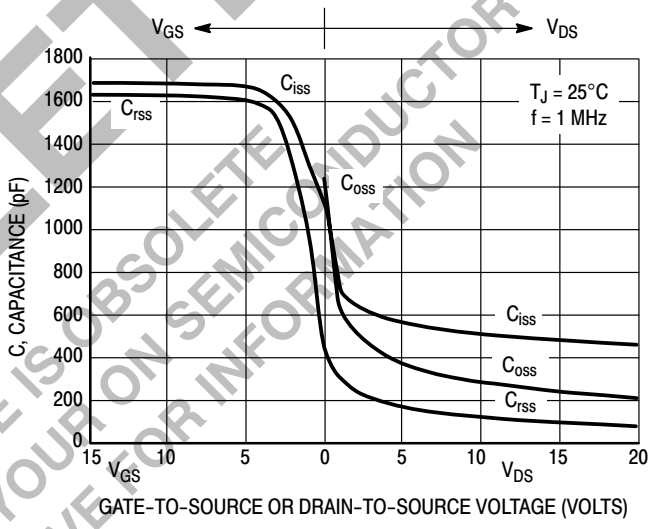


Figure 14. Capacitance Variation with Voltage

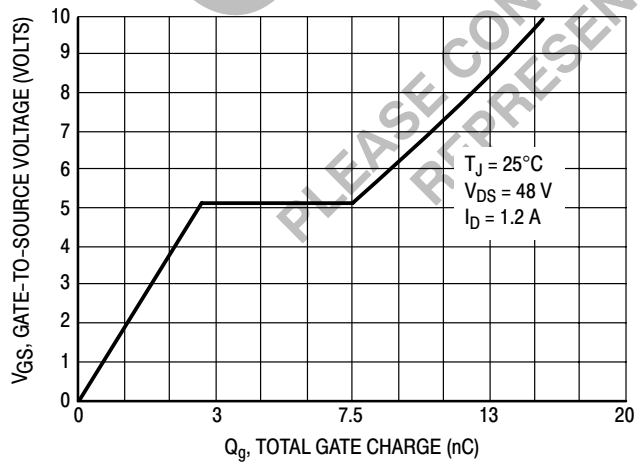


Figure 15. Gate Charge versus Gate−To−Source Voltage

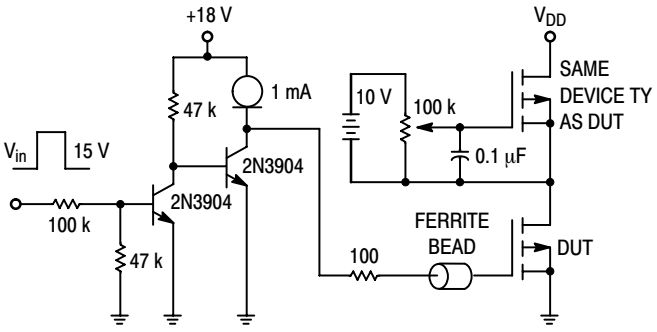
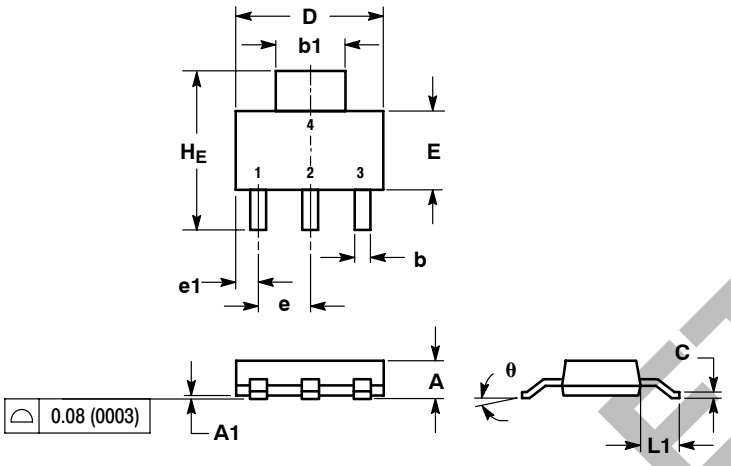


Figure 16. Gate Charge Test Circuit

MMFT2955E

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE L

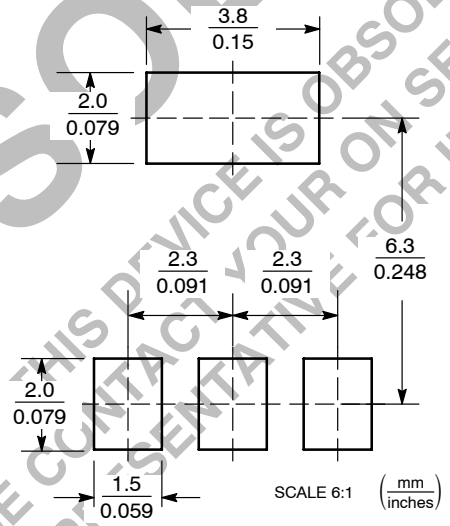


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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