FMN1xD5SBB-50IA

Stacked Multi-Chip Product
(NAND=1G, DDR=512M)

Document Title

Stacked Multi-Chip Product (NAND=1G, DDR=512M)

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Sep. 1st, 2014	Preliminary
0.1	Added Guarantee of the First block (NAND)	Oct. 27th, 2014	
0.2	Added 67B FBGA Ball Assignments of NAND	Nov. 1st, 2014	
0.3	Changed typical tPROG of NAND	Feb. 11th, 2015	
0.4	Added Block zero retention of NAND(1K with ECC)	Jun. 1st, 2015	
0.5	Modify general description for NAND and some alignment	Nov. 11st, 2019	
0.6	Modify several AC timing parameters	Feb, 10th, 2020	

Stacked Multi-Chip Product(MCP)

1.8V NAND Flash Memory and Mobile DDR

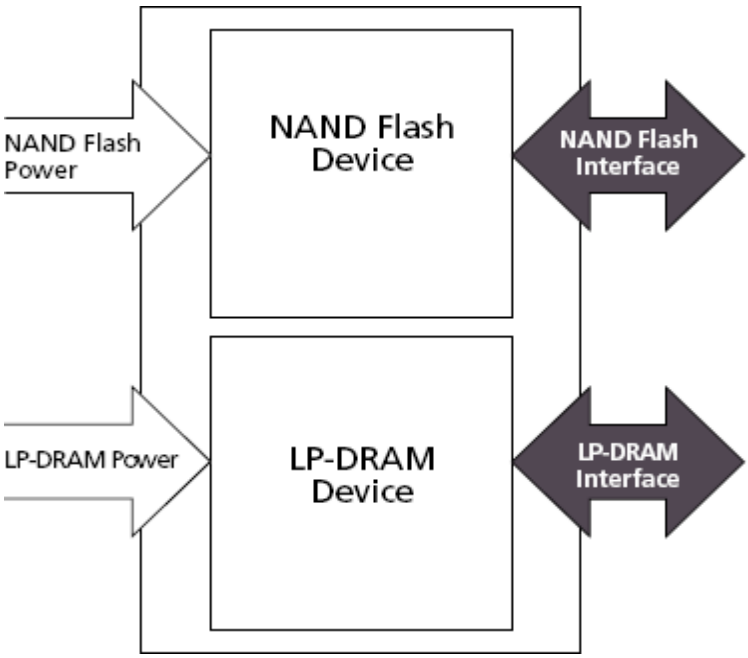
1. MCP Features

- Supply Voltages : 1.8V Operation
  - VCC : 1.7V~1.95V for Core/IO Power
- Operating Temperature Range
  - Industrial Part : -40°C ~ 85°C
- Package Type :
  - 130-ball FBGA, 8.0x9.0mm², 1.0T, 0.65mm Ball Pitch
  - Lead & Halogen Free

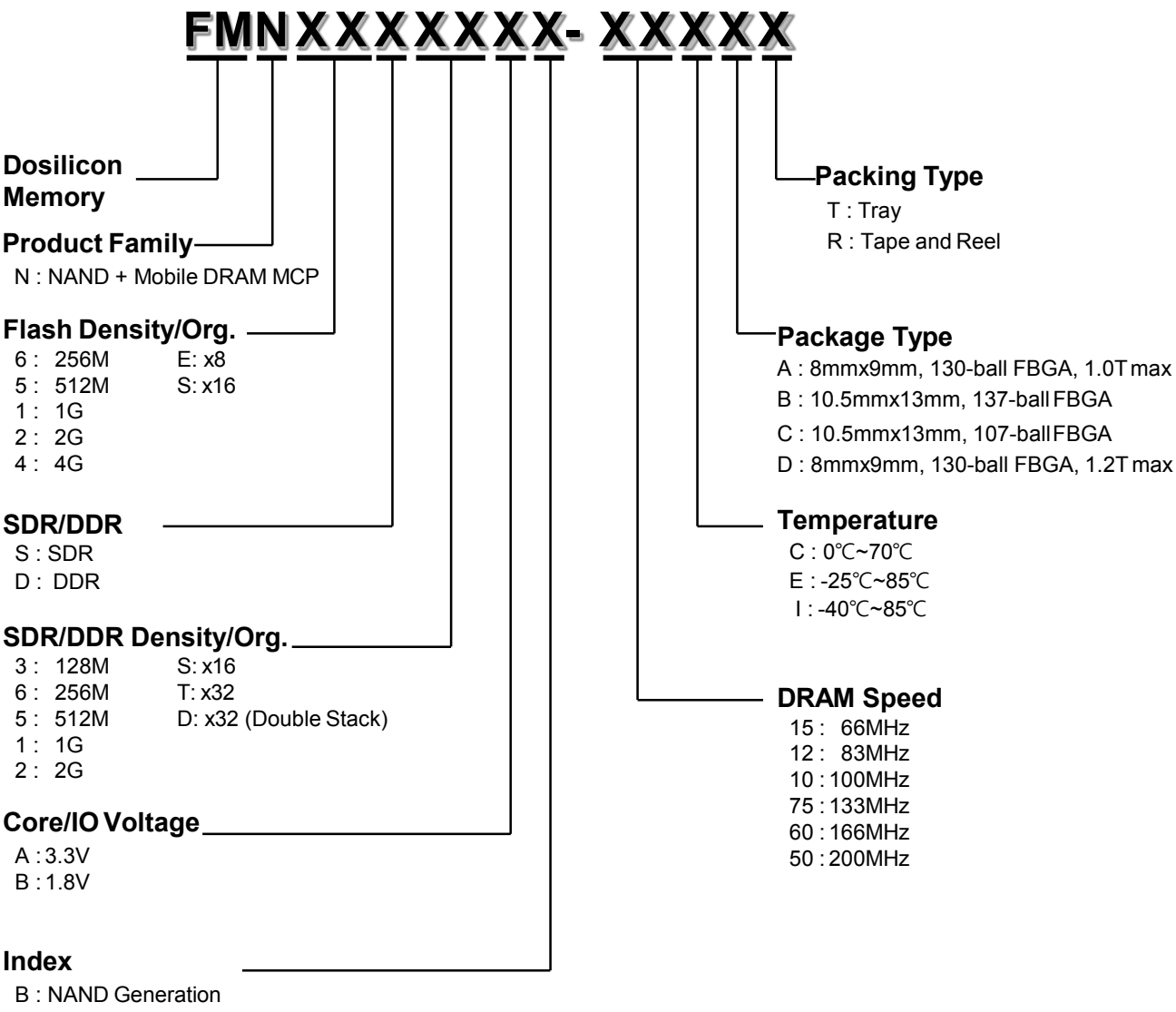
2. MCP Selection Guide

MCP Part Number	Flash	LP-DRAM	DRAM Freq.	Individual Datasheet		PKG Type
				Flash	LP-DRAM	
FMN1SD5SBB-50IA	1Gb x16	512Mb x16	200MHz	FMND1G16S3B	FMD8C16LAx-25Ex	130ball
FMN1ED5SBB-50IA	1Gb x8	512Mb x16	200MHz	FMND1G08S3B	FMD8C16LAx-25Ex	130ball

3. MCP Block Diagram

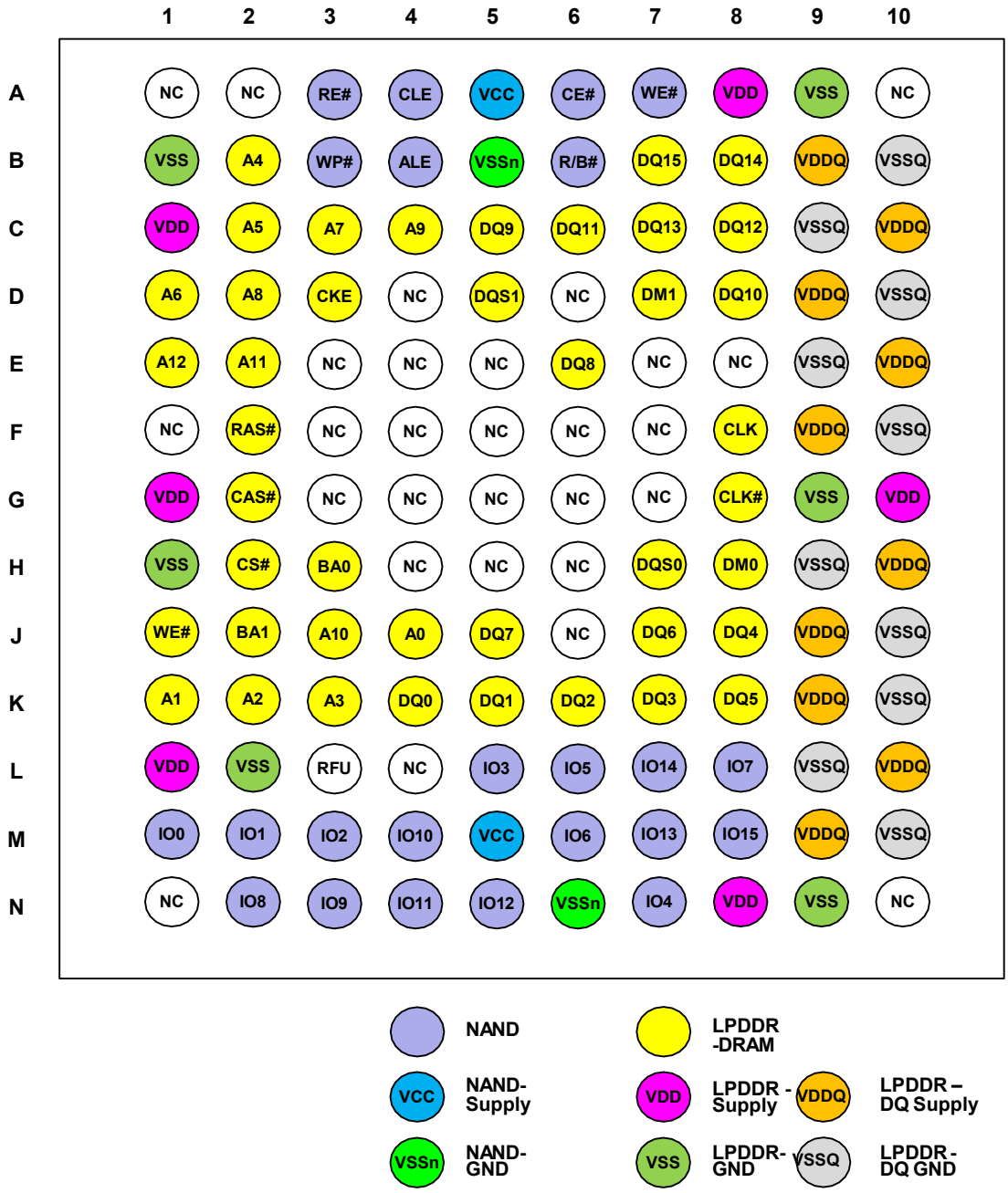


4. MCP Part Numbering System



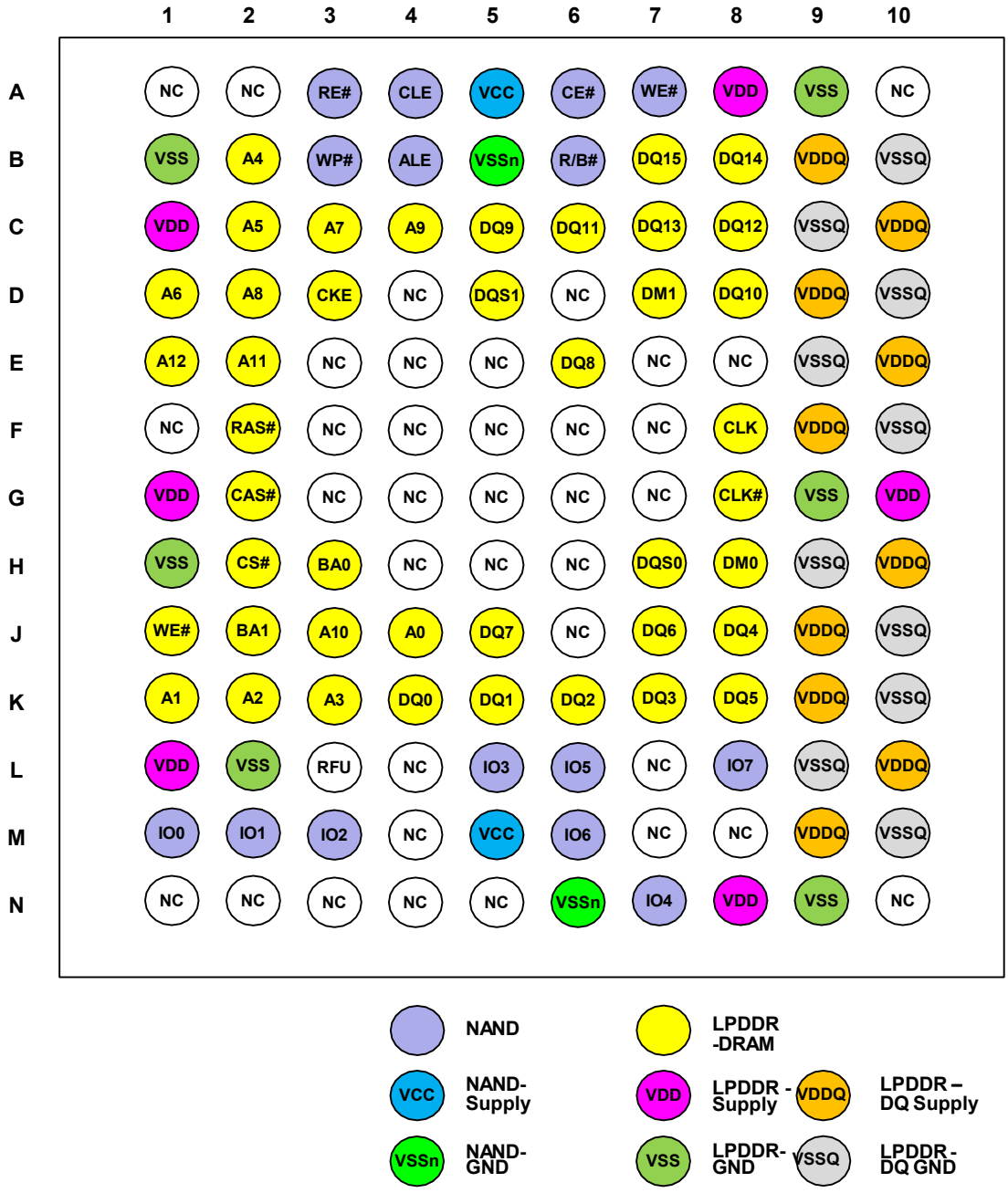
5-1. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND (x16) + DDR (x16)

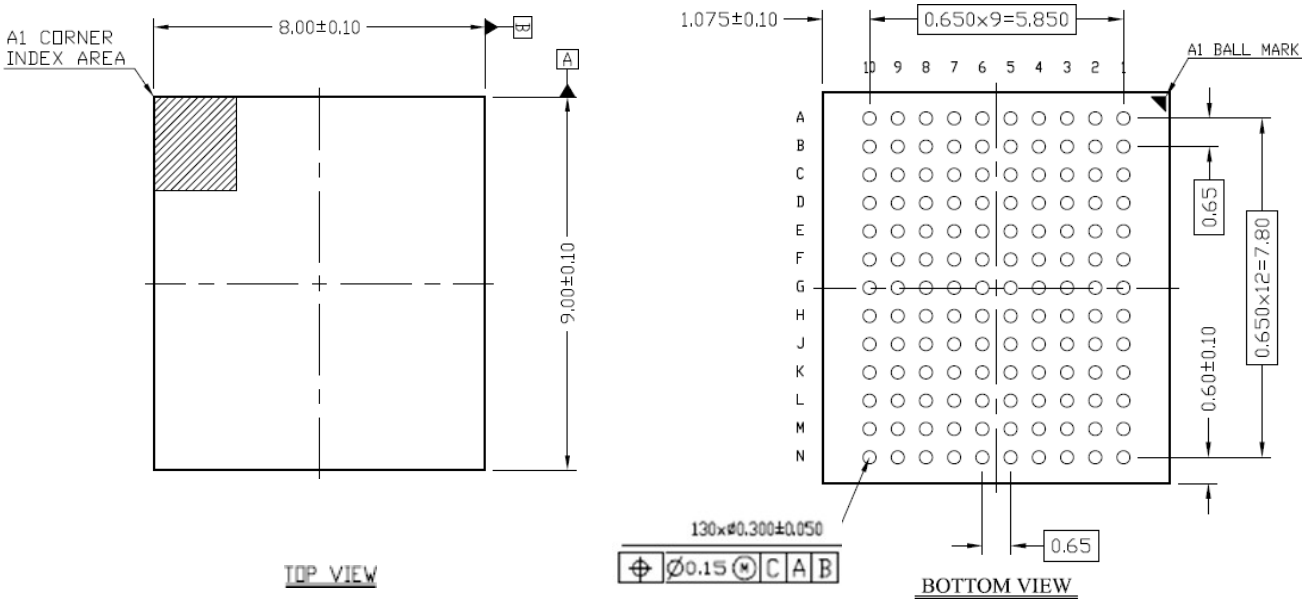


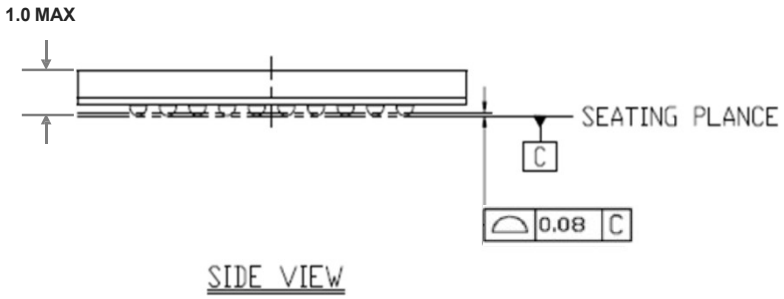
5-2. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND (x8) + DDR (x16)



5-3. 130-ball FBGA Package Dimension (8.0mm x 9.0mm)





FMND1GXXX3B

3V/1.8V, x8/x16 1G-BIT NAND FLASH

dosilicon

Documents title

1Gbit (128Mx8Bit, 64Mx16Bit) NAND FLASH

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Apr.05.2013	preliminary
0.1	Added 63B FBGA Ball Assignments Added ECC information	Sep.16.2013	
0.2	Updated operating voltage range of 1.8V device Added 63B FBGA package dimension	Oct.22.2013	
0.3	Changed ECC size	Aug.27.2014	
0.4	Added guarantee of the First block.	Oct.27.2014	
0.5	Added 67B FBGA Ball Assignments	Nov.1.2014	
0.6	Changed typical TPROG	Feb.11.2015	
0.7	Added Block zero retention(1K with ECC)	Jun.1.2015	Final

FEATURES

■ X8/X16 I/O BUS
— NAND Interface
— ADDRESS / DATA Multiplexing

■ SUPPLY VOLTAGE
— VCC = 1.8/2.7/3.3 Volt core supply voltage for Program, Erase and Read operations

■ PAGE READ / PROGRAM
— x8: (2048+64 spare) byte
— x16: (1024+32 spare) word page
— Synchronous Page Read Operation
— Random access: 25us (Max)
— Serial access: 45ns (1.8V)
25ns (2.7/3.0V)
— Page program time: 200us (Typ)

■ PAGE COPY BACK
— Fast data copy without external buffering

■ CACHE PROGRAM
— Internal buffer to improve the program throughput

■ READ CACHE

■ LEGACY/ONFI 1.0 COMMAND SET

■ FAST BLOCK ERASE
— Block size:
x8: (128K + 4K) bytes
x16: (64K+2K) words
— Block erase time: 2ms (Typ)

■ MEMORY CELL ARRAY
— x8: (2K + 64) bytes x 64 pages x 1024 blocks
– x16: (1K + 32) words x 64 pages x 1024 blocks

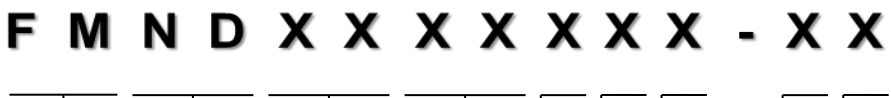
■ ELECTRONIC SIGNATURE
— Manufacturer Code
— Device Code

■ STATUS REGISTER

■ HARDWARE DATA PROTECTION

■ DATA RETENTION
— Cycling: 100K Program / Erase cycles
— Data retention: 10 Years (4bit/512byte ECC)
— Block zero is a valid block and will be valid for at least 1K program-erase cycles with ECC

Part Numbering System



Dosilicon Memory

Product Family
- ND : NAND

Density
- 28 : 128Mb
- 56 : 256Mb
- 12 : 512Mb
- 1G : 1Gb
- 2G : 2Gb
- 4G : 4Gb
- 8G : 8Gb
- 6G : 16Gb

Organization
- 08 : x8
- 16 : x16

Operation Voltage
- U : 3.3V
- L : 2.5V
- S : 1.8V

Package Type
- 0 : Bare Die
- W : KGD
- A : 12 x 20 mm^2 (TSOP1 48) H-ROHS & Halogen Free
- B : 12 x 17 mm^2 (ULGA 52) H-ROHS & Halogen Free
- C : 9 x 9 mm^2 (48 FBGA) H-ROHS & Halogen Free
- D : 9 x 11 mm^2 (63 FBGA) H-ROHS & Halogen Free
- F : 6.5 x 8 mm^2 (67 FBGA) H-ROHS & Halogen Free

Temperature
- C : Commercial (0°C~70°C)
- E : Extended (-25°C~85°C)
- I : Industrial (-40°C~85°C)

Generation
- B : 2nd

Classification
- 1 : SLC S/B
- 2 : MLC S/B
- 3 : SLC L/B
- 4 : MLC L/B

1 SUMMARY DESCRIPTION

FMND1GXXXXX is a **128Mx8bit** with spare **4Mx8 (x8), 64Mx16bit** with spare **2Mx16(x16)** bit capacity.
The device is offered in 3.3/1.8 Vcc Power Supply, and with x8 and x16 I/O interface.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains **1024 blocks**, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells.
Program operation allows the 2112-byte page writing in typical 200us and an erase operation can be performed in typical 2 ms on a 128K-byte block.
Data in the page can be read out at **25ns** cycle time per word **(2.7/3V version)**, and at **45ns** cycle time per word **(1.8V version)**. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP# input pin.
This device supports ONFI 1.0 specification.
The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal.

The **FMND1GXXXXX** is available in the following packages : 48 - TSOP1 12 x 20 mm package, **FBGA63 9 x 11 mm.**

1.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
FMND1G08S3B	X8	1.7 – 1.95 Volt	FBGA
FMND1G16S3B	X16	1.7 – 1.95 Volt	FBGA
FMND1G08L3B	X8	2.5 – 3.0 Volt	FBGA, TSOP
FMND1G16L3B	X16	2.5 – 3.0 Volt	FBGA, TSOP
FMND1G08U3B	X8	2.7 – 3.6 Volt	FBGA, TSOP
FMND1G16U3B	X16	2.7 – 3.6 Volt	FBGA, TSOP

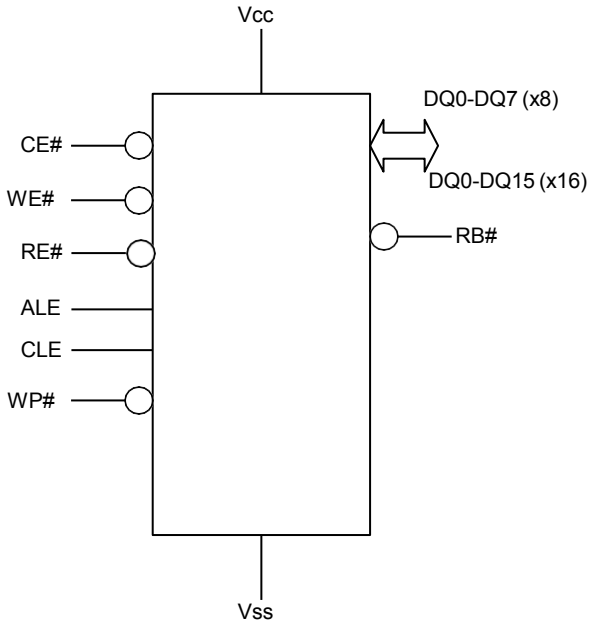


Figure 1: Logic Diagram

DQ7 - DQ0	Data Input / Outputs (x8/x16)
DQ15 – DQ8	Data Input / Outputs (x16)
CLE	Command latch enable
ALE	Address latch enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
RB#	Ready / Busy
Vcc	Power supply
Vss	Ground
NC	No Connection

Table 1: signal names

1.2 Pin description

Pin Name	Description
DQ0-DQ7(x8) **DQ0-DQ15(x16)**	DATA INPUTS/OUTPUTS The DQ pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE#). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	COMMAND LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	ADDRESS LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
CE#	CHIP ENABLE This input controls the selection of the device. When the device is busy CE# low does not deselect the memory.
WE#	WRITE ENABLE This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
RE#	READ ENABLE The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WP#	WRITE PROTECT The WP# pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
RB#	READY BUSY The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	SUPPLY VOLTAGE The VCC supplies the power for all the operations (Read, Write, Erase). An internal lock circuit prevent the insertion of Commands when V_{CC} is less than V_{LKO}
V_{SS}	GROUND
NC / DNU	NOT CONNECTED / DON'T USE

Table 2 : pin description

Notes:
1. A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3 Functional block diagram

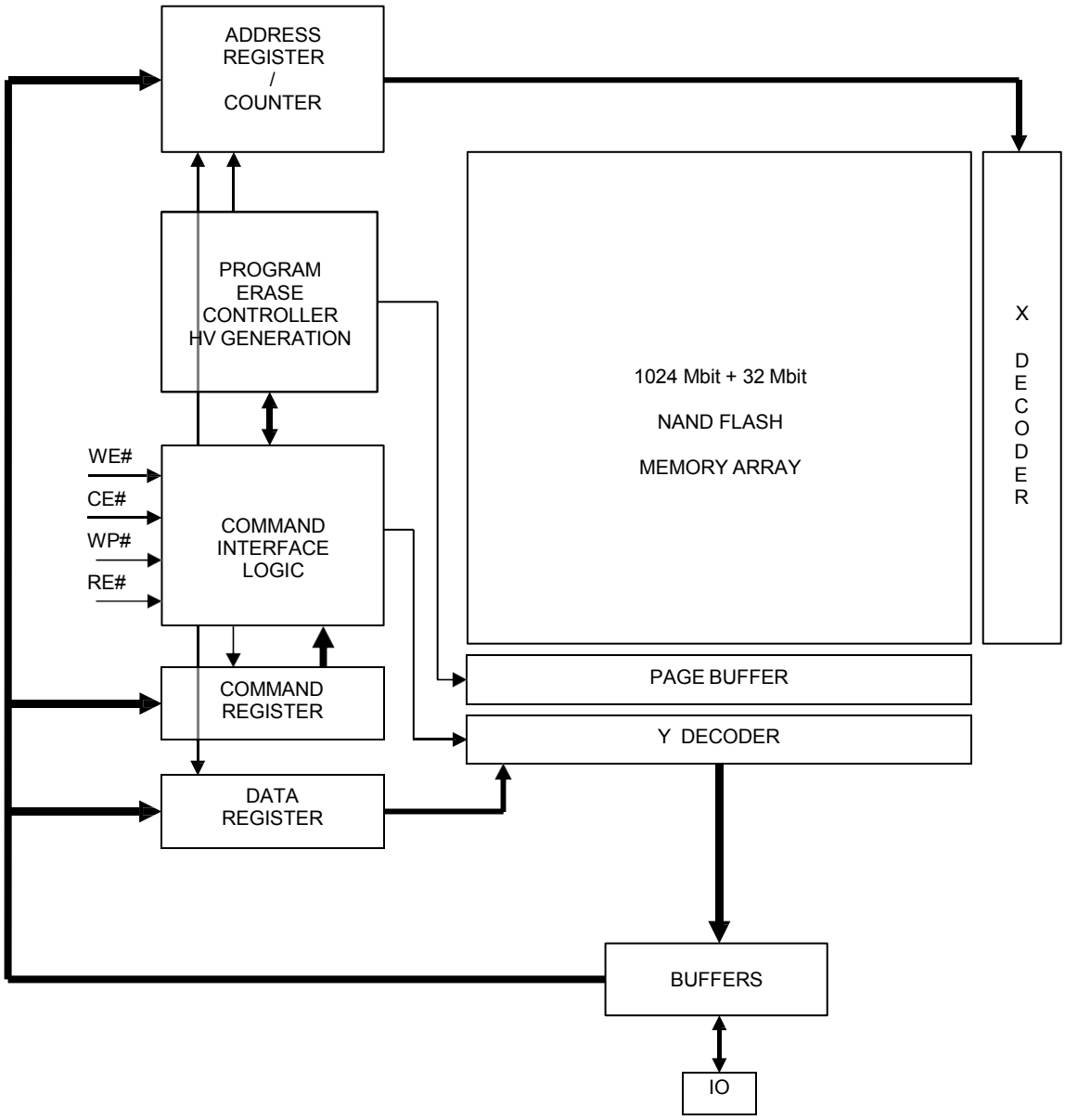


Figure 2 : block description

1.4 Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	0	0	0	0
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 3 : Address Cycle Map (x8)

A0 – A11 : byte (column) address in the page
A12 – A17 : page address in the block
A18 – A27 : block address

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	0	0	0	0	0
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26

Table 4 : Address cycle Map (x16)

A0 – A10 : word (column) address in the page
A11 – A16 : page address in the block
A17 – A26 : block address

1.5 Command Set

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PGM (start) / CACHE PGM (end)	80h	10h	-	-	
CACHE PGM (Start/continue)	80h	15h	-	-	
COPY BACK PGM	85h	10h	-	-	
BLOCK ERASE	60h	D0h	-	-	
READ STATUS REGISTER	70h	-	-	-	Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (SEQUENTIAL)	31h				
READ CACHE ENHANCED (RANDOM)	00h	31h	-	-	
READ CACHE END	3Fh	-	-	-	
READ PARAMETER PAGE	ECh				

Table 5 : Command Set

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L	H	Falling	X	Data Output (on going)	
X	X	L	H	H	X	Data Output (suspended)	
L	L	L	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V / V_{CC}	Stand By	

Table 6 : Mode Selection

2 BUS OPERATION

1. Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 3 and Table 19 for details of the timings requirements. Command codes are always applied on IO<7:0>, disregarding the bus configuration (X8/X16).

2. Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the **28 addresses** needed to access the **4 clock cycles (x8 version)** are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 4 and Table 19 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8/X16).

3. Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 5 and Table 19 for details of the timings requirements.

4. Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 6,7,8 and Table 19 for details of the timings requirements.

5. Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

6. Standby.

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

3 DEVICE OPERATION

1. Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing **00h** and **30h** to the command register along with **4** address cycles. In two consecutive read operations, the second one does need 00h command, which **4** address cycles and **30h** command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.
Two types of operations are available: random read , serial page read. The random read mode is enabled when the page address is changed. The **2112** bytes (X8 device) or **1056** words (X16 device) of data within the selected page are transferred to the data registers in less than **25us(tR).** The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in **25ns cycle time (3V version) or 45ns cycle time (1.8V version)** by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command.
The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.
Any operation other than read or random data output causes device to exit read mode.
Check Figure 9,10,11 as references.

2. Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in **3.1**, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.
The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read. Figure 12 defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure 13 defines the Read Cache behavior and timings for the end of cache operation.

3. Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112 (X8 device) or words up to 1056 (X16 device), in a single page program cycle.
A page program cycle consists of a serial data loading period in which up to **2112 bytes** (X8 device) or **1056 words** (X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command **(80h)**, followed by the **4** cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The

device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (**85h**). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command **(10h)** initiates the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 and Figure 15 detail the sequence.

4. Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "**35h**" command and the address of the source page moves the whole 2112byte (X8 device) or 1056word (X16 device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (**85h**) with the address cycles of destination page may be written. The Program Confirm command (**10h**) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 17.
Figure 16 and Figure 17 show the command sequence for the copy-back operation.

5. Cache Program

Cache Program is an extension of the standard page program which is executed with two 2112 bytes(x8 device) or 1056 words(x16 device) registers, the data and the cache register.
In short, the cache program allows data insertion for one page while program of another page is under execution.
Cache program is available only within a block.
After the serial data input command (80h) is loaded to the command register, followed by 4 cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (t_{PCBSY}). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The busy time following the first sequence 80h – 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.
In case of any subsequent sequence 80h – 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (t_{PCBSY}).
Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b)the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete
c)the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .

d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1".
I/O<1> may be read together with I/O<0> .
If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. Figure 18,19 detail the sequence.

6. Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command **(60h).** Only address **A18 to A27 (X8)** or **A17 to A26 (X16)** is valid while **A12 to A17 (X8) or A11 to A16 (X16) are ignored**. The Erase Confirm command (**D0h**) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify.
Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 20 details the sequence.

7. Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing **70h** command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to Table 7 for specific Status Register definitions, and Figure 8 for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (**00h**) should be given before starting read cycles.

3.8 Read Status Register field definition

Table below lists the meaning of each bit of Read Status Register and Read Status Enhanced

IO	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass/Fail	N page Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass/Fail	N-1page Pass: '0' Fail: '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Active: '0' Idle:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data cache Read/Busy Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 7 : Status Register Coding

3.9 Read ID.

The device contains a product identification mode, initiated by writing **90h** to the command register, followed by an address input of 00h.

DENSITY	ORG.	VCC	1st	2nd	3rd	4th (1)
1Gbit	X8	3.0V	F8h	F1h	80h	91h
	X16	3.0V	00F8h	C1h	80h	D1h
	X8	1.8V	F8h	A1h	80h	11h
	X16	1.8V	00F8h	B1h	80h	51h

Table 8: Read ID for supported configurations

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type,….
4th	Page Size, Block Size, Spare Size, Organization

Table 9 : Read ID bytes meaning

	Description	DQ7	DQ6	DQ5-4	DQ3-2	DQ1-0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of simultaneously programmed pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleaved program between multiple dice	Not Supported Supported		0 1			
Cache Program	Not Supported Supported	0 1				

Table 10 : 3rd byte of Device Identifier Description

	Description	DQ7	DQ6	DQ5-4	DQ3	DQ2	DQ1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512 Byte)	16 32					0 1	
Block Size (Without Spare Area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				
Serial Access Time	50ns/45ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

Table 11 : 4th Byte of Device Identifier Description

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 22 shows the operation sequence .

3.10 Reset.

The device offers a reset feature, executed by writing **FFh** to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command

register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to Table 7 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written (see Figure 23).

11. Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. Figure 24 defines the Read Parameter Page behavior.
Values in the parameter page are static and shall not change. The host is not required to read the parameter page after power management events.
The Change Read Column command can be issued during execution of the Read Parameter Page to read specific portions of the parameter page.
Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

12. Parameter Page Data Structure Definition

Table 12 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data *bytes* are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use.
Unused fields should be cleared to 0h.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Byte	O/M	Description
		Revision information and features block
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache 18ntegrit 0 1 = supports Page Cache Program command
10-31		Reserved (0)
		Manufacturer information block

Byte	O/M	Description
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-163		Reserved (0)

Byte	O/M	Description
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Table 12 : Parameter page data

Note : "O" stands for Optional, "M" for Mandatory

4 Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	1004		1024	Blocks

Table 13: Valid Blocks Number

The First block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over lifetime.

Symbol	Parameter	Value			Unit
		1.8V	2.7V	3.0V	
T_A	Ambient Operating Temperature (Temperature Range Option 1)	0 to 70	0 to 70	0 to 70	°C
	Ambient Operating Temperature (Temperature Range Option 6)	–40 to 85	–40 to 85	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	–50 to 125	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	–65 to 150	–65 to 150	°C
V_{IO}	Input or Output Voltage	–0.6 to 2.7	–0.6 to 4.6	–0.6 to 4.6	V
V_{CC}	Supply Voltage	–0.6 to 2.7	–0.6 to 4.6	–0.6 to 4.6	V

Table 14: Absolute maximum ratings

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Parameter		Symbol	Test Conditions	1.8Volt			2.7Volt			3.0Volt			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC} = 50ns, CE#=V_{IL}, I_{OUT}=0mA	-	10	20	-	15	30	-	15	30	mA
	Program	I_{CC2}	-	-	10	20	-	15	30	-	15	30	mA
	Erase	I_{CC3}	-	-	10	20	-	15	30	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	-		1			1	mA
Stand-By Current (CMOS)		I_{CC5}	CE#=V_{CC}-0.2, WP#=0/V_{CC}	-	10	50	-	10	50		10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vc (max)	-	-	±10	-	-	±10		-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10		-	±10	uA
Input High Voltage		V_{IH}	-	0.8x V_{CC}	-	V_{CC} +0.3	0.8x Vcc	-	V_{CC} +0.3	0.8x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2x V_{CC}	-0.3	-	0.2x V_{CC}	-0.3	-	0.2x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = -100uA	V_{CC}-0.1	-	-	V_{CC}-0.4	-	-				V
			I_{OH} = -400uA							2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 100uA	-	-	0.1	-	-	0.4				V
			I_{OL} = 2.1mA							-	-	0.4	V
Output Low Current (RB#)		I_{OL} (RB#)	V_{OL}=0.1V	3	4	-	3	4	-				mA
			V_{OL}=0.4V							8	10	-	mA

Table 15: DC and Operating Characteristics

Parameter	Value		
	1.8Volt	2.7Volt	3.0Volt
Input Pulse Levels	0V to V_{CC}	0V to V_{CC}	0V to V_{CC}
Input Rise and Fall Times	5ns	5ns	5ns
Input and Output Timing Levels	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
Output Load (1.7V – 1.95V & 2.5V - 3.6V)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF

Table 16: AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance (1)	C_{IN}	V_{IN} = 0V	-	10	pF

Table 17 : Pin Capacitance (TA = 25C, f=1.0MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	700	us
Cache program short busy time		t_{PCBSY}		3	t_{PROG}	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	4	Cycle
Block Erase Time		t_{BERS}	-	2.0	10	ms
Read Cache busy time		t_{RCBSY}		3	t_R	us

Table 18: Program / Erase Characteristics

Parameter	Symbol	1.8 Volt		2.7 Volt		3.0 Volt		Unit
		Min	Max			Min	Max	
CLE Setup time	t_{CLS}	10		10		10		ns
CLE Hold time	t_{CLH}	5		5		5		ns
CE# Setup time	t_{CS}	20		15		15		ns
CE# Hold time	t_{CH}	5		5		5		ns
WE# Pulse width	t_{WP}	15		10		10		ns
ALE Setup time	t_{ALS}	10		10		10		ns
ALE Hold time	t_{ALH}	5		5		5		ns
Data Setup time	t_{DS}	10		7		7		ns
Data Hold time	t_{DH}	5		5		5		ns
Write Cycle time	t_{WC}	45		25		25		ns
WE# High Hold time	t_{WH}	10		7		7		ns
Address to Data Loading time	t_{ADL}	100		70		70		ns
Data Transfer from Cell to Register	t_{R}		25		25		25	us
ALE to RE# Delay	t_{AR}	10		10		10		ns
CLE to RE# Delay	t_{CLR}	10		10		10		ns
Ready to RE# Low	t_{RR}	20		20		20		ns
RE# Pulse Width	t_{RP}	15		10		10		ns
WE# High to Busy	t_{WB}		100		100		100	ns
Read Cycle Time	t_{RC}	45		25		25		ns
RE# Access Time	t_{REA}		30		16		16	ns
CE# Access Time	t_{CEA}		45		25		25	ns
RE# High to Output Hi-Z	t_{RHZ}		100		100		100	ns
CE# High to Output Hi-Z	t_{CHZ}		30		30		30	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10		10		10		ns
RE# High to Output Hold	t_{RHOH}	15		15		15		ns
RE# Low to Output Hold	t_{RLOH}	-		5		5		ns
CE# High to Output Hold	t_{COH}	15		15		15		ns
RE# High Hold Time	t_{REH}	10		7		7		ns
Output Hi-Z to RE# Low	t_{IR}	0		0		0		ns
RE# High to WE# Low	t_{RHW}	100		100		100		ns
WE# High to RE# Low	t_{WHR}	60		60		60		ns
Device Resetting Time (Read/Program/Erase)	t_{RST}		5/10/ 500 (1)		5/10/ 500 (1)		5/10/ 500 (1)	us
Write protection time	t_{WW}	100		100		100		ns

Table 19 : AC Timing Characteristics

NOTE:
(1) If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us

5 Timing Diagrams

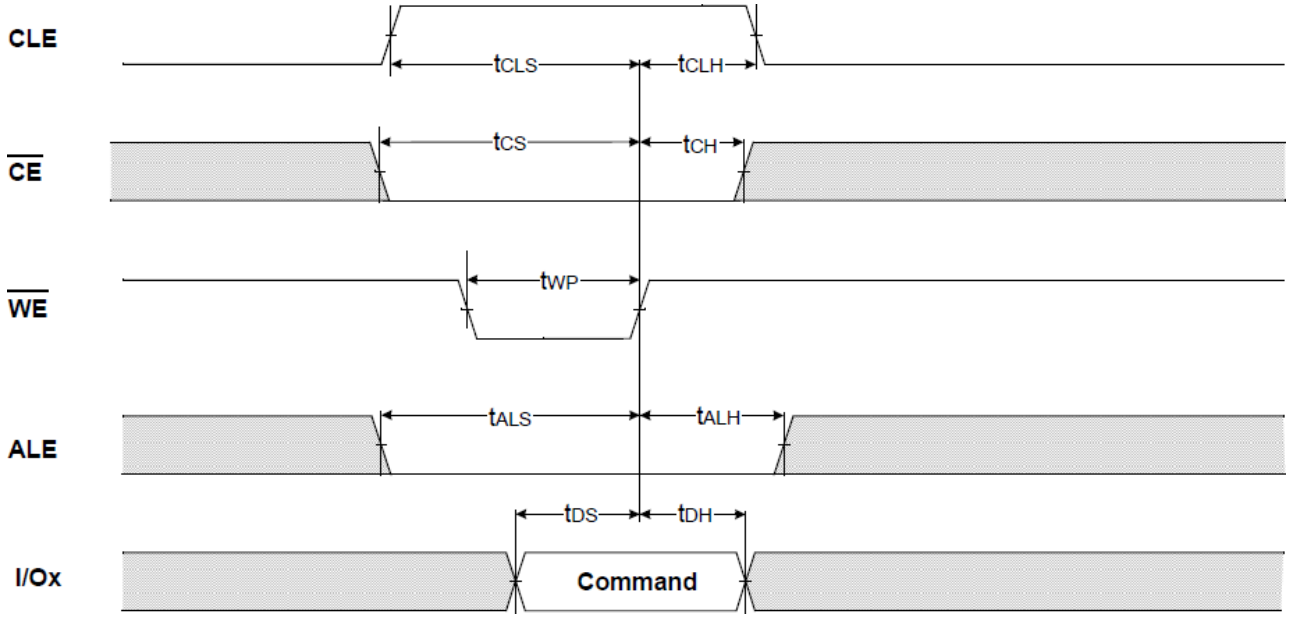


Figure 3 : Command Latch Cycle

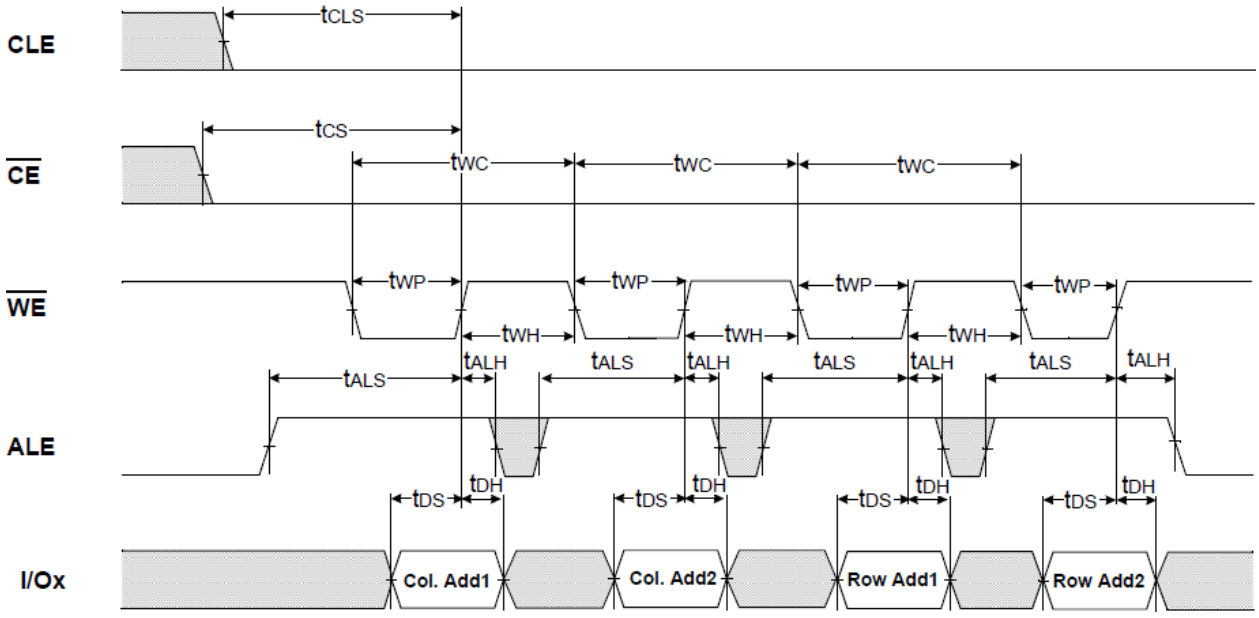


Figure 4 : Address Latch Cycle

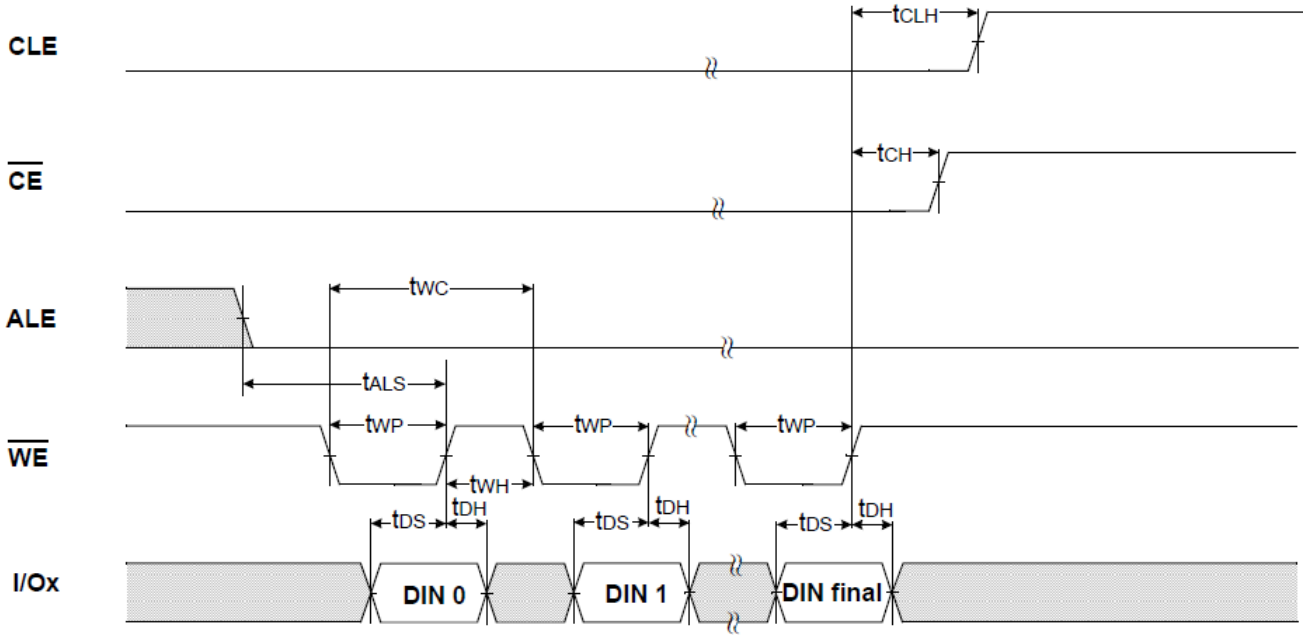
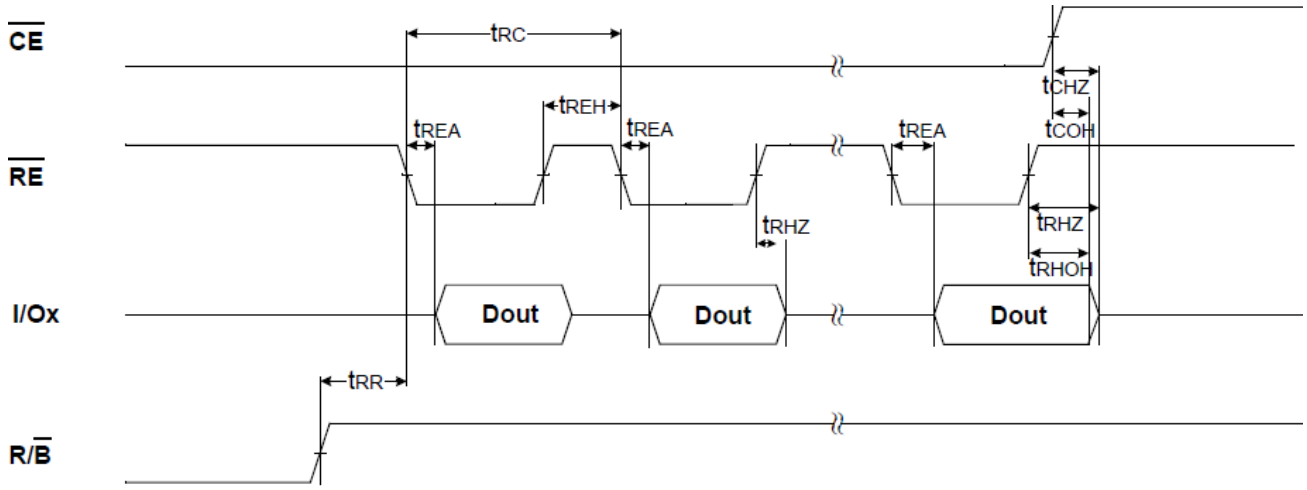
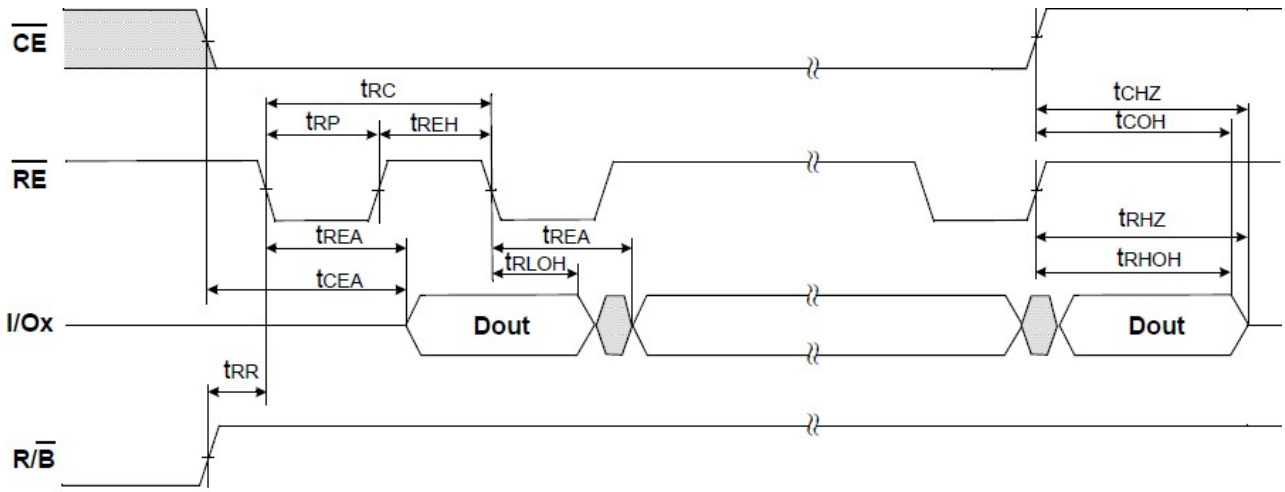


Figure 5 : Input Data Latch Cycle



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 6 : Sequential Out Cycle after Read



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 7 : Sequential Out Cycle after Read

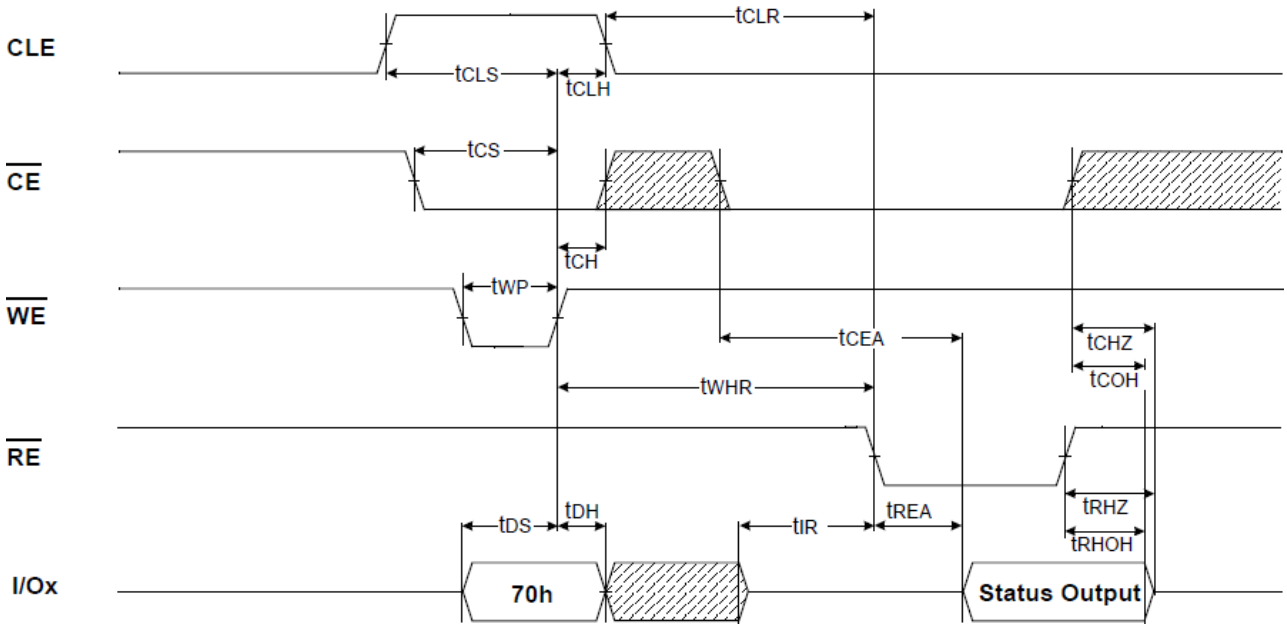


Figure 8 : Status Read Cycle

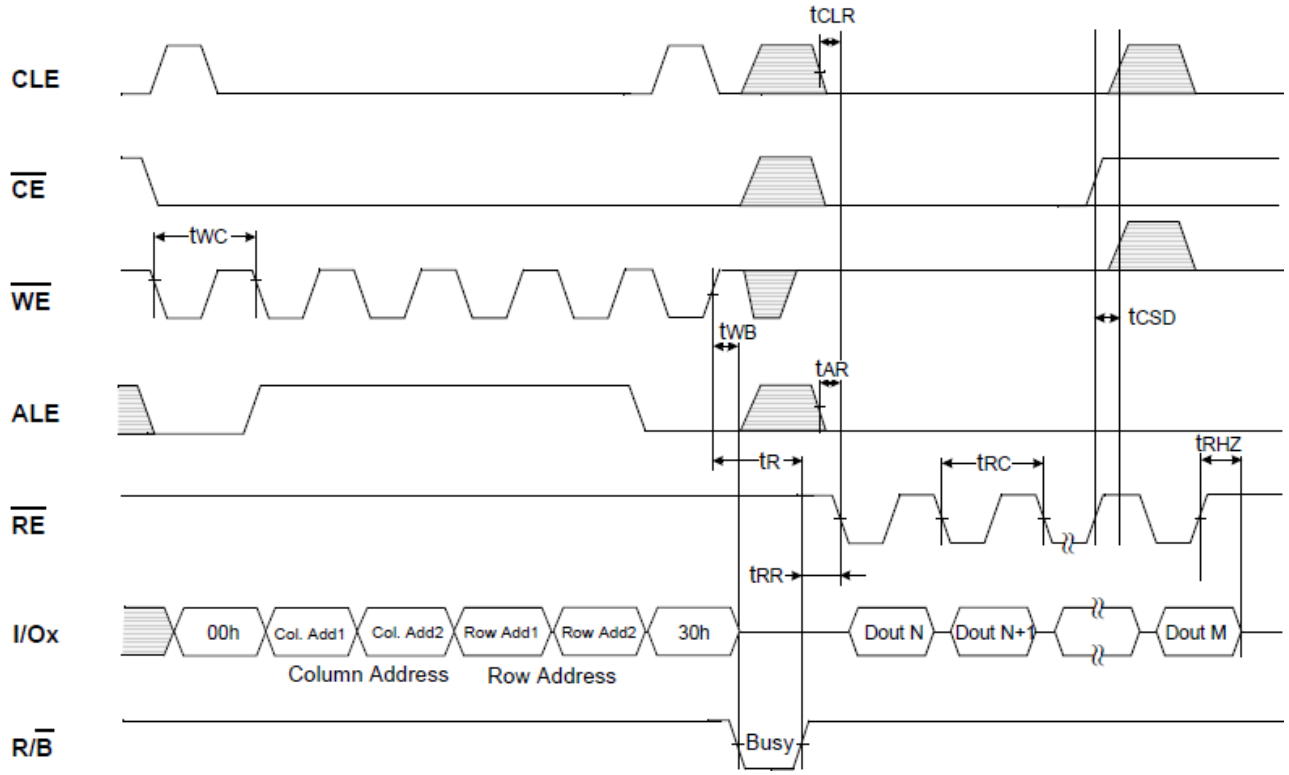


Figure 9 : Read Operation (Read One Page)

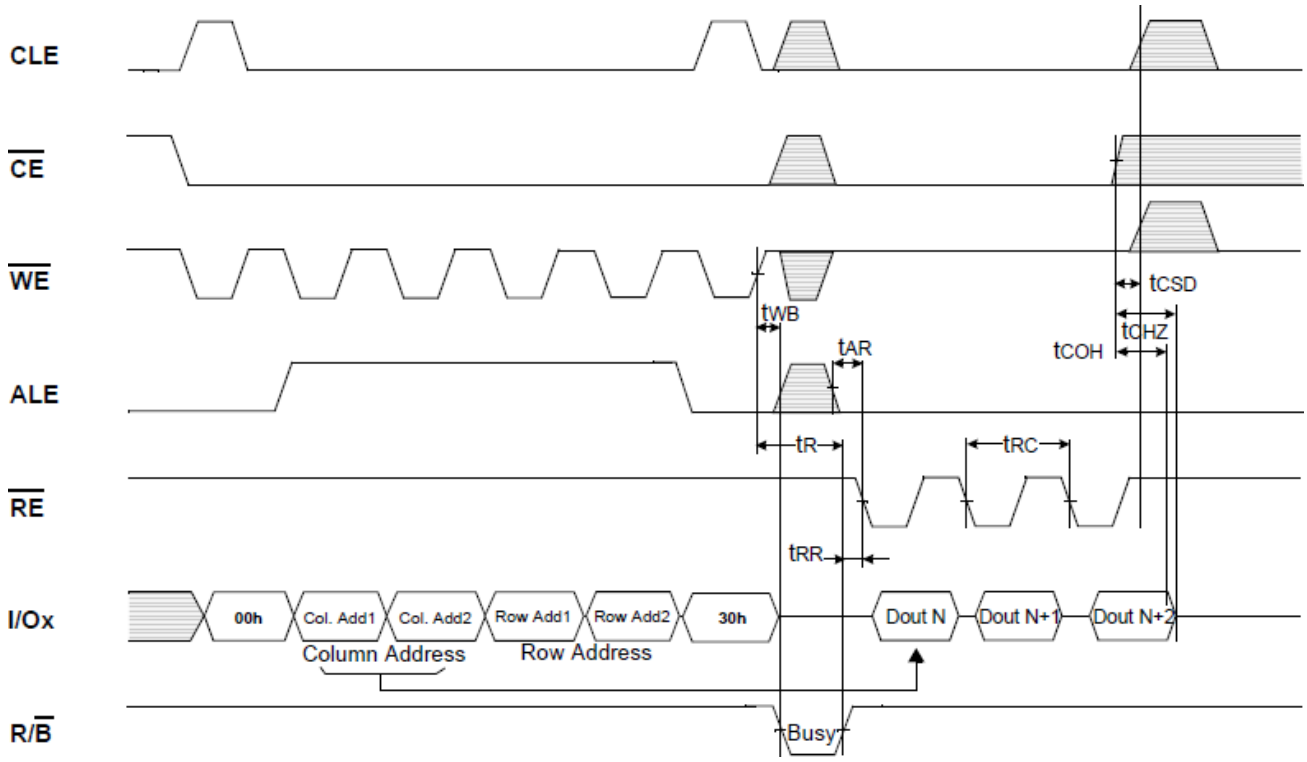


Figure 10 : Read Operation intercepted by CE#

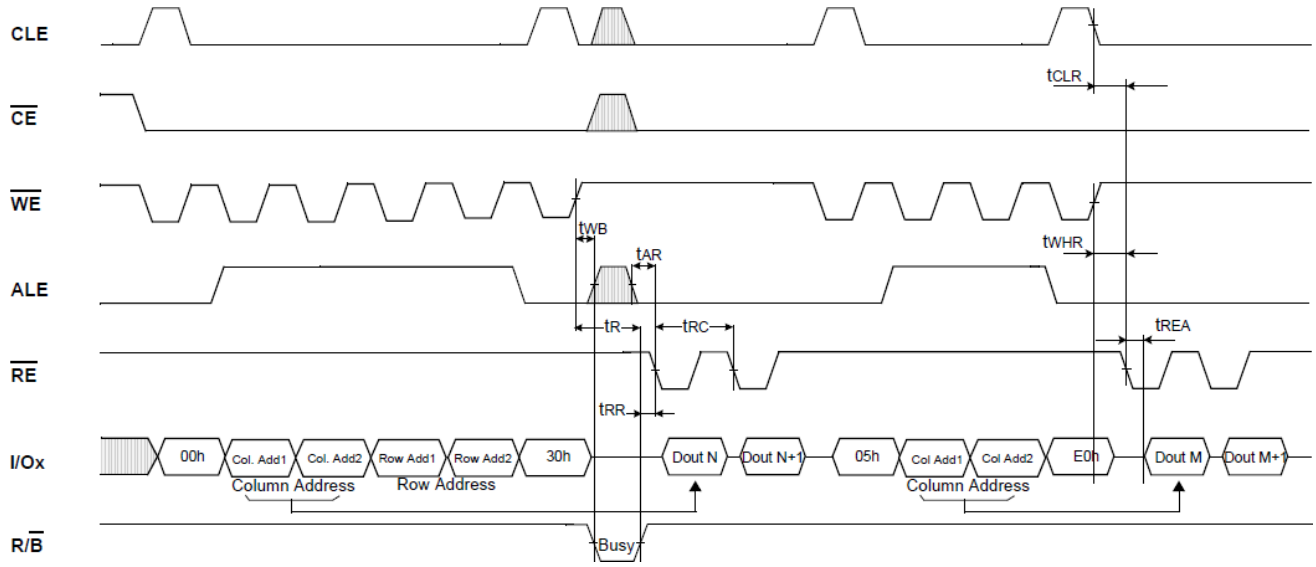


Figure 11 : Random Data Output

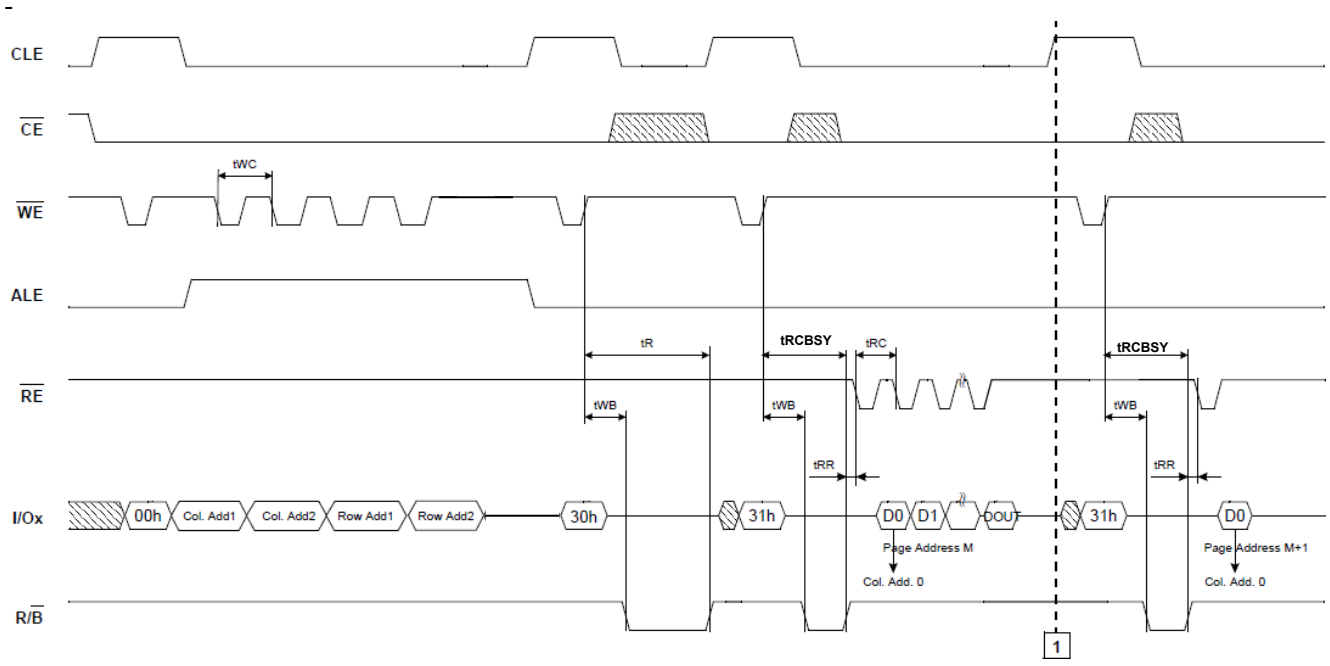


Figure 12 : read cache timings, start of cache operation

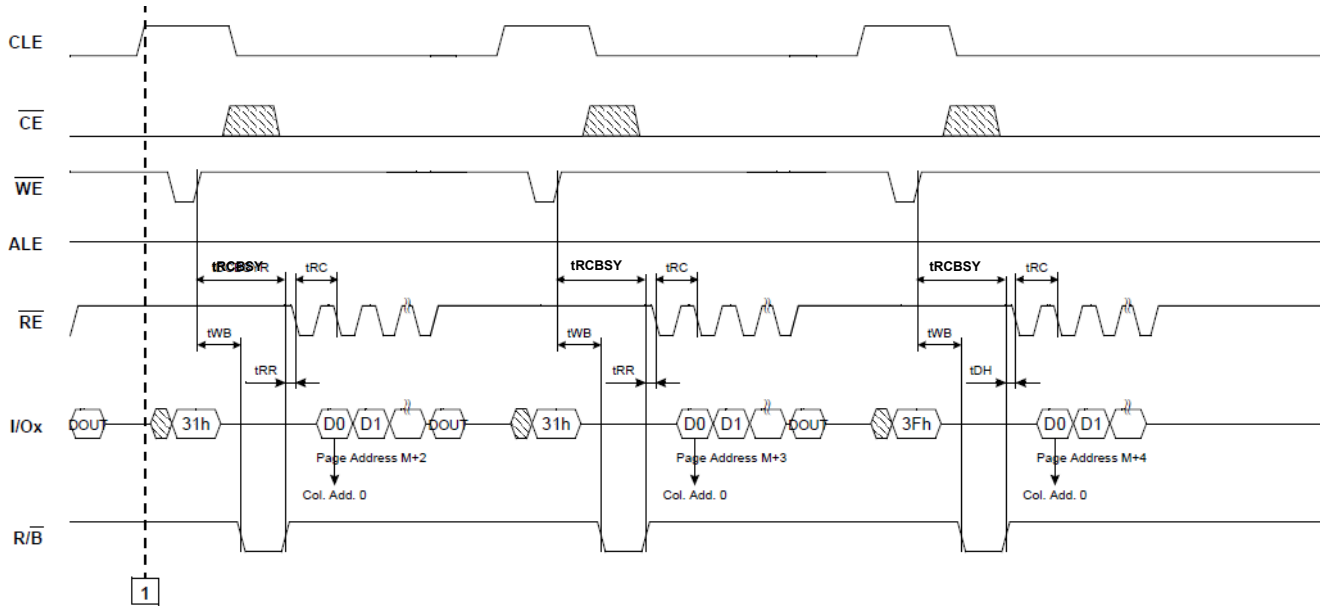


Figure 13 : read cache timings, end of cache operation

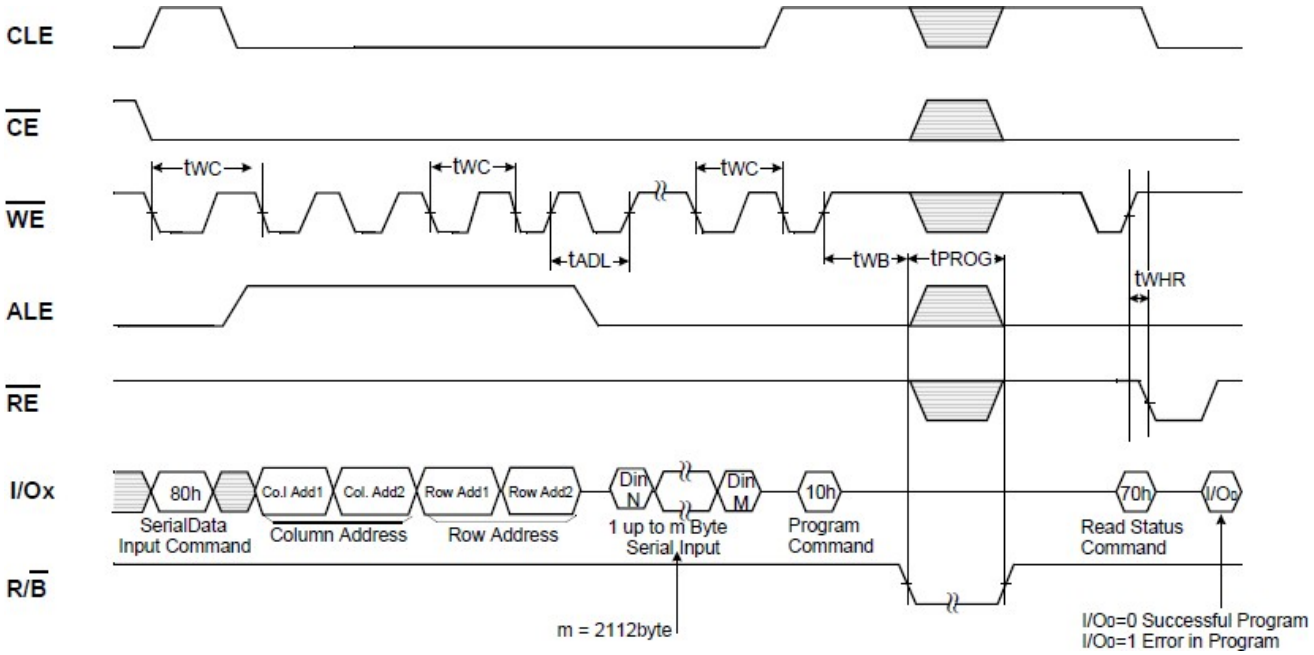


Figure 14 : Page Program Operation

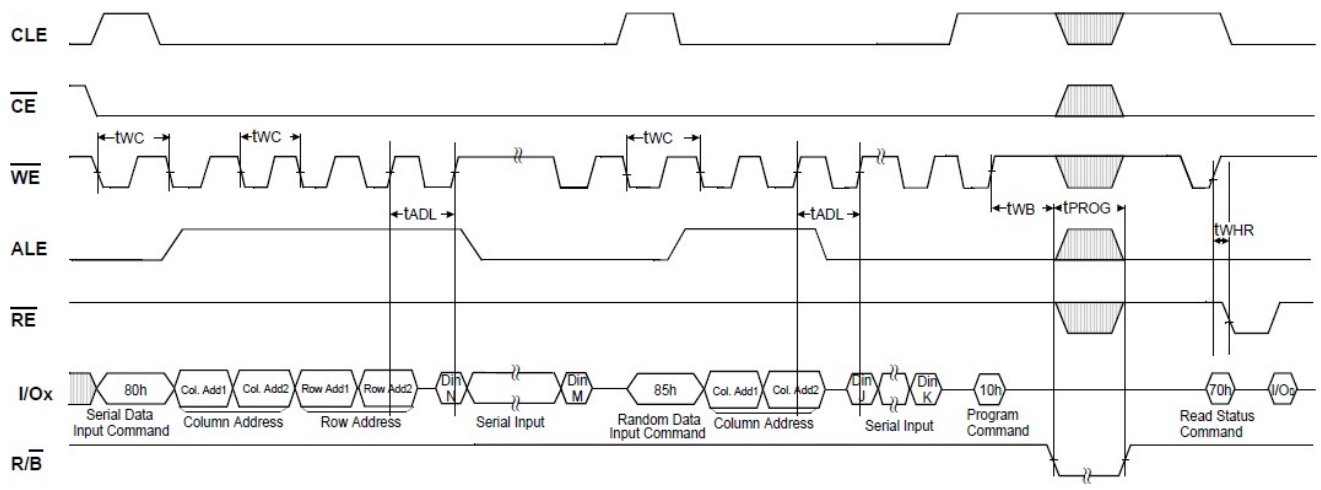


Figure 15 : Random Data In

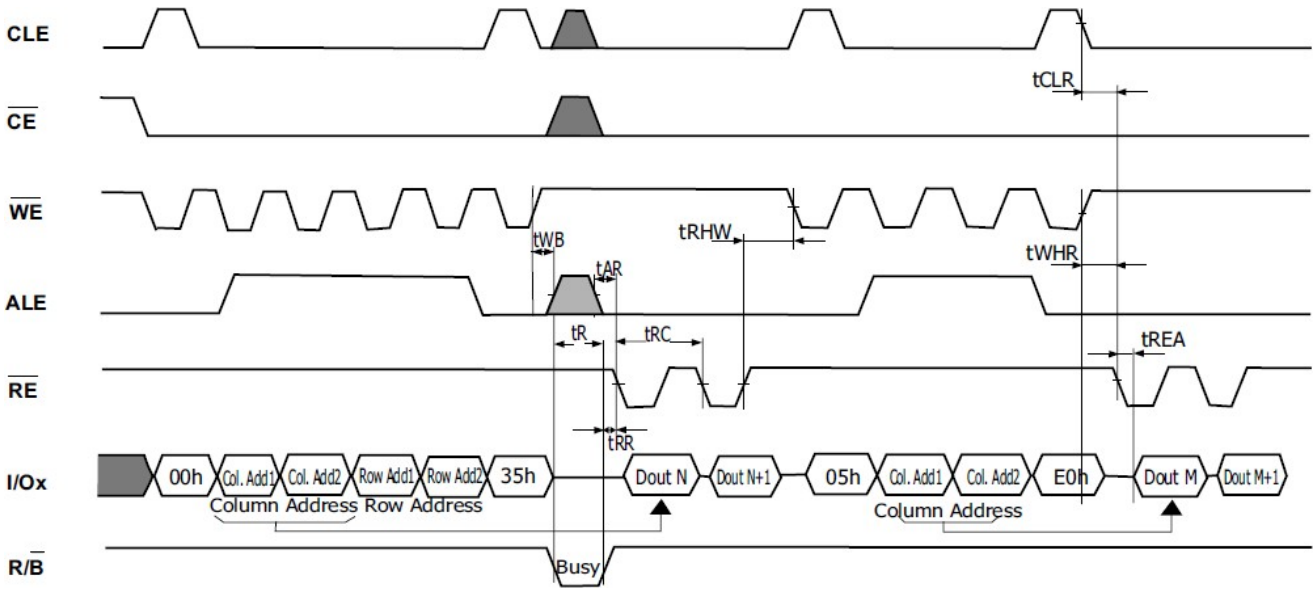


Figure 16 : Copy Back read with optional data readout

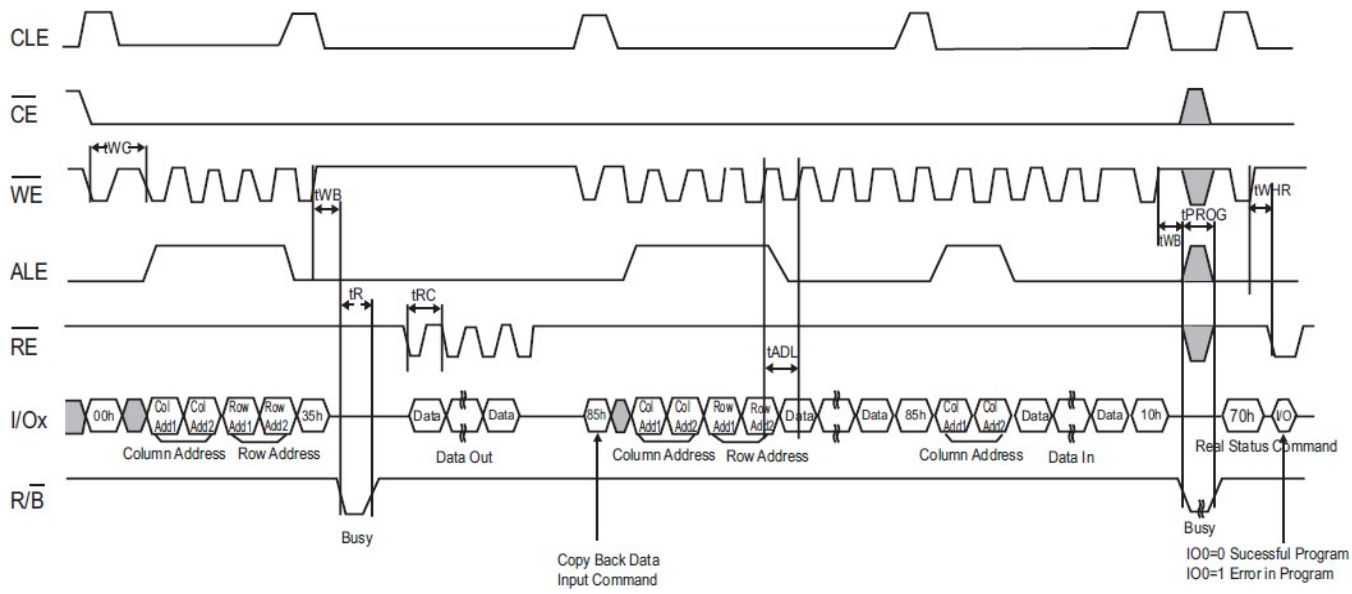


Figure 17 : Copy Back Program with Random Data Input

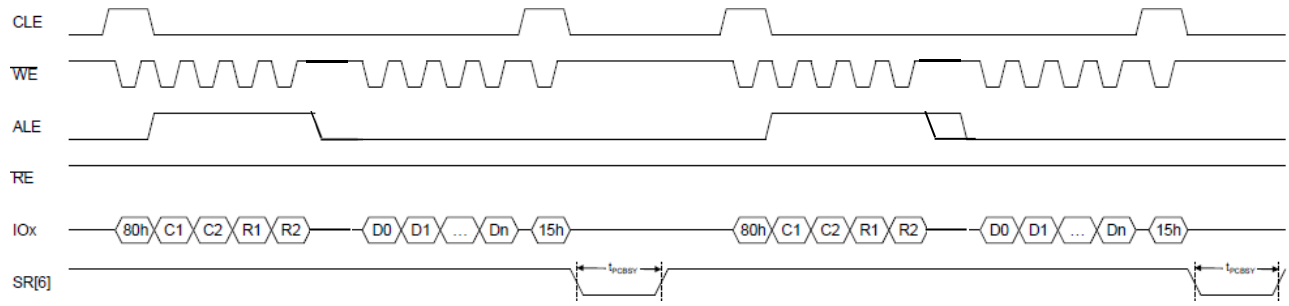


Figure 18: Cache Program Start

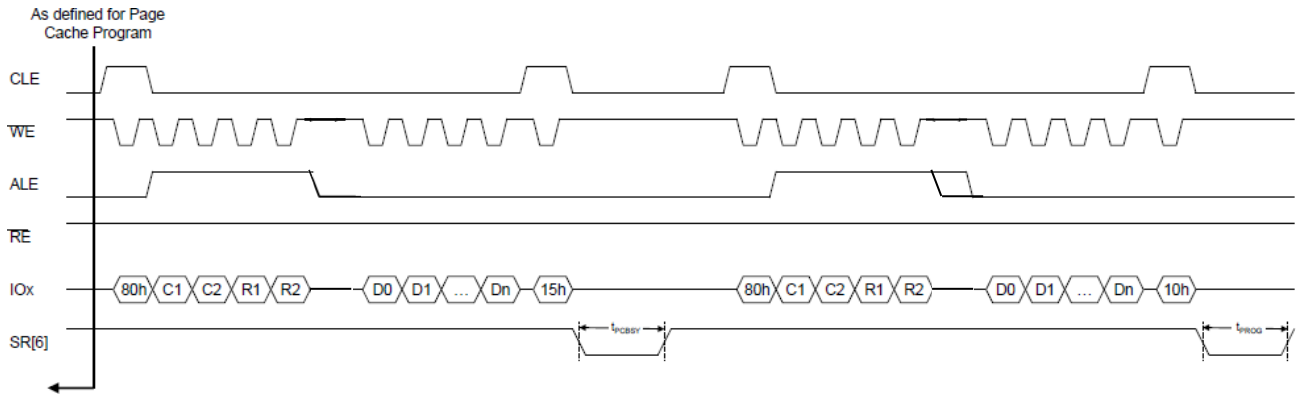


Figure 19: Cache Program End

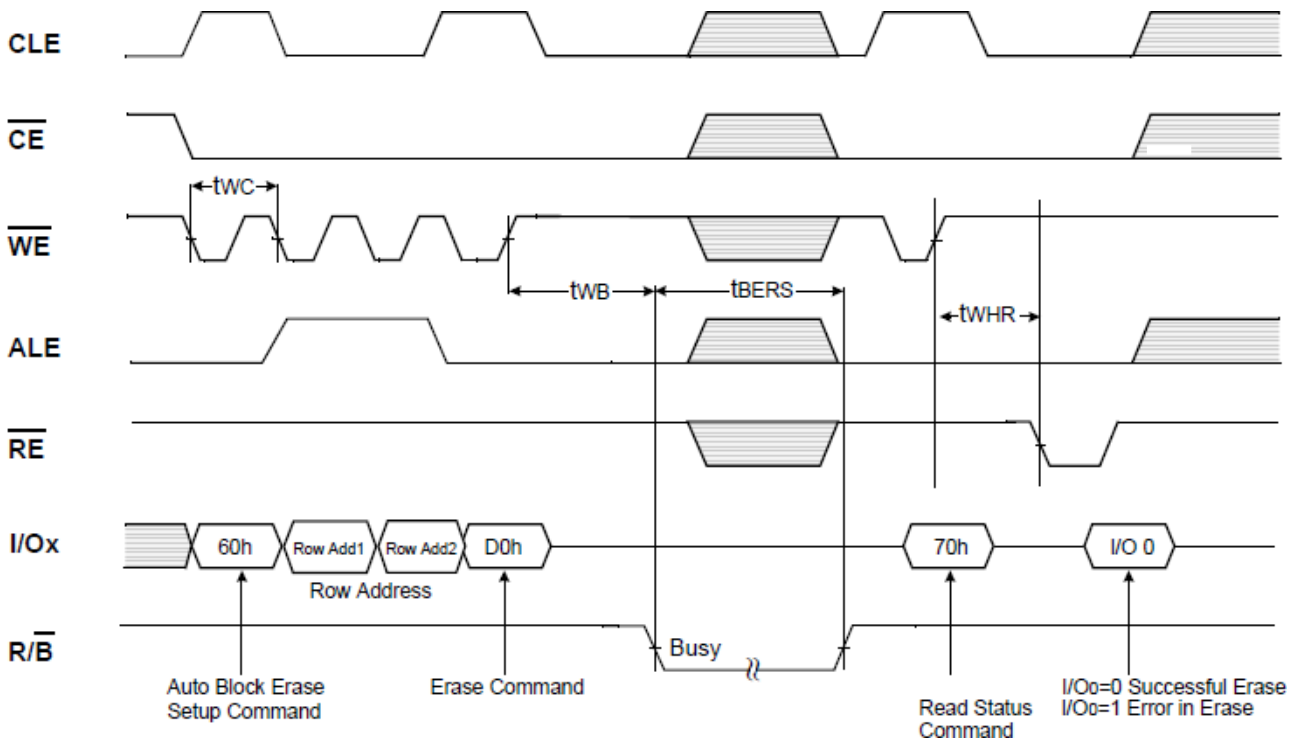


Figure 20 : Block Erase Operation (Erase One Block)

Read ID Operation

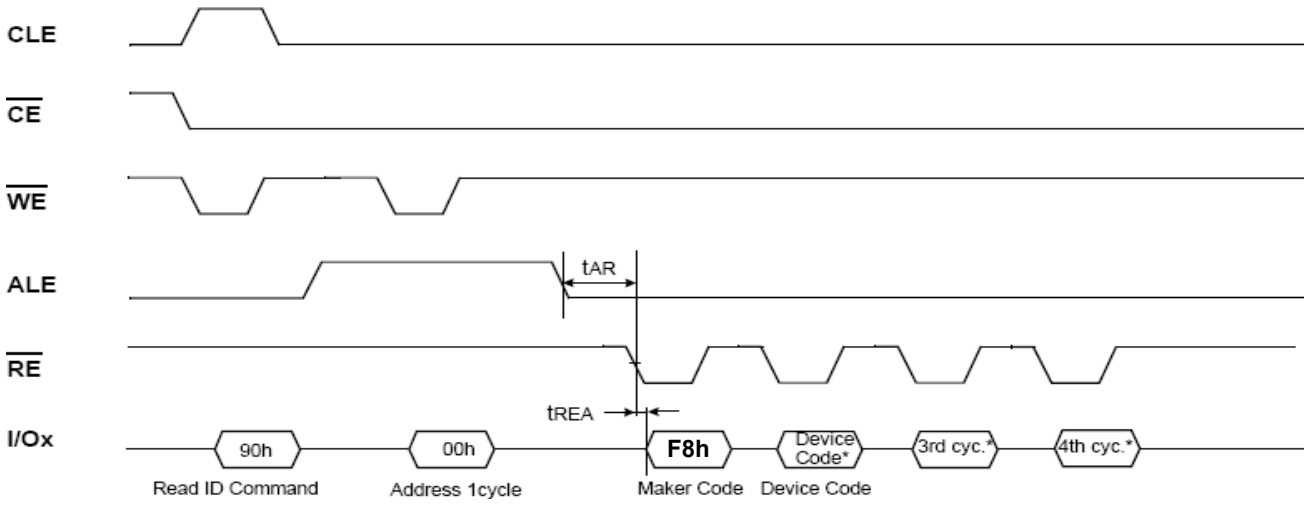


Figure 21 : READ ID Operation

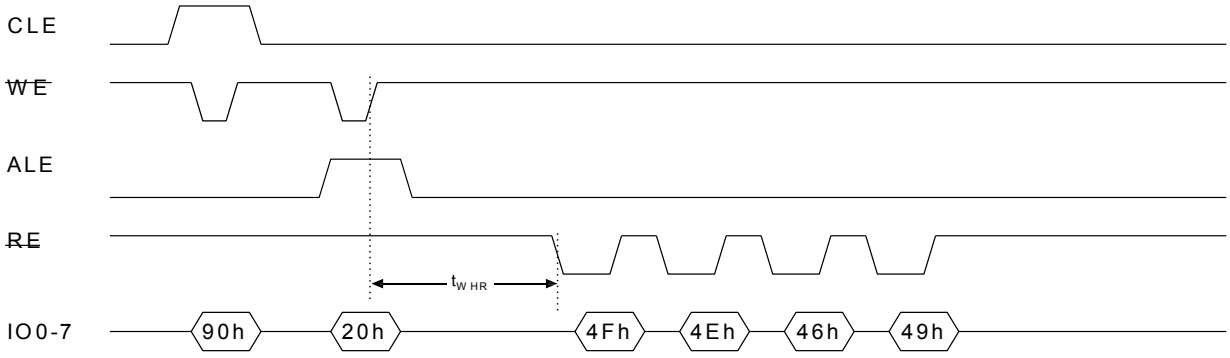


Figure 22 : ONFI signature timing diagram

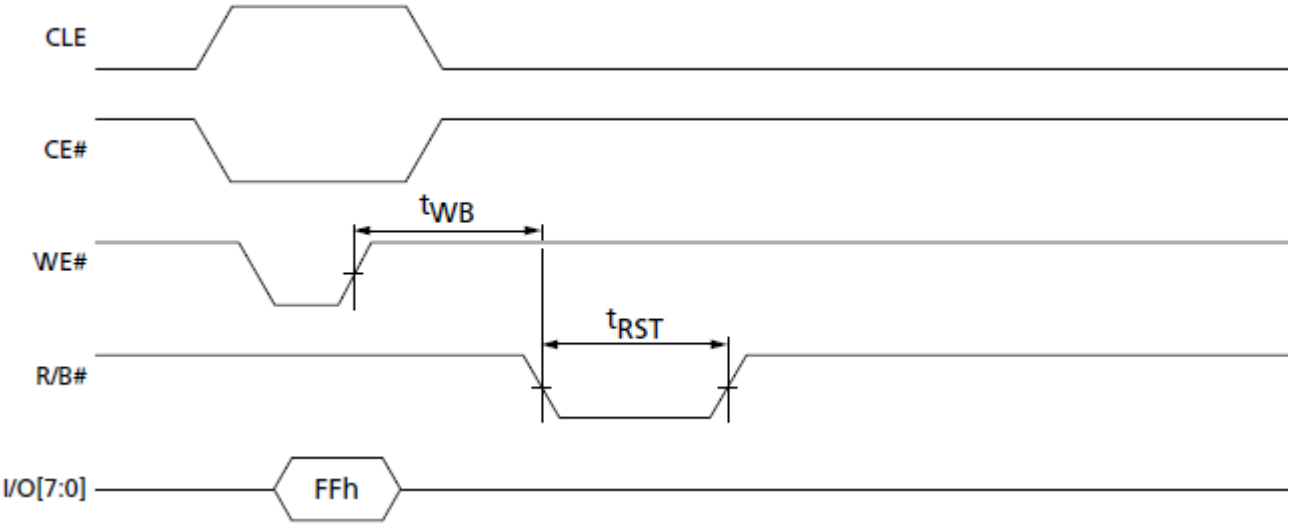


Figure 23 : Reset operation timing

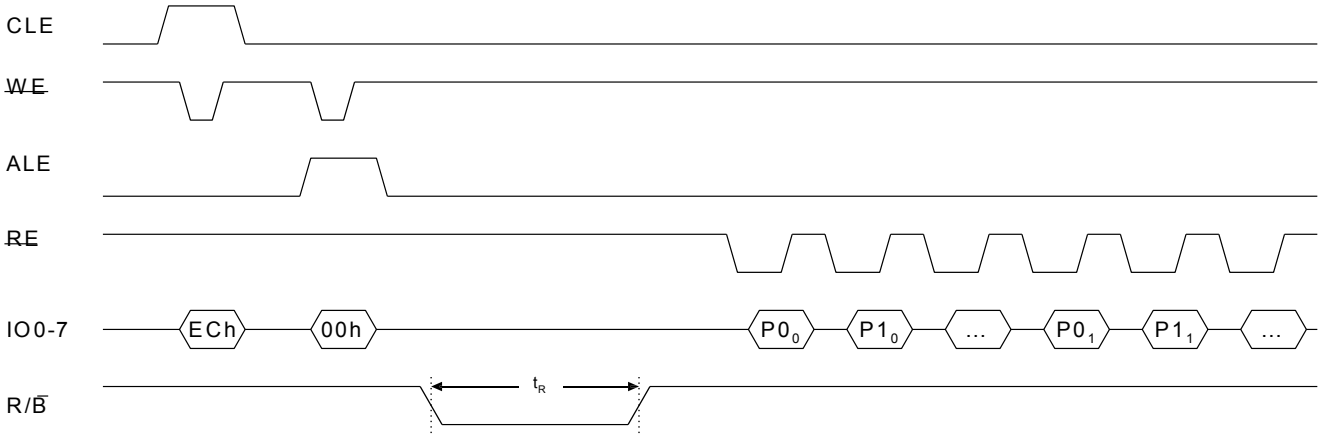


Figure 24 : Read Parameter Page timings

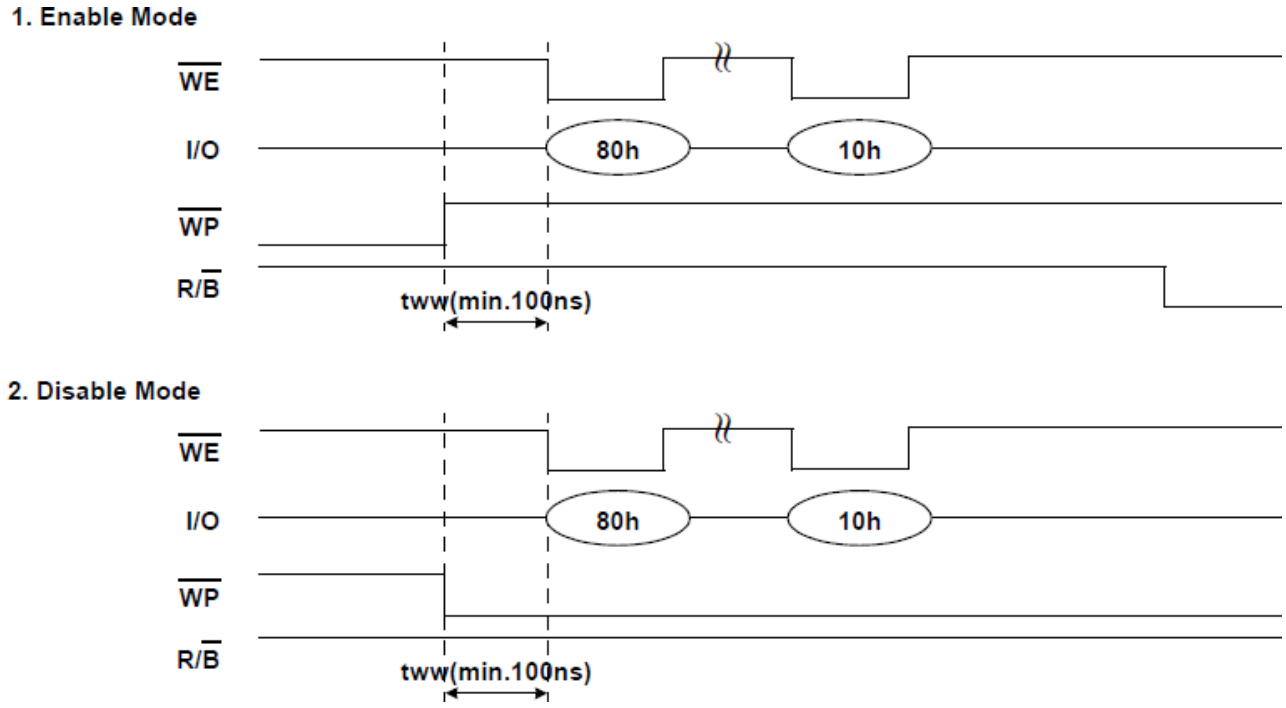


Figure 25 : tWW in Program Operation

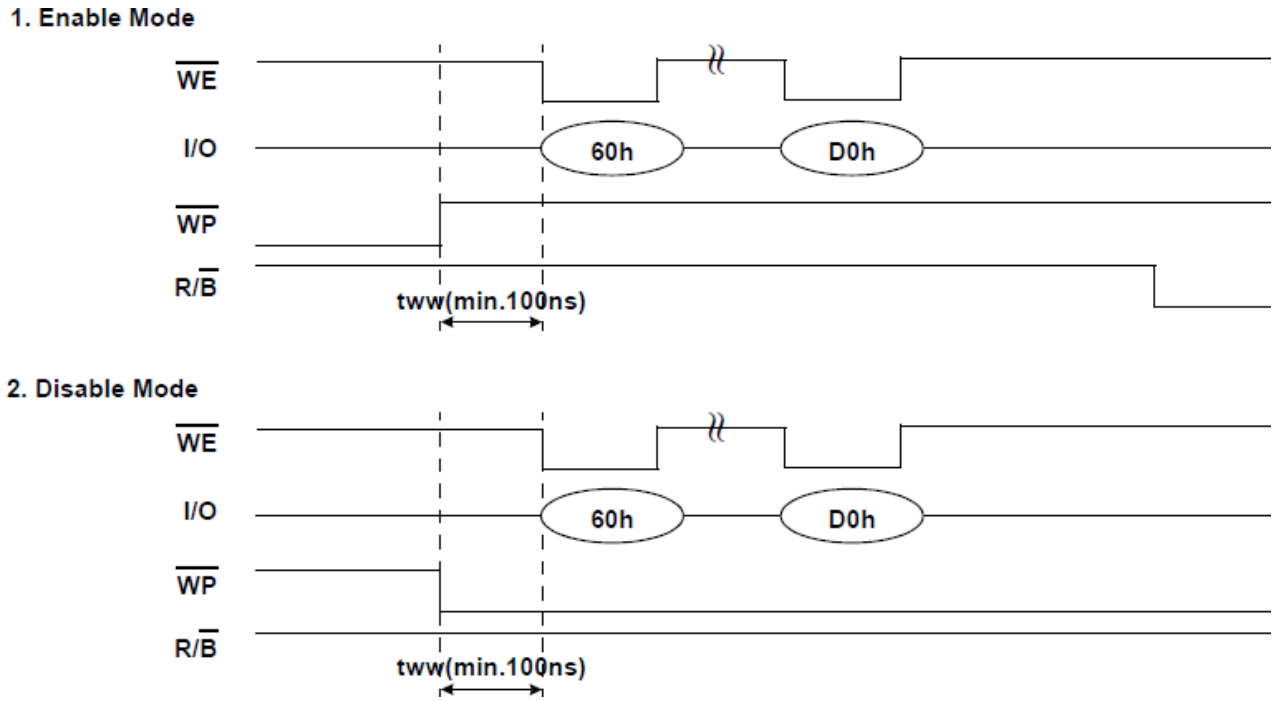


Figure 26 : tWW in Erase Operation

Note : V_{TH} = **1.5** Volt for 1.8 Volt Supply devices; **2.5** Volt for 3.0 Volt Supply devices

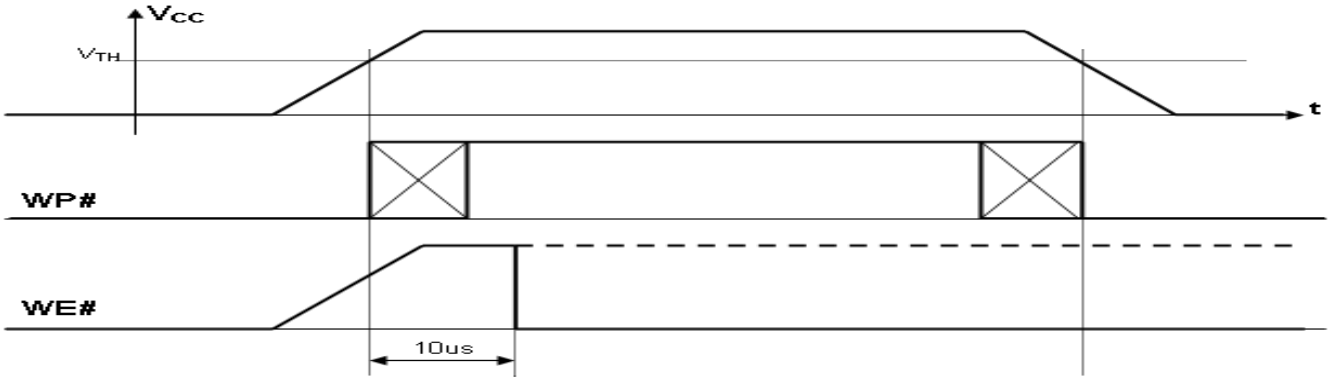


Figure 27 : Power on and Data Protection timings

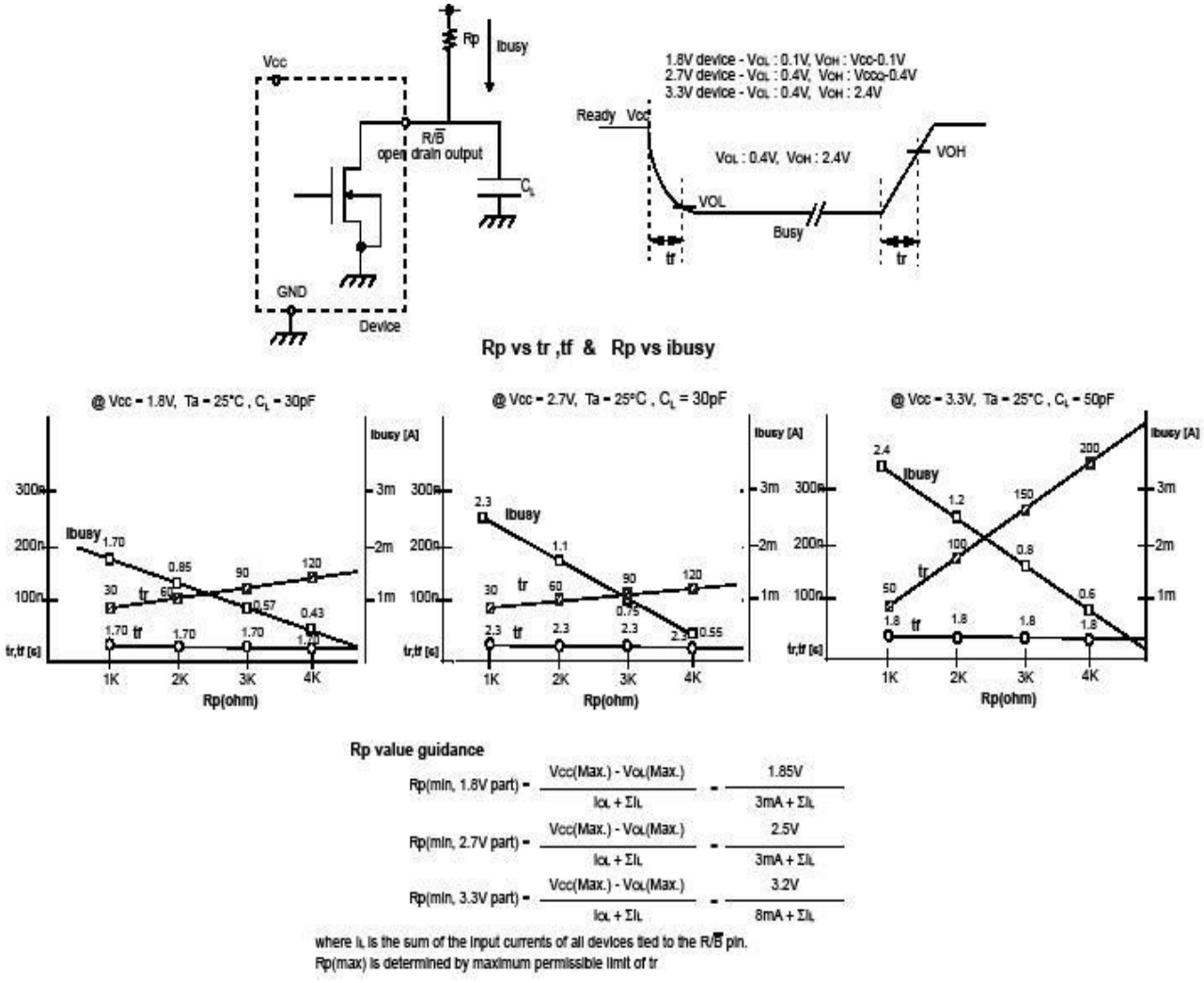


Figure 28 : Ready/Busy Pin electrical application

6 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart

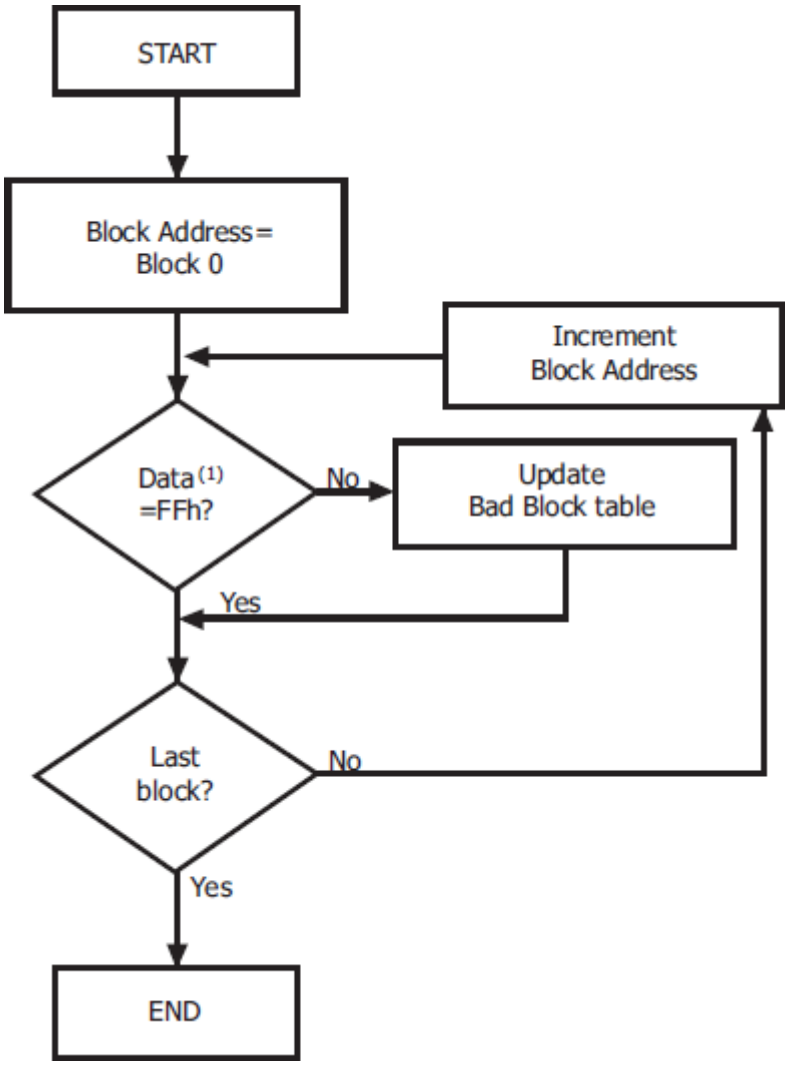


Figure 29 : Bad Block Management Flowchart

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

Figure 30 : Block Failure

Block Replacement flow is as below
1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3.Copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4.Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

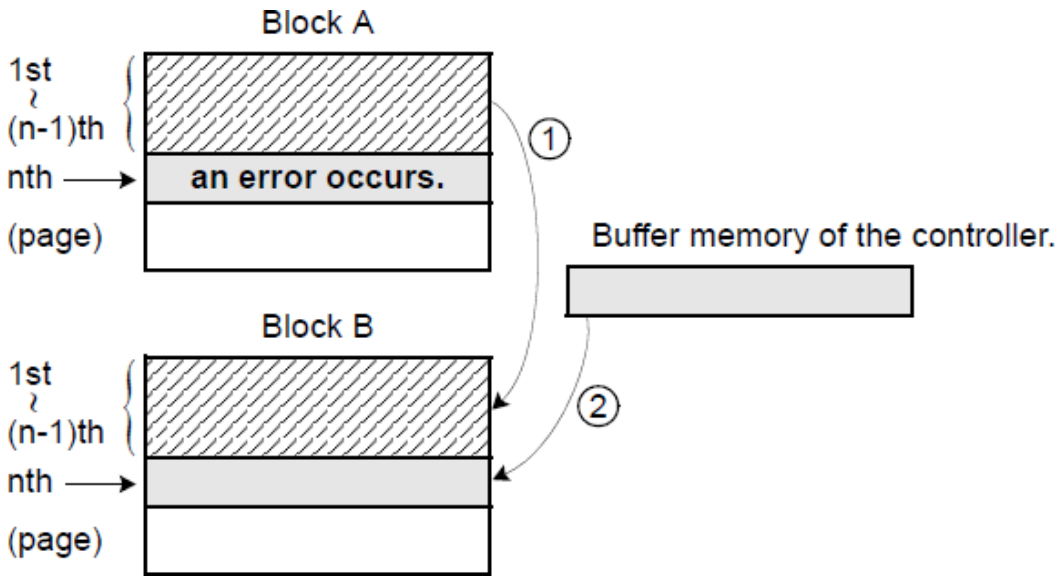


Figure 31 : Bad Block Replacement

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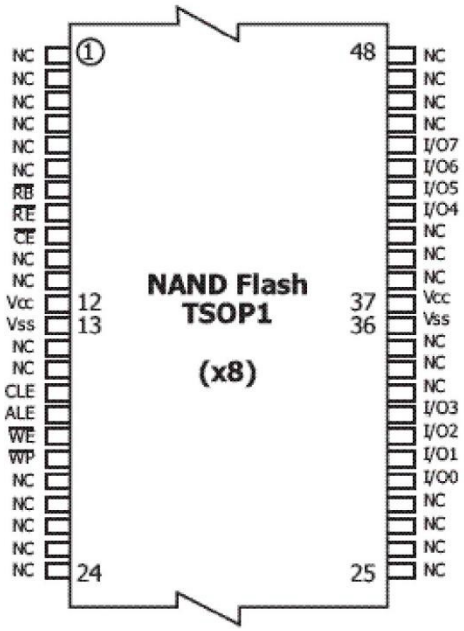
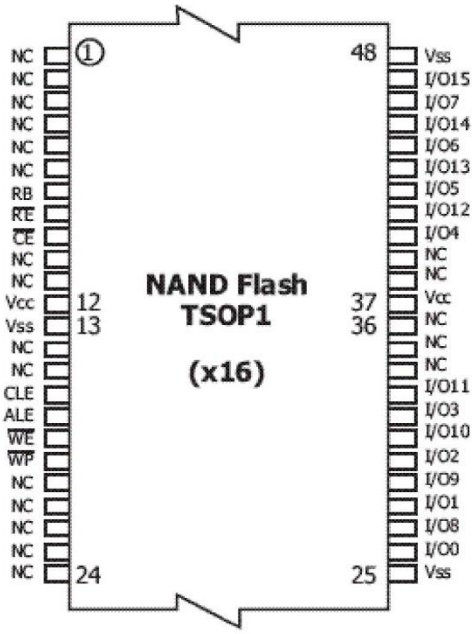
7 Supported Packages

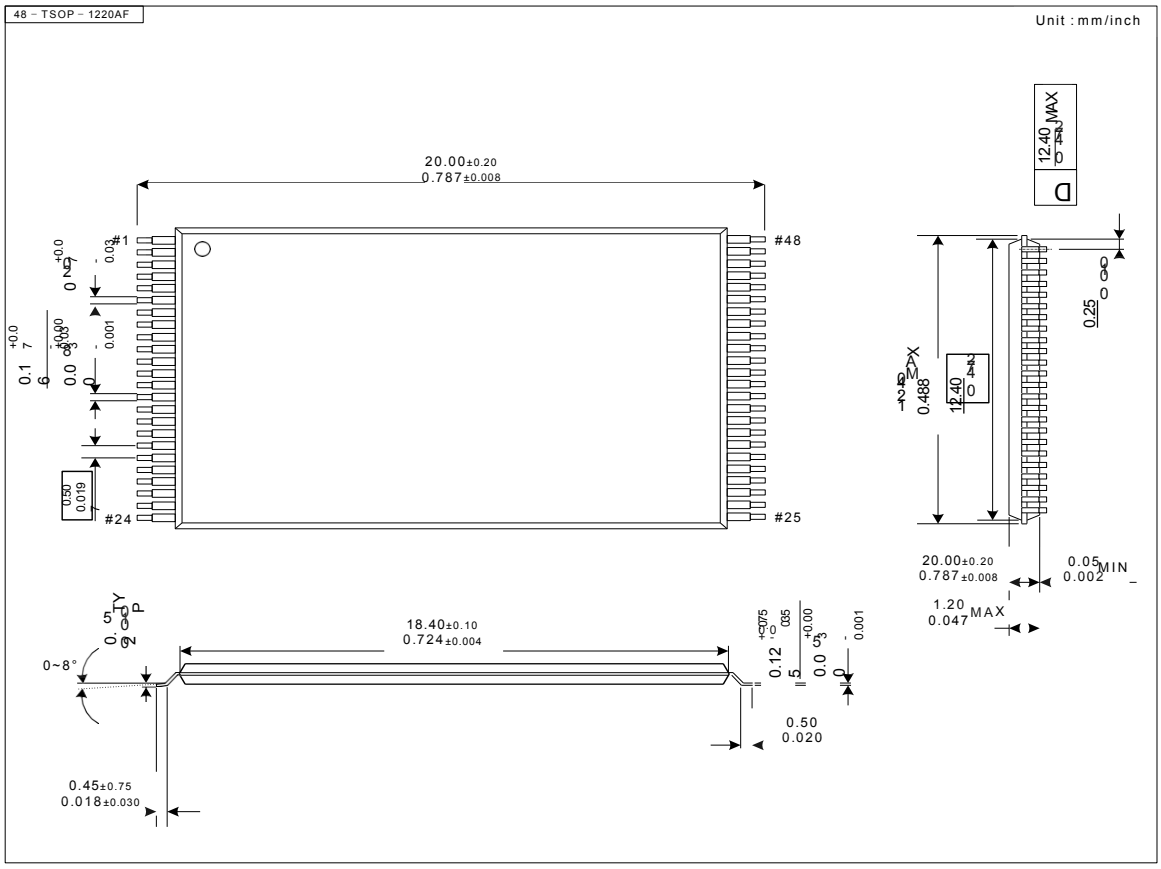
7.1 PIN CONFIGURATION (48 TSOP)





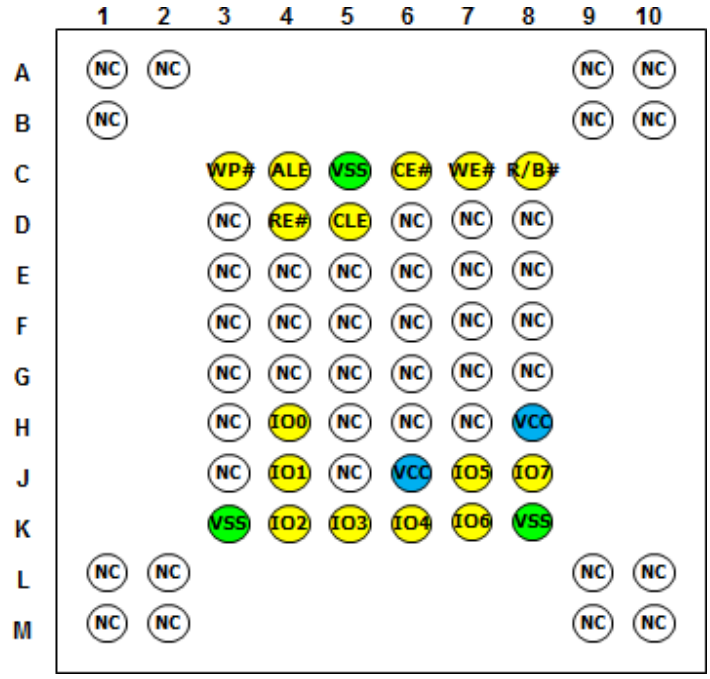
7.2 PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

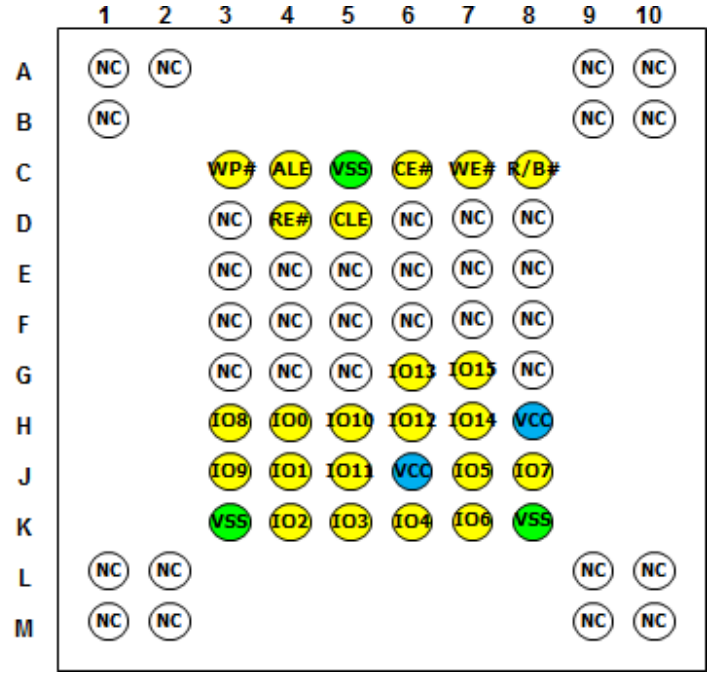


7.3 Ball Assignment: 63-Ball FBGA (Balls Down, Top View)

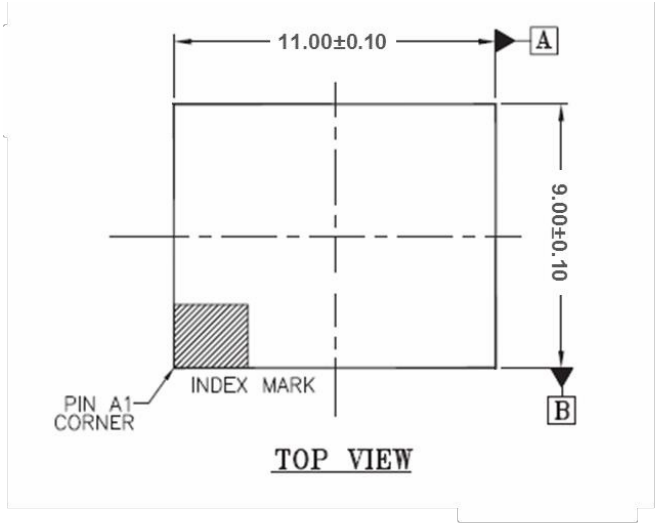
x8

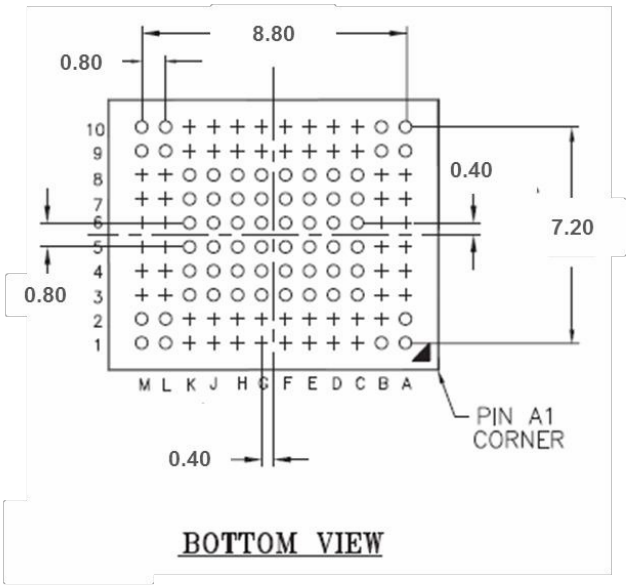


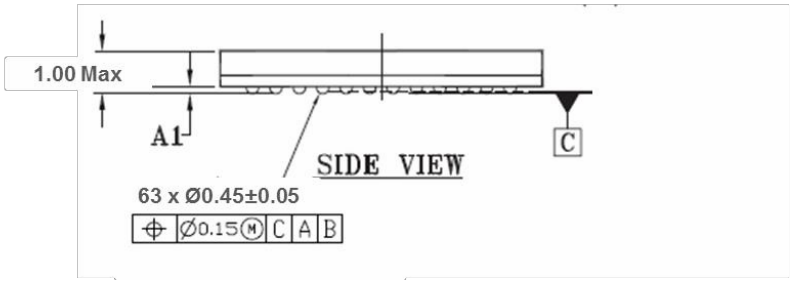
x16



7.4 PACKAGE DIMENSIONS
63-Ball FBGA PACKAGE TYPE

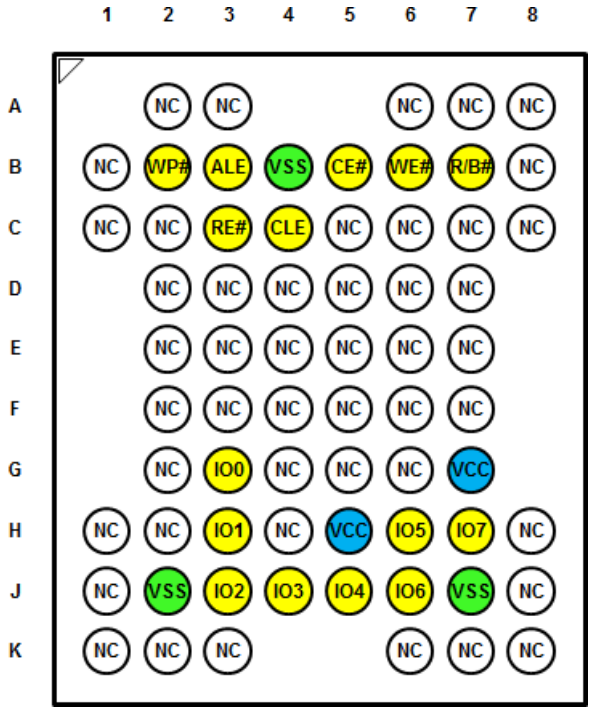




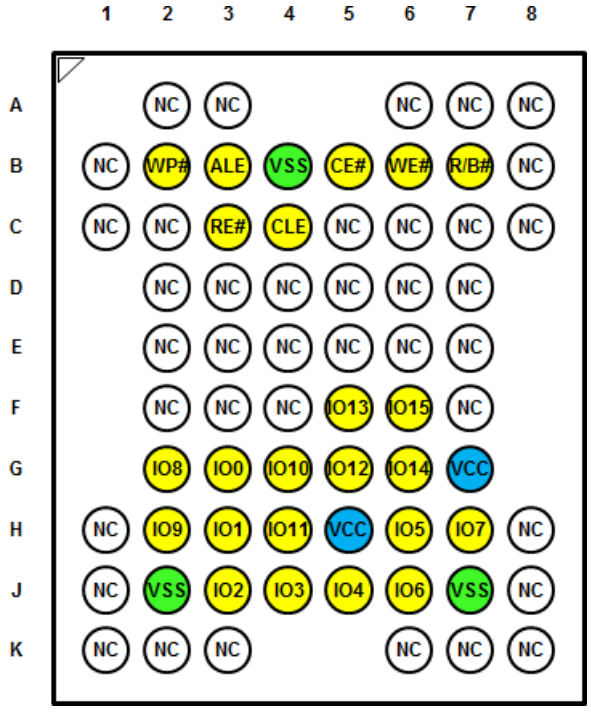


7.5 Ball Assignment: 67-Ball FBGA (Balls Down, Top View)a

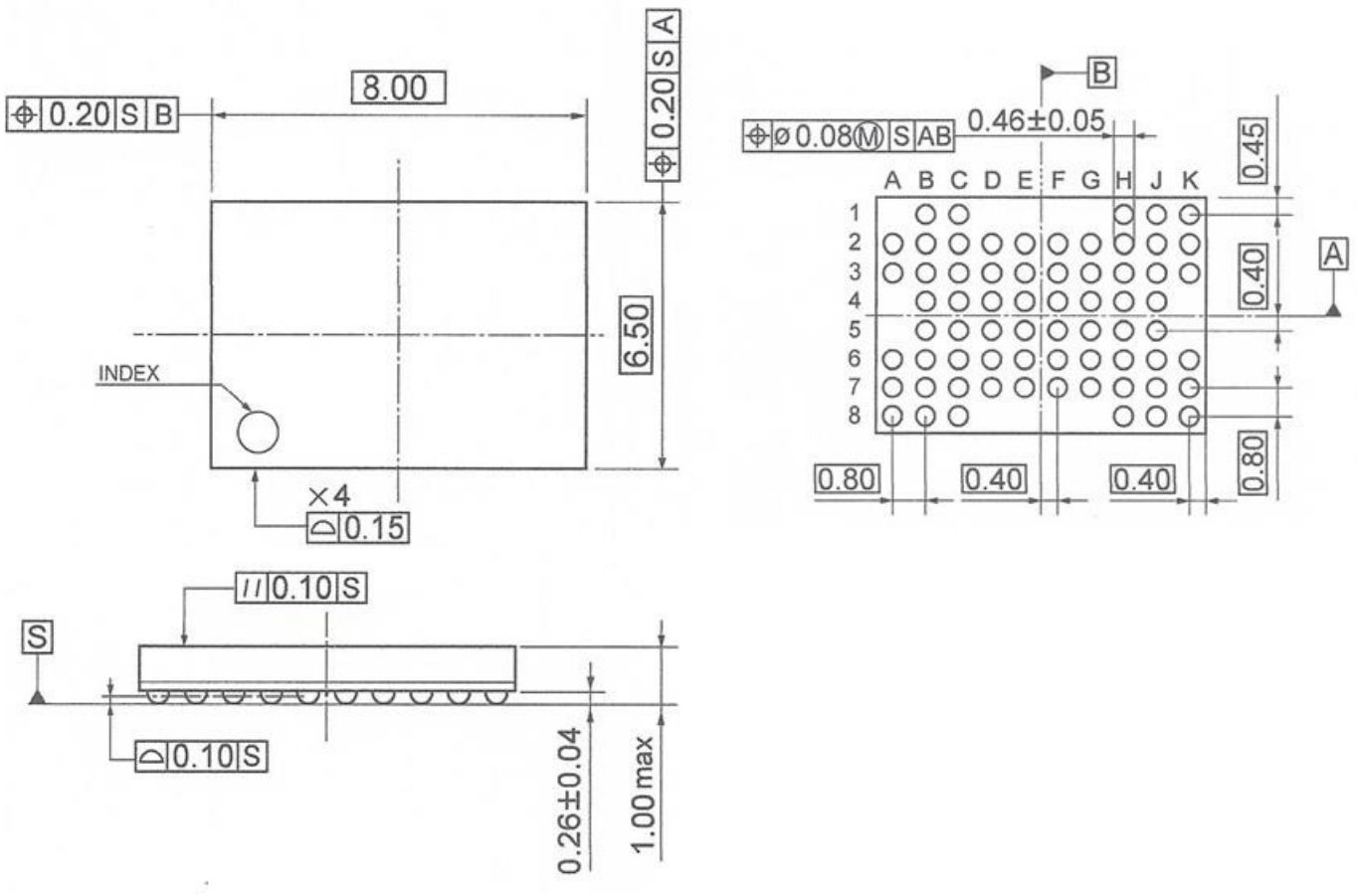
X8



X16



7.6 PACKAGE DIMENSIONS
67-Ball FBGA PACKAGE TYPE



dosilicon

512M(32Mx16) Low Power DDR SDRAM

Revision 0.3

Jun. 2013

Document Title

512M(32Mx16) Low Power DDR SDRAM

Revision History

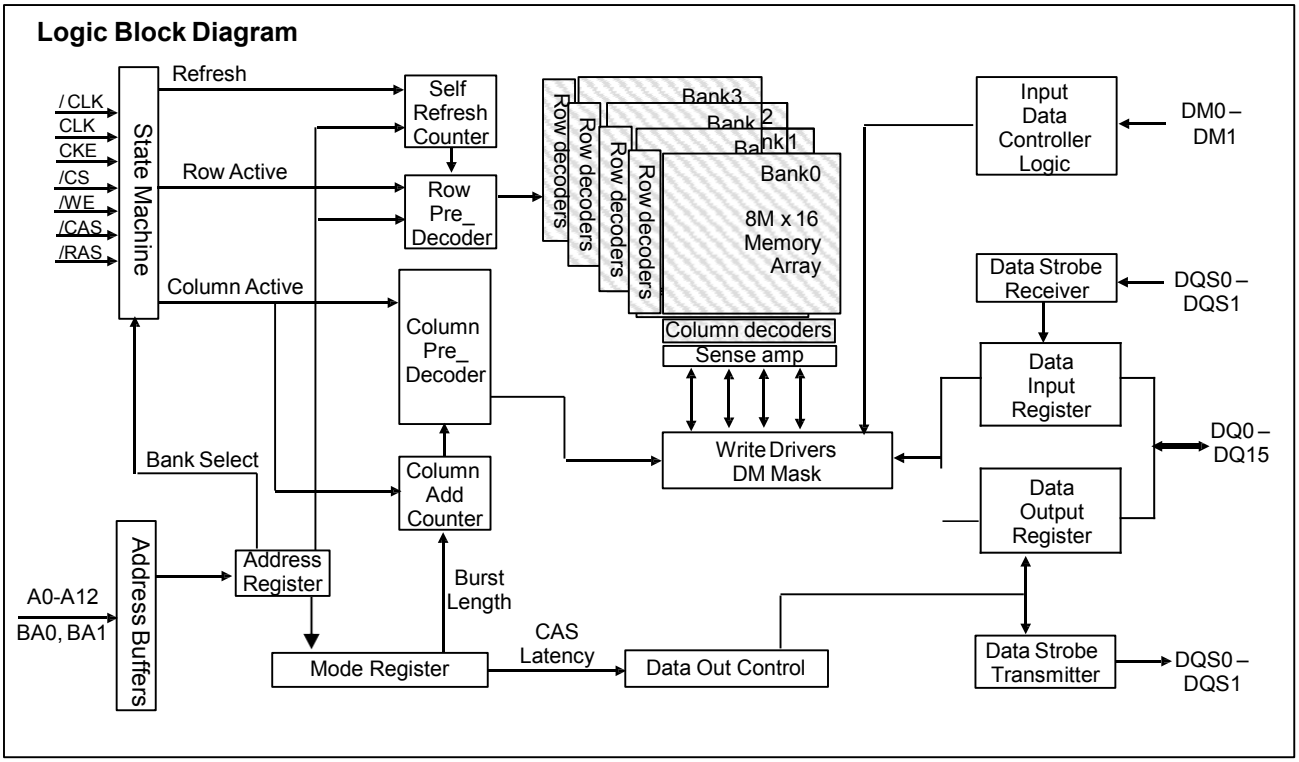
Revision No.	History	Draft date	Remark
0.0	Initial Draft	Dec. 15th, 2011	Preliminary
0.1	Adjusted DC parameters(IDD0, IDD4R, IDD4W, IDD6)	Jun. 28th, 2012	
0.2	Changed tWTR (1CLK → 2CLKs)	Jul. 27th, 2012	
0.3	Revise typo(remove max of tSRR, tSRC)	Jun. 17th, 2013	Final

DDR Sync DRAM Features

- **Functionality**
  - Double-data-rate architecture ; two data transfers per CLK cycle.
  - Bidirectional data strobe per byte data (DQS).
  - No DLL ; CLK to DQS is not Synchronized.
  - Differential CLK inputs(CLK and /CLK).
  - Commands entered on each positive CLK edge.
  - DQS edge-aligned with data for Reads; center-aligned with data for Writes.
  - Four internal banks for concurrent operation.
  - Data masks (DM) for masking write data-one mask per byte.
  - Programmable burst lengths : 2, 4, 8, 16.
  - Programmable CAS Latency : 2, 3.
  - Concurrent auto pre-charge option is supported.
  - Auto refresh and self refresh modes.
  - Status read register (SRR)
  - LVCMOS-compatible inputs.
- **Configuration**
  - 32 Meg X 16 (8 Meg X 16 X 4Bank).
- **Low Power Features**
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - Partial Array Self Refresh power-saving mode.
  - Deep Power Down Mode.
  - Driver Strength Control.
- **Operating Temperature Ranges**
  - Commercial (0℃ to +70℃).
  - Extended (-25℃ to +85℃).
  - Industrial (-40℃ to +85℃).
- **Package**
  - 60-Ball FBGA (8 X 9 X 0.8mm)
- **Functional Description**

The FMD8B16LBx Family is high-performance CMOS Dynamic RAMs (DRAM) organized as 32M x 16. These devices feature advanced circuit design to provide low active current and extremely low standby current. The device is compatible with the JEDEC standard Low Power DDR SDRAM specifications.

Logic Block Diagram



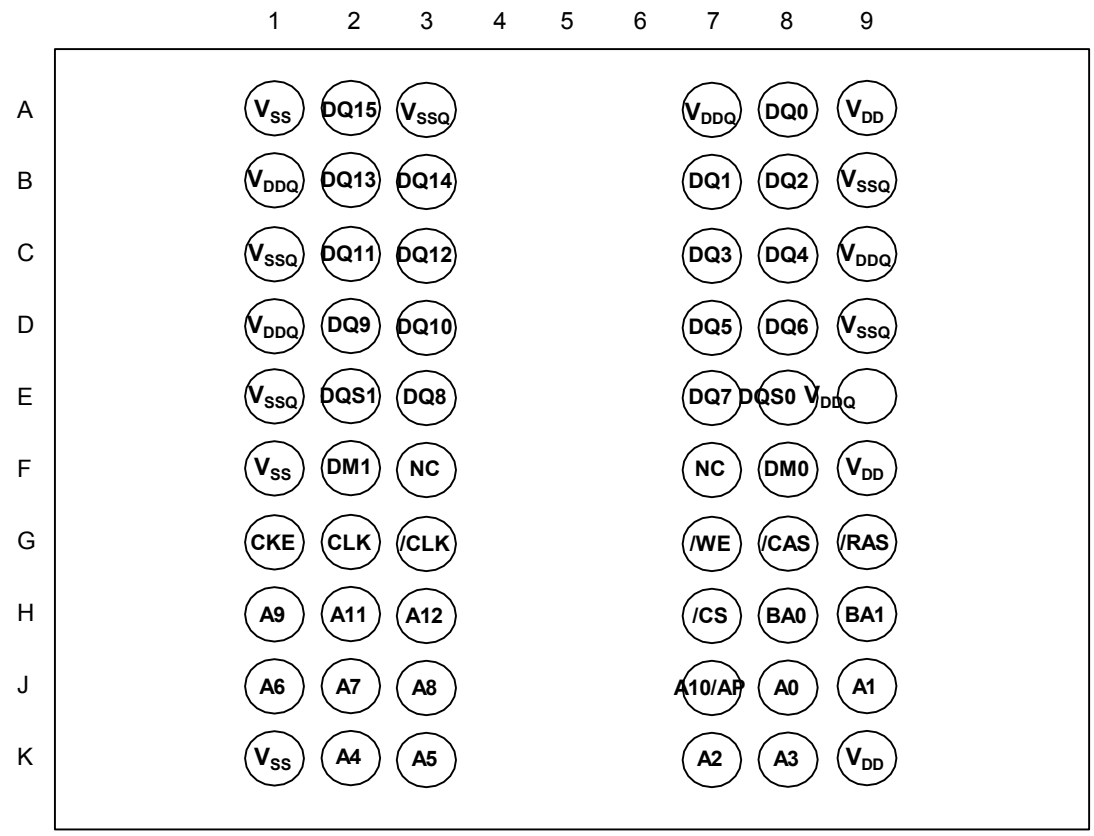
Selection Guide

Device	Voltage		Clock Frequency	Access Time(t_{AC})		tRCD	tRP
	V_{DD}	V_{DDQ}		CL=2	CL=3		
FMD8C16LAx-25Ex	1.70-1.95V	1.70-V_{DD}	200MHz		5.0ns	15ns	15ns
			83MHz	6.0ns		15ns	15ns

Pin Configuration

60 ball 0.8mm pitch FBGA(8mm x 9mm)

Top View



General Description

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer four data words per clock cycle at the I/O balls. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Low Power DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes.

The 512Mb Low Power DDR SDRAM operates from a differential clock (CLK and /CLK); the crossing of CLK going HIGH and /CLK going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Low Power DDR SDRAM provides for programmable READ or WRITE burst lengths of 2,4,8 or 16. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Low Power DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Notes :

1. Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes. For the first byte (DQ0–DQ7) DM refers to DM0 and DQS refers to DQS0. For the second byte (DQ8–DQ15) DM refers to DM1 and DQS refers to DQS1.
2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

Pin Description

Symbol	Type	Description
CLK, /CLK	Input	Clock: CLK is the system clock input. CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Input and output data is referenced to the crossing of CLK and /CLK (both directions of the crossing).
CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions expect SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
/CS	Input	Chip select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is consideredpart of the command code.
/RAS, /CAS, /WE	Input	Command inputs: /RAS, /CAS, and /WE (along with /CS) define the command being entered.
DM0–DM1	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, DM0 corresponds to DQ0 – DQ7, DM1 corresponds to DQ8–DQ15.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
A0-A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address andauto pre-charge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. For 512Mb(X16), Row Address : A0 ~ A12, Column Address: A0 ~ A9.
DQ0-DQ15	I/O	Data input/output: Data bus for x16.
DQS0-DQS1	I/O	Data strobe: Output with read data, input with write data. DQS is edge aligned with read data, centered in write data. It is used to capture data. For the x16, DQS0 corresponds to DQ0 – DQ7, DQS1 corresponds to DQ8–DQ15.
TQ	Output	Temperature sensor output : TQ High when LPDDR Tj exceeds 85℃. When TQ is 'High', self refresh is not supported.
VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
VDD	Supply	Power Supply: Voltage dependant on option.
VSS	Supply	Ground.

Functional Description

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 67,108,864-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer four data words per clock cycle at the I/O balls. single read or write access for the 512Mb Low Power DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command.

The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL signal that is typically used on standard DDR devices is not necessary on the Low Power DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Low Power DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

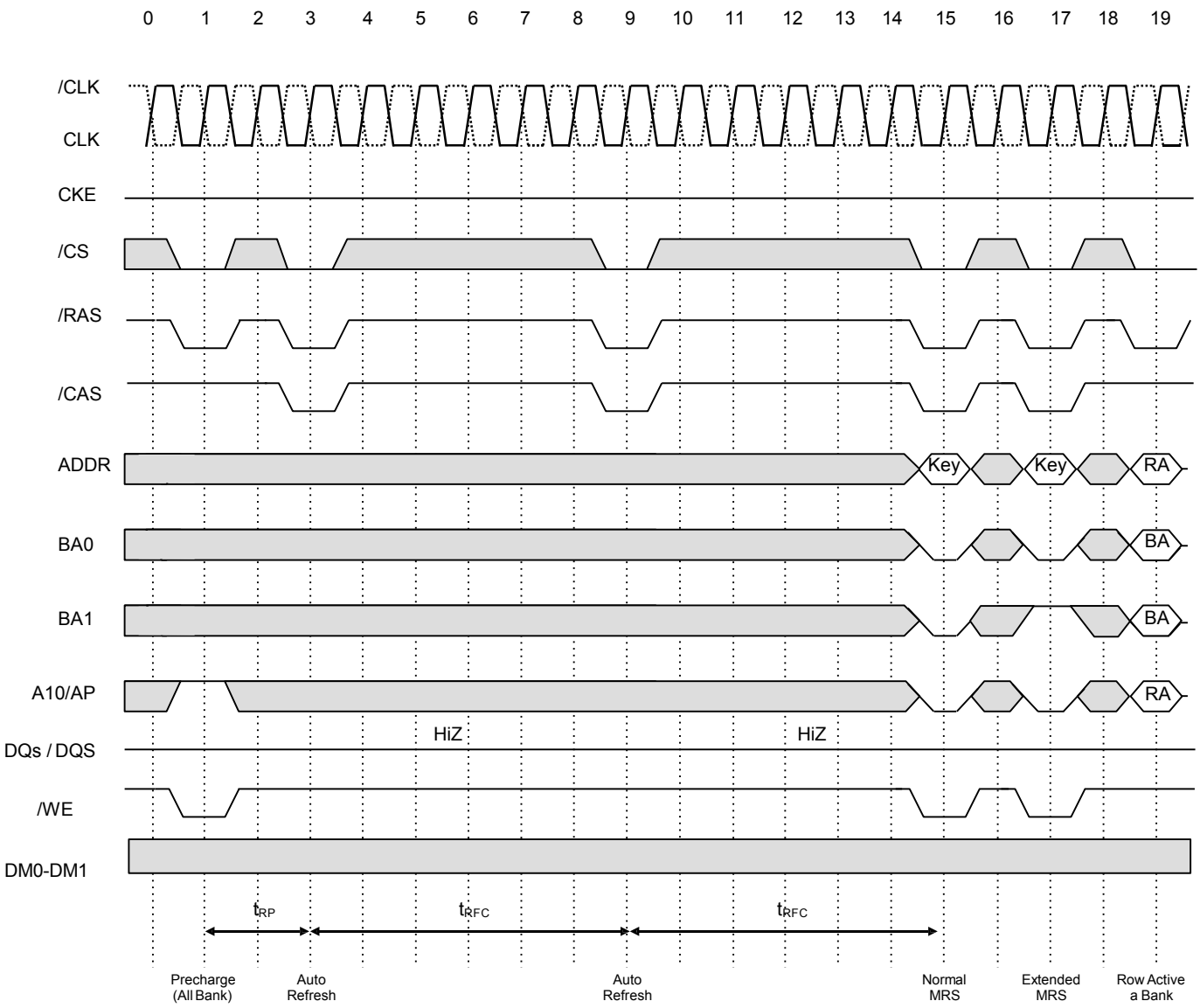
Low Power DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Low Power DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Low Power DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended the core power (VDD) and I/O power (VDDQ) be from the same power source and brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs (minimum) delay is required by the Low Power DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued between steps 10 and 11.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least tMRD time.
11. The Low Power DDR SDRAM has been properly initialized and is ready to receive any valid command.

Figure 1. Initialize and Load Mode Register[1.2.3.]



Note :

1. The two AUTO REFRESH commands at T3 and T9 may be applied before either LOAD MODE REGISTER (LMR) command.
2. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address
3. The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order; However, all must occur prior to an Active command.
4. NOP or DESELECT commands are required for at least 200μs.
5. Other valid commands are possible.
6. NOPs or DESELECTs are required during this time.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Low Power DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all Low Power DDR SDRAM devices, and the extended mode register, which exists on all Low Power DDR SDRAM devices.

Standard Mode Register

The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Table 1 on page 10. The standard mode register is programmed via the LOAD MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again. Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.
Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Low Power DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Table 1 on page 10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2,4,8 or 16 are available for both the sequential and the interleaved burst types.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap until a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, by A3–Ai when BL = 8, by A4–Ai when BL=16(where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.
The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.
The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See Table 2 on page 11 for more information.

READ Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in Table 1 on page 10. For CL = 3, if the READ command is registered at clock edge n, then the data will nominally be available at (2 clocks + tAC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally be available at (1 clock + tAC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 1: Standard Mode Register Definition

M14-BA1	M13-BA0	M12-A12	M11-A11	M10-A10	M9-A9	M8-A8	M7-A7	M6-A6	M5-A5	M4-A4	M3-A3	M2-A2	M1-A1	M0-A0
0	0	Operation Mode						CAS Latency			BT	Burst Length		

M14	M13	Mode Register Definition
0	**0**	**Standard Mode Register**
0	1	Status Read Register
1	0	Extended Mode Register
1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M12	M11	M10	M9	M8	M7		Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
-	-	-	-	-	-	-	All other states reserved

M3	Burst Type
0	Sequential
1	Interleaved

Table 2: Burst Definition

Burst Length			Starting Column Address		Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
2				A0		
				0	0-1	0-1
				1	1-0	1-0
4			A1	A0		
			0	0	0-1-2-3	0-1-2-3
			0	1	1-2-3-0	1-0-3-2
			1	0	2-3-0-1	2-3-0-1
			1	1	3-0-1-2	3-2-1-0
8		A2	A1	A0		
		0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
		0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
		0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
		0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
		1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
		1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
		1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
		1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	A3	A2	A1	A0		
	0	0	0	0	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
	0	0	0	1	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14
	0	0	1	0	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13
	0	0	1	1	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12
	0	1	0	0	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-0-1-2-3-12-13-14-15-8-9-10-11
	0	1	0	1	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-4-7-6-1-0-3-2-13-12-15-14-9-8-11-10
	0	1	1	0	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-4-5-2-3-0-1-14-15-12-13-10-11-8-9
	0	1	1	1	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8
	1	0	0	0	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7
	1	0	0	1	9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-8-11-10-13-12-15-14-1-0-3-2-5-4-7-6
	1	0	1	0	10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-8-9-14-15-12-13-2-3-0-1-6-7-4-5
	1	0	1	1	11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-10-9-8-15-14-13-12-3-2-1-0-7-6-5-4
	1	1	0	0	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-8-9-10-11-4-5-6-7-0-1-2-3
	1	1	0	1	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-12-15-14-9-8-11-10-5-4-7-6-1-0-3-2
	1	1	1	0	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-12-13-10-11-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8-7-6-5-4-3-2-1-0

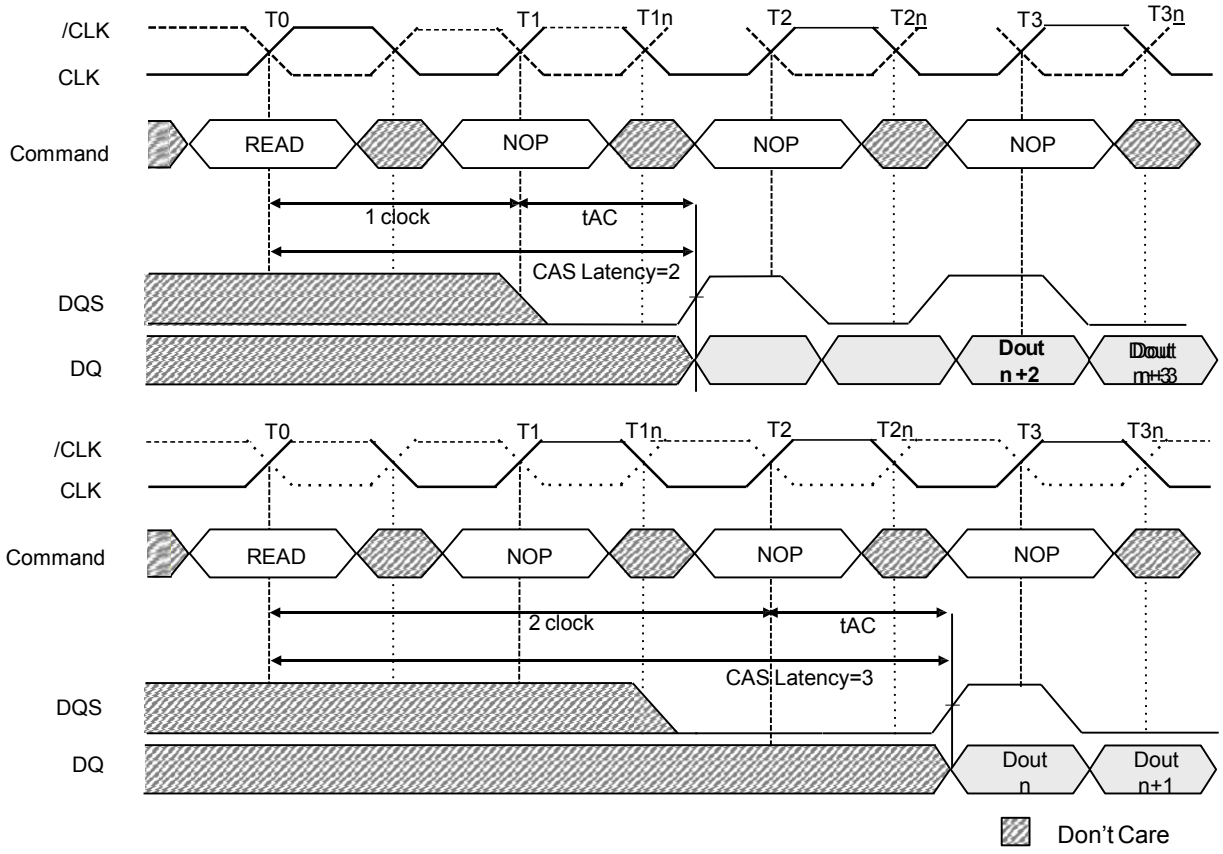
Notes:

1. For BL = 2, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For BL = 4, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For BL = 8, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. For BL=16, A4–A*i* select the sixteen-data-element block; A0–A3 select the first access within the block.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. A*i* = the most significant column address bit for a given configuration.

Table 3: CAS Latency

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 3
-25	f ≤83	f ≤200

Figure 2: CAS Latency



Notes:

1. BL = 4 in the cases shown.
2. Shown with nominal tAC and nominal tDQSCLK.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7–A12 each set to zero, and bits A0–A6 set to the desired values. All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh. This device has default values for the extended mode register (if not programmed, the device will operate with the default values – PASR = Full Array, DS = Full Drive).

Temperature Compensated Self Refresh

A temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device.The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the mount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 & 1
- Quarter array: bank 0
- One Eighth array: Half of Bank0
- One Sixteenth array: Quarter of Bank0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength

Because the Low Power DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 ~ A7 of the extended mode register can be used to select the driver strength of the DQ outputs. There are five allowable settings for the output drivers.

Table 4: Extended Mode Register Table[1.2.].

EM14-BA1	EM13-BA0	EM12-A12	EM11-A11	EM10-A10	EM9-A9	EM8-A8	EM7-A7	EM6-A6	EM5-A5	EM4-A4	EM3-A3	EM2-A2	EM1-A1	EM0-A0
1	0	All must be set to '0'					Driver Strength			0	0	PASR		

EM14	EM13	Mode Register Definition
0	0	Standard Mode Register
0	1	Status Read Register
1	**0**	**Extended Mode Register**
1	1	Reserved

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank(BA1=0)
0	1	0	Quarter of Total Bank(BA1=BA0=0)
0	1	1	RFU
1	0	0	RFU
1	0	1	One Eighth of Total Bank (BA1=BA0=Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1=BA0=Row Address2 MSBs=0)
1	1	1	RFU

A7	A6	A5	Driver Strength
0	0	0	100%
0	0	1	50%
0	1	0	25%
0	1	1	12.5%
1	0	0	75%
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Note :

1. EM14 and EM13 (BA1 and BA0) must be "1, 0" to select the Extended Mode Register(vs. the base Mode Register).
2. RFU: Reserved for Future Use

Status Read Registers

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the device, as shown in Table 5 (page 14). The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

- The device must be properly initialized and in the idle or all banks precharged state.
- Issue a LOAD MODE REGISTER command with BA[1:0] = 01 and all address pins set to 0.
- Wait tSRR; only NOP or DESELECT commands are supported during the tSRR time.
- Issue a READ command.
- Subsequent commands to the device must be issued tSRC after the SRR READ command is issued; only NOP or DESELECT commands are supported during tSRC.

SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first bit of the burst, with the output being “Don’t Care” on the second bit of the burst.

Table 5: Status Register Table.

S31~S16[1]	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Reserved	Density			Type	Width	Refresh Rate			Revision ID				Manufacturer ID			

S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S12	Device Type
0	LPDDR
1	Reserve

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier[2]
0	0	0	Reserved
0	0	1	Reserved
1	1	0	Reserved
0	1	1	2X
1	0	0	1X
1	0	1	Reserved
1	1	0	0.25X
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer’s revision number starts at ‘0000’ and increments by ‘0001’ each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
~				
1	1	1	1	

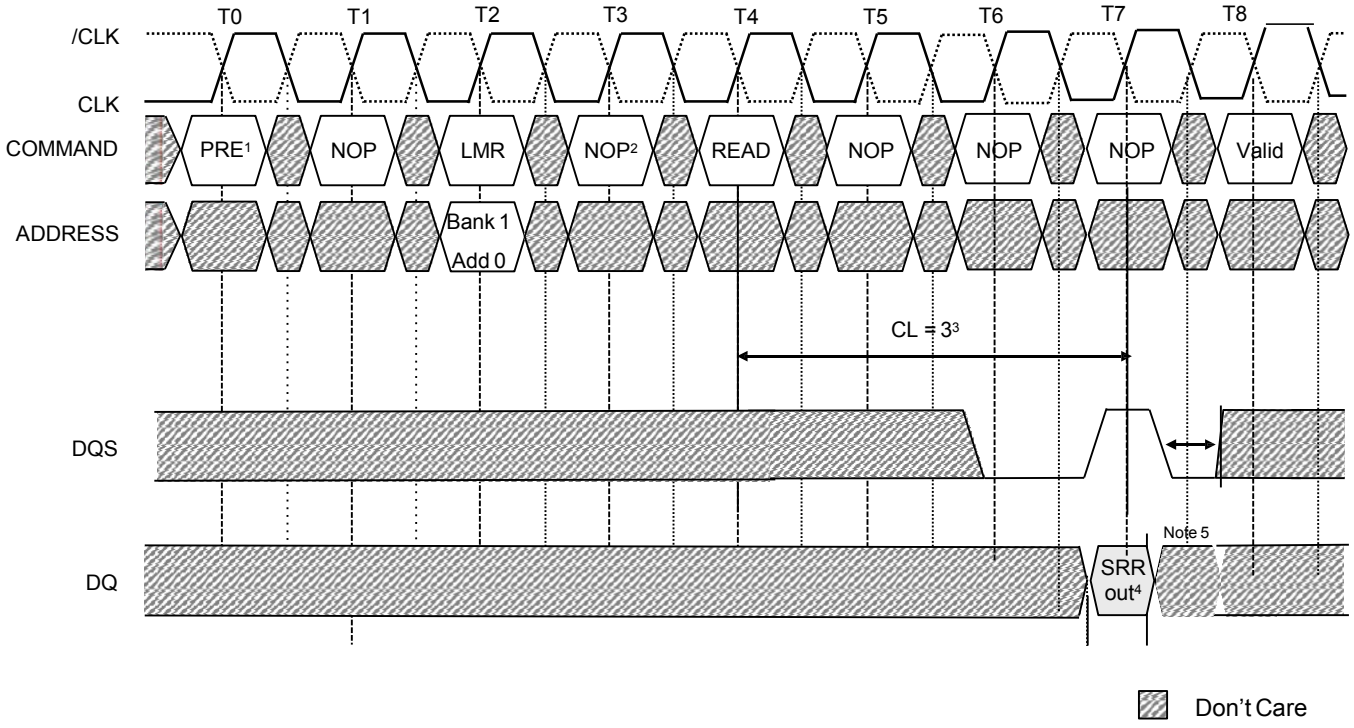
Note : 1. Reserved bits should be set to 0 for future compatibility.

2. Refresh multiplier is based on the device on-board temperature sensor.

Requited periodic refresh interval = tREFI X multiplier.

Self refresh is not supported for automotive device at high temperature. (85℃ to 105℃)

Figure 3: Status Read Register Timing



Note : 1. All banks must be idle prior to status register read.

2. NOP or DESELECT commands are required between the LMR and READ commands(tSRR), and between the READ and the next VALID command (tSRC).
3. CAS latency is predetermined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a "Don't Care."

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the Low Power DDR SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency, when the data transfers require a different rate of speed.
2. Stopping the clock altogether.

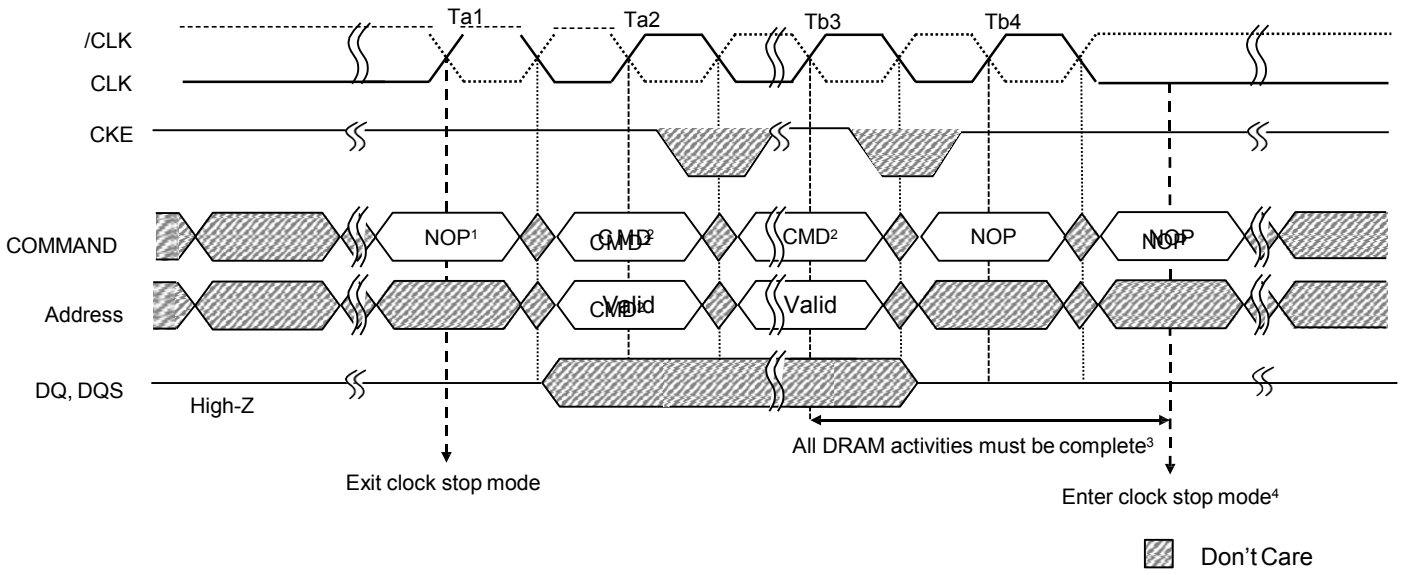
Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Low Power DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped all together, if there are no data accesses in progress, either WRITEs or READs that would be effected by this change; i.e., if a WRITE or a READ is in progress the entire data burst must be through the pipeline prior to stopping the clock. CKE must be held HIGH with CLK = LOW and /CLK = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued. Figure 4 on page 16 illustrates the clock stop mode.

It is recommended that the Low Power DDR SDRAM should be in a precharged state if any changes to the clock frequency are expected. This will eliminate timing violations that may otherwise occur during normal operational accesses.

Figure 4: Clock Stop Mode



Notes:

1. Prior to Ta1 the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is allowed, device is not in clock suspend mode.
3. Any DRAM operation already in process must be completed before entering clock stop mode. This includes tRCD, tRP, tRFC, tMRD, tWR, all data-out for READ bursts. This means the DRAM must be either in the idle or precharge state before clock suspend mode can be entered.
4. To enter and maintain a clock stop mode: CLK = LOW, /CLK = HIGH, CKE = HIGH.

Commands

Table 6 and Table 7 provide quick references of available commands. This is followed by a written description of each command. Three additional Truth Tables (Table 13 on page 46, Table 14 on page 47, and Table 15 on page 49) provide CKE commands and current/ next state information.

Table 6: Truth Table – Commands

Notes : 1 and 11 apply to all commands

Name (Function)	/CS	/RAS	/CAS	/WE	ADDR	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8, 10
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code2	2
Deep Power Down(Enter DPD Mode)	L	H	H	L	Op-Code2	11

Notes:

1. CKE is HIGH for all commands shown except SELF REFRESH and Deep Power Down.
2. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12 provide the op- code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A12 provide row address.
4. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW : BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. This command is a BURST TERMINATE if CKE is HIGH.
11. This command is a Deep Power Down if CKE is Low.
12. All states and sequences not shown are reserved and/or illegal.

Table 7: Truth Table – DM Operation

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

Note: Used to mask write data; provided coincident with corresponding data.

DESELECT

The DESELECT function (/CS HIGH) prevents new commands from being executed by the Low Power DDR SDRAM. The Low Power DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (/CS = LOW, /RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A12. See mode register descriptions in “Register Definition” on page 9. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS (MIN), as described for each burst type in "Operations" on page 24. The user must not issue another command to the same bank until the precharge time (tRP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 24. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Low Power DDR SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 512Mb Low Power DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends tRFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Low Power DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Low Power DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting). For a the full array refresh, all four banks are refreshed simultaneously with the refresh frequency set by an internal self refresh oscillator. This oscillator changes due to the temperature sensors input. As the case temperature of the Low Power DDR SDRAM increases, the oscillation frequency will change to accommodate the change of temperature. This happens because the DRAM capacitors lose charge faster at higher temperatures. To ensure efficient power dissipation during self refresh, the oscillator will change to refresh at the slowest rate possible to maintain the devices data.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Low Power DDR SDRAM must have NOP commands issued for tXSR is required for the completion of any internal refresh in progress.

Self refresh is not supported for automotive device at high temperature.(85℃ to 105℃)

DEEP POWER DOWN

Deep Power Down Mode is an operating mode to achieve extreme power reduction by cutting the power of the whole memory array of the device. Data will not be retained once the device enters DPD Mode. Full initialization is required when the device exits from DPD Mode. [Figure 38,39]

Maximum Ratings

Voltage on V_{DD}/V_{DDQ} Supply
Relative to V_{SS} .....-0.5V to + 2.3V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... –0.5V to +2.3V
Storage Temperature (plastic) ..... -55℃ to + 150℃
Power Dissipation 1W

*Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
FMD8C16LAx-xxEC	Commercial	0℃ to +70℃	1.7V ~ 1.95V	1.7V ~ V_{DD}
FMD8C16LAx-xxEE	Extended	-25℃ to +85℃		
FMD8C16LAx-xxEI	Industrial	-40℃ to +85℃		

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS [1,2]

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	1.7	1.95	V
I/O Supply Voltage	V_{DDQ}	1.7	V_{DD}	V
Input High Voltage : Logic 1 All Inputs [3.]	V_{IH}	0.7* V_{DDQ}	V_{DDQ} +0.3	V
Input Low Voltage : Logic 0 All Inputs [3.]	V_{IL}	-0.3	0.3*V_{DDQ}	V
Data Output High Voltage : Logic 1 : All Inputs(-0.1mA)	V_{OH}	0.9* V_{DDQ}		V
Data Output Low Voltage : Logic 0 : All Inputs(0.1mA)	V_{OL}		0.1* V_{DDQ}	V
Input Leakage Current : Any Input 0V=V_{IN}=V_{DD} (All other pins not under test=0V)	II	-5	5	μA
Output Leakage Current : DQs are disabled ; 0V= V_{OUT}=V_{DDQ}	I_{OZ}	-5	5	μA

Table 8. AC Operating Conditions[1,2,3,4,5,6]

Parameter / Condition	Value	Units
AC input levels (Vih / Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	AC Output Load Circuit on page 21	V

Note :

1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C ≤ TA ≤ +85°C for IT parts) is ensured.
2. An initial pause of 200μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
3. All states and sequences not shown are illegal or reserved.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
6. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to V_{IH}/2 = crossover point. If the input transition time is longer than t_T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the V_{IH}/2 crossover point.

Table 9: IDD Specifications and Conditions

Parameter/Condition		Symbol	Max -25	Units	Notes
Operating one bank active precharge current: tRC = tRC(MIN); tCLK = tCLK(MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD0	60	mA	1, 6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2P	300	µA	2, 4
Precharge power-down standby current with CLK stopped: All banks idle; CKE is LOW, CS is HIGH; CLK = LOW, /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2PS	300	µA	2, 4
Precharge non power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; tCLK =tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2N	15	mA	5
Precharge non power-down standby current: CLK stopped; All banks idle; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2NS	8	mA	5
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3P	3	mA	2, 4
Active power-down standby current: CLK stopped; One bank active; CKE = LOW; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3PS	2	mA	2, 4
Active non power-down standby: One bank active; CKE = HIGH; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two cycles; Data bus inputs are stable.		IDD3N	15	mA	1
Active non-power-down standby: CLK stopped; One bank active; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3NS	8	mA	1
Operating burst read : One bank active; BL = 4; tCLK = tCLK(MIN); Continuous READ bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4R	80	mA	1, 6
Operating burst write: One bank active; BL = 4; tCLK = tCLK(MIN); Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4W	80	mA	1, 6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable.	tRC = tRFC(138ns)	IDD5	95	mA	7
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.	tRC = 7.8125µs	IDD5a	3	mA	3, 7
Self refresh: CKE = LOW; tCLK = tCLK(MIN); Address and control inputs are stable; Data bus inputs are Stable.	Full Array, 85°C	IDD6a	600	µA	8, 9
	Full Array, 45°C	IDD6a	450	µA	8, 9
	Half Array, 85°C	IDD6b	500	µA	8, 9
	¼ Array, 85°C	IDD6c	400	µA	8, 9
Deep Power Down Current ; Address, control and data bus inputs are STABLE		IDD7	10	µA	10

Notes :

1. MIN (tRC or tRFC) for IDD measurements is the smallest multiple of tCLK that meets the minimum absolute value for the respective parameter. tRAS (MAX) for IDD measurements is the largest multiple of tCLK that meets the maximum absolute value for tRAS.
2. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.
3. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (tRFC [MIN]) else CKE is LOW (i.e., during standby).
4. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/ DM/DQS slew rate is less than 0.5V/ns, timing must be derated: ***50ps (pending) must be added to tDS and tDH for each 100mv/ns reduction in slew rate.*** If slew rate exceeds 4V/ns, functionality is uncertain.

5. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
6. Switching is defined as :
   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.
7. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
8. With the inclusion of the temperature sensor on the low-power DDR device, these numbers are shown as examples only, and will change due to the junction temperature that the device is sensing. They are expected to be maximum values at this time.
9. Enables on-chip refresh and address counters.
10. Device must be in the all banks idle state prior to entering Deep Power Down.

Table 10: Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance (A0-A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE)	CIN1	1.5	3.0	pF
Input capacitance (CLK, /CLK)	CIN2	1.5	3.0	pF
Data & DQS input / output capacitance	COUT	3.0	5.0	pF
Input capacitance(DM)	CIN3	3.0	5.0	pF

AC Output Load Circuit

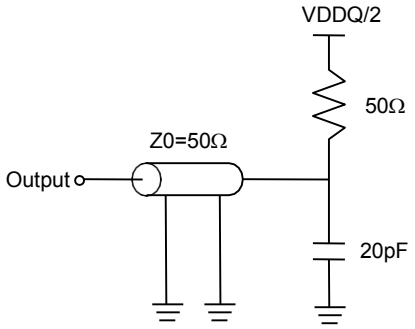


Table 11: Electrical Characteristics and Recommended AC Operating Conditions

AC Characteristics		Symbol	-25		Units	Notes
Parameter			Min	Max		
Access window of DQ from CLK & /CLK	CL=3	tAC(3)	2.0	5.0	ns	
	CL=2	tAC(2)	2.0	6.0		
CLK high-level width		tCH	0.45	0.55	tCLK	
CLK low-level width		tCL	0.45	0.55	tCLK	
System Clock cycle time	CL=3	tCLK(3)	5	100	ns	1
	CL=2	tCLK(2)	12	-	ns	
Auto precharge write recovery + precharge time		tDAL	5	-	tCLK	16
DQ and DM input hold time relative to DQS		tDH	0.48	-	ns	9, 13, 15
DQ and DM input setup time relative to DQS		tDS	0.48	-	ns	17
DQ and DM input pulse width (for each input)		tDIPW	1.6	-	ns	
Access window of DQS from CLK & /CLK		tDQSCLK	2.0	5.0	ns	
DQS input high-pulse width		tDQSH	0.4	0.6	tCLK	
DQS input low-pulse width		tDQSL	0.4	0.6	tCLK	
Data strobe edge to Dout edge		tDQSQ	-	0.4	ns	8, 9
WRITE command to first DQS latching transition		tDQSS	0.75	1.25	tCLK	
DQS falling edge to CLK rising – setup time		tDSS	0.2	-	tCLK	
DQS falling edge from CLK rising – hold time		tDSH	0.2	-	tCLK	
Half-CLK period		tHP	tCH, tCL	-	ns	12
Data-out High-Z window from CLK & /CLK		tHZ	-	5.0	ns	3, 11
Data-out Low-Z window from CLK & /CLK		tLZ	1.0	-	ns	3, 11
Transition Time		t_T	0.5	1.2	ns	
Address and control input hold time		tIH	0.9	-	ns	2, 15
Address and control input setup time		tIS	0.9	-	ns	2, 15
Address and control input pulse width		tIPW	2.2	-	ns	17
LOAD MODE REGISTER command cycle time		tMRD	2	-	tCLK	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		tQH	tHP -tQHS	-	ns	8, 9
Data hold skew factor		tQHS	-	0.5	ns	
ACTIVE-to-PRECHARGE command		tRAS	42	70,000	ns	10
ACTIVE-to-ACTIVE command period		tRC	55	-	ns	
AUTO REFRESH command period		tRFC	80	-	ns	14
ACTIVE-to-READ or WRITE delay		tRCD	15	-	ns	
PRECHARGE command period		tRP	15	-	ns	
DQS read preamble	CL=3	tRPRE(3)	0.9	1.1	tCLK	11
	CL=2	tRPRE(2)	0.5	1.1	tCLK	11
DQS read postamble		tRPST	0.4	0.6	tCLK	
Read of SRR to next valid command		tSRC	CL+1	-	tCLK	
SRR to Read		tSRR	2	-	tCLK	
Internal temperature sensor valid temperature output enable		tTQ	2	2	ms	
ACTIVE bank *a* to ACTIVE bank *b* Delay		tRRD	10	-	ns	

Table 12: Electrical Characteristics and Recommended AC Operating Conditions (continued)

AC Characteristics Parameter	Symbol	-25 Min	-25 Max	Units	Notes
DQS write preamble	tWPRE	0.25	-	tCLK	
DQS write preamble setup time	tWPRES	0	-	ns	5, 6
DQS write postamble	tWPST	0.4	0.6	tCLK	4
Write recovery time	tWR	15	-	ns	
Internal WRITE to READ command delay	tWTR	2	-	tCLK	
Average periodic refresh interval	tREFI	-	7.8	µs	7
Exit SELF REFRESH to first valid command	tXSR	120	-	ns	18
Exit power-down mode to first valid command	tPDX	25	-	ns	19
Minimum tCKE HIGH/LOW time	tCKE	1	-	tCLK	

Notes

1. CAS latency definition: for CL = 2, the first data element is valid at (tCLK + tAC) after the CLK at which the READ command was registered; for CL = 3, the first data element is valid at (2 × tCLK + tAC) after the first CLK at which the READ command was registered.
2. Fast command/address input slew rate ≥ 1V/ns. Slow command/address input slew rate ≥ 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: tIS has ***an additional 50ps (pending) per each 100mV/ns*** reduction in slew rate from the 0.5V/ns. ***tIH has 0ps added (pending);*** that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions.These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
6. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command.
7. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.
8. The valid data window is derived by achieving other specifications: tHP (tCLK/2), tDQSQ, and tQH (tHP - tQHS). The data valid window derates directly proportional with the CLK duty cycle and a practical data valid window can be derived. The CLK is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
9. Referenced to each output group: DQS0 with DQ0–DQ7; and DQ1 with DQ8–DQ1
10. READs and WRITEs with auto precharge are allowed to be issued before tRAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
11. tHZ (MAX) will prevail over tDQSCLK (MAX) + tRPST (MAX) condition.
12. tHP (MIN) is the lesser of tCL minimum and tCH minimum actually applied to the device CLK and /CLK inputs, collectively.
13. Random addressing changing 50 percent of data changing at every transfer.
14. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
15. The transition time for input signals (/CAS, CKE, /CS, DM, DQ, DQS, /RAS, /WE, and addresses) are measured between VIL(DC) to VIH(AC) for rising input signals and VIH(DC) to VIL(AC) for falling input signals.
16. tDAL = (tWR/tCLK) + (tRP/tCLK): for each term, if not already an integer, round to the next higher integer.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. CLK must be toggled a minimum of two times during this period.
19. CLK must be toggled a minimum of one time during this period.
20. This device can support 45/55 of duty rate for tDQSCLK in case of 50/50 of CLK input.

Operations

Bank/row Activation

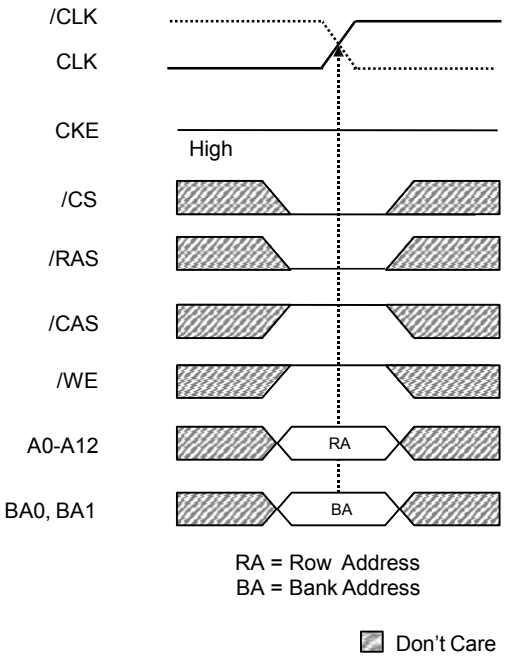
Before any READ or WRITE commands can be issued to a bank within the Low Power DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 5.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 18ns with a 133 MHz clock (7.5ns period) results in 2.4 clocks rounded to 3.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure 5: Activating a Specific Row in a Specific Bank



READ

READ bursts are initiated with a READ command, as shown in Figure 6 on page 26.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CLK and /CLK). Figure 7 on page 27 shows general timing for each possible CAS latency setting. DQS is driven by the Low Power DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of tDQSCLK (DQS transition skew to CLK) and tAC (data-out transition skew to CLK) is depicted in Figure 28 on page 52.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued ***x*** cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 8 on page 28.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 9 on page 29. Full speed random read accesses within a page (or pages) can be performed as shown in Figure 10 on page 30.

Figure 6: READ Command

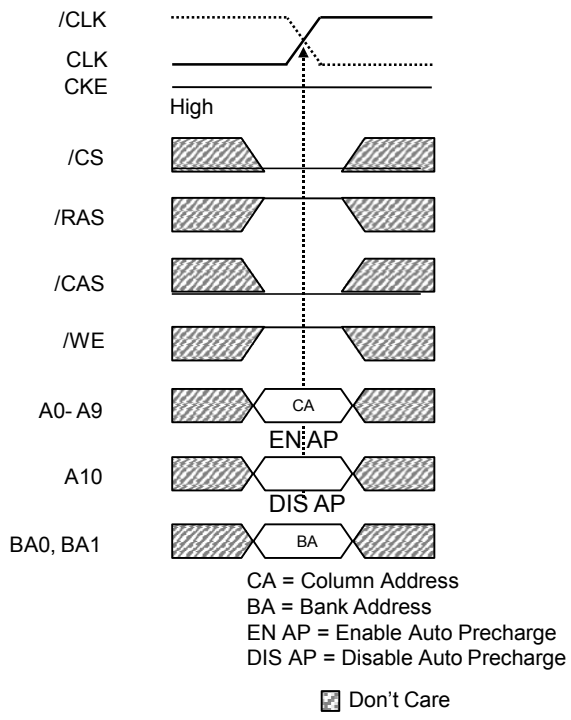
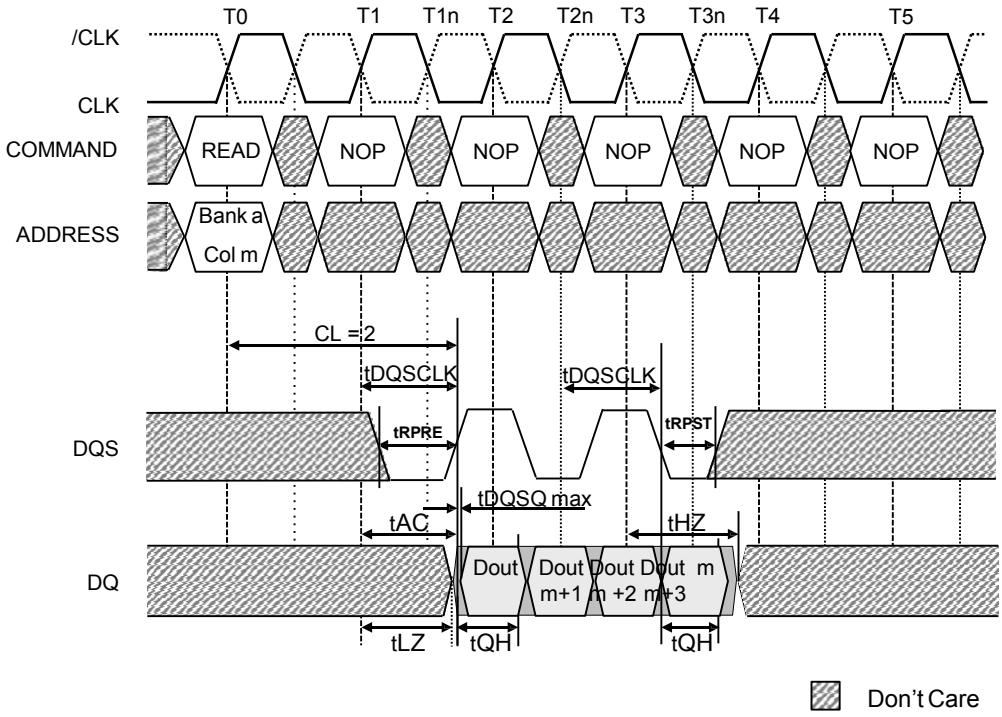


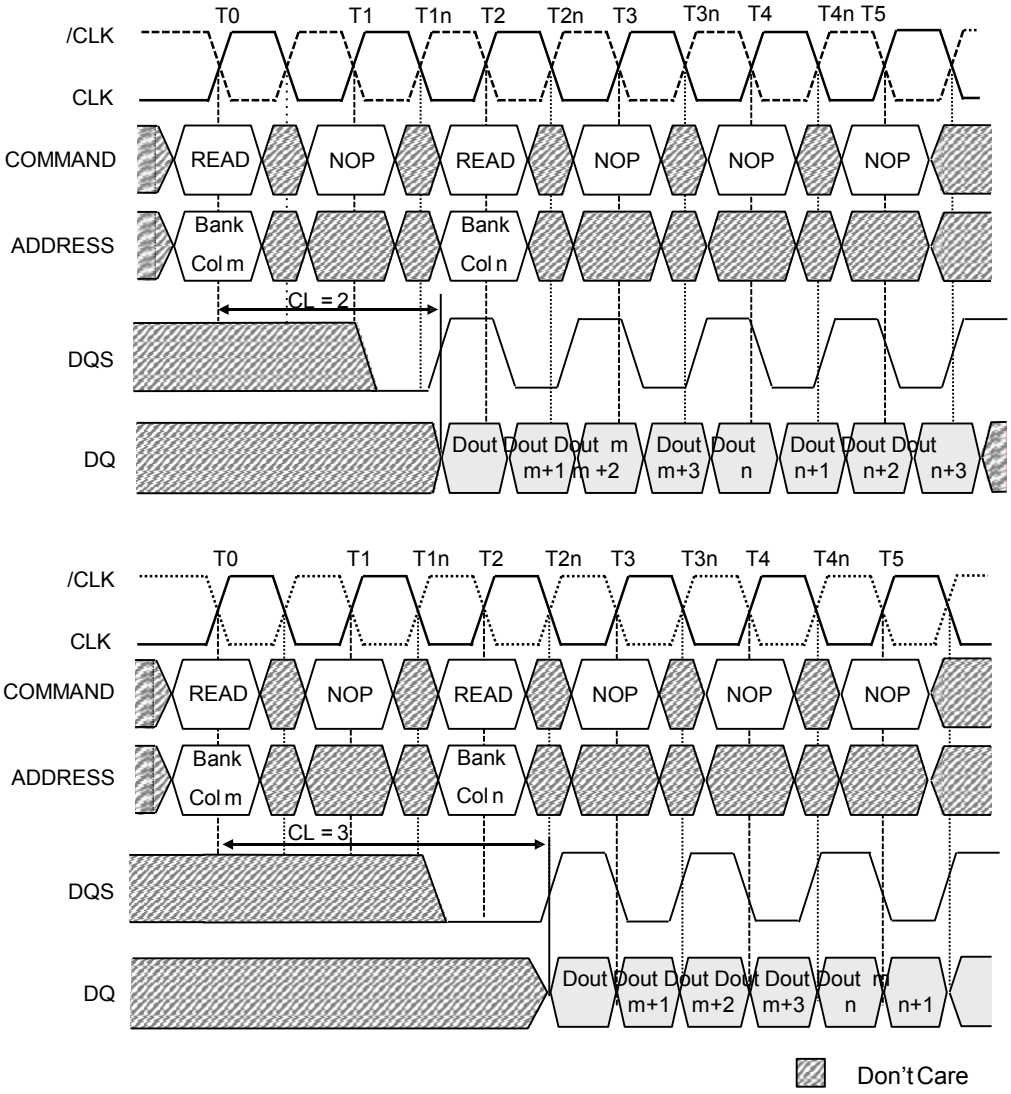
Figure 7: READ Operation



Notes :

1. Dout m = data-out from column m.
2. BL = 4.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.

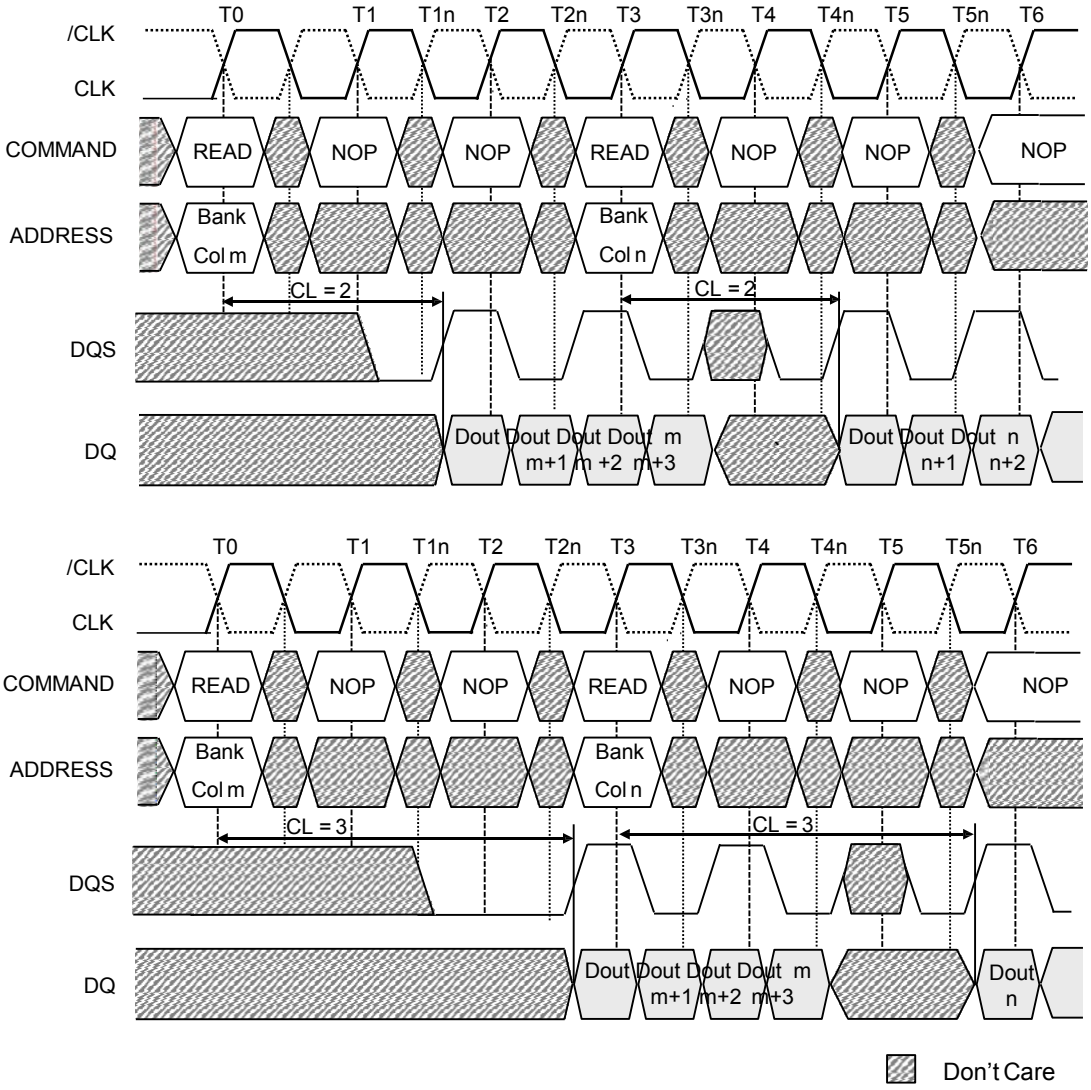
Figure 8: Consecutive Read Bursts



Notes :

1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents consecutive READ commands issued to the device.

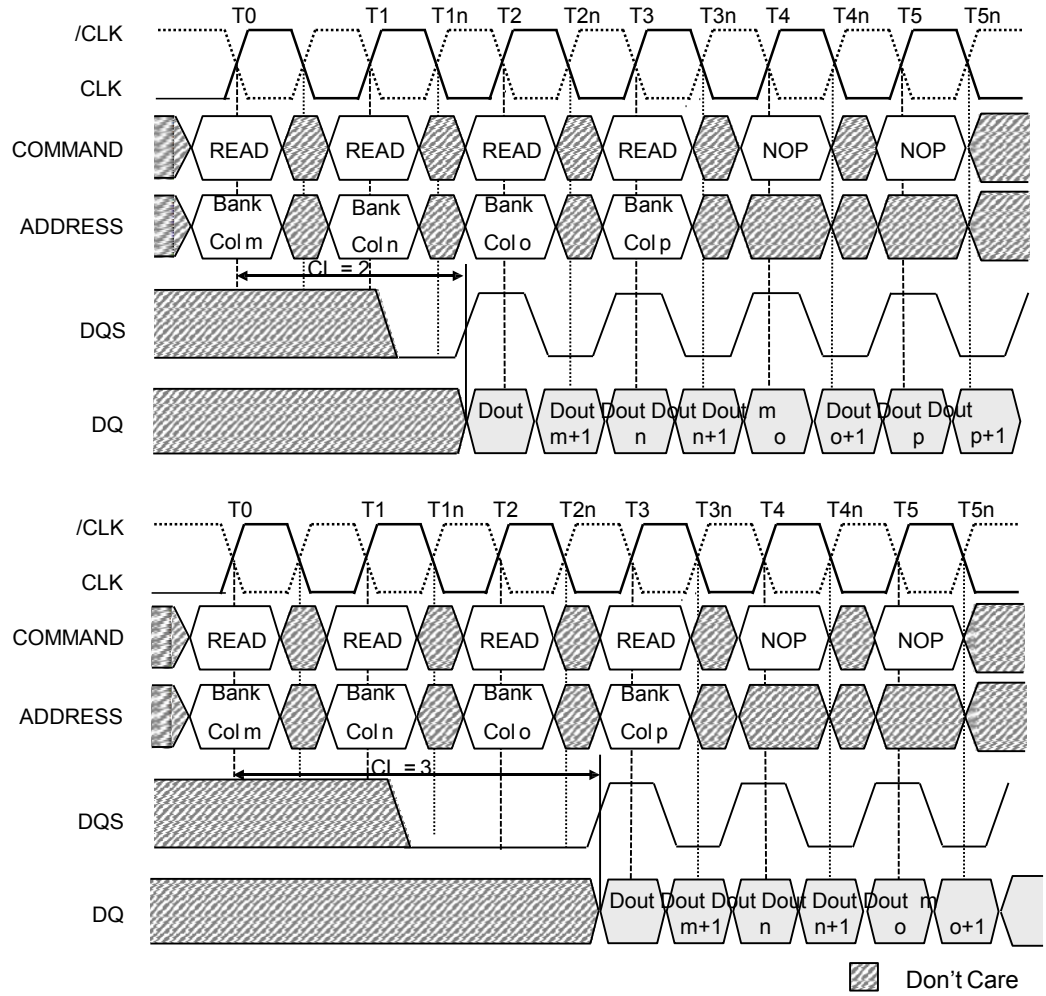
Figure 9: Read-to-Read Operation



Notes :

1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents nonconsecutive READ commands issued to the device.

Figure 10: Random READ Accesses



Notes :

1. Dout m (or n, o, p) = data-out from column m *(*or column n, column o, column p).
2. BL = 4 in the cases shown.
3. READs are to an active row in any bank.
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.

Truncated READs

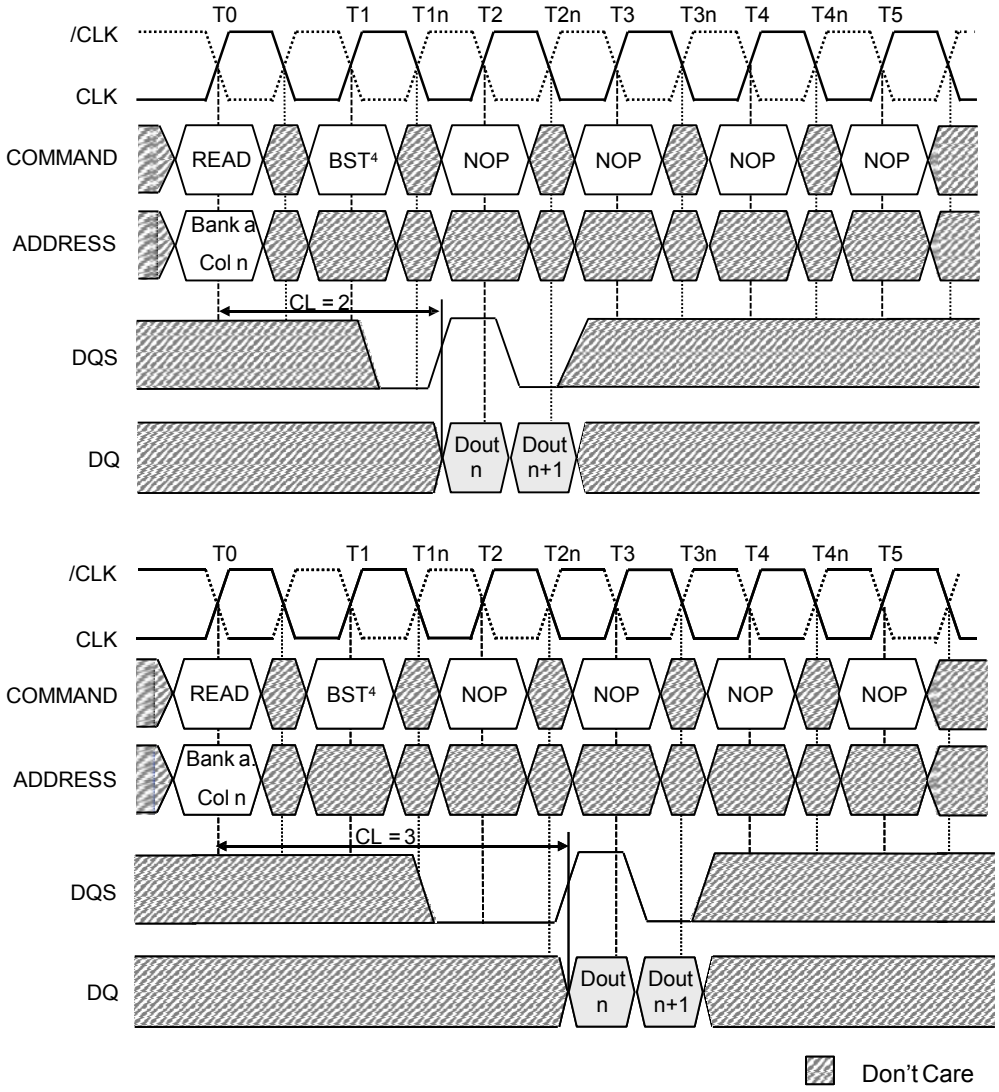
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11 on page 31. The BURST TERMINATE latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12 on page 32. The tDQSS (MIN) case is shown; the tDQSS (MAX) case has a longer bus idle time. (tDQSS [MIN] and tDQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the *n*-prefetch architecture). This is shown in Figure 13 on page 33. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

Note: Part of the row precharge time is hidden during the access of the last data elements

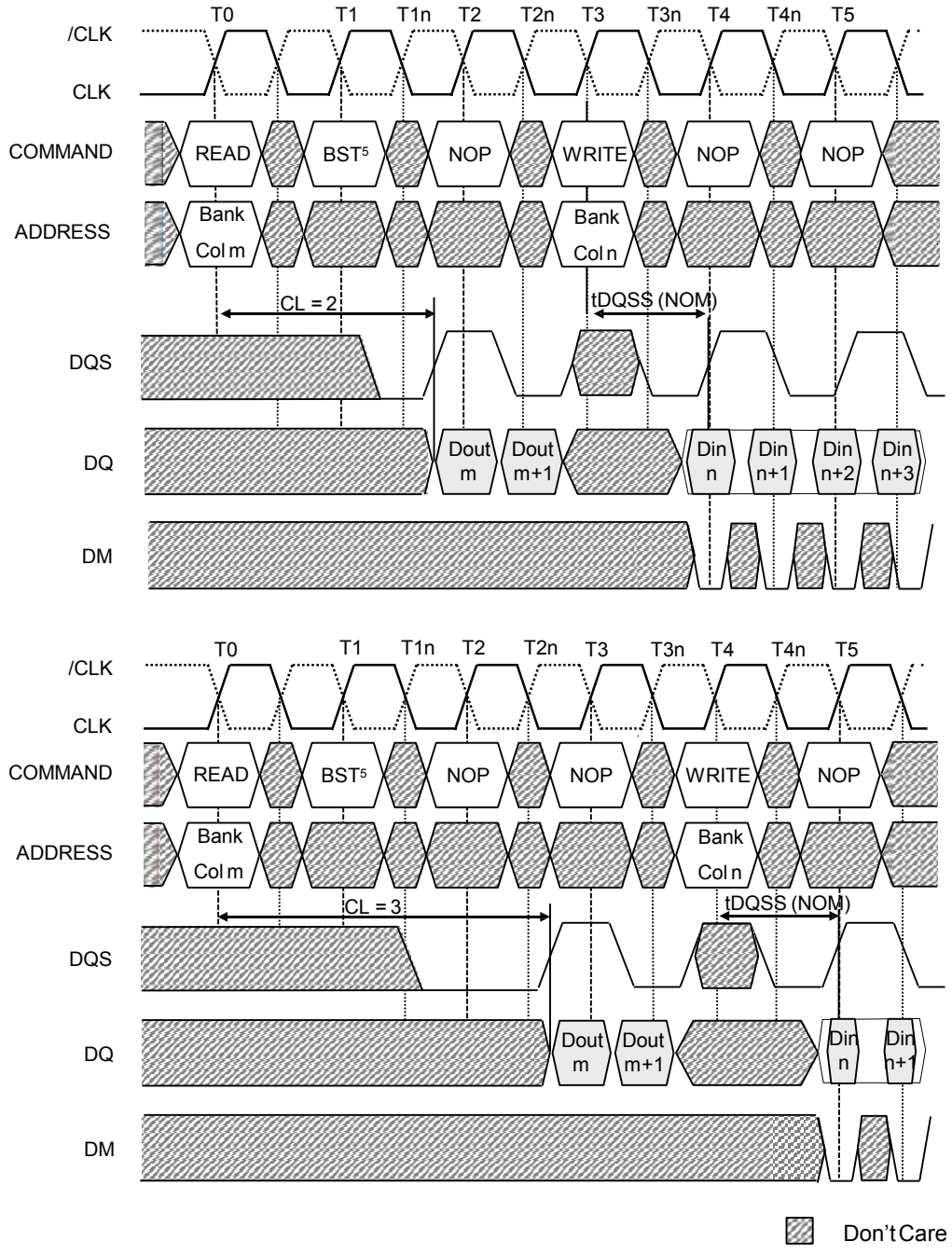
Figure 11: READ Burst Terminated



Notes :

1. Dout n = data-out from column n.
2. Only valid for BL = 4 and BL = 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

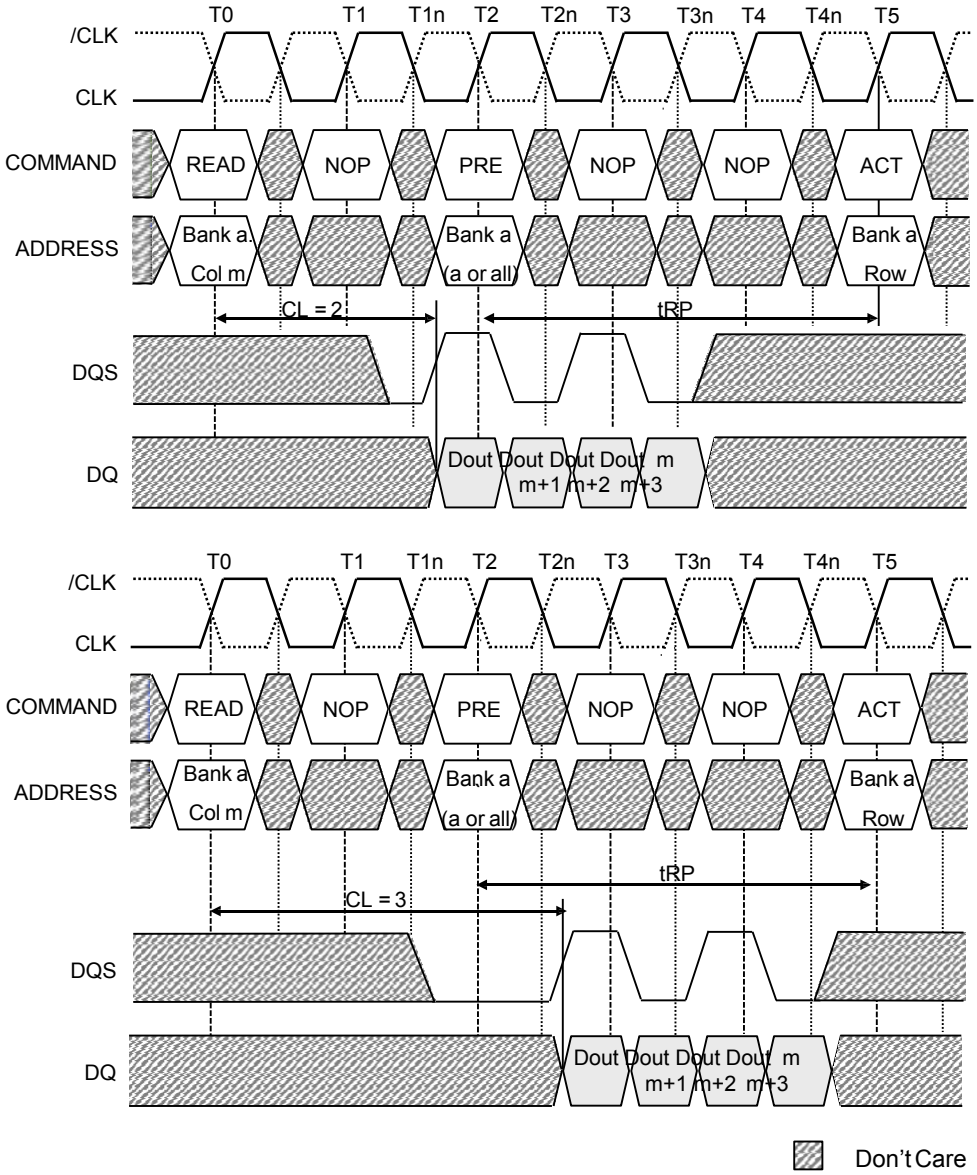
Figure 12: READ-to-WRITE Operation



Notes :

1. Dout m = data-out from column m.
2. Din n = data-in from column n.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.

Figure 13: READ-to-PRECHARGE Operation



Notes :

1. Dout m = data-out from column m.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided tRAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL / 2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITE

WRITE bursts are initiated with a WRITE command, as shown in Figure 14 on page 35. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS [MIN] and tDQSS [MAX]) might not be intuitive, they have also been included. Figure 15 on page 36 shows the nominal case and the extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

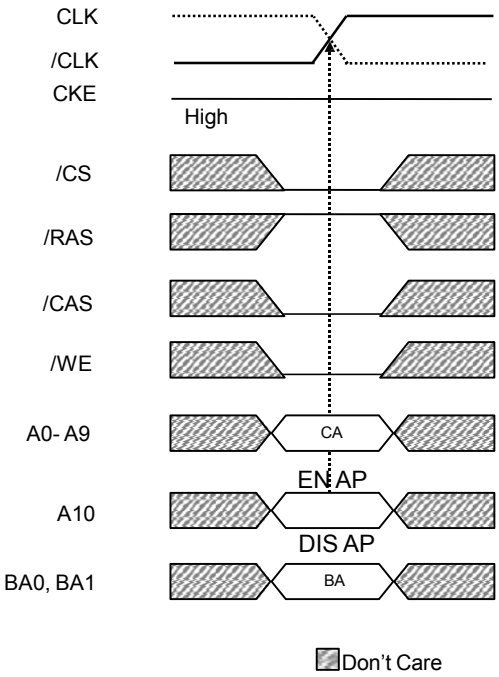
Figure 16 on page 37 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 17 on page 37. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 18 on page 38. Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, tWTR should be met, as shown in Figure 19 on page 39.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 20 on page 40. Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 21 on page 41.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, tWR should be met, as shown in Figure 22 on page 42.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 23 on page 43 and Figure 24 on page 44. Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 23 on page 43 and Figure 24 on page 44. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

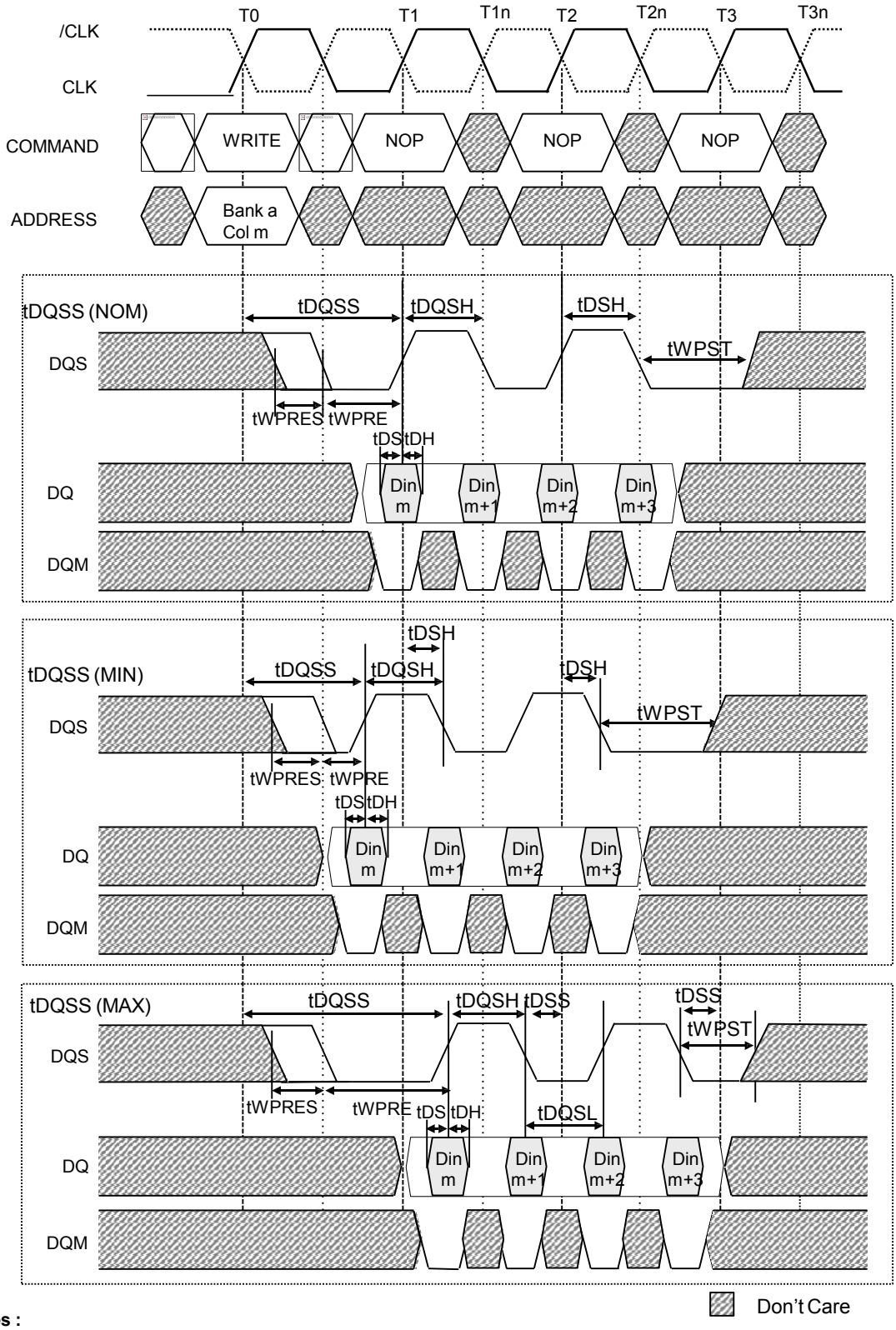
Figure 14: WRITE Command



Note :

1. DIS AP = Disable Auto Precharge
2. EN AP = Enable Auto Precharge
3. BA = Bank Address
4. CA = Column Address

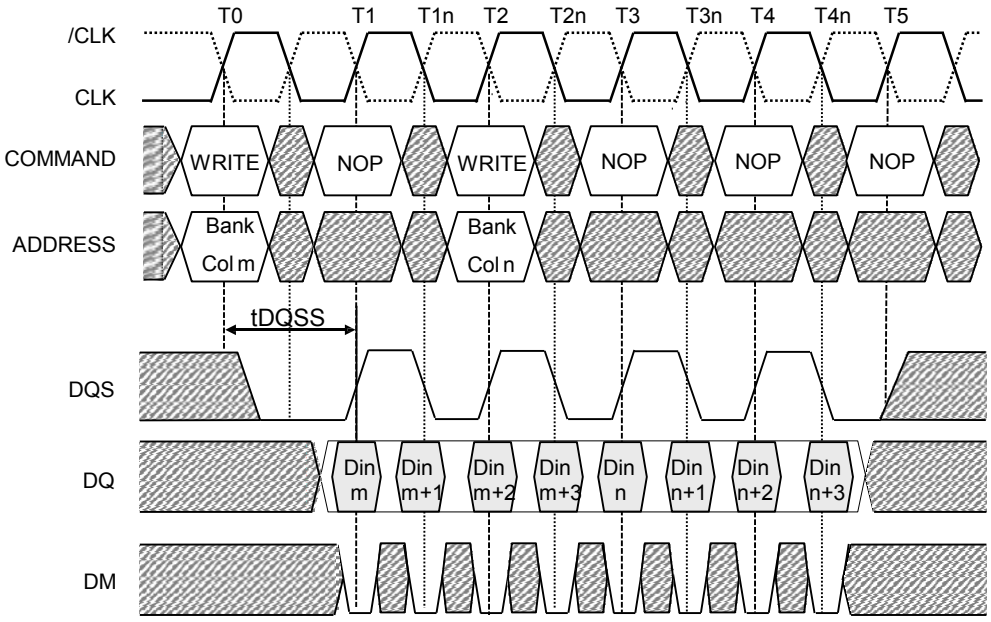
Figure 15: WRITE Operation



Notes :

1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (auto precharge is disabled).

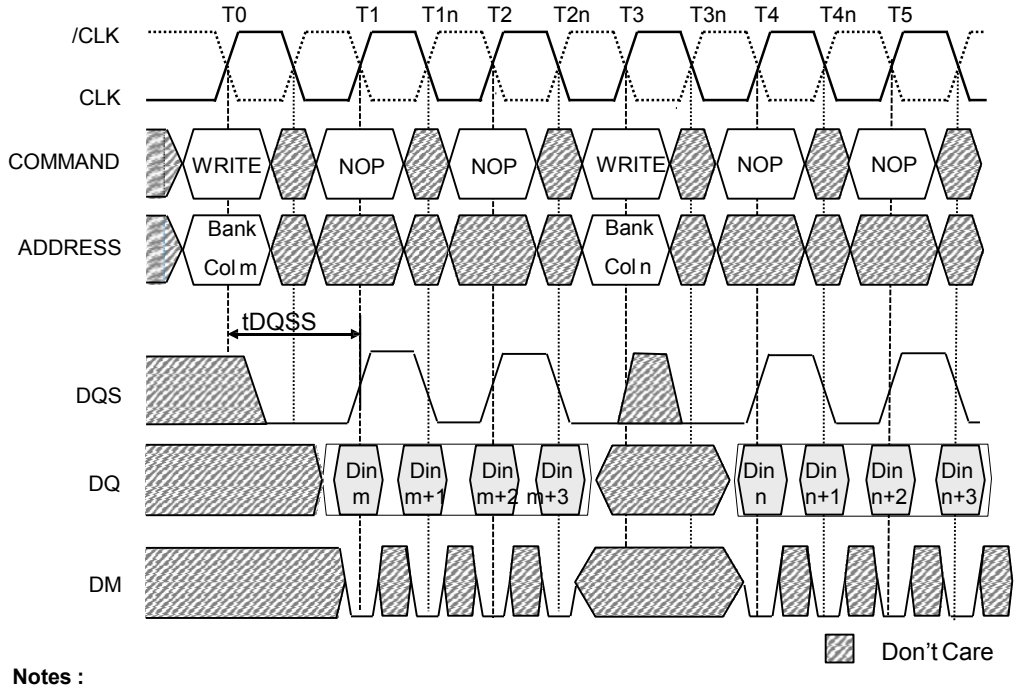
Figure 16: Consecutive WRITE-to-WRITE



Notes :

1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

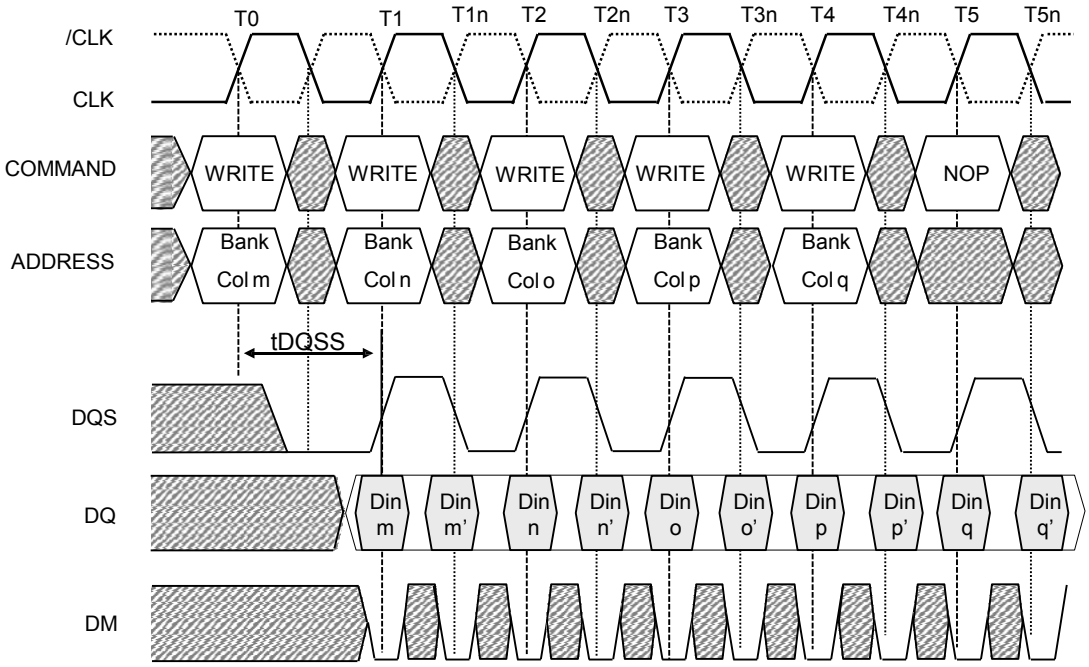
Figure 17: WRITE-to-WRITE Operation



Notes :

1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

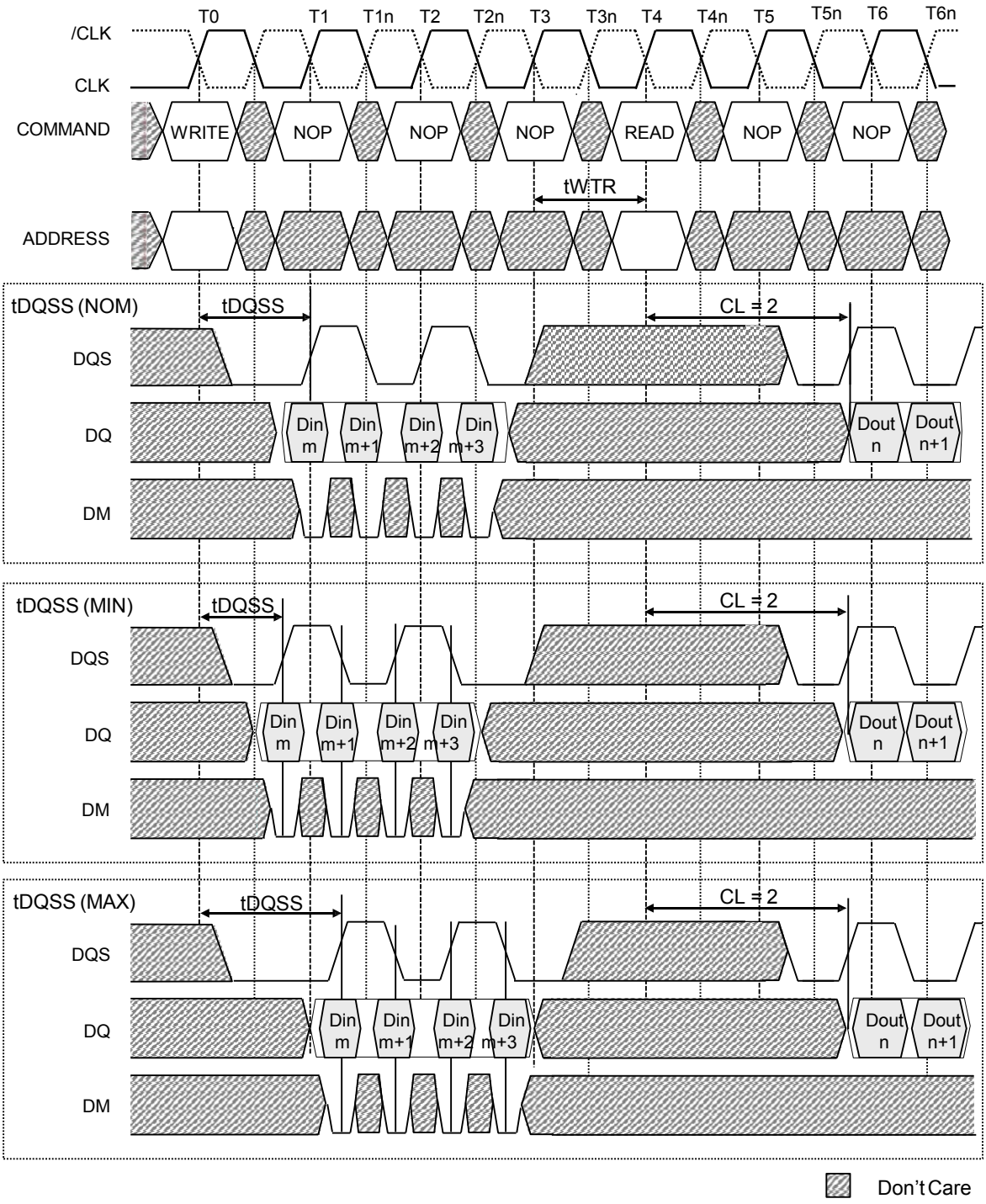
Figure 18: Random WRITE Cycles



Notes :

1. Din m (or n, o, p, q) = data-in for column m (or n, o, p, q)
2. m' (or n, o, p, q) = the next data-in following Din m (or n, o, p, q), according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.

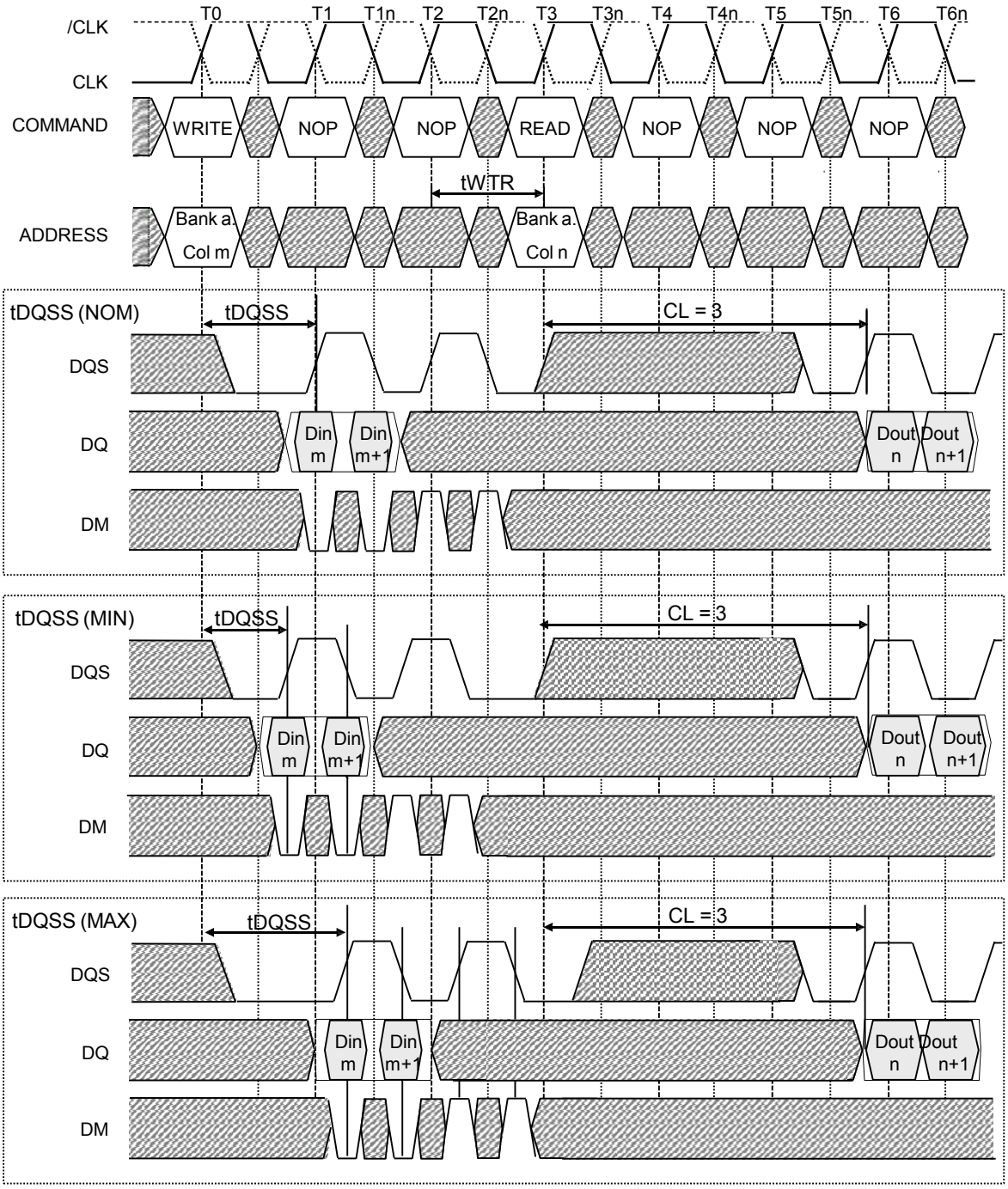
Figure 19: WRITE-to-READ – Uninterrupting



Notes :

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An uninterrupted burst of 4 is shown.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. The READ and WRITE commands are to same device. However, the READ and WRITE commands may be to different devices, in which case tWTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

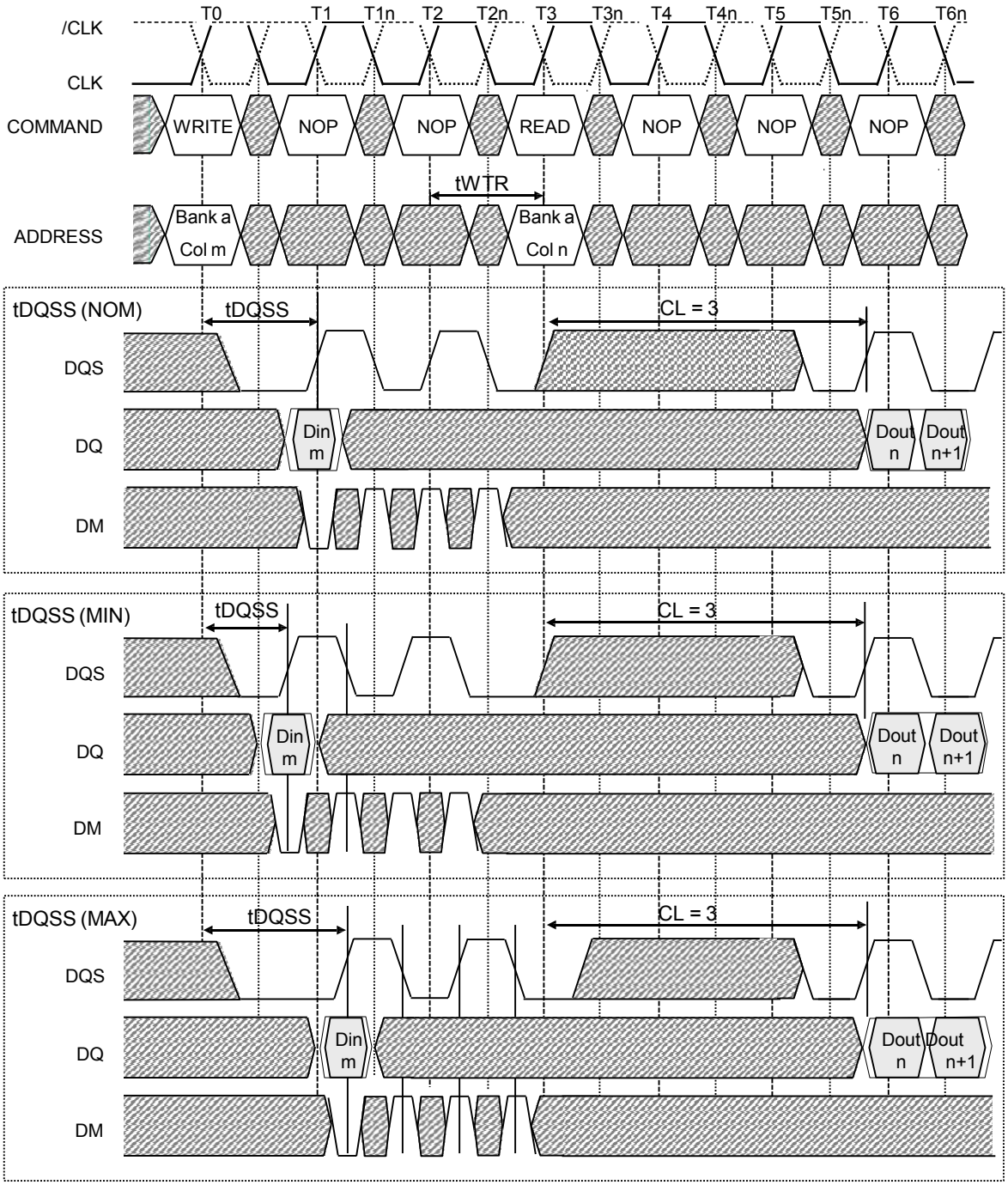
Figure 20: WRITE-to-READ – Interrupting



Notes :

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

Figure 21: WRITE-to-READ – Odd Number of Data, Interrupting

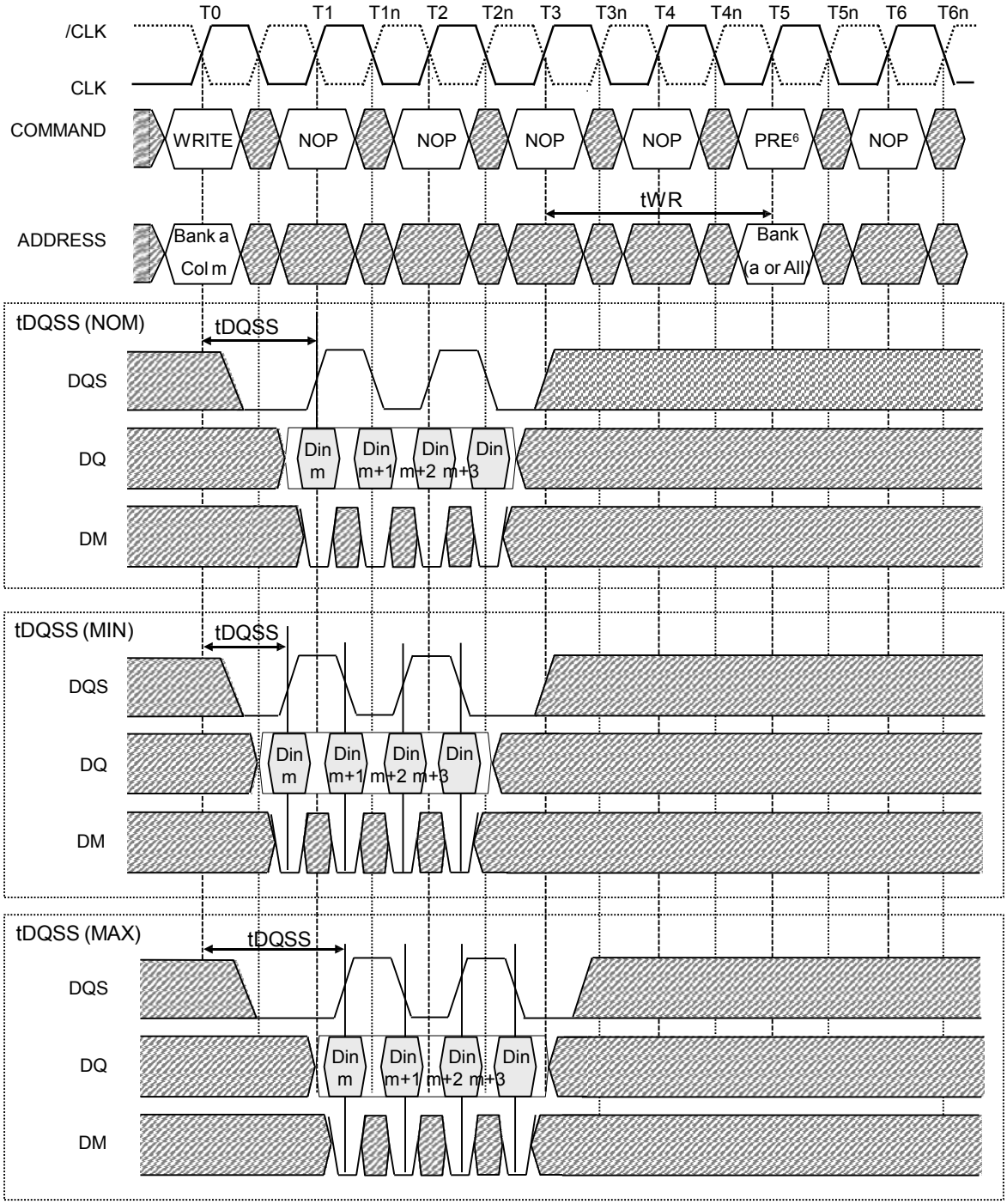


Notes :

Don't Care

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written, three are masked.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

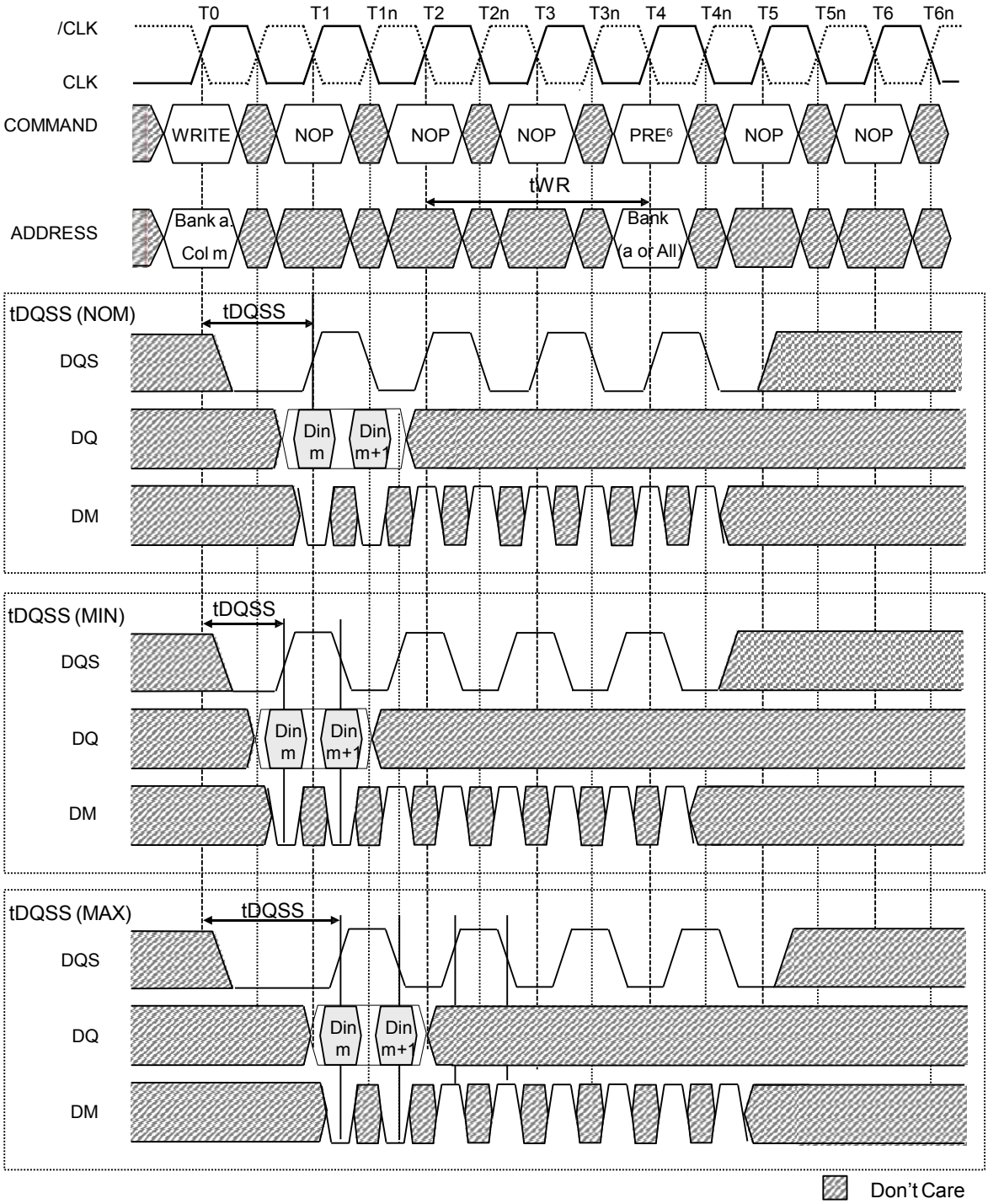
Figure 22: WRITE-to-PRECHARGE – Uninterrupting



Notes :

1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

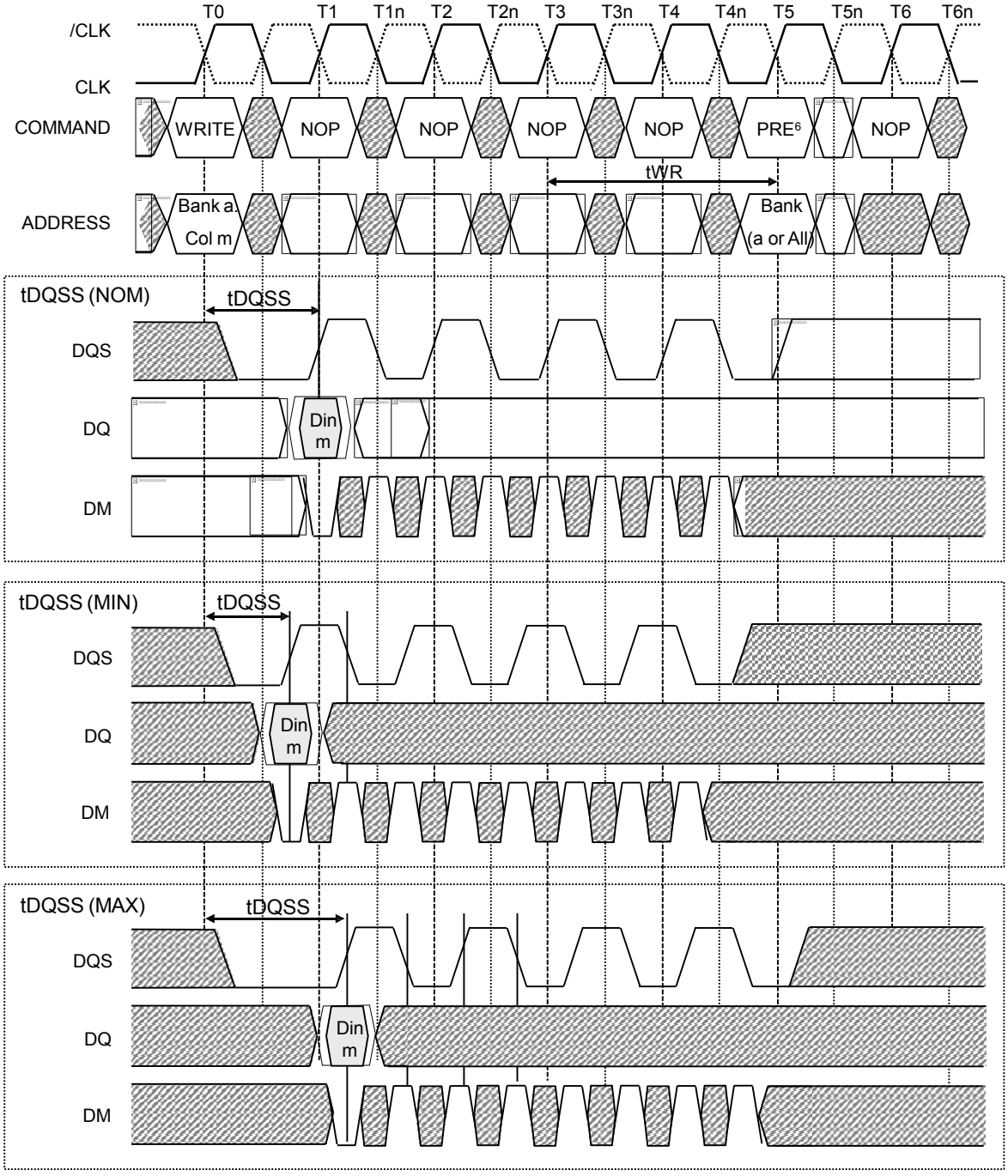
Figure 23: WRITE-to-PRECHARGE – Interrupting



Notes :

1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

Figure 24: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting



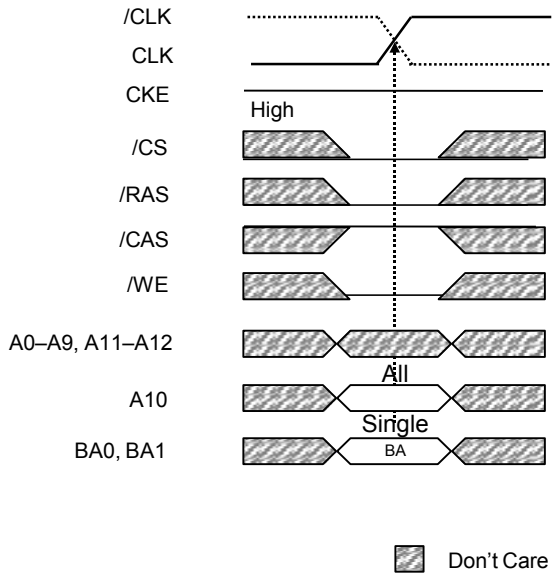
Notes :

1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

PRECHARGE

The PRECHARGE command (Figure 25) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 25: PRECHARGE Command



Note :

1. BA = Bank Address.
2. All = All banks to be Precharged, BA1, BA0 are "Don't Care."
3. Single = Only bank selected by BA1 and BA0 will be precharged.

Power-Down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst; thus a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.

Power-Down (Active or Precharge)

Power-down (Figure 27) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, including CLK and /CLK. Exiting power-down requires the device to be at the same voltage as when it entered power-down and a stable clock.

Note :

The power-down duration is limited by the refresh requirements of the device. While in power-down, CKE LOW must be maintained at the inputs of the Low Power DDR SDRAM, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until tPDX is satisfied.

Figure 26: Power-Down Command (Active or Precharge)

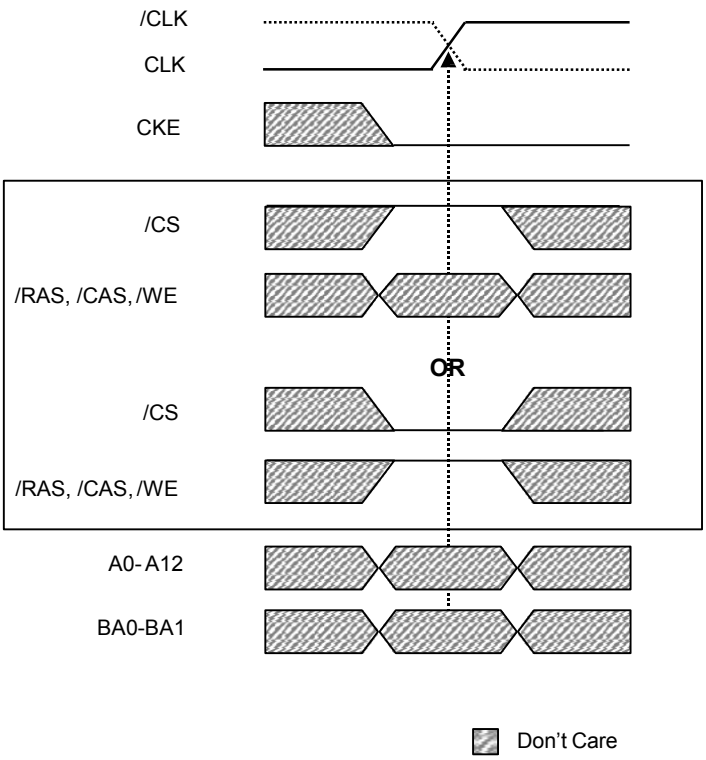
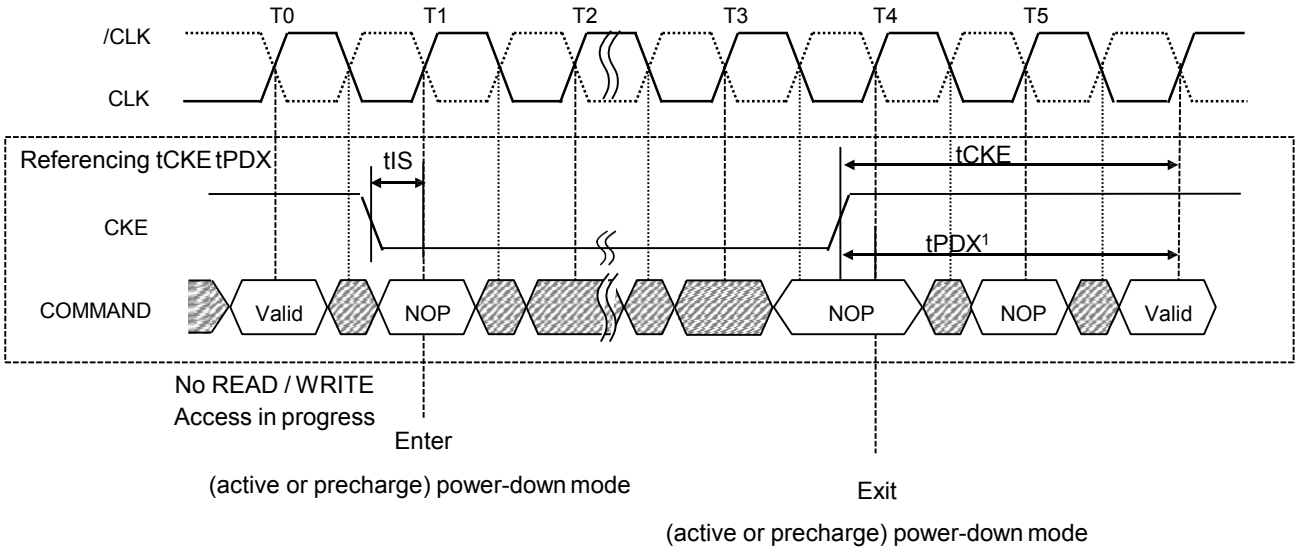


Figure 27: Power-Down (Active or Precharge)



Notes: 1. Clock must toggle a minimum of once during this time.

Truth Tables

Table 13: Truth Table – CKE

Notes: 1–5

CKEn-1	CKEn	Current State	COMMANDn	ACTIONn	Notes
L	L	(Active) Power-Down	X	Maintain (active) power-down	
L	L	(Precharge) Power-Down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	(Active) Power-Down	DESELECT or NOP	Exit (active) power-down	6, 7
L	H	(Precharge) Power-Down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	(Active) power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 15 on page 49		
H	H		See Table 15 on page 49		

Notes :

1. CKEn is the logic state of CKE at clock edge *n*; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n,* and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. tCKE pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the tPDX period.
7. The clock must toggle at least once during the tPDX period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSR period.
9. The clock must toggle at least once during the tXSR period.

Table 14 Truth Table – Current State Bank *n* - Command to Bank *n*

Notes : 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes :

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) and after tPDX has been met (if the previous state was power-down).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 14, and according to Table15.

   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the row active state.

   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the DDR SDRAM will be in the all banks idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. Once tMRD is met, the Low Power DDR SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.

10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 15: Truth Table – Current State Bank *n* - Command to Bank *m*

Notes : 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7. 9, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes :

1. This table applies when CKE*n*-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) or after tPDX has been met (if the previous state was power-down).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read with auto precharge enabled: See following text – 3a

   Write with auto precharge enabled: See following text – 3a

3a. The read with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins.

   This device supports concurrent auto precharge such that when a read with auto precharge enabled or a write with auto precharge is enabled any command to other banks is allowed, long as that command does not interrupt the read or write data transfer already in process. either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

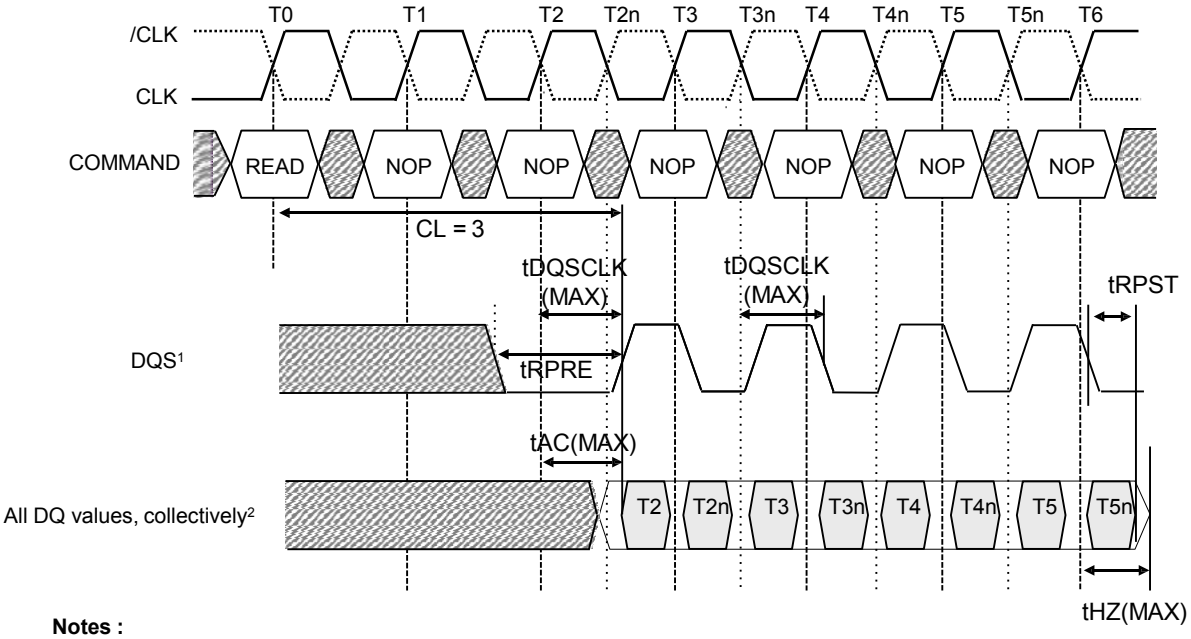
From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	[1 + (BL/2)] tCLK + tWTR
	WRITE or WRITE w/AP	(BL/2) tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK
READ w/AP	READ or READ w/AP	(BL/2) × tCLK
	WRITE or WRITE w/AP	[CLRU + (BL/2)] tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK

CLRU = CAS Latency (CL) rounded up to the next integer

BL = Burst Length

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

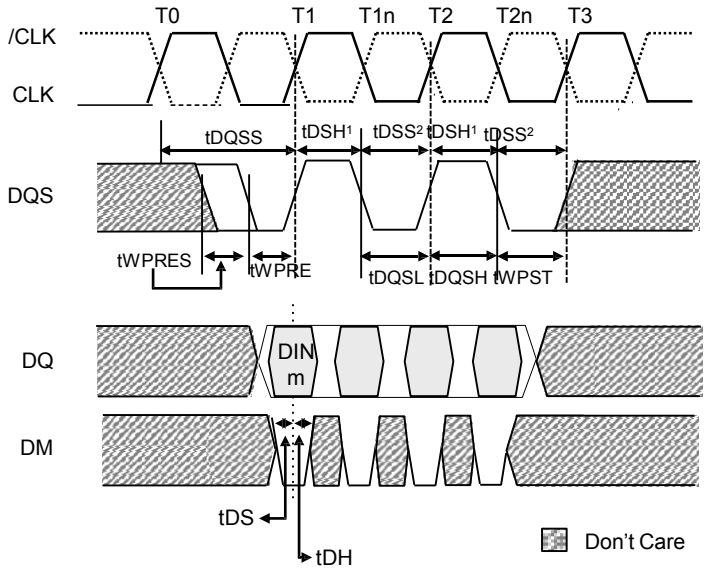
Figure 28: Data Output Timing – tAC and tDQSCLK



Notes :

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CLK, and is the “long term” component of DQ skew.

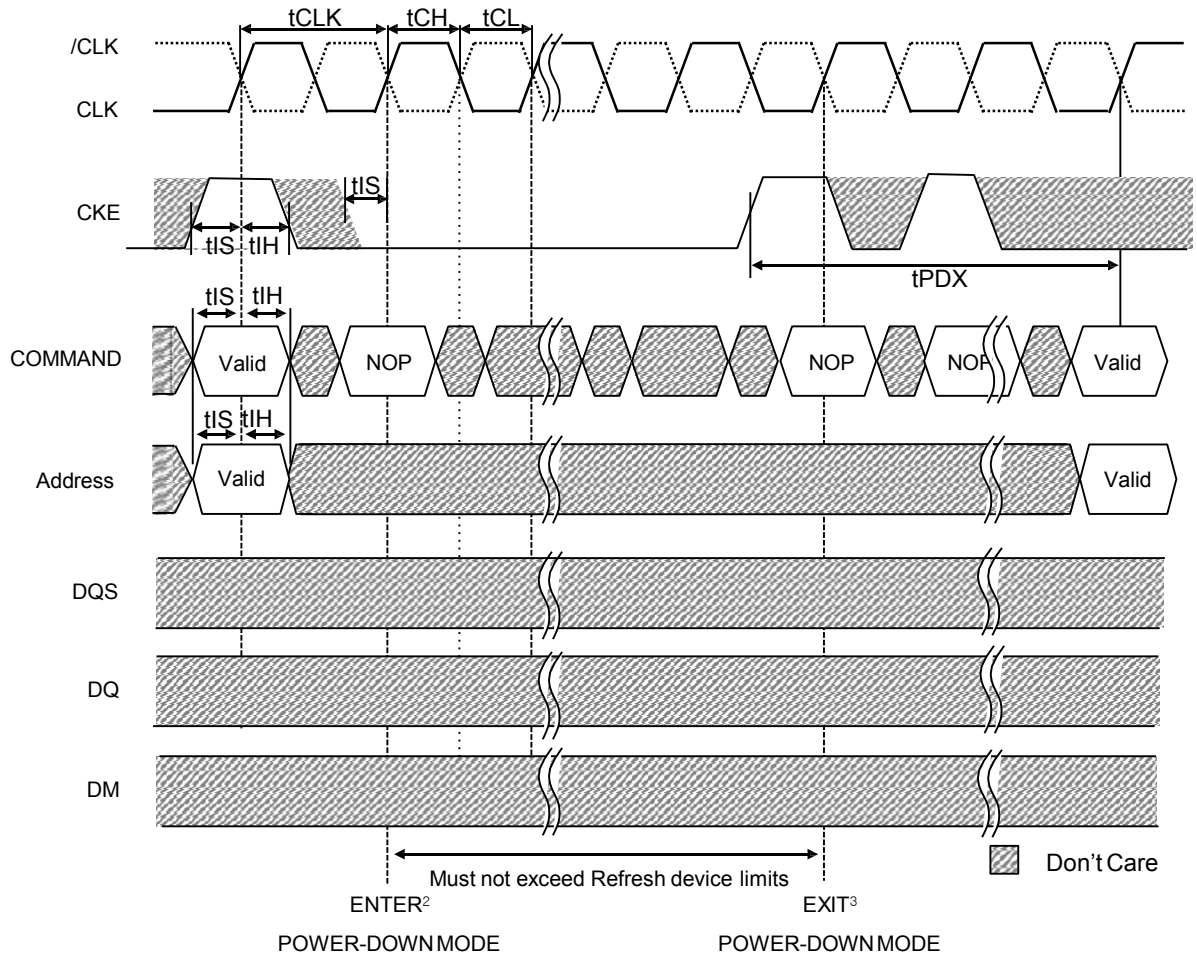
Figure 29: Data Input Timing



Notes :

1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).
3. WRITE command issued at T0.

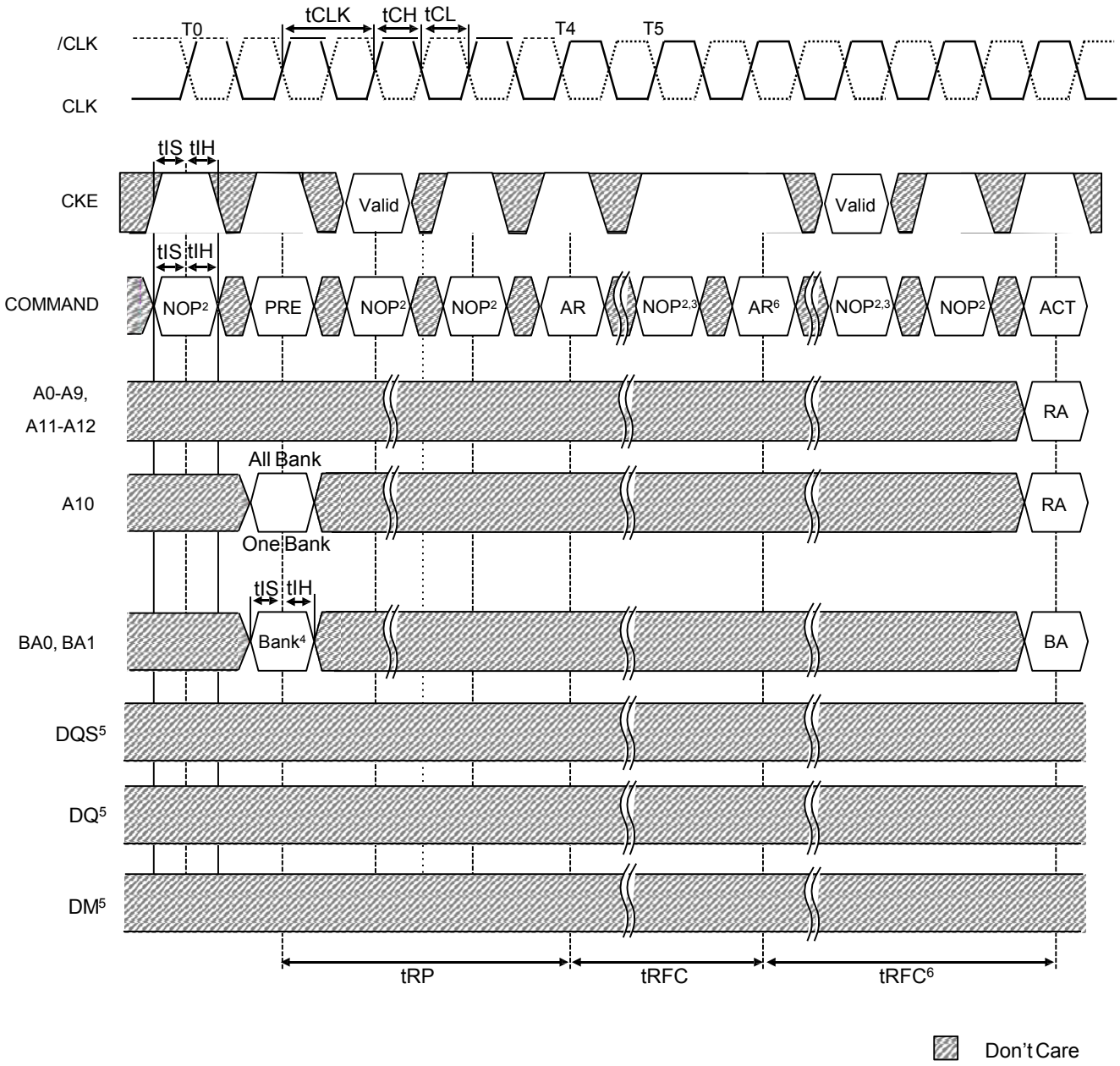
Figure 30: Power-Down Mode (Active or Precharge)



Notes :

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during tPDX time.

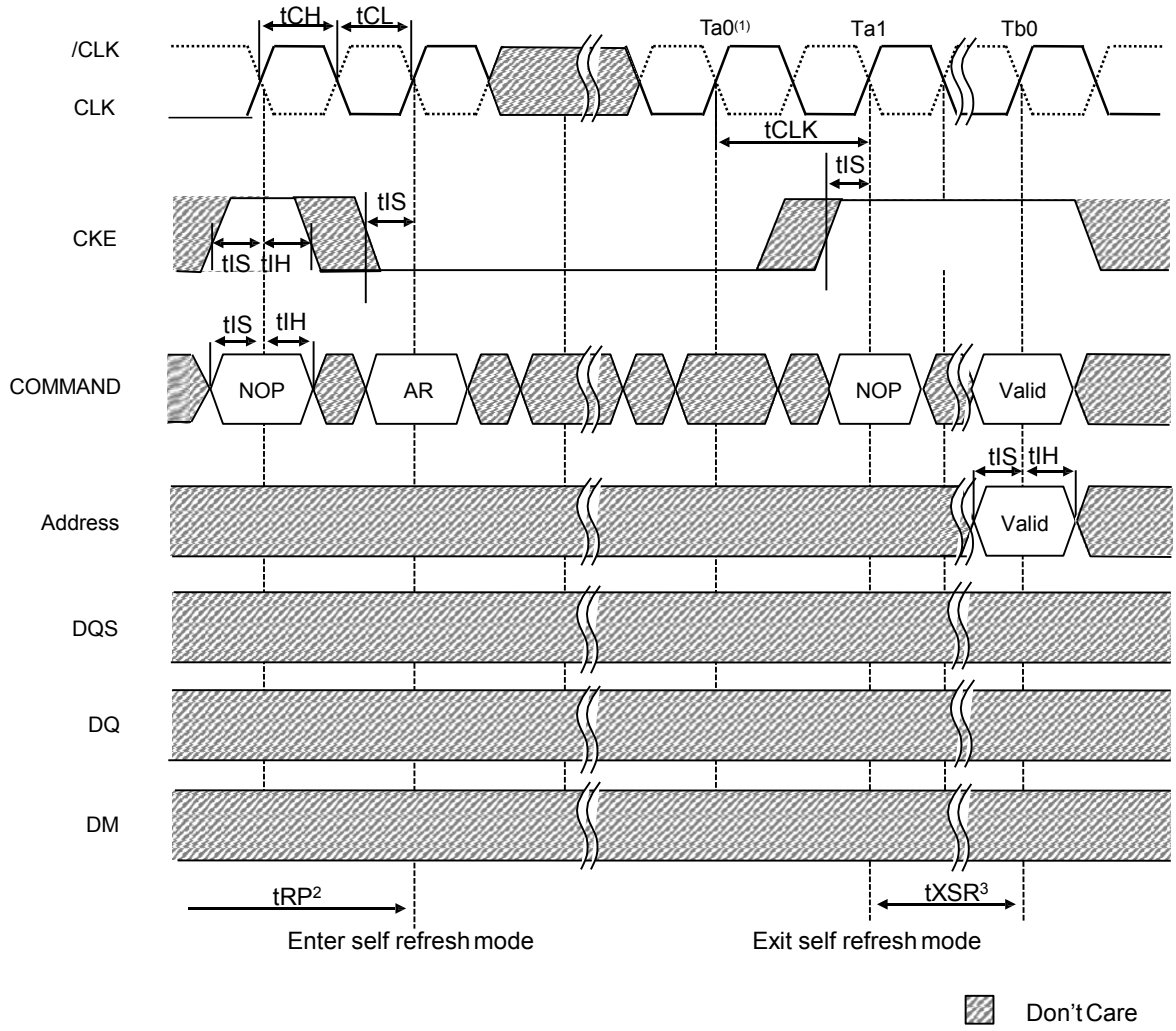
Figure 31: Auto Refresh Mode



Notes :

1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row address, BA = Bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after tRFC time, CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

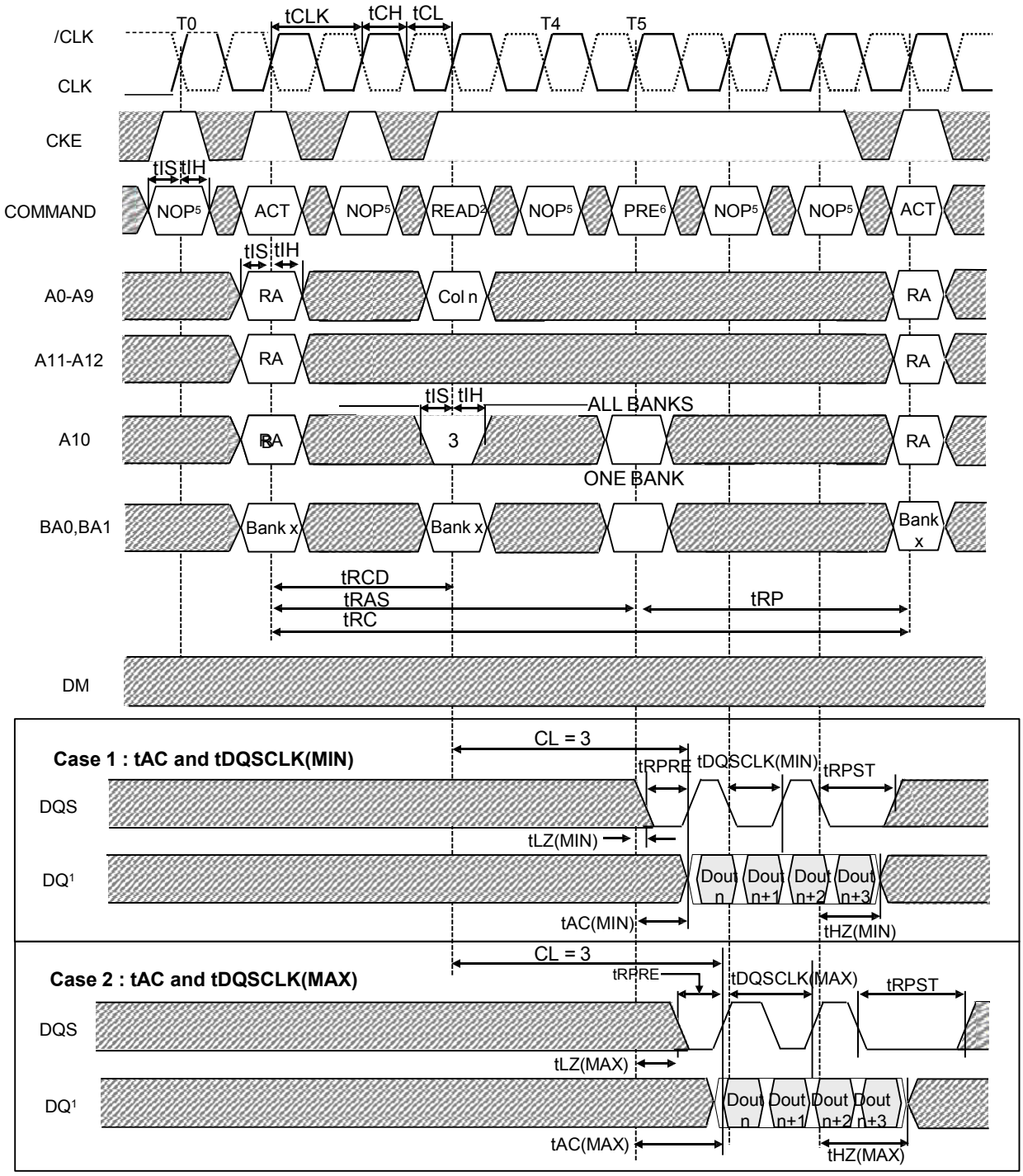
Figure 32: Self Refresh Mode



Notes :

1. Clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT are required for tXSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.

Figure 33: Bank Read – Without Auto Precharge

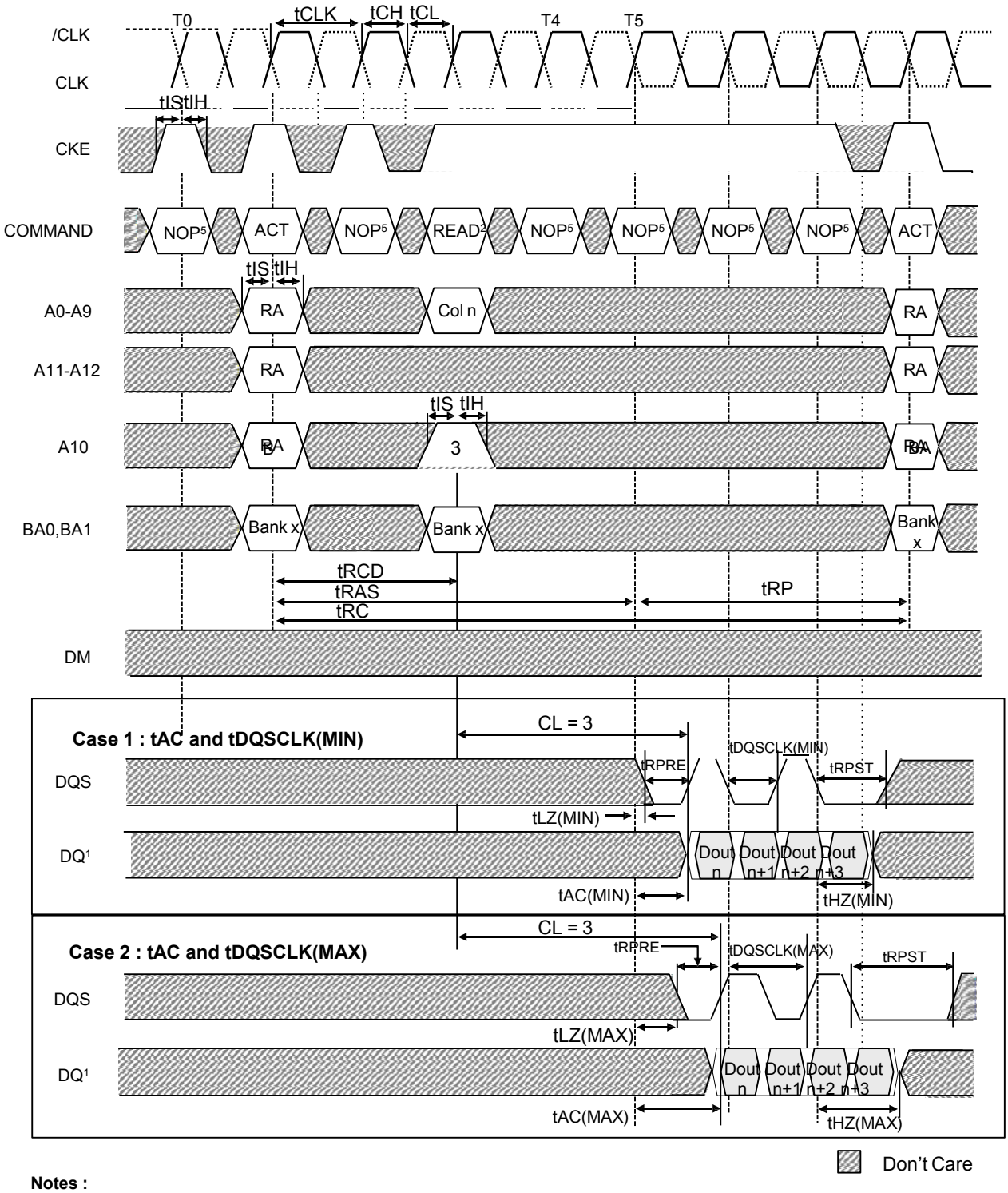


Notes :

1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The PRECHARGE command can only be applied at T5 if tRAS minimum is met.

Don't Care

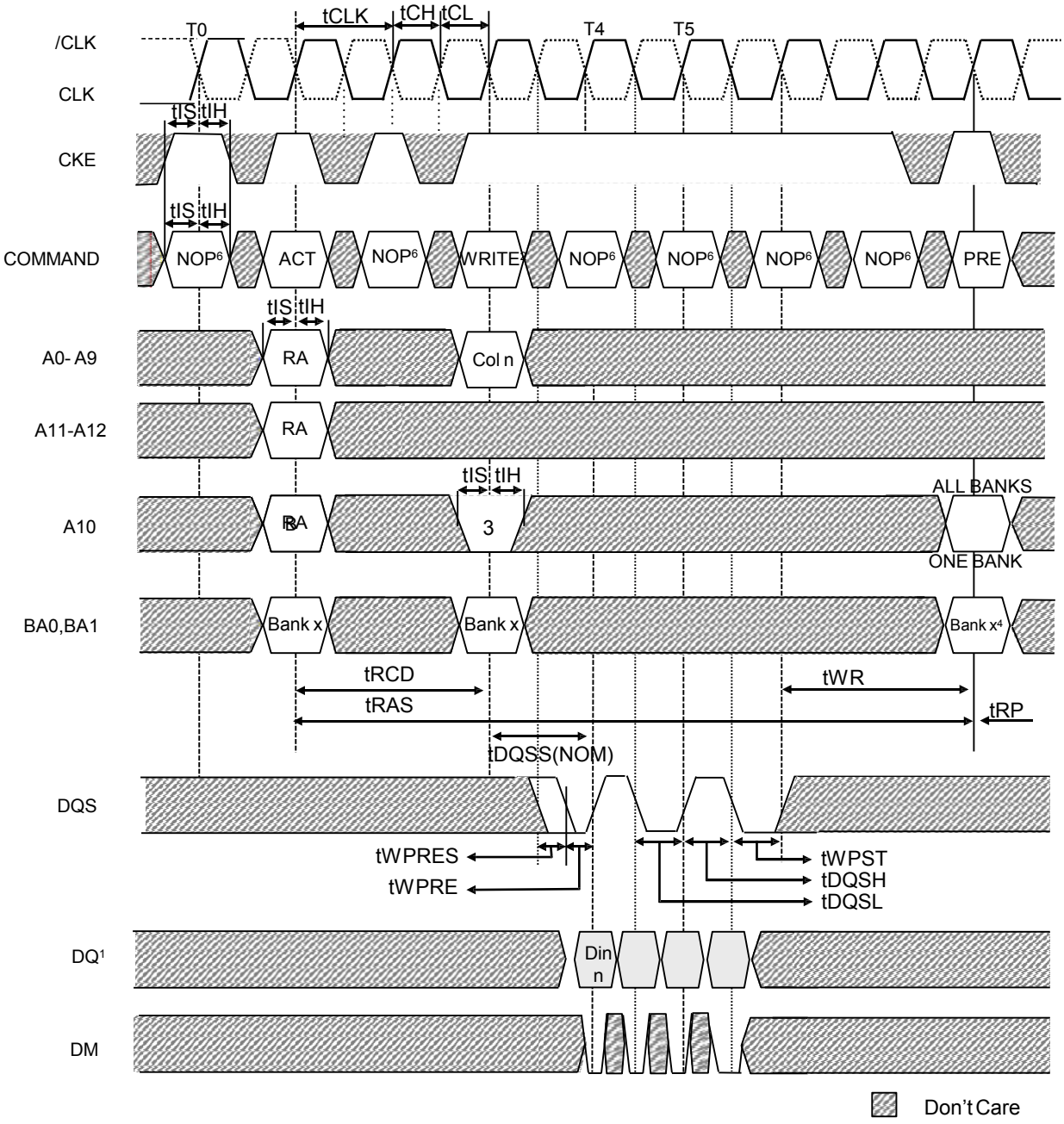
Figure 34: Bank Read – With Auto Precharge



Notes :

1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.

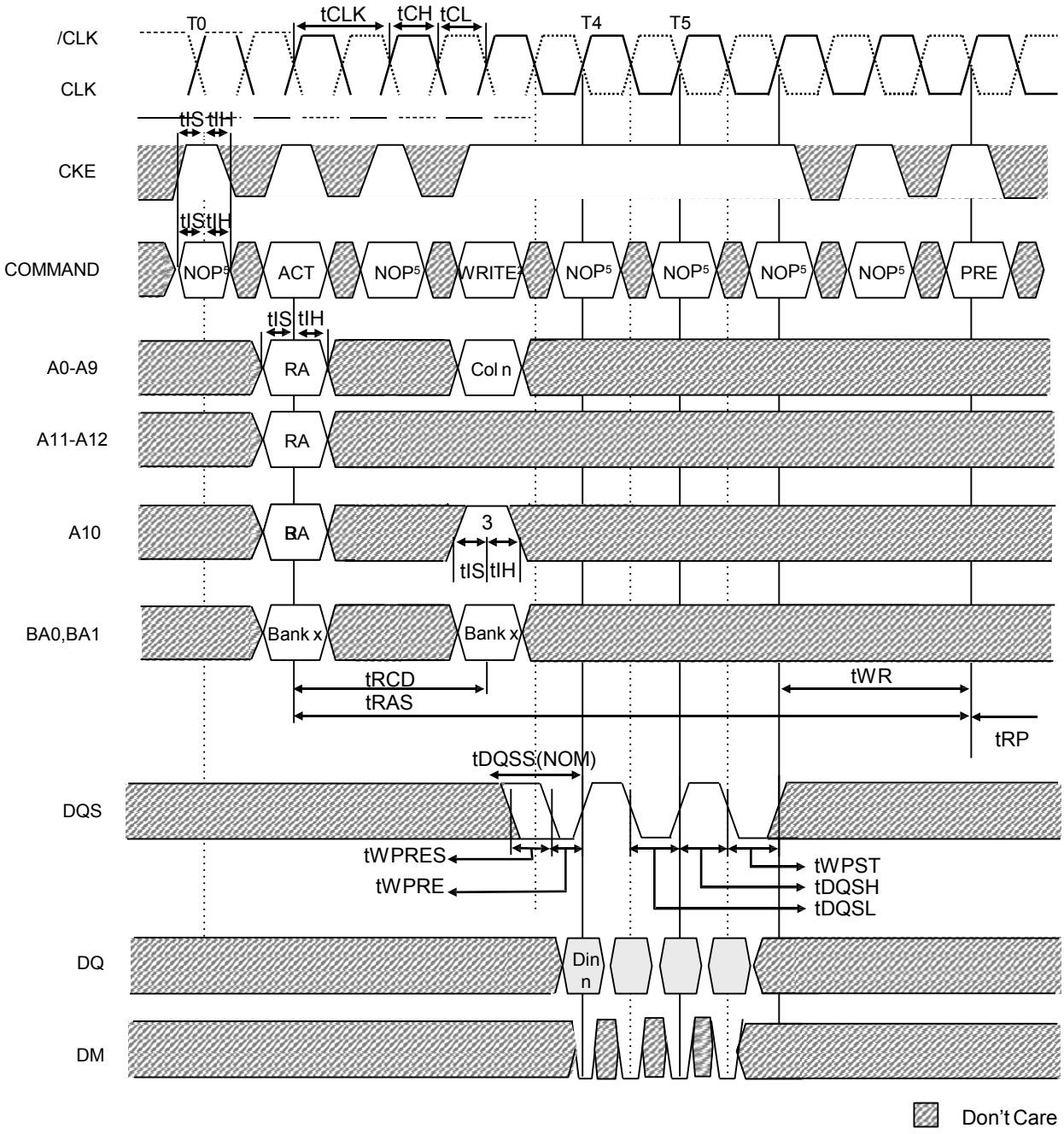
Figure 35: Bank Write – Without Auto Precharge



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

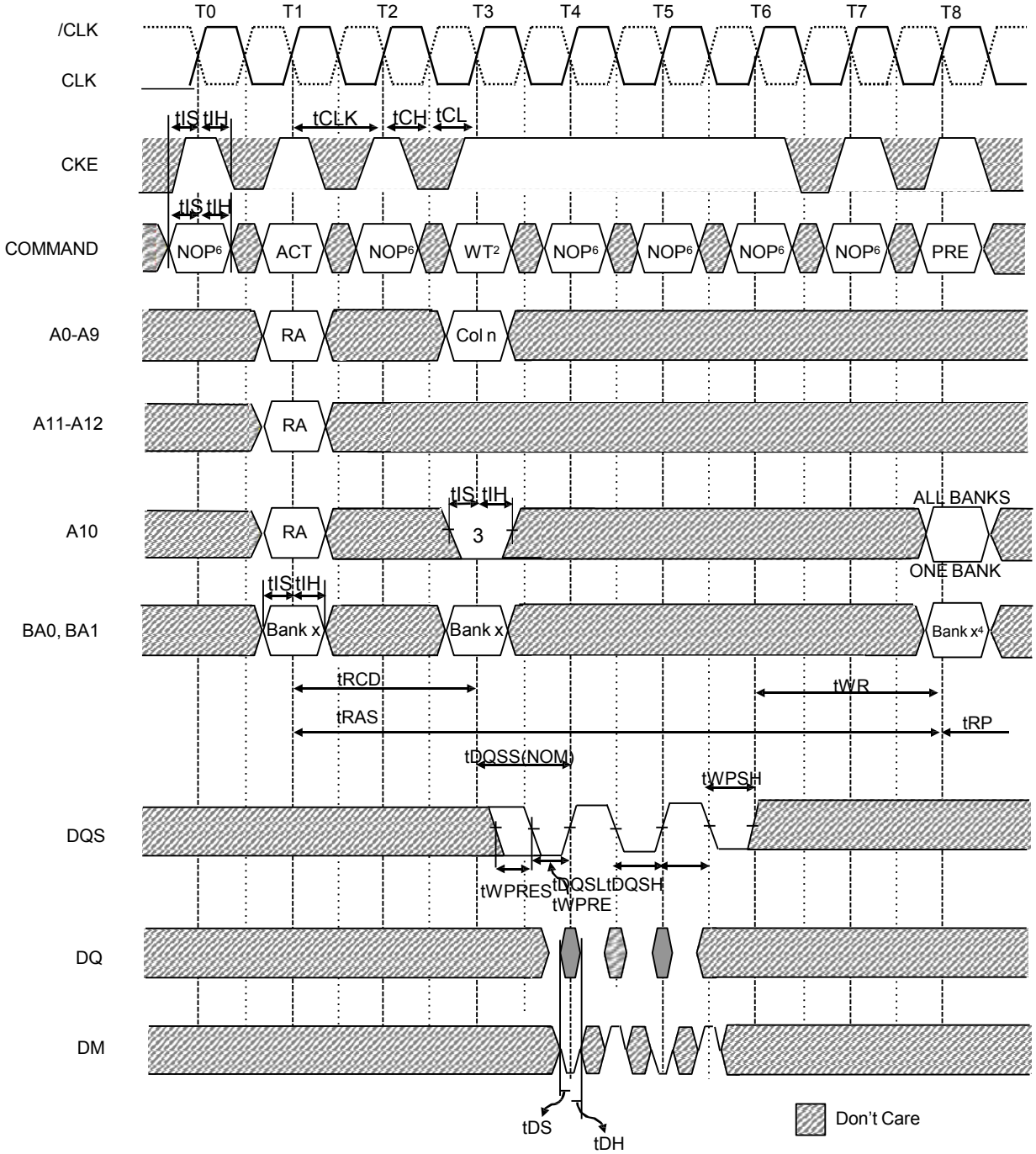
Figure 36: Bank Write – With Auto Precharge



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
7. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

Figure 37: Write – DM Operation



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

DEEP POWER DOWN MODE ENTRY

The Deep Power Down Mode is entered by having burst termination command, while CKE is low. The Deep Power Down Mode has to be maintained for a minimum of 100us. The following diagram illustrates Deep Power Down mode entry.

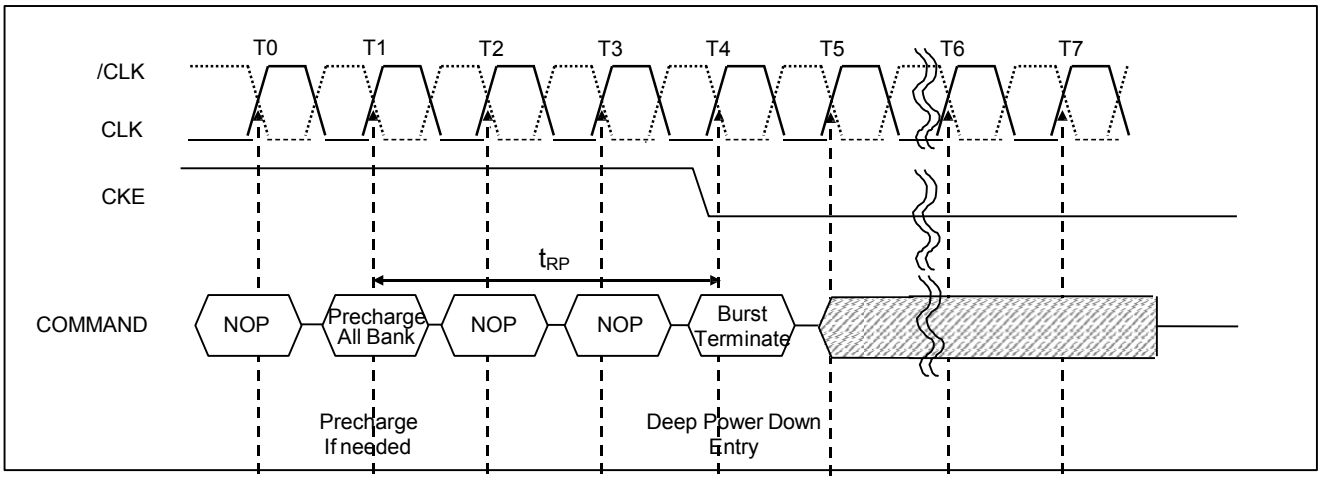


Figure 38. Deep Power Down Mode Entry

DEEP POWER DOWN MODE EXIT SEQUENCE

The Deep Power Down Mode is exited by asserting CKE high.
After the exit, the following sequence is needed to enter a new command

1. Maintain NOP input conditions for a minimum of 200us
2. Issue precharge commands for all banks of the device
3. Issue 2 or more auto refresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue a extended mode register set command to initialize the extended mode register

The following timing diagram illustrates deep power down exit sequence

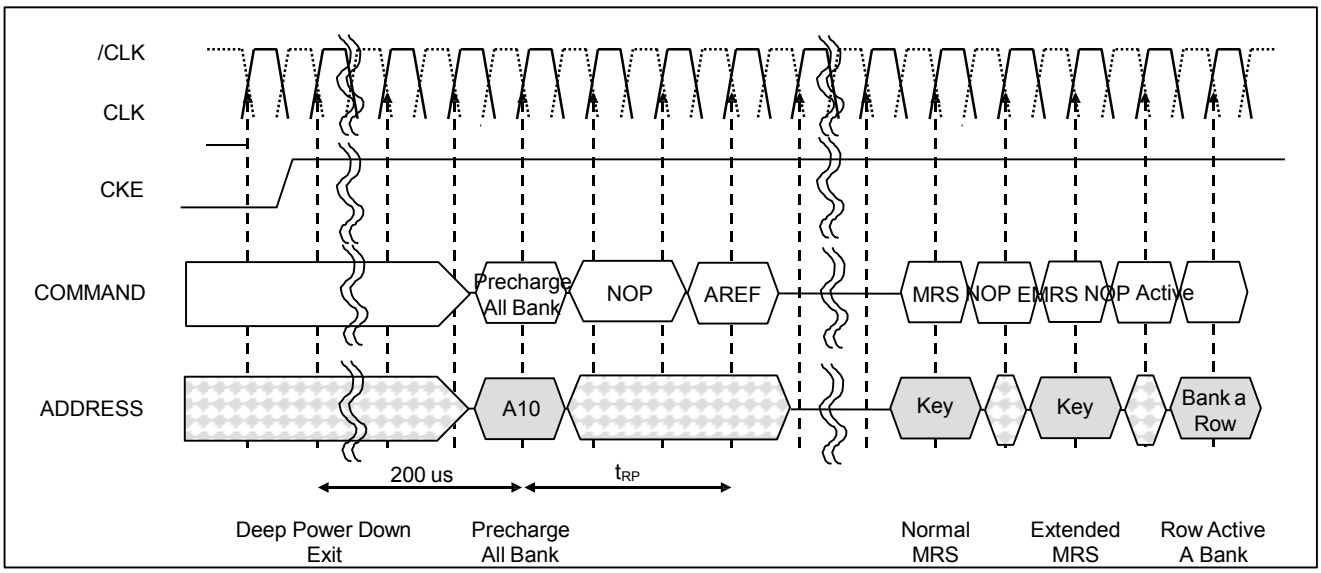
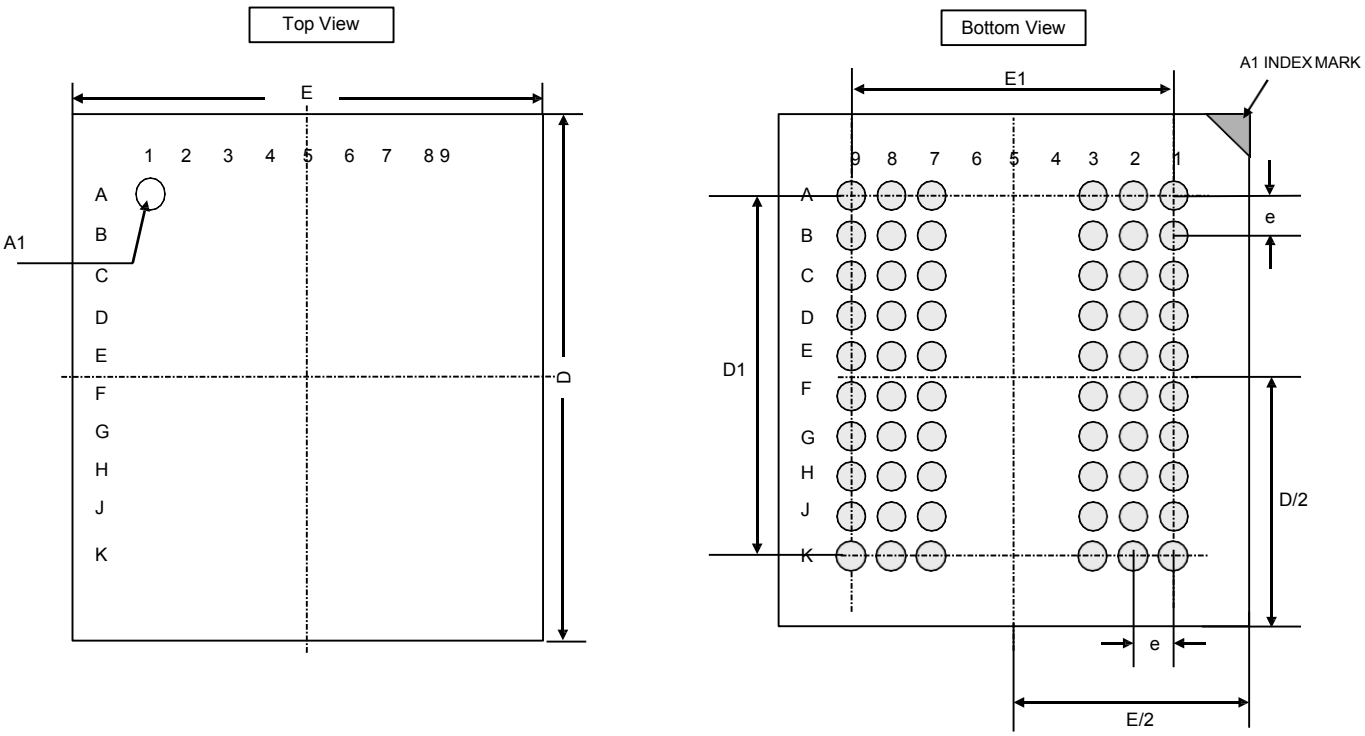
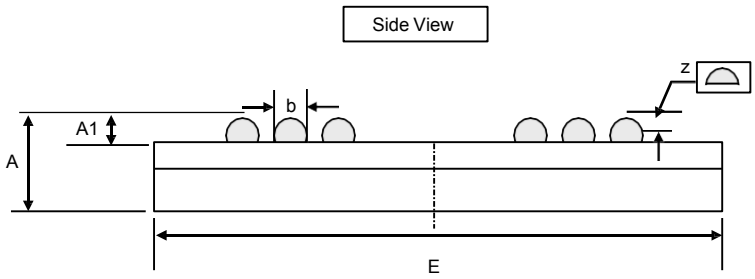


Figure 39. Deep Power Down Mode Exit

Unit : millimeters

60 BALL FBGA





Unit : mm

-	Min	Typ	Max
A	-	-	1.00
A1	0.275	0.30	0.325
E	-	8.00	-
E1	-	6.40	-
D	-	9.00	-
D1	-	7.20	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10