DESCRIPTION

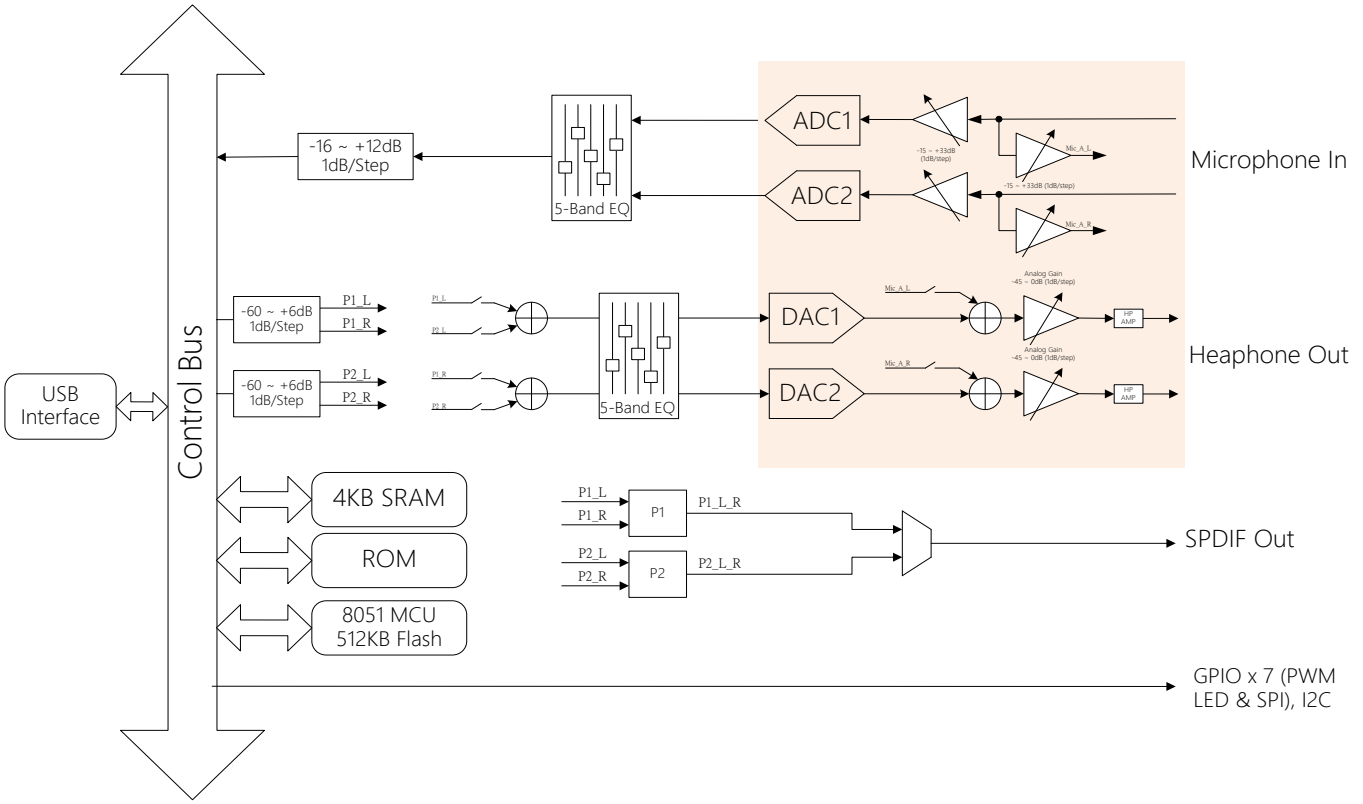
The CM6646 is a USB 2.0 high-speed audio codec with 2-channel DAC and 2-channel ADC for Headphone, Microphone and Headset applications. It supports USB Audio Class 2.0 and high-definition audio formats(Up to 192KHz/32bits). The CM6646 provides standard S/PDIF output digital audio interface. Moreover, the CM6646 supports I2C, SPI and GPIOs to communicate with external device. It also supports 5 bands EQ for both playback and recording interface.

The CM6646 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates 6 PWM LED drivers for status indication.

FEATURES

- USB specification 2.0 full-speed/high speed compliant
- USB audio class 2.0 compliant
- USB human interface device (HID) class 1.1 compliant
- Support USB suspend/resume/reset functions
- Support control, interrupt and isochronous data transfers
- Integrate 2-channel DAC and 2-channel ADC
- True Cap-less/zero-ground headphone driver with patent applied anti-pop technology
- Embedded oscillator for Crystal-less design
- Embedded 7-bits SAR ADC supports Combo jack and Google button detection
- S/PDIF output up to 192K/24bits
- 1 I2C master, 1 I2C slave, 1 SPI master and 7 GPIOs
- Integrate 6 PWM LED drivers
- Support 5 bands playback and recording EQ
- Support 2 output end-points audio stream mixing

BLOCK DIAGRAM



Release notes

Revision	Date	Description
0.95	2021/03/11	- Preliminary release
0.96	2021/09/06	- Modify pin description - Add more feature descriptions - Add more codec descritpions - Modify codec performance
0.97	2021/09/11	- Add more descriptions
1.00	2021/09/30	- Formal release
1.10	2022/02/14	- Modify Block Diagram - Modify 7.5 PSRR - Modify Microphone Bias Open Circuit Voltage
1.20	2022/08/23	- Modify Package Dimensions
		-

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1 Description and Overview

The CM6646 is a USB 2.0 high-speed audio codec with 2-channel DAC and 2-channel ADC for Headphone, Microphone and Headset applications. It supports USB Audio Class 2.0 and high-definition audio formats(Up to 192KHz/32bits). The CM6646 provides standard S/PDIF output digital audio interface. Moreover, the CM6646 supports I2C, SPI and GPIOs to communicate with external device. It also supports 5 bands EQ for both playback and recording interface.

The CM6646 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates 6 PWM LED drivers for status indication.

2 Ordering Information

Product	Package Marking	Package Type	Transport Media
CM6646	CM6646	QFN-48(5x5mm)	Tray

3 Features

3.1 USB Compliance

- USB 2.0 full-speed/high speed compliant
- USB audio class 2.0 compliant
- USB human interface device (HID) class 1.1 compliant
- Support USB suspend/resume/reset functions
- Support control, interrupt and isochronous data transfers

3.2 Integrated 8051 Micro Processor

- Embedded 8051 micro-processor handles the USB transfers(control, isochronous and interrupt)
- Communicate with external peripheral devices(I2C, SPI, GPIO, etc.)
- The MCU speed is programmable from 3.072 to 65.536 MHz
- HID interrupts can be implemented via firmware codes
- Provide maximum HW configuration flexibility with a firmware code upgrade
- VID/PID/product string and others can be customized via firmware code programming

3.3 Control Interface

- 1 Master I2C control interface to communicate with external devices or EEPROM, the master I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 Slave I2C control interface for external MCU communication, the slave I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 SPI master(share with GPIO), supports speed up to 24.576 Mb/s (Depends on MCU speed)
- 7 GPIOs(programmable multi functions I/O)
- 6 PWM LED drivers output share with GPIO

3.4 Audio Engine and Codec

- Playback Stream:
  - Stereo DAC:
    - Sample Rates: 44.1K/48K/88.2K/96K/ 176.4K/ 192K Hz
    - Bit Depth: 16/24/32 bit
    - Analog Gain Range: -45 ~ 0dB, 1dB/step
    - Digital Gain Range: -60 ~ +6dB, 1dB/step
    - True Cap-less/zero-ground headphone driver with patent applied anti-pop technology
  - S/PDIF Transmitter:
    - Sample Rates: 44.1K/48K/88.2K/96K/ 176.4K/ 192K Hz
    - Bit Depth: 16/24 bits
  - 5-band Digital Parametric Equalizer
- Recording Stream:
  - Stereo ADC
    - Sample Rates: 44.1K/48K/88.2K/96K/ 176.4K/ 192K Hz
    - Bit Depth: 16/24/32 bit
    - Microphone gain range: -15~ +33dB, 1dB/step
    - Digital Gain Range: -16 ~ +12dB, 1dB/step
  - 5-band Digital Parametric Equalizer

- A-A Mixer (Sidetone):
  - Analog input to analog output mixer path with independent volume control: -15 ~ +33dB, 1dB/step

3.5 General

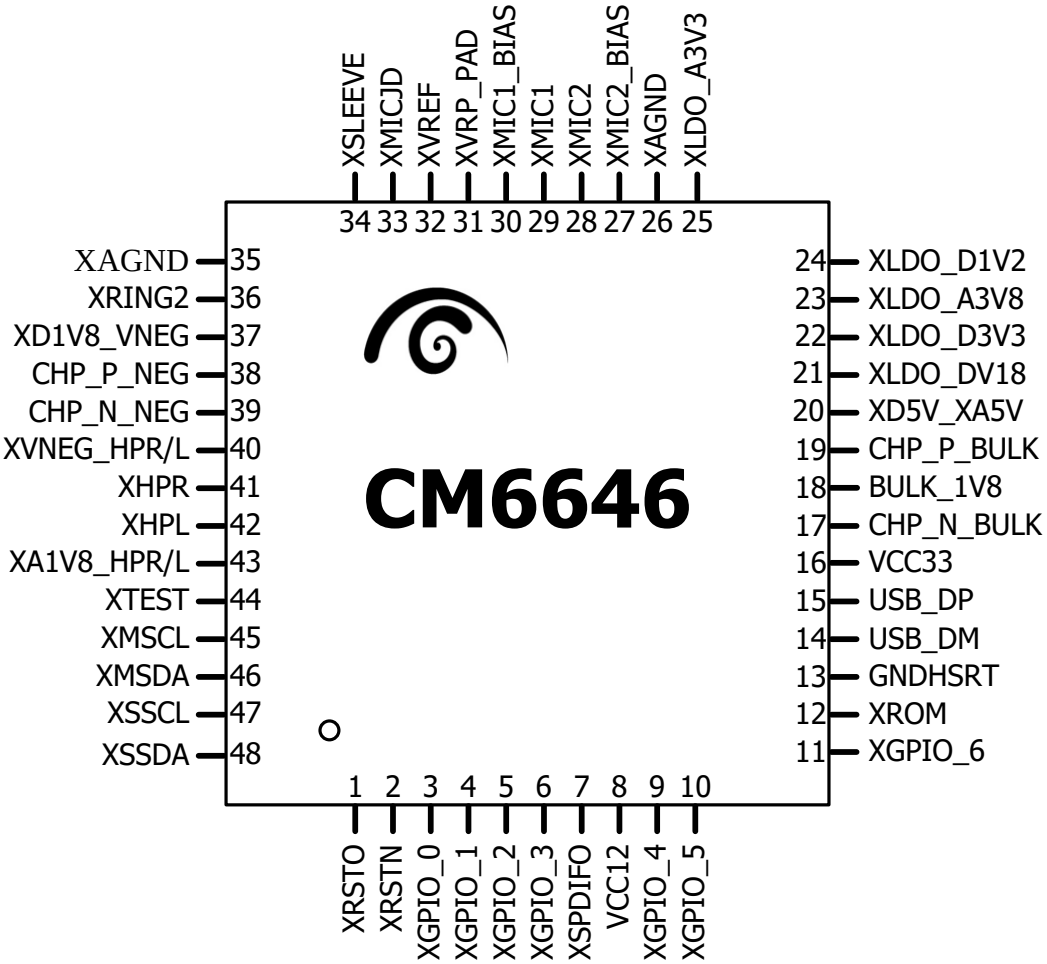
- Embedded USB 2.0 transceiver and power-on reset circuit
- Bus-power and self-power options
- Embedded oscillator for Crystal-less design
- True Cap-less/zero-ground headphone driver with patent applied anti-pop technology
- Single 5V power supply with embedded 5V to 3.3V regulator
- 3.3V digital I/O pads with 5V tolerance
- Compliant with USB IF certification requirements
- QFN-48 package (5 x 5 mm)

4 Applications

- USB Microphone with Headphone Monitor
- PC Gaming Headset with 2-Output End Point mixing function
- USB Audio Dongle

5 Pin Assignment

5.1 Pin-out Diagram



5.2 I/O Type Description

I/O Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DIL	Digital Input with internal pull-down 50K
DIH	Digital Input with internal pull-up 50K
DO	Digital Output
DIOL	Digital Input/Output with internal pull-down 50K
DIOH	Digital Input/Output with internal pull-up 50K
IOU	USB related IO
PWRO	Power output pin
PWRI	Power input pin
GND	Ground related pin

5.3 Pin Description

Pin #	Symbol	I/O	Description
USB 2.0 BUS Interface			
15	USB_DP	IOU	USB 2.0 data positive
14	USB_DM	IOU	USB 2.0 data negative
Power/Ground			
13	GNDHSRT	GND	Digital ground
20	XD5V_XA5V	PWRI	Digital/Analog supply power (4.3V~5V) ; Connect to capacitor filter
26	XAGND	GND	Analog ground
35	XAGND	GND	Analog ground
18	BULK_1V8	PWRO	DC to DC 1.8V output, 40mA driving current ; Connect to capacitor filter
37	XD1V8_VNEG	PWRI	DC to DC 1.8V input Input power of negative charge pump ; Connect to capacitor filter
43	XA1V8_HPR/L	PWRI	Analog 1.8V input Positive Power of headphone driver R/L CH ; Connect to capacitor filter
40	XVNEG_HPR/L	PWRO	DC to DC -1.8V output, 10mA driving current ; Connect to capacitor filter
23	XLDO_A3V8	PWRO	LDO 3.8V output, 20mA driving current ; Connect to capacitor filter
25	XLDO_A3V3	PWRO	LDO 3.3V output, 20mA driving current ; Connect to capacitor filter
22	XLDO_D3V3	PWRO	LDO 3.3V output, 30mA driving current ; Connect to capacitor filter
21	XLDO_D1V8	PWRO	LDO 1.8V output, 20mA driving current ; Connect to capacitor filter
24	XLDO_D1V2	PWRO	LDO 1.2V output, 10mA driving current ; Connect to capacitor filter
16	VCC33	PWRI	VCC 3.3V input Digital supply voltage 3.3V for digital I/O
8	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
Analog			

32	XVREF	AO	Voltage reference for common mode voltage (~1.5V)
31	XVRP_PAD	AO	Voltage reference for DAC (~3.1V)
30	XMIC1_BIAS	AO	Microphone 1 bias volage output (~3.1V)
29	XMIC1	AI	Microphone 1 input
27	XMIC2_BIAS	AO	Microphone 2 bias volage output (~3.1V)
28	XMIC2	AI	Microphone 2 input
33	XMICJD	AO	Combo jack detect and auto switch, detect combo jack type and switch to XRING2 or XSLEEVE
34	XSLEEVE	AI	Combo jack connectoe: Sleeve
36	XRING2	AI	Combo jack connector: Ring2
19	CHP_P_BULK	AO	Charge pump positive output of DC to DC
17	CHP_N_BULK	AO	Charge pump negative output of DC to DC
38	CHP_P_NEG	AO	Charge pump positive output of high negative DC to DC
39	CHP_N_NEG	AO	Charge pump negative output of high negative DC to DC
42	XHPL	AO	Headphone driver output L CH
41	XHPR	AO	Headphone driver output R CH
S/PDIF I/O			
7	XSPDIFO	DO	S/PDIF transmitter
GPIO			
3	XGPIO_0	DIOL	1). General purpose input/output 0 (default input) 2). LED module 1 output 3). R8051 SPI master clock output, Internal pull low, 4mA driving current
4	XGPIO_1	DIOL	1). General purpose input/output 1 (default input) 2). LED module 2 output 3). R8051 SPI master data output, Internal pull low, 4mA driving current
5	XGPIO_2	DIOL	1). General purpose input/output 2 (default input) 2). LED module 3 output 3). R8051 SPI master data input, Internal pull low, 4mA driving current
6	XGPIO_3	DIOL	1). General purpose input/output 3 (default input) 2). LED module 4 output 3). R8051 SPI master chip enable 0 output, Internal pull low, 4mA driving current
9	XGPIO_4	DIOL	1). General purpose input/output 4 (default input) 2). LED module 5 output 3). I2C slave interrupt output to external MCU Internal pull low, 4mA driving current

10	XGPIO_5	DIOL	1). General purpose input/output 5 (default input) 2). LED module 6 output 3). I2C slave data ready indication output Internal pull low, 4mA driving current
11	XGPIO_6	DIOL	General purpose input/output 6 (default input) Internal pull low, 4mA driving current
I2C Master Serial Bus			
45	XMSCL	DIOH	1). I2C master serial clock 2). R8051 I2C serial clock
46	XMSDA	DIOH	1). I2C master serial data 2). R8051 I2C serial data
I2C Slave Serial Bus			
47	XSSCL	DIOH	1). I2C slave serial clock 2). R8051 I2C serial clock (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
48	XSSDA	DIOH	1). I2C slave serial data 2). R8051 I2C serial data (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
Miscellaneous			
1	XRSTO	DIOL	External codec reset output (default tri-state)
44	XTEST	DIL	Test mode input (Connect to Ground)
2	XRSTN	DIH	Reset input, active low
12	XROM	DIL	Reserve for restore to ROM mode

6 Function Description

6.1 USB Topology

The CM6646 USB Topology is programmable by changing firmware. If the internal firmware is empty, the CM6646 will report a WinUSB device to the system. It is used to load the firmware.

6.2 USB Endpoint

All USB devices must support a control pipe at endpoint number zero (default control pipe). The endpoint table of CM6646 is listed as follows.

EndpointNumber	Direction	Type	Description
0	IN	Control	
	OUT		
1	IN	Isochronous	Audio, Recording
3	IN	Feedback	Audio, Playback
	OUT	Isochronous	
4	IN/OUT	Interrupt A	
C	IN	Feedback	Audio, playback
	OUT	Isochronous	
E	IN	Isochronous	Audio, Recording
F	IN/OUT	Interrupt B	

6.3 S/PDIF Interface

SPDIF is an audio transmission format in digital domain. The data stream format is illustrated in Fig. 6.3.1. The maximum unit of the S/PDIF stream is a block. A block is composed of 192 frames, and each frame is composed of two subframes. One frame contains one audio sample, so the frame rate is equal to the sampling rate. The left channel audio data is carried by bit slot 4-27 (or time slot 4-27) of subframe A, and right channel is carried by bit slot 4-27 of subframe B. The Sync slot takes preamble signal which is used to label the beginning of a subframe. There are three types for preamble signal, the first is B type, used only in the first subframe of a block; the W type, used in all subframe B; the M format, used in all subframe A, besides the first subframe of a block. The block format is shown in Fig. 7.3.1. The logical level at the start of a bit is always inverted to the level at the end of the previous bit. The level at the end of a bit is equal (a 0 transmitted) or inverted (a 1 transmitted) to the start of that bit.

The S/PDIF data signal is coded by the “biphase-mark-code,” which is a kind of phase modulation. It is illustrated in Fig. 6.3.2. The base clock of a S/PDIF signal is twice the bit rate, and the frequency of the base clock is only determined by the sampling rate. The period of the base clock is called the Unit interval (UI). For example, for a 48KHz 2-channel S/PDIF signal, the frame rate is also 48KHz, so a frame period is 20.833us, and a subframe period is 10.416us. A subframe contains 32-bit slot, so a bit slot period is 325.52ns. As we said above, the base clock is twice the bit rate. Therefore, the period of the base clock is 162.76ns. In other words, the frequency of base clock is 6.144 MHz. Bi-phase coding can prevent PCM data from DC isolated and insensitive to level polarity. A maximum up to 24 data bits can be transmitted by the S/PDIF signal, and the sequence is from LSB to MSB.

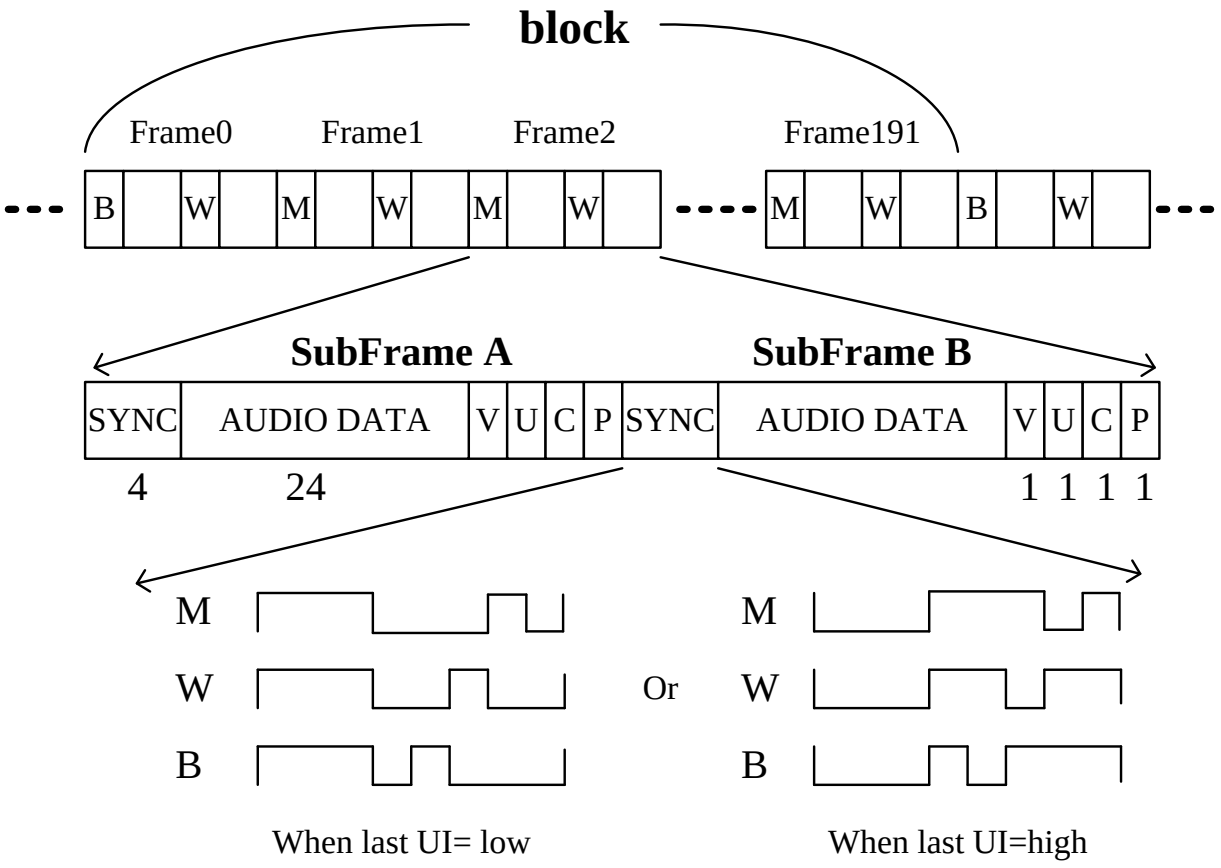


Fig. 6.3.1 S/PDIF Frame format.

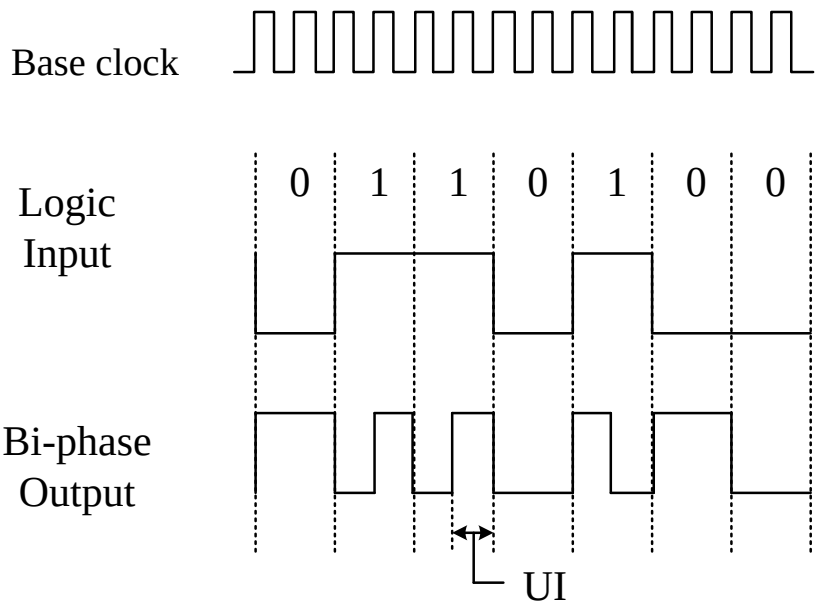


Fig. 6.3.2 S/PDIF biphase-mark-code (BMC).

6.4 Two-Wire Master and Slave Serial Buses (I2C)

The 2-wire master and slave serial buses are designed separately in the CM6646.

6.4.1 The Concept of Two-Wire Bus

The 2-wire bus, as its name reveals, has 2 lines. One is the serial clock line (*SCL*), and the other is the serial data line (*SDA*). Both of them are operated under open drain. That means if the 2 lines are not driven by a master or a slave, they are pulled high by the external pull-up resistors as indicated by Fig. 6.4.1.1. A device connected on the bus can be recognized as a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. Another concept that we should know is the transmitter-receiver relation. *The transmitter is the device which sends data to the bus, and receiver is the device which receives data from the bus.* Note that the definition of transmitter-receiver is different from that of master-slave. We will use these terms to explain 2-wire read/write transactions later. The CM6646 use 7 bits to address the slave devices such as codecs, so theoretically, the 2-wire bus is able to connect 128 slave devices. However, in the audio system application, the limitation is on the codecs, not on the CM6646. Usually, the codecs which support 2-wire bus only have one or two pins to select their address. Therefore, two or four codecs is allowed in the system indicated by Fig. 6.4.1.1, unless the codecs are from different manufactures. In the MCU application, the CM6646 is a slave device, and it can be addressed by the MCU via four different addresses, 0001000b, 0001001b, 0001010b, 0001011b.

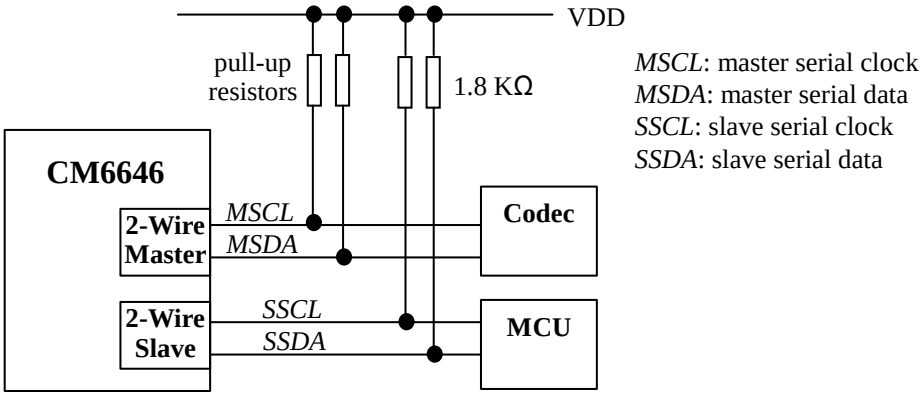


Fig. 6.4.1.1 The connection of 2-wire master and slave buses.

6.4.2 Start and Stop Condition

For a 2-wire bus transaction, the start and stop condition is defined as follows and shown in Fig.6.4.2.1.

- Start: a high to low transition on the *SDA* line while *SCL* is high.
- Stop: a low to high transition on the *SDA* line while *SCL* is high.

Start and stop conditions always generated by the master device. The bus is considered to be busy after the start condition. The bus is considered to be free again after the stop condition.

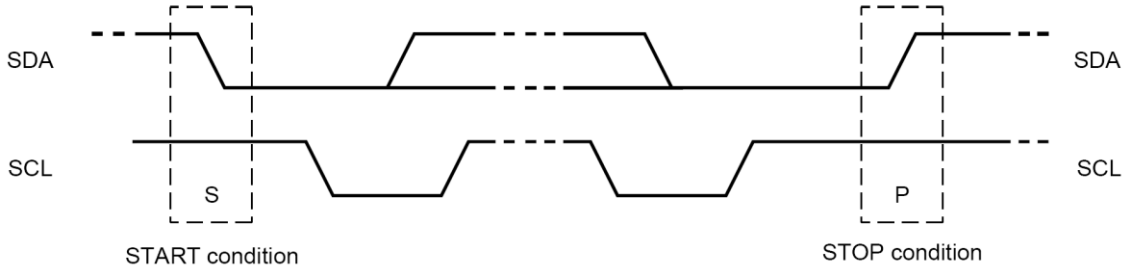


Fig. 6.4.2.1 Start and stop conditions of 2-wire bus.

6.4.3 Bit Transfer

The data on the *SDA* line must be stable during the high period of the clock. The state of the data line can only transit when the clock signal on *SCL* line is low. The bit transfer is indicated in Fig. 6.4.3.1.

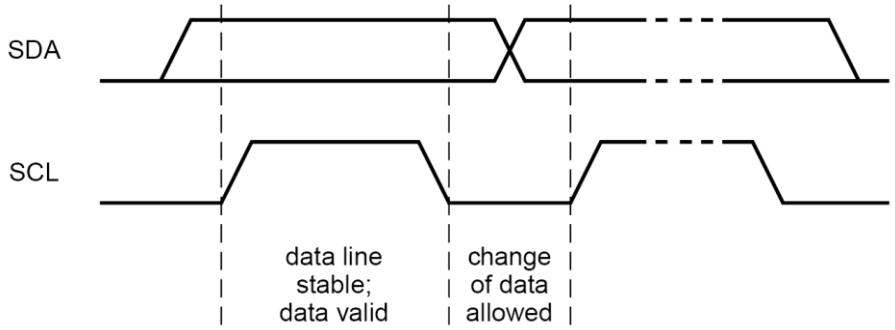


Fig. 6.4.3.1 Bit transfer of 2-wire bus.

6.4.4 Transferring Data with Read/Write Transactions and Acknowledge

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is 3 or 4 bytes in the CM6646. The first byte is always the address byte which is composed of the 7-bit address and 1 read/write bit, listed in Fig. 6.4.4.1 For a write transaction, the second byte is called *Memory Address Pointer* (MAP), which is usually used to indicate the target register in the slave device that the followed third and fourth bytes will be applied on. For a read transaction (only 3 bytes), the second and third bytes is the data returned by the slave device. Each byte has to be ended by an acknowledge bit. Data is transferred with the most significant bit first.

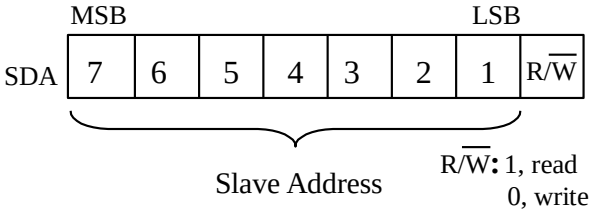


Fig. 6.4.4.1 The first byte after start condition.

The 2-wire master bus of the CM6646 supports read/write transactions. All these transactions are depicted in Fig.

6.4.4.2 to give a whole picture about what the CM6646 can do.

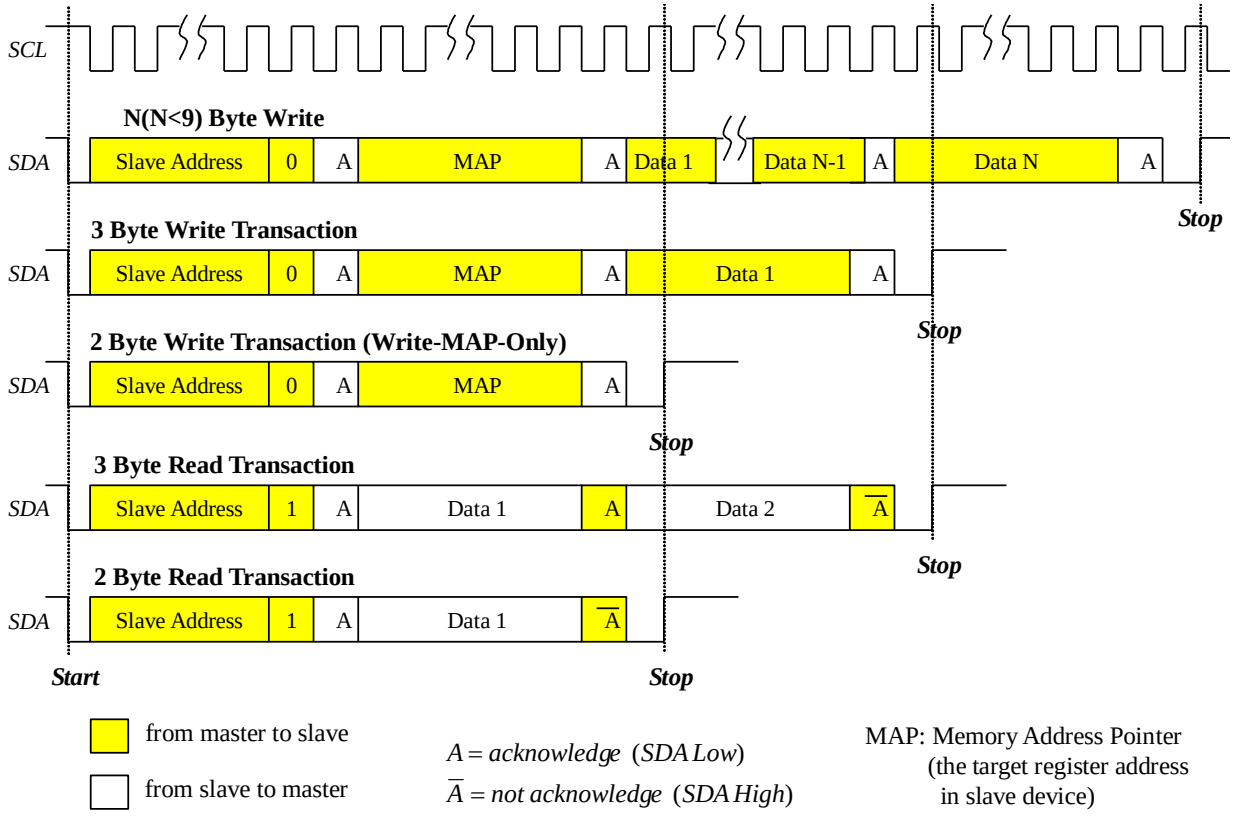


Fig. 6.4.4.2 The 5 basic transactions of the 2-wire master bus supported by the CM6646.

In a read transaction, usually the slave device returns the data of the register whose address is in the MAP. If the read transaction is a 3 byte read transaction, the second returned byte is the data in the (address+1) register. Therefore, the action of obtaining the data in slave device is composed of two transactions, namely a 2 byte write transaction (Write-MAP-Only) followed by a read transaction. For the convenience of users, we have designed an auto read transaction, shown in Fig. 6.4.4.3, which is actually the combination of a write and a read transactions.

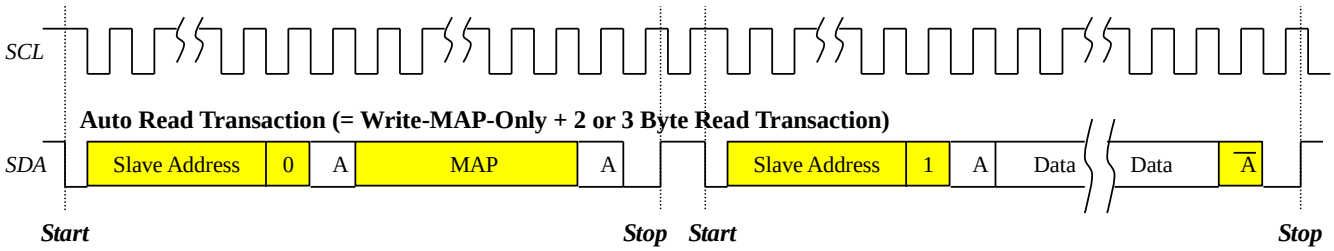


Fig. 6.4.4.3 Auto read transaction in the CM6646.

Data transfer with acknowledge is obligatory. The transmitter release SDA line during the acknowledge clock pulse. Then, the receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low for the entire acknowledge clock high period. This is shown in Fig. 6.4.4.4. When a salve does not acknowledge the slave address byte. For example, it is unable to receive or transmit because it is performing some real-time function. The data line should be left high by the slave. The master can then generate either a stop condition to abort the transfer, or a repeated start condition to start a new transfer.

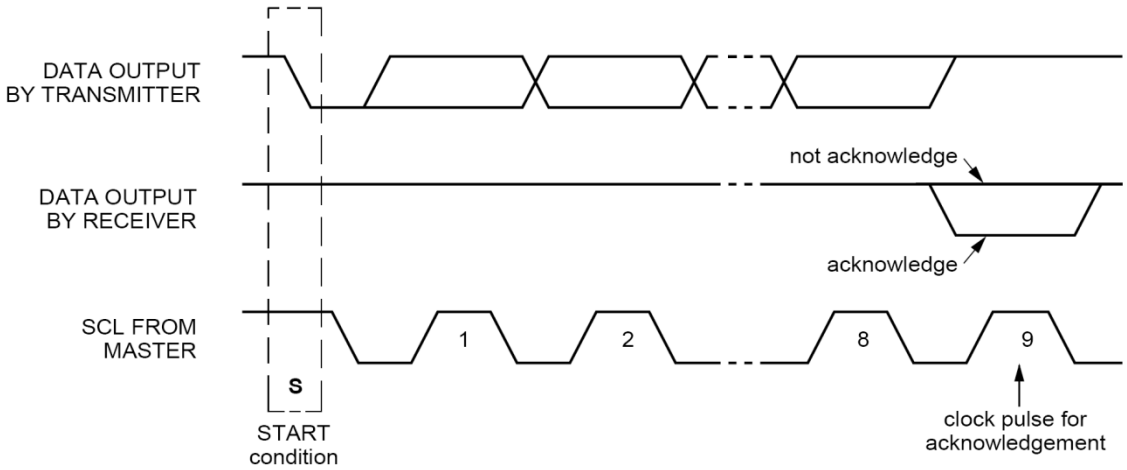


Fig. 6.4.4.4 Acknowledge of the 2-wire bus.

For a read transaction, after the slave address byte is transmitted and acknowledged by slave device, the role of master-transmitter is altered to become master-receiver, and the original slave-receiver is altered to become slave-transmitter. This conception can be easily observed in Fig. 6.4.4.3 and 6.4.4.4, where we use yellow and white blocks to denote the data bit transfer direction. Yellow means the data direction is from the master to the slave. White means the data direction is from the slave to the master. Meanwhile, in a read transaction, the master-receiver must signal the end of the data to the slave transmitter by generating a not-acknowledge ($\overline{A}$) on the last byte that was clocked out of the slave-transmitter. The slave-transmitter should release the *SDA* line to allow the

master to generate a stop or repeated start condition.

6.4.5 Synchronization

The synchronization of the 2-wire bus in the CM6646 can be described in two aspects. The first aspect is the synchronization used in arbitration. Although we did not implement arbitration, we did implement clock synchronization. Clock synchronization is used when there are more than two masters connected on the bus. A high to low transition on the *SCL* line will cause the concerned masters start counting the clock low period. Before the clock high state is reached, the masters will hold the *SCL* line in low state. However, the low to high clock transition of one of the masters may not change the state of the *SCL* line if another master's clock is still in low period (because the *SCL* line of the devices are wire-AND connected by open-drain technique). Therefore, the *SCL* line will be held low by the device with the longest clock low period. The other devices with shorter low period, including the CM6646, enter a high wait state during this time. Figure 6.4.5.1 listed below is the timing of clock synchronization.

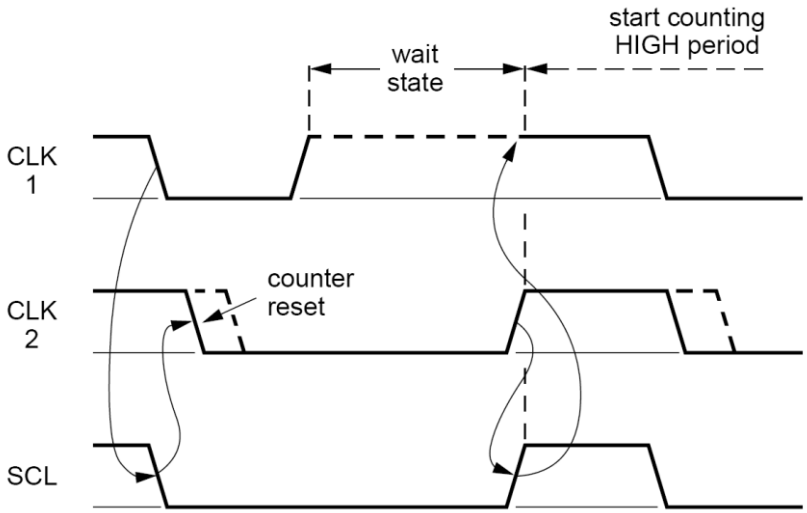


Fig. 6.4.5.1 Clock synchronization for more than two masters in the bus.

Another aspect of synchronization is the data synchronization between master and slave. If a slave cannot receive or transmit another complete byte of the data until it has performed some other function, for example servicing an internal interrupt or waiting for the driver to prepare the data needed, the salve can hold the clock line *SCL* low to force the master into a wait state. Data transfer then continues when the slave is ready and releases the clock line *SCL*. The data synchronization is shown in Fig. 6.4.5.2.

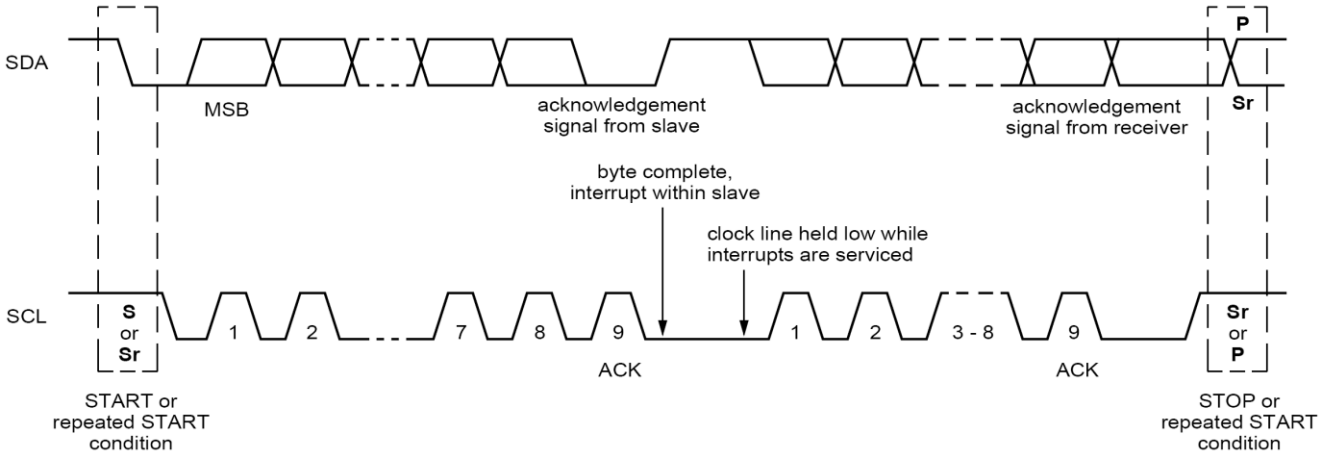


Fig. 6.4.5.2 The data synchronization of the 2-wire master and slave buses in the CM6646.

6.4.6 Standard Mode and Fast Mode

Both the 2-wire master and slave buses in the CM6646 can support standard mode transfer and fast mode transfer. The data transfer rate of the standard mode is up to 100 Kbits/sec, and the fast mode is up to 400 Kbits/sec. The clock timing of these modes are listed in Fig. 6.4.6.1 and Table 6.4.6.1

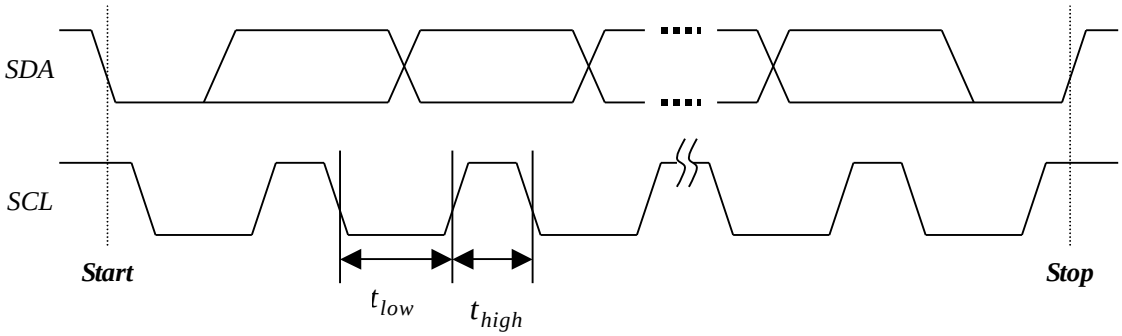


Fig. 6.4.6.1 Standard mode and fast mode timing.

Table 6.4.6.1 Standard mode and fast mode timing.

Parameter	Symbol	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Low period of *SCL* clock	t_{low}	4.8	—	1.3	—	μS
High period of *SCL* clock	t_{high}	4.8	—	0.6	—	μS

6.5 GPIO

All the GPIO pins can be configured as input or output by the GPIO direction control registers and also can be configure as remote wake up input pin. If they are assigned as outputs, then the contents in the GPIO data registers will be reflected to the corresponding GPIO pins. If they are assigned as inputs, they can be used for jack activity detection. If a speaker is plugged or unplugged, the state of the pin connected with that jack will be changed. As a result, an interrupt is issued to R8051, and an interrupt mask control bit is utilized to decide if the interrupt from that corresponding GPIO pin should be sent. After receiving the interrupt, R8051 must read the GPIO data register (address offset 0x0300h) to discover what pins have changed their states. Then, the R8051 will make some appropriate manipulation in response to the jack activity.

CM6646 supports two kinds of Remote-wakeup. One is hardware Remote-wakeup, and the other is software Remote-wakeup. When in Configuration, CM6646 has to report the host via the descriptor whether CM6646 supports the Remote-wakeup or not. If CM6646 reports it supports Remote-wakeup and the host also supports Remote-wakeup, the host will issue the request of Set-feature to enable the Remote-Wakeup feature. If the user selects hardware Remote-wakeup, the user has to select one of the GPIOs to configure as a remote wakeup pin. If there is a transition from 0 to 1 on this pin, that will cause a remote-wakeup to wake up the host from the suspend state. The transition can be from outer world or from the control of the R8051. If the transition is from the control of the R8051, this is called Software Remote-wakeup. Software Remote-wakeup is implemented by the register. If the user selects software Remote-wakeup, the 8051 has to write the register to cause the transition from 0 to 1 to wake up the host.

CM6646 has a de-bouncing circuit to filter the interrupt to R8051. There are two options to select which are 16ms and 8ms. The user can select one option to use according to their application.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Test conditions: XD5V_XA5V = 4.3V, AGND =0V, TA=+25 °C

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-25	-	150	°C
Operating ambient temperature	T_A	0	25	70	°C
Digital supply voltage(XD5V_XA5V)	PWR	4.3	5.0	5.5	V
ESD (Body mode)	-	-	±4000	-	V
ESD (Machine mode)	-	-	±200	-	V

7.2 Recommended Operation Conditions

Parameter	Symbol	Min.	Typ	Max.	Units
Supply voltage(XD5V_XA5V)	PWR	-	4.3	-	V
Digital Core(VCC12)	PWR	1.08	1.2	1.32	V
Input voltage range (V_{DD}=3.3V)	PWR	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage rage (V_{DD}=3.3V)	PWR	0	-	V_{DD}	V
Operating ambient temperature	-	-	25	-	°C

7.3 Power Consumption

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, TA=+25°C, MCU Clock = 6MHz.
Sample Rate=48kHz, 24Bits, Operation: Headphone output, Microphone input,
Volume setting = Gain 0dB

Parameter	Symbol	Min.	Typ	Max.	Units
Total power consumption (Playback + Record)	-	-	54	-	mA
Standby power consumption	-	-	51	-	mA
Suspend mode power consumption	-	-	1.1	-	mA

7.4 DC Characteristics

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
High-level input voltage	Vih	2.0	-	-	V
Low-level input voltage	Vil	-	-	0.8	V
High-level output voltage	Voh	2.4	-	-	V
Low-level output voltage	Vol	-	-	0.4	V

7.5 Analog I/O Characteristics

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Microphone Input Impedance	MII	MIC IN	-	20	-	kΩ	
Microphone A-A Input Impedance	MAII	MIC IN	-	20	-	kΩ	Mic Gain=0dB
Microphone Bias Open Circuit Voltage	VMICBIAS	MICBIAS	2.7	3	3.3	V	
Microphone Bias Output Current	IMICBIAS	MICBIAS	-	-	1.25	mA	RMIN=2.2kΩ
Microphone Bias Output Impedance	ROUTMICB	MICBIAS	600	650	700	Ω	
Power Supply Rejection Ratio (PSRR) for Microphone Bias	PSRRMICB	MICBIAS	-	100	-	dB	Internal regulators active, at maximum load current (0.5 mA), 1 kHz sine wave at 1 Vrms

8 Analog Performance

8.1 DAC audio quality

TA=25℃, XD5V_XA5V = 4.3V, AGND =0V, 997Hz Sine-wave, measure bandwidth is 20Hz to 20kHz, Equalizer disable, Master Volume= 0dB,

Test Platform:HP EliteBook 840r G4 8G RAM , Windows 10

Items	Test Conditions			Test Values			Unit
				Min.	Typ.(1KHZ)	Max.	
Full Scale Output Voltage	10KΩ loading			-	1085	-	mVrms
	32Ω loading			-	940	-	
	32Ω loading with 33 ohm cascade, Note 1			-	495	-	
THD+N With None Filter.	10KΩ Loading	0dBFS (Fig1)	44.1K/16bits	-	-84.0	-	dB
			48K/16bits	-	-80.1	-	
			88.2K/24bits	-	-80.8	-	
			96K/24bits	-	-81.1	-	
			176.4K/32bits	-	-83,9	-	
			192K/32bits	-	-83.1	-	
		-3dBFS (Fig2)	44.1K/16bits	-	-87.7	-	dB
			48K/16bits	-	-83.7	-	
			88.2K/24bits	-	-86.3	-	
			96K/24bits	-	-85.8	-	
			176.4K/32bits	-	-87.7	-	
			192K/32bits	-	-87.5	-	
	32Ω Loading	0dBFS (Fig3)	44.1K/16bits	-	-76.1	-	dB
			48K/16bits	-	-76.6	-	
			88.2K/24bits	-	-76.0	-	
			96K/24bits	-	-76.4	-	
			176.4K/32bits	-	-76.7	-	
			192K/32bits	-	-75.0	-	
		-3dBFS (Fig4)	44.1K/16bits	-	-81.0	-	dB
			48K/16bits	-	-82.4	-	
			88.2K/24bits	-	-82.0	-	
			96K/24bits	-	-81.9	-	
			176.4K/32bits	-	-81.4	-	
			192K/32bits	-	-81.2	-	
	32Ω loading Cascade 33 ohm	0dBFS (Fig5)	44.1K/16bits	-	-76.3	-	dB
			48K/16bits	-	-77.0	-	
			88.2K/24bits	-	-76.0	-	
			96K/24bits	-	-77.1	-	
			176.4K/32bits	-	-76.8	-	
			192K/32bits	-	-76.9	-	
		-3dBFS (Fig6)	44.1K/16bits	-	-81.7	-	dB
			48K/16bits	-	-80.5	-	
			88.2K/24bits	-	-81.7	-	
			96K/24bits	-	-82.3	-	
			176.4K/32bits	-	-81.8	-	
			192K/32bits	-	-82.0	-	

Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	10KΩ loading	44.1K/16bits	-	-91.9	-	dB
		48K/16bits	-	-92.5	-	
		88.2K/24bits	-	-92.8	-	
		96K/24bits	-	-94.7	-	
		176.4K/32bits	-	-94.7	-	
		192K/32bits	-	-94.7	-	
	32Ω loading	44.1K/16bits	-	-92.0	-	dB
		48K/16bits	-	-92.8	-	
		88.2K/24bits	-	-95.0	-	
		96K/24bits	-	-95.0	-	
		176.4K/32bits	-	-94.5	-	
		192K/32bits	-	-94.5	-	
	32Ω loading Cascade 33 ohm	44.1K/16bits	-	-91.8	-	dB
		48K/16bits	-	-92.3	-	
		88.2K/24bits	-	-94.8	-	
		96K/24bits	-	-94.8	-	
		176.4K/32bits	-	-94.5	-	
		192K/32bits	-	-94.5	-	
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	10KΩ loading	44.1K/16bits	-	-92.2	-	dB
		48K/16bits	-	-92.5	-	
		88.2K/24bits	-	-93.2	-	
		96K/24bits	-	-94.7	-	
		176.4K/32bits	-	-94.7	-	
		192K/32bits	-	-94.7	-	
	32Ω loading	44.1K/16bits	-	-92.8	-	dB
		48K/16bits	-	-92.8	-	
		88.2K/24bits	-	-95.5	-	
		96K/24bits	-	-95.5	-	
		176.4K/32bits	-	-95.0	-	
		192K/32bits	-	-95.0	-	
	32Ω loading Cascade 33 ohm	44.1K/16bits	-	-92.5	-	dB
		48K/16bits	-	-92.7	-	
		88.2K/24bits	-	-94.8	-	
		96K/24bits	-	-95.0	-	
		176.4K/32bits	-	-94.8	-	
		192K/32bits	-	-94.6	-	

Channel Separation (Cross-talk)		Sampling frequency	100	-	10K	HZ
	10KΩ Loading (Fig7)	44.1K/16bits	-104.9	-	-97.1	dB
		48K/16bits	-104.5	-	-97.6	
		88.2K/24bits	-104.4	-	-97.3	
		96K/24bits	-102.7	-	-97.6	
		176.4K/32bits	-103.3	-	-96.6	
		192K/32bits	-104.7	-	-95.9	
	32Ω Loading (Fig8)	44.1K/16bits	-84.7	-	-73.6	dB
		48K/16bits	-84.7	-	-73.0	
		88.2K/24bits	-84.1	-	-73.5	
		96K/24bits	-84.0	-	-74.4	
		176.4K/32bits	-84.0	-	-73.6	
		192K/32bits	-84.3	-	-73.6	
	32Ω loading Cascade 33 ohm (Fig9)	44.1K/16bits	-97.1	-	-77.2	dB
		48K/16bits	-96.4	-	-76.9	
		88.2K/24bits	-96.7	-	-78.2	
		96K/24bits	-96.3	-	-77.1	
		176.4K/32bits	-96.9	-	-77.0	
		192K/32bits	-96.1	-	-77.0	
Frequency Response		Band Edge	20	-	20K	HZ
	10KΩ Loading (Fig10)	44.1K/16bits	0.1	-	-4.6	dB
		48K/16bits	0.1	-	-1.0	
		88.2K/24bits	0.1	-	-0.2	
		96K/24bits	0.1	-	-0.3	
		176.4K/32bits	0.04	-	-0.1	
		192K/32bits	0.04	-	-0.2	
	32Ω Loading (Fig11)	44.1K/16bits	0.1	-	-4.6	dB
		48K/16bits	0.1	-	-1.0	
		88.2K/24bits	0.04	-	-0.2	
		96K/24bits	0.02	-	-0.3	
		176.4K/32bits	0.01	-	-0.1	
		192K/32bits	0.02	-	-0.2	
	32Ω loading Cascade 33 ohm (Fig12)	44.1K/16bits	0.1	-	-4.6	dB
		48K/16bits	0.1	-	-1.0	
		88.2K/24bits	0.1	-	-0.3	
		96K/24bits	0.1	-	-0.4	
		176.4K/32bits	0.03	-	-0.2	
		192K/32bits	0.05	-	-0.3	

Passband Ripple	10KΩ loading	44.1K/16bits		0.30		dB
		48K/16bits		0.30		
		88.2K/24bits		0.32		
		96K/24bits		0.31		
		176.4K/32bits		0.34		
		192K/32bits		0.30		
	32Ω loading	44.1K/16bits		0.26		dB
		48K/16bits		0.26		
		88.2K/24bits		0.27		
		96K/24bits		0.28		
		176.4K/32bits		0.28		
		192K/32bits		0.25		
	32Ω loading Cascade 33 ohm	44.1K/16bits		0.32		dB
		48K/16bits		0.30		
		88.2K/24bits		0.30		
		96K/24bits		0.31		
		176.4K/32bits		0.28		
		192K/32bits		0.24		
Interchannel phase delay	10KΩ Loading (Fig13)	44.1K/16bits		0.02		%
		48K/16bits		0.03		
		88.2K/24bits		0.0		
		96K/24bits		0.0		
		176.4K/32bits		-0.01		
		192K/32bits		0.01		
	32Ω Loading (Fig14)	44.1K/16bits		0.01		%
		48K/16bits		0.01		
		88.2K/24bits		0.01		
		96K/24bits		0.01		
		176.4K/32bits		0.01		
		192K/32bits		0.01		
	32Ω loading Cascade 33 ohm (Fig15)	44.1K/16bits		0.07		%
		48K/16bits		0.09		
		88.2K/24bits		0.01		
		96K/24bits		0.01		
		176.4K/32bits		0.01		
		192K/32bits		0.08		

Note 1: Headphone 32 ohm loading audio quality measure by cascading 33 or 0 ohm resistors, the schematic diagram as below.

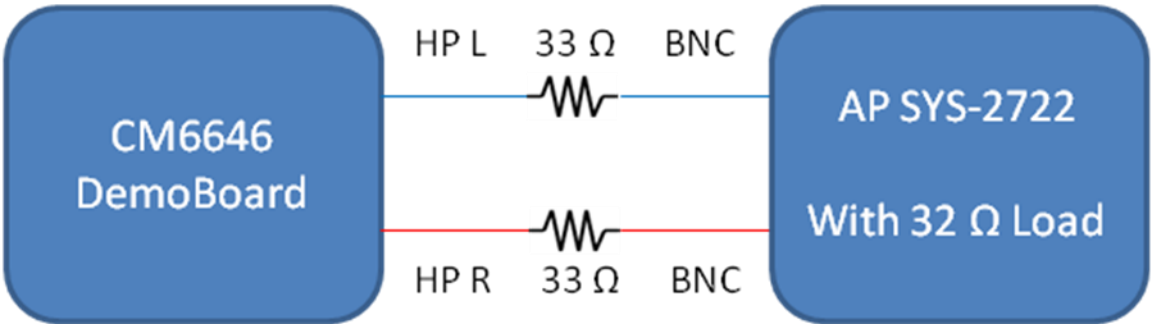
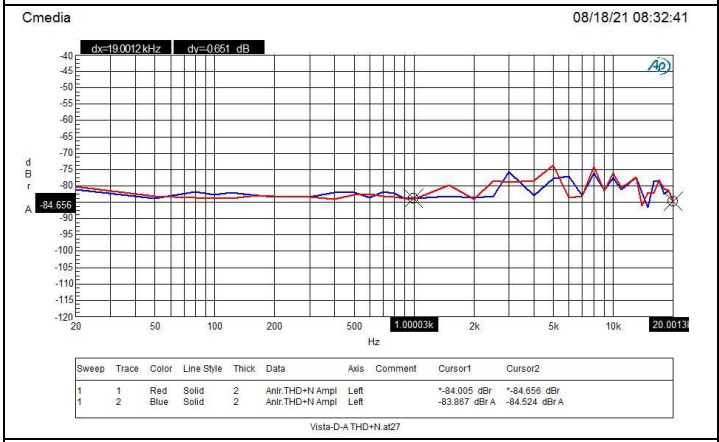
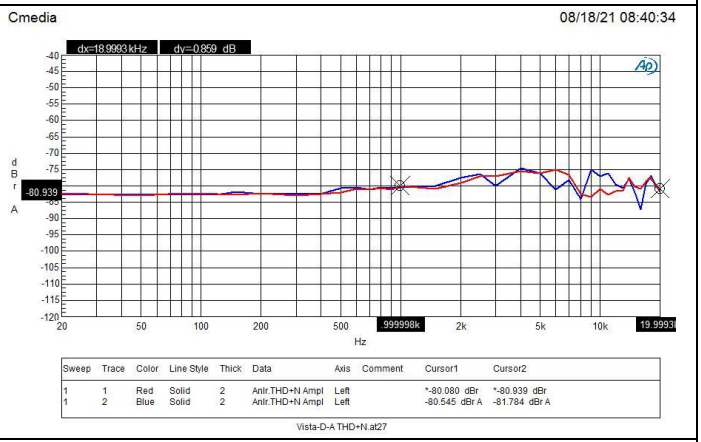


Figure 1： DAC 10KΩ loading, 0dB, THD+N

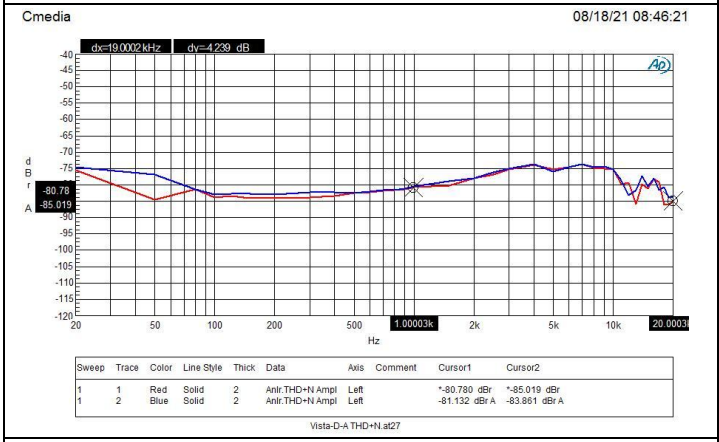
44.1K/16bits



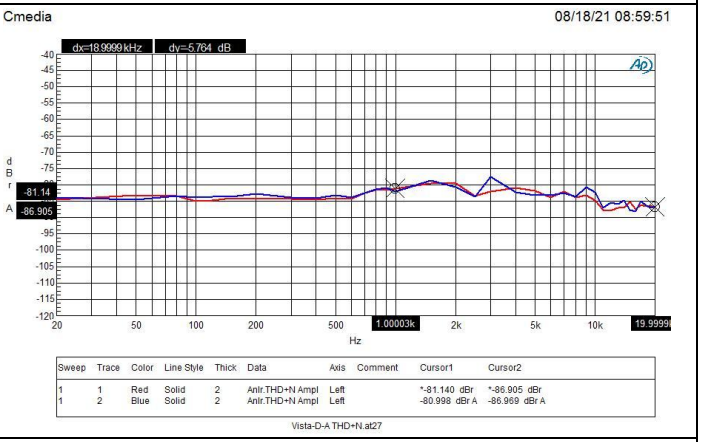
48K/16bits



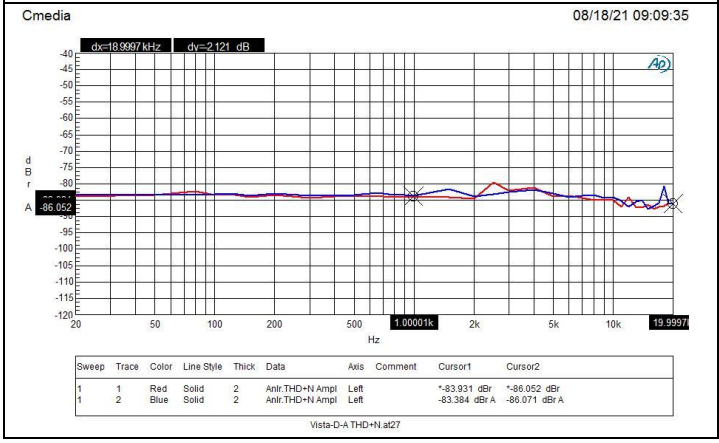
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

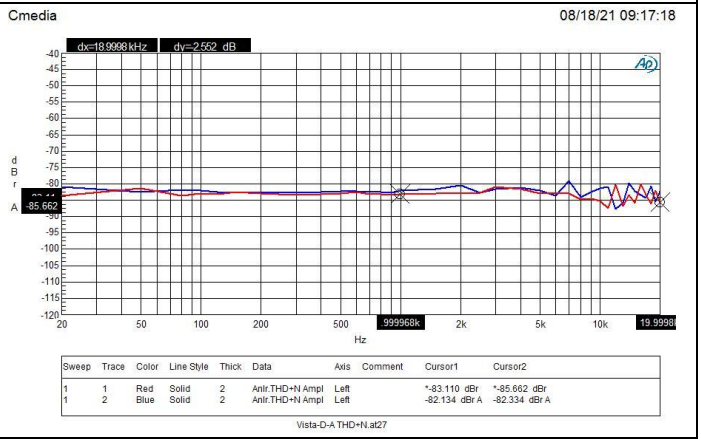
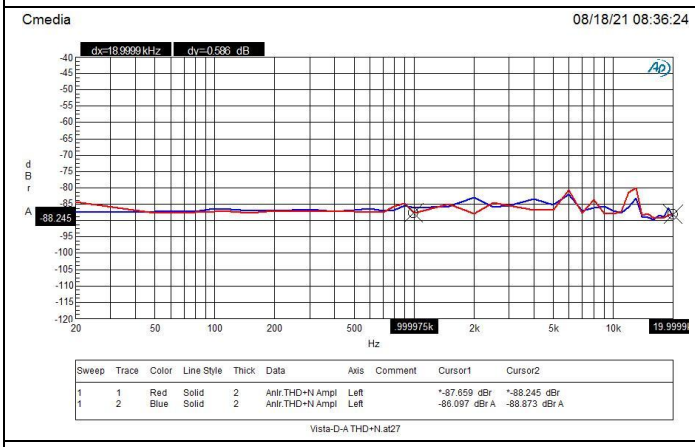
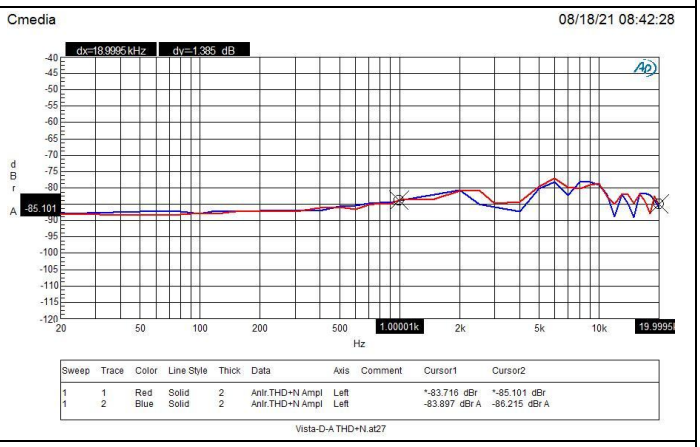


Figure 2： DAC 10KΩ loading, -3dB, THD+N

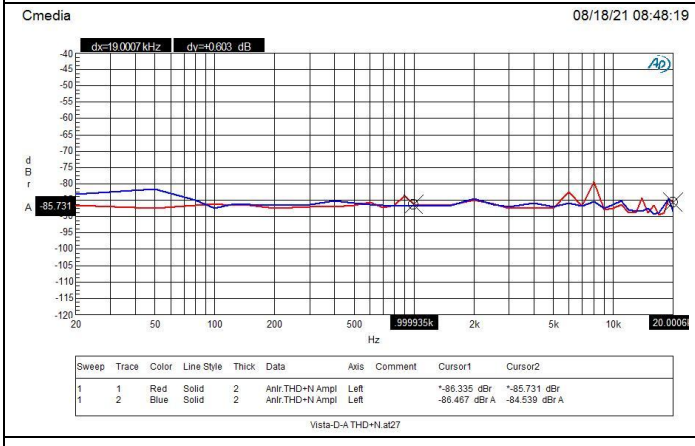
44.1K/16bits



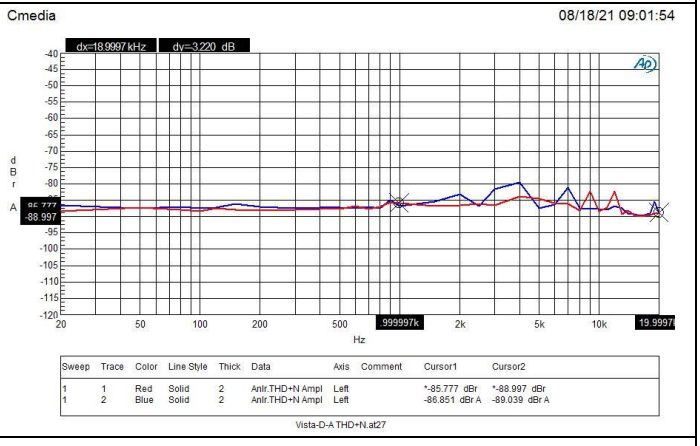
48K/16bits



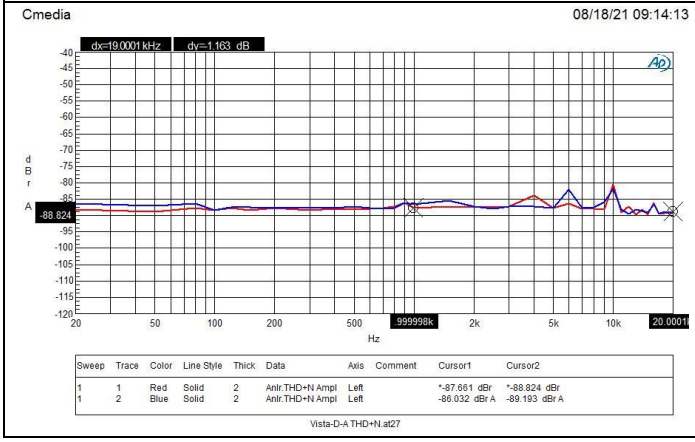
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

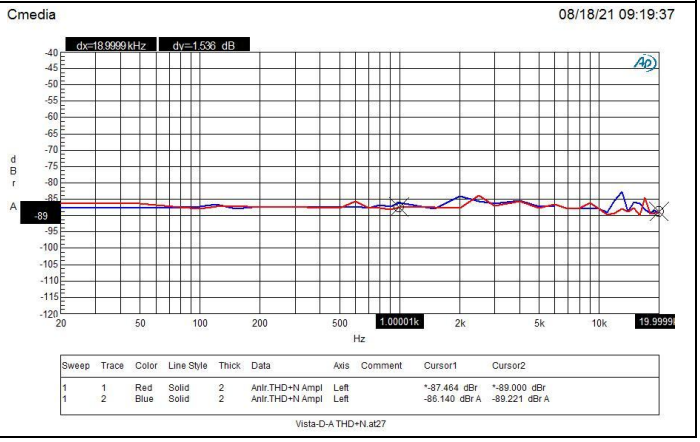
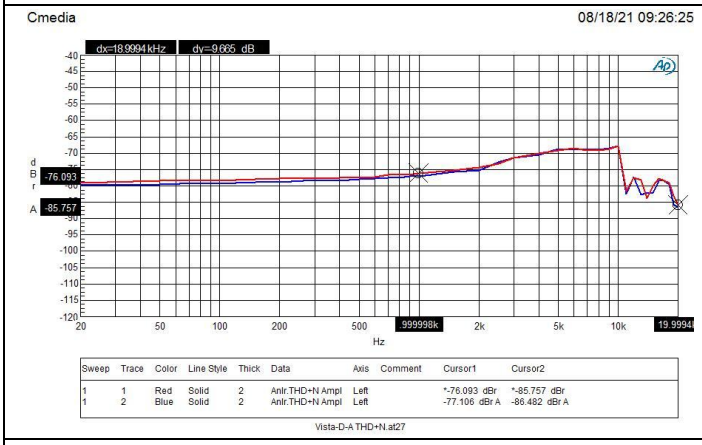
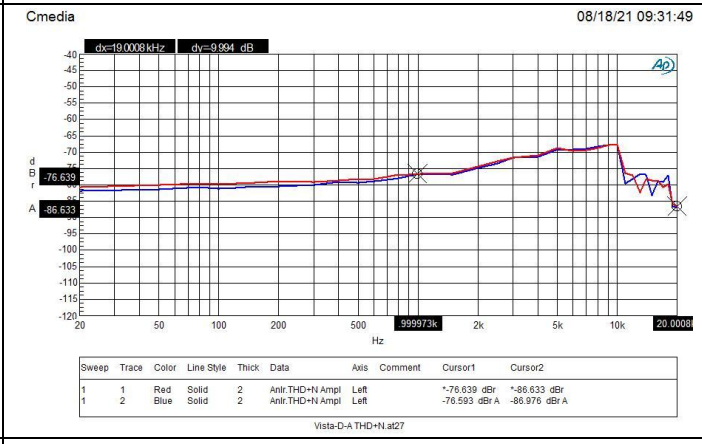


Figure 3： DAC 32Ω loading, 0dB, THD+N

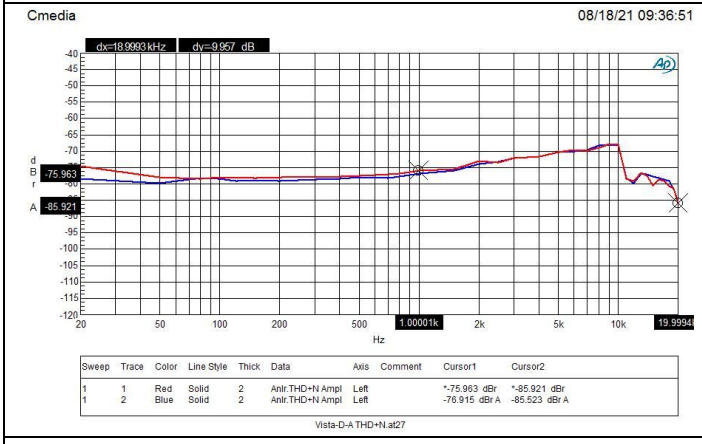
44.1K/16bits



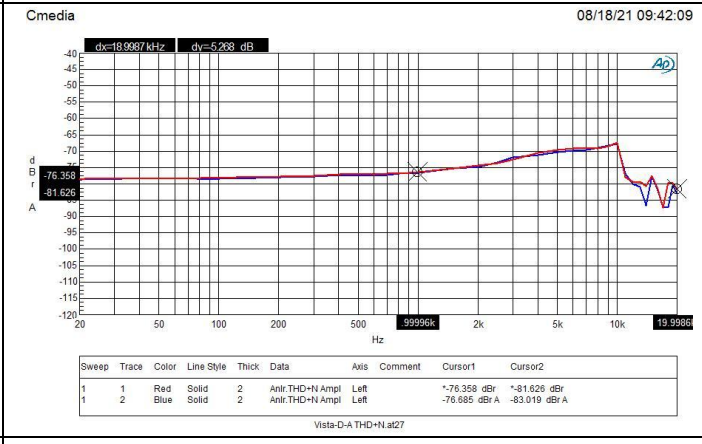
48K/16bits



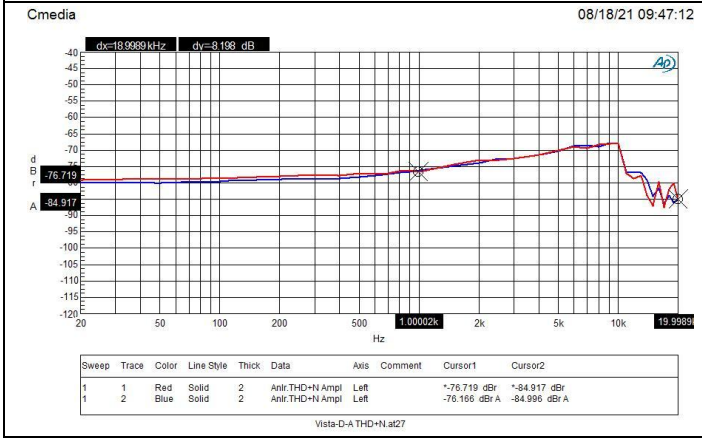
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

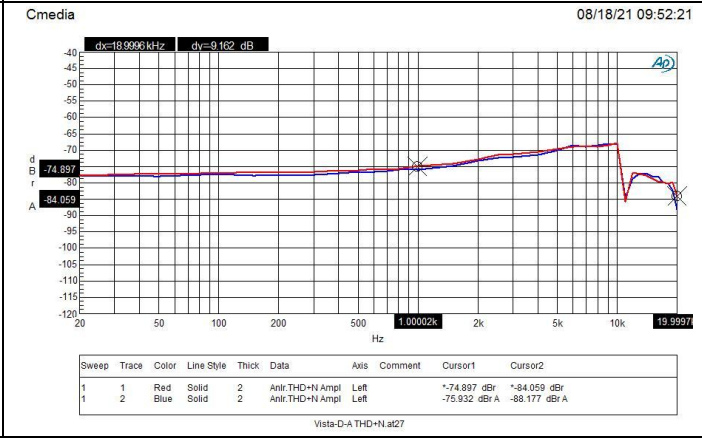
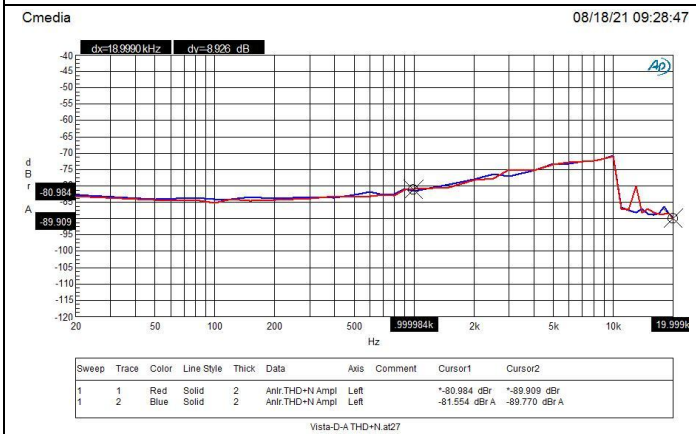
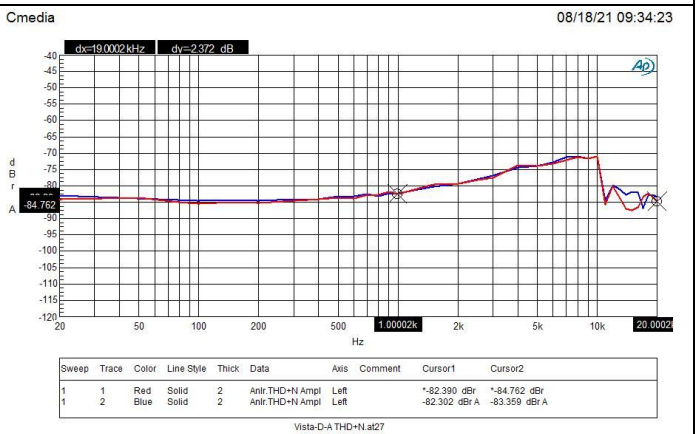


Figure 4： DAC 32Ω loading, -3dB, THD+N

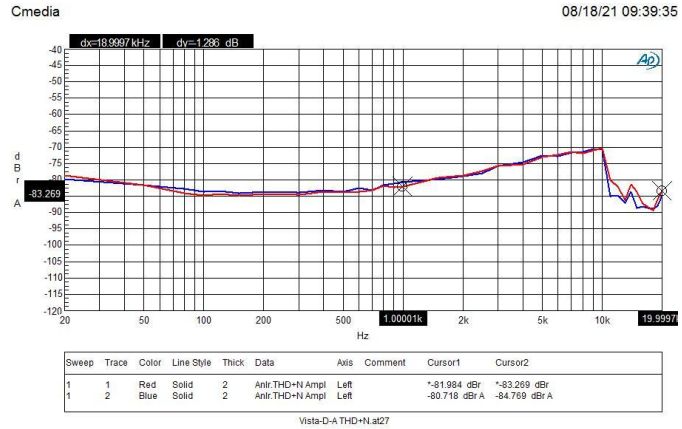
44.1K/16bits



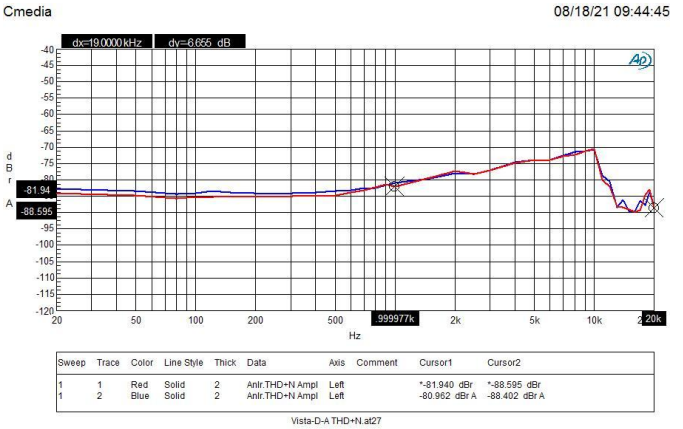
48K/16bits



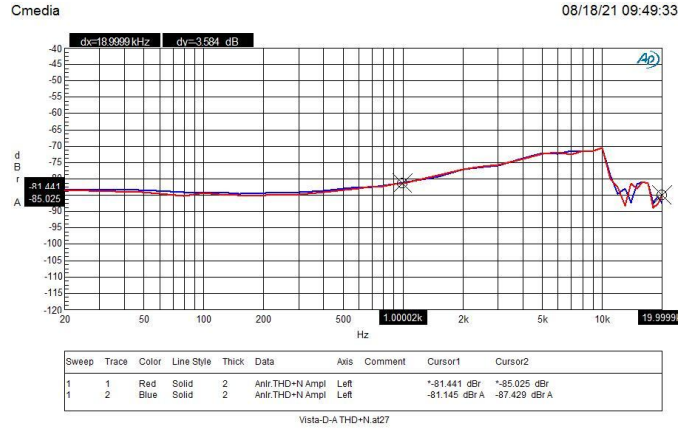
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

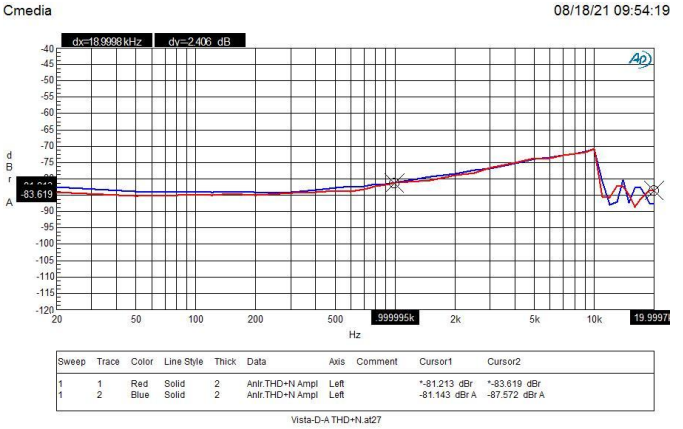
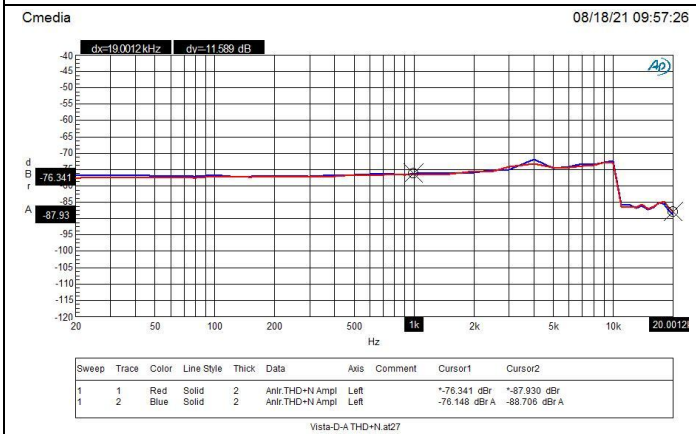
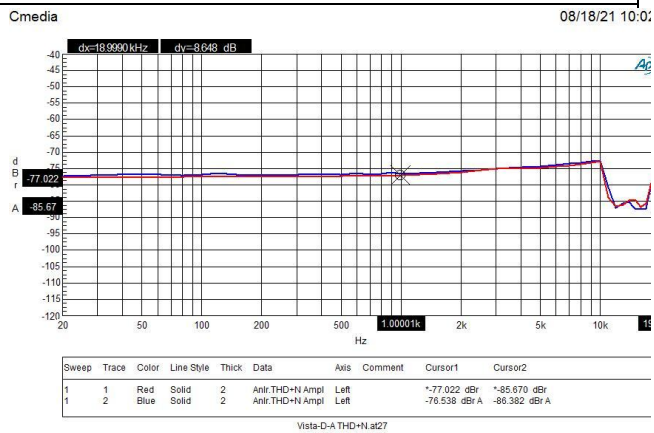


Figure 5： DAC 32Ω loading Cascade 33 ohm, 0dB, THD+N

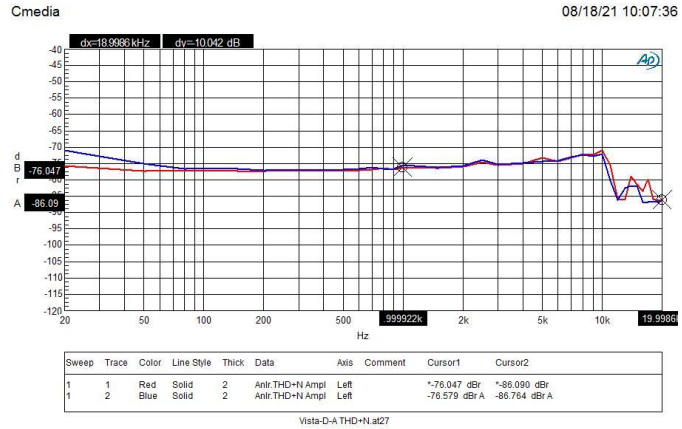
44.1K/16bits



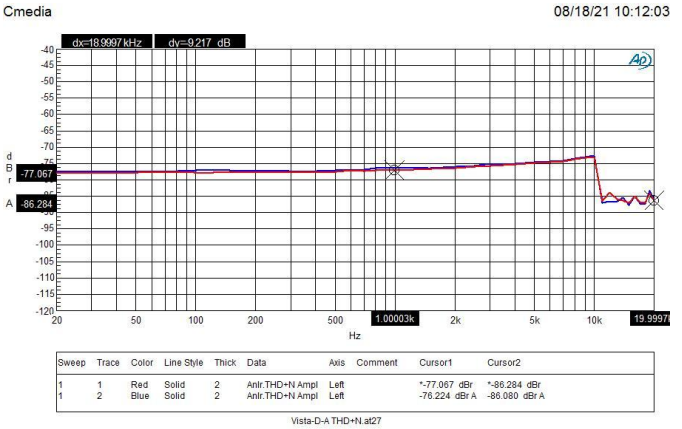
48K/16bits



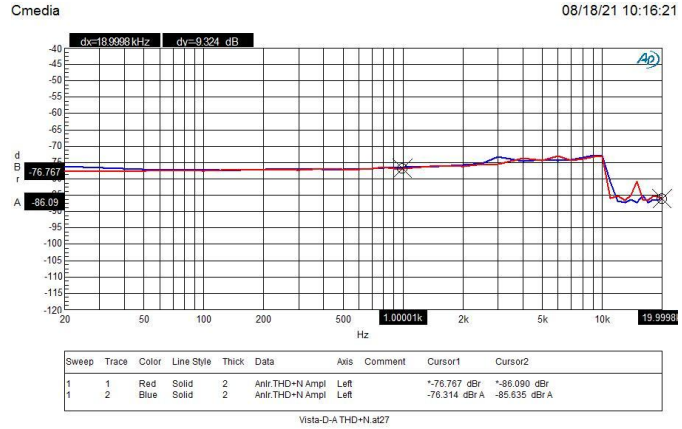
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

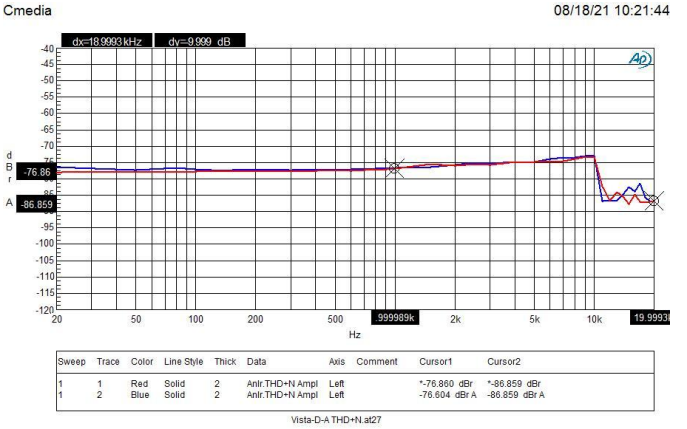
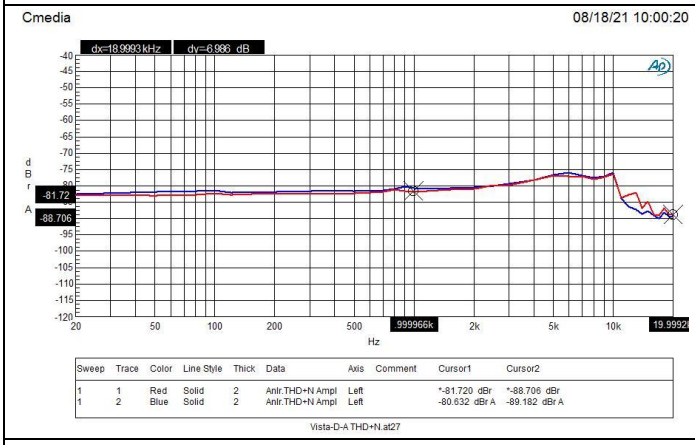
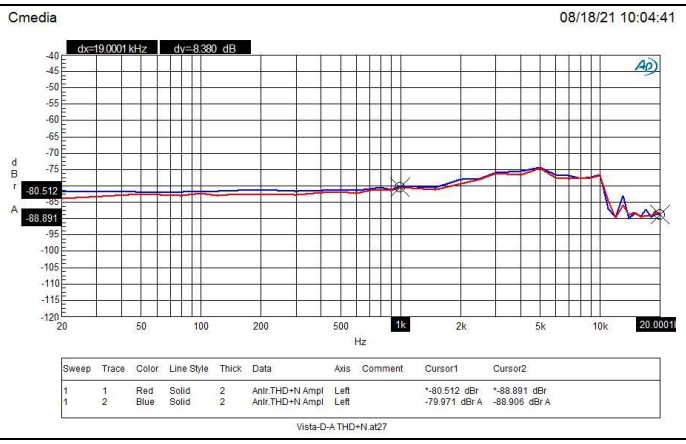


Figure 6： DAC 32Ω loading Cascade 33 Ω, -3dB, THD+N

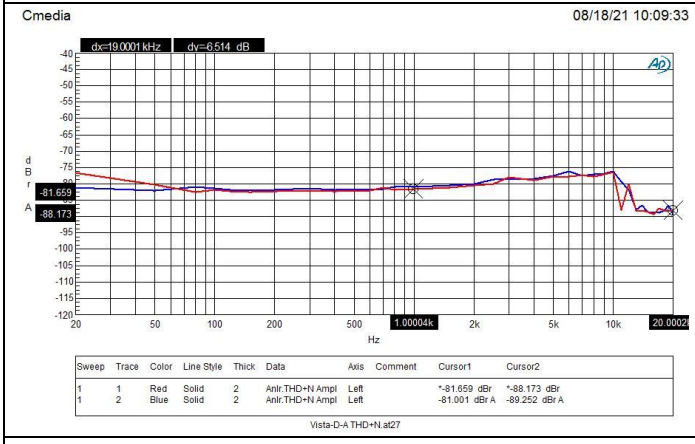
44.1K/16bits



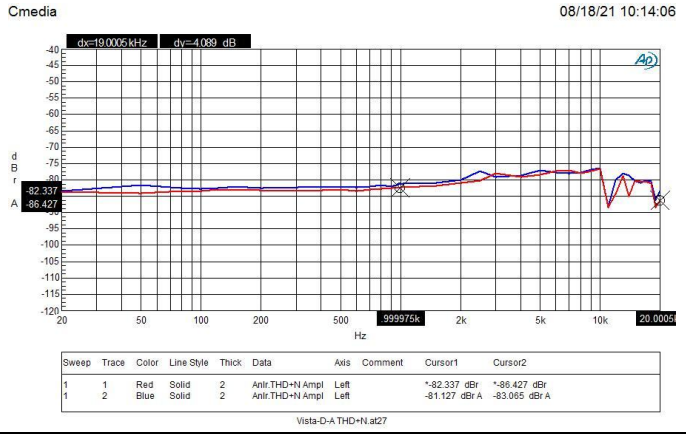
48K/16bits



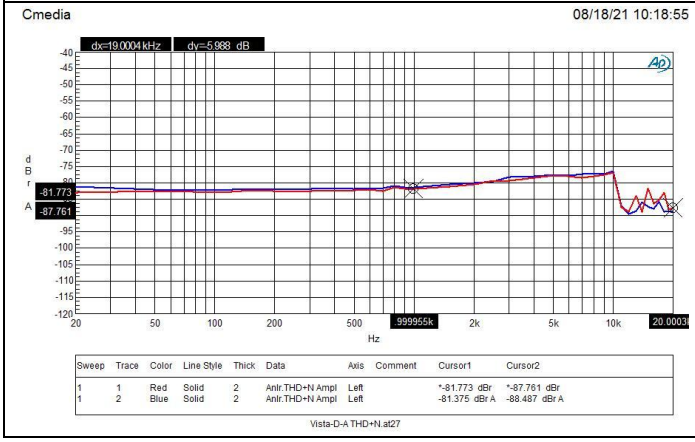
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

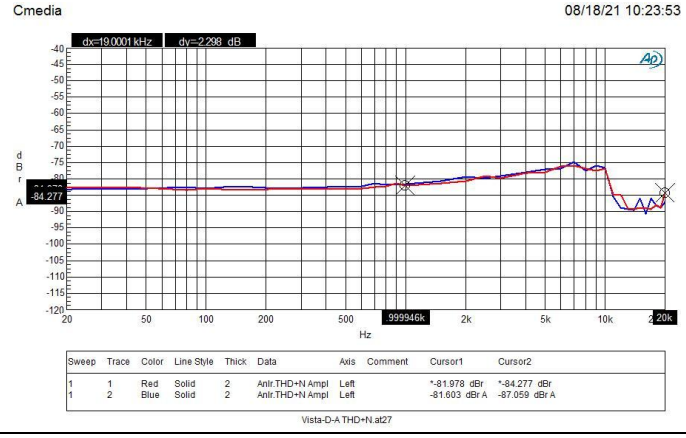
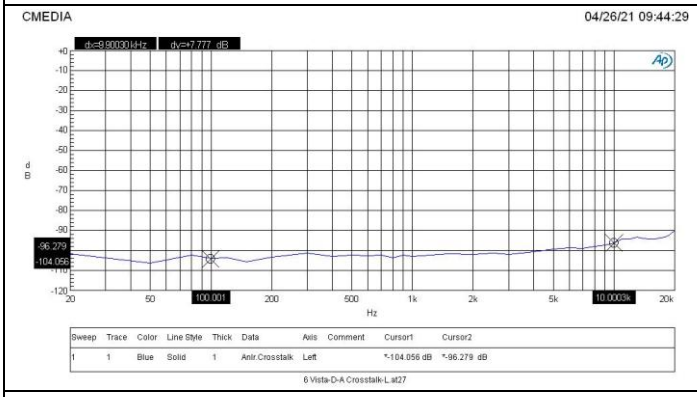
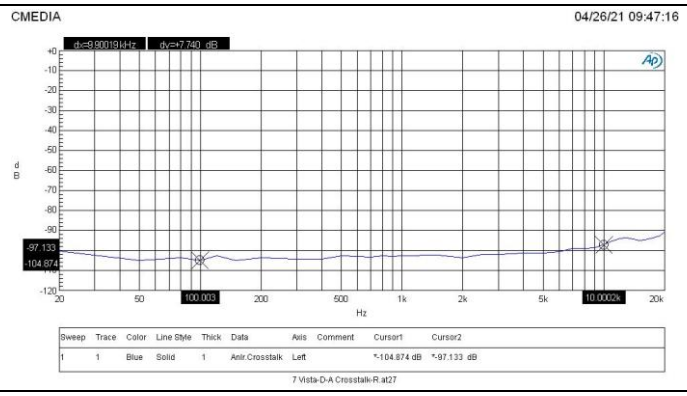


Figure 7： DAC 10KΩ loading, Cross-talk

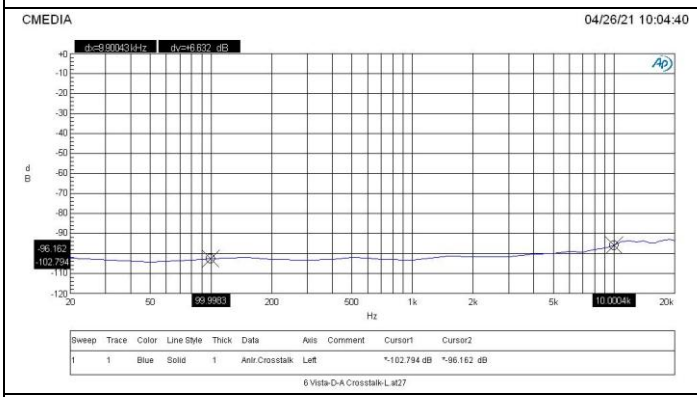
44.1K/16bits L



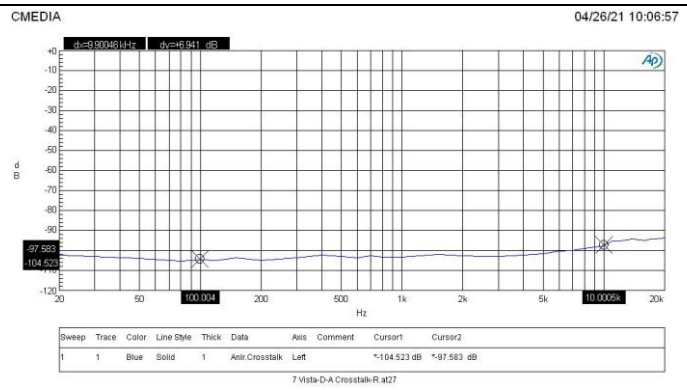
44.1K/16bits R



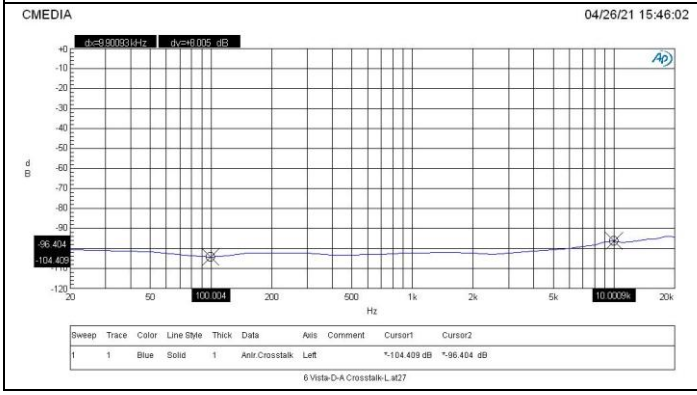
48K/16bits L



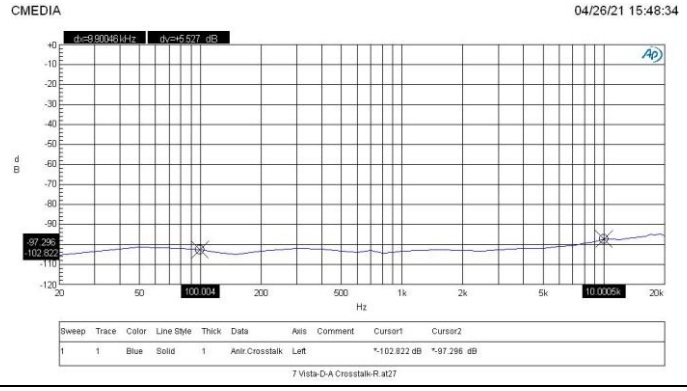
48K/16bits R



88.2K/24bits L



88.2K/24bits R



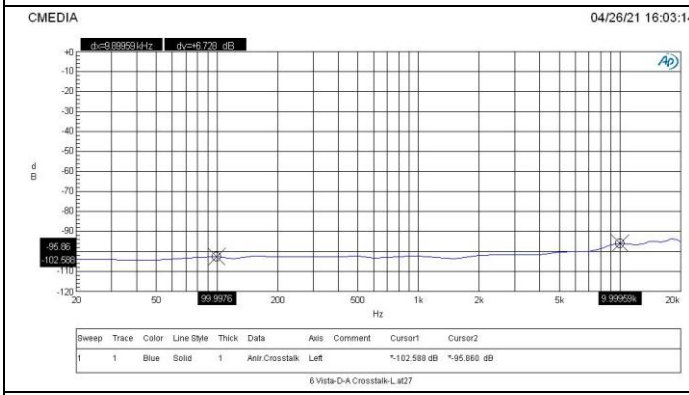
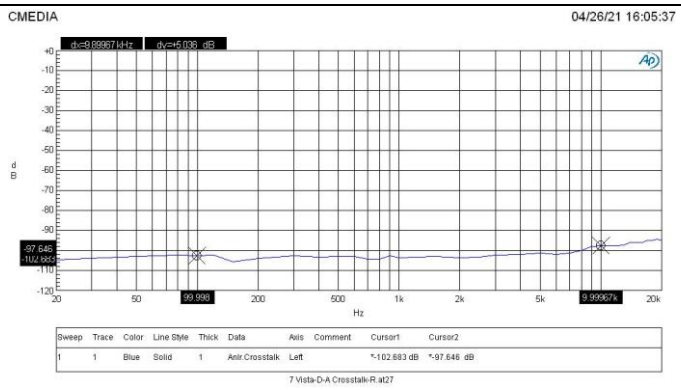
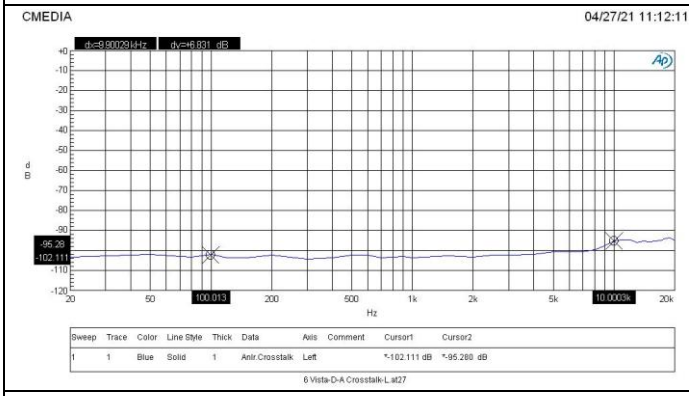
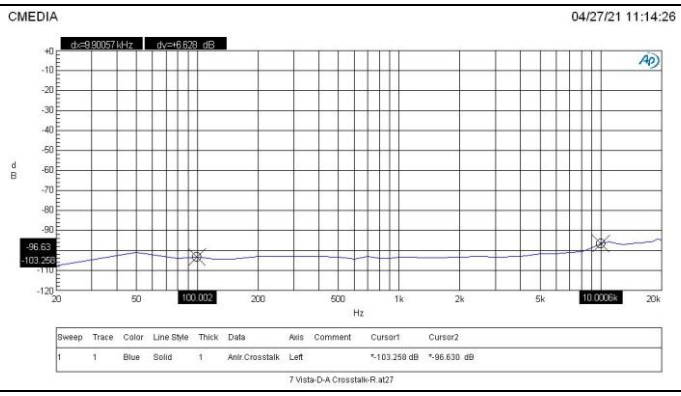
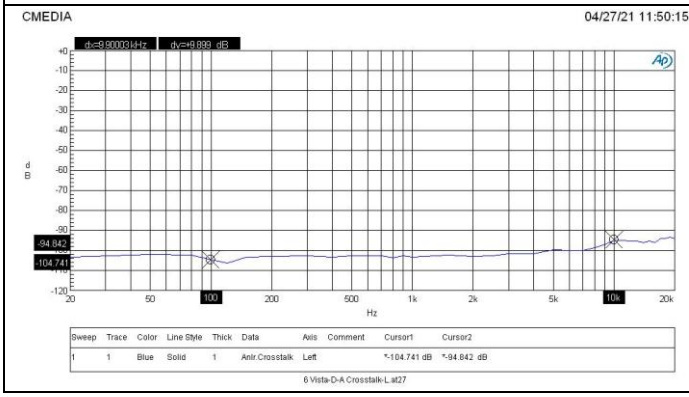
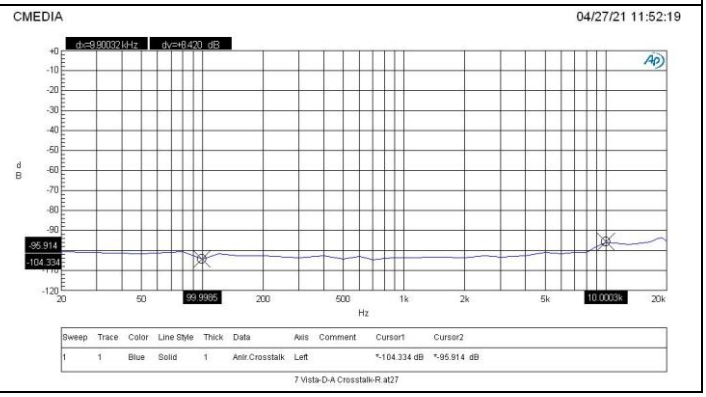
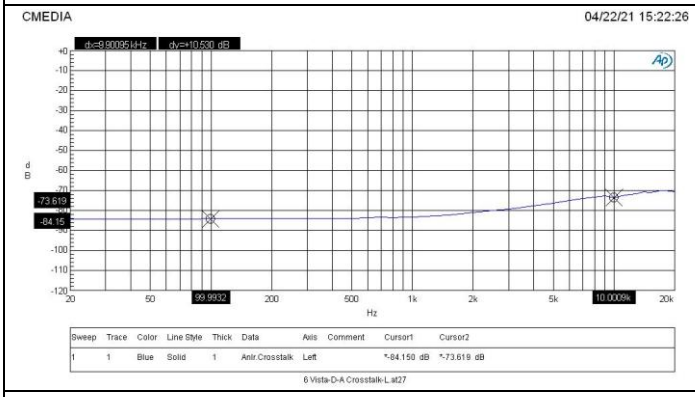
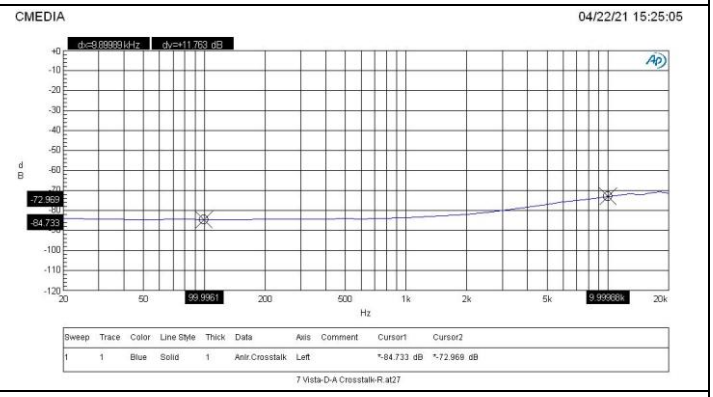
96K/24bits L	96K/24bits R
	
176.4K/32bits L	176.4K/32bits R
	
192K/32bits L	192K/32bits R
	

Figure 8： DAC 32Ω loading, Cross-talk

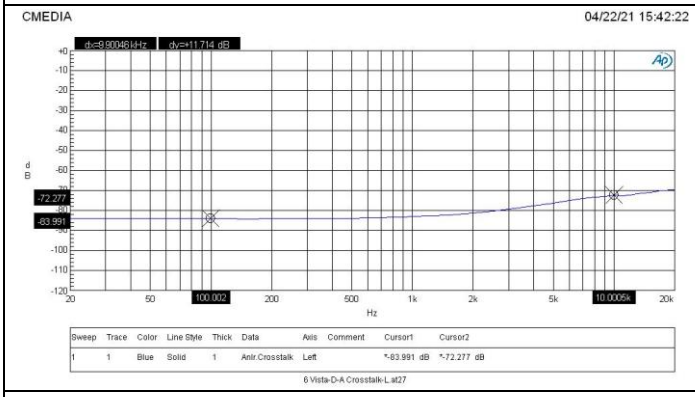
44.1K/16bits L



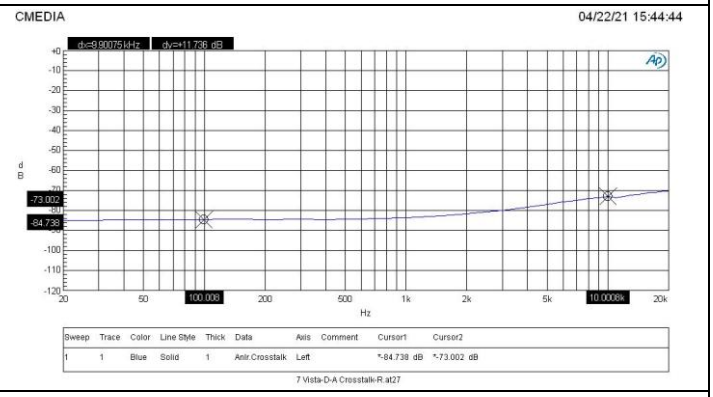
44.1K/16bits R



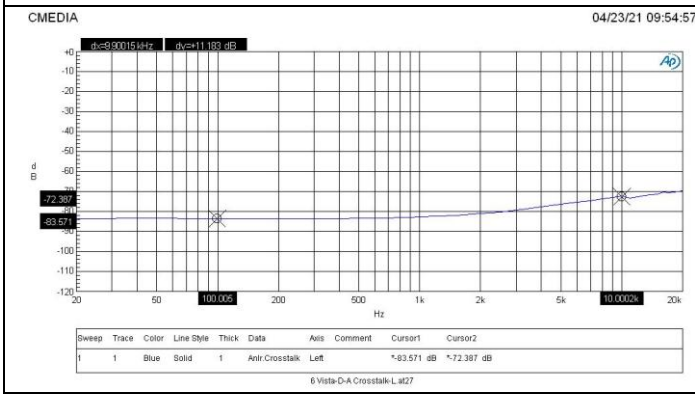
48K/16bits L



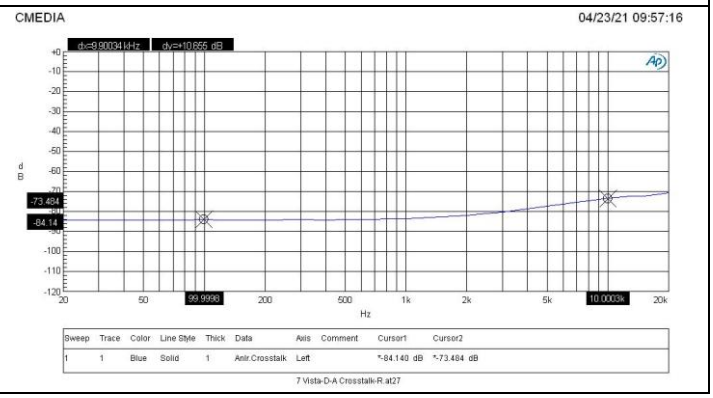
48K/16bits R



88.2K/24bits L



88.2K/24bits R



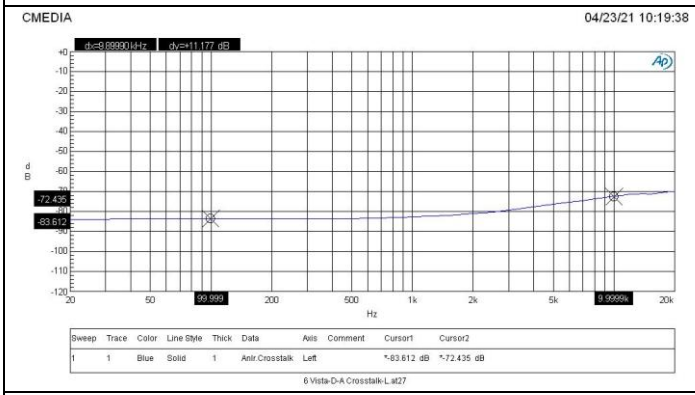
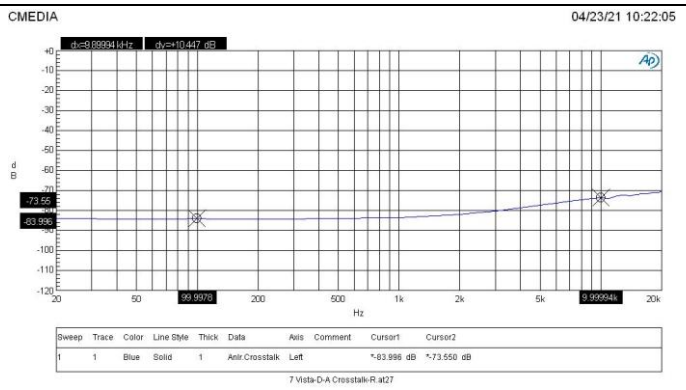
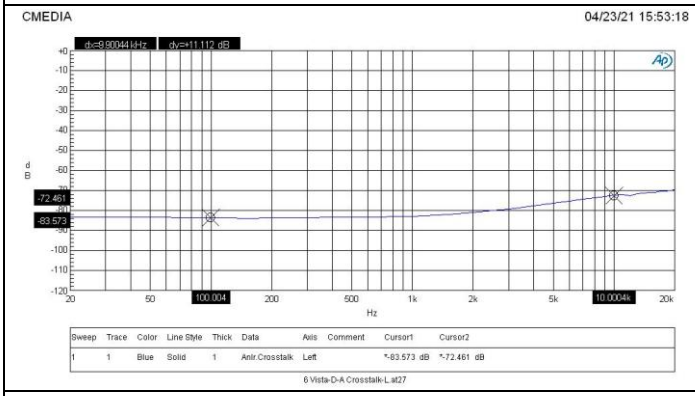
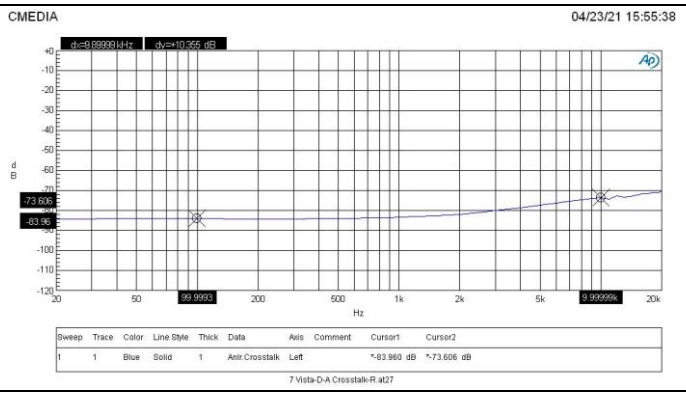
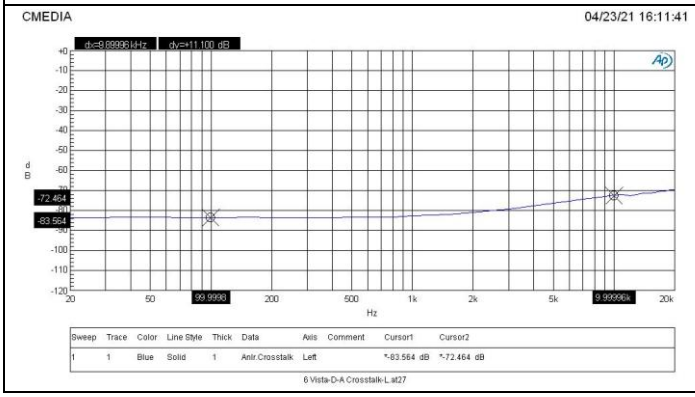
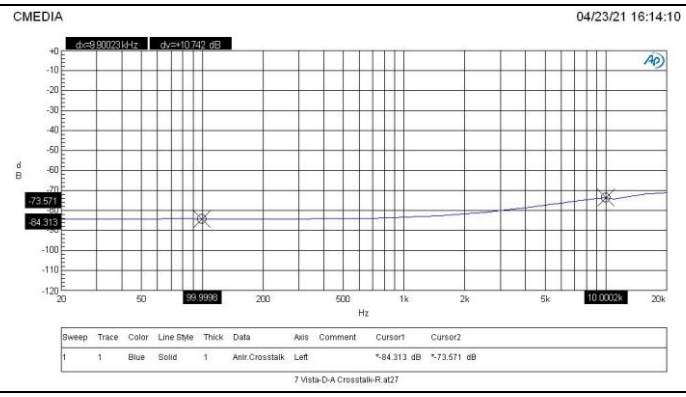
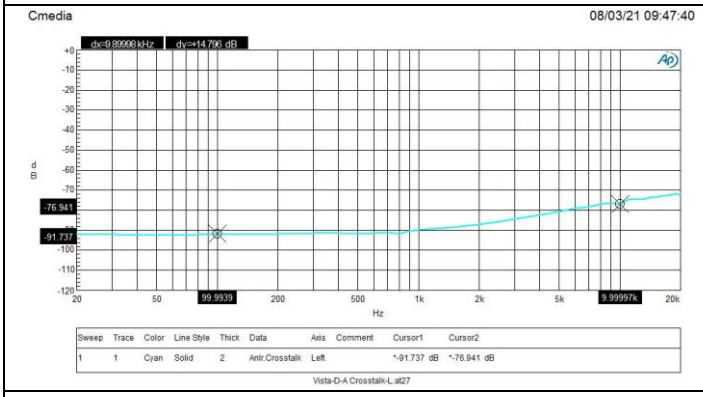
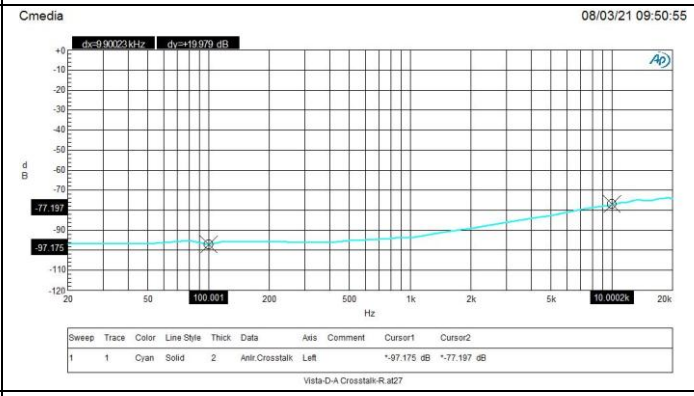
96K/24bits L	96K/24bits R
	
176.4K/32bits L	176.4K/32bits R
	
192K/32bits L	192K/32bits R
	

Figure 9： DAC 32Ω loading Cascade 33 Ω, Cross-talk

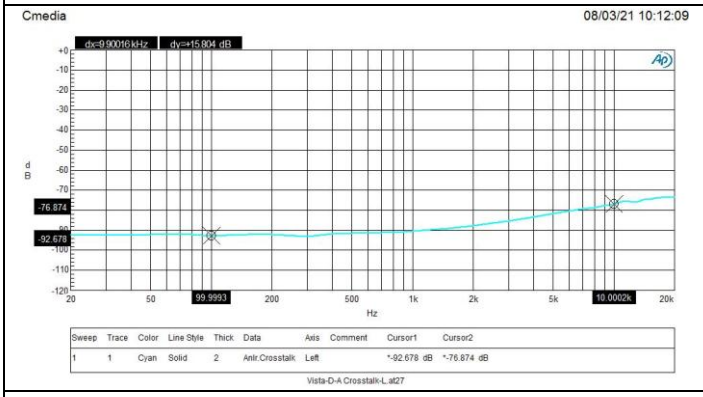
44.1K/16bits L



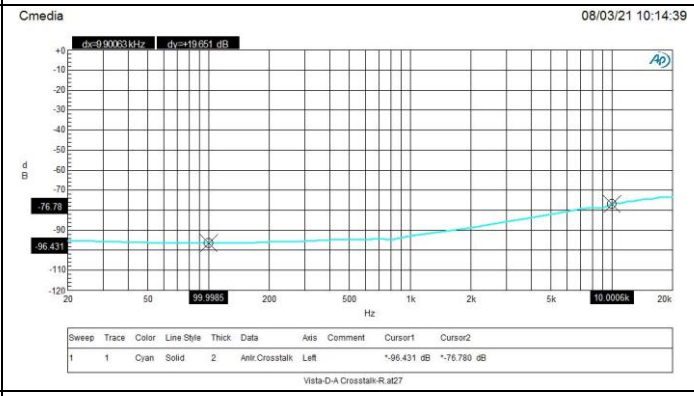
44.1K/16bits R



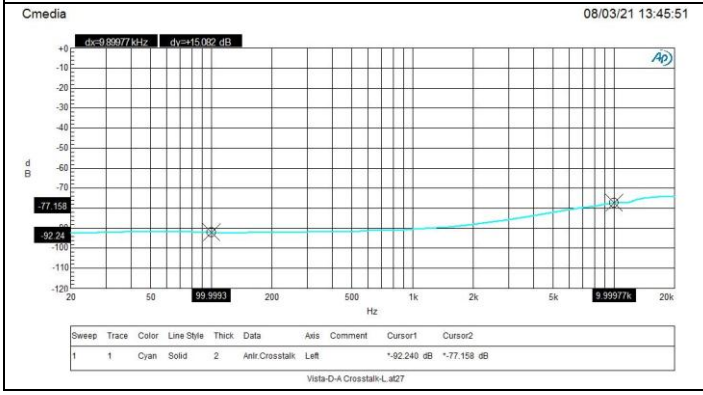
48K/16bits L



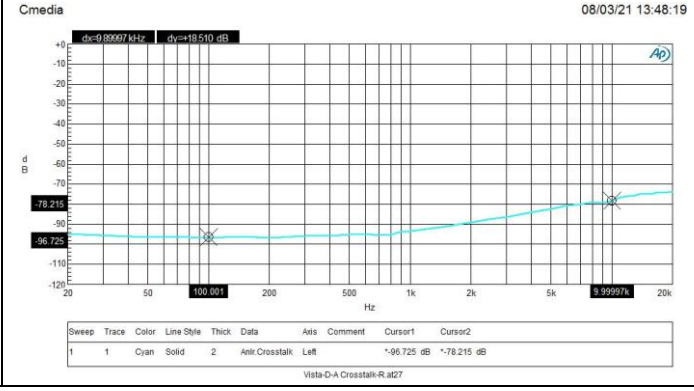
48K/16bits R



88.2K/24bits L



88.2K/24bits R



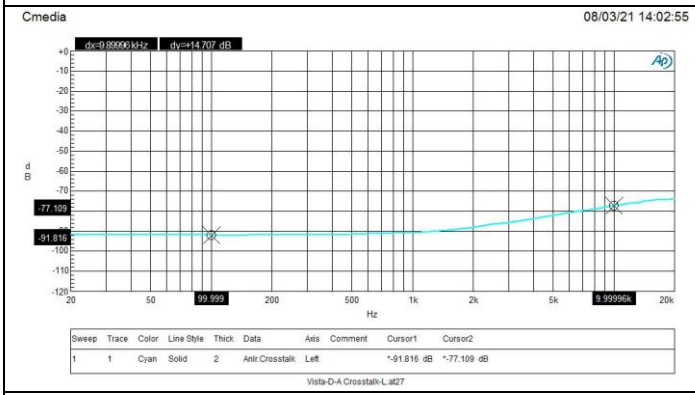
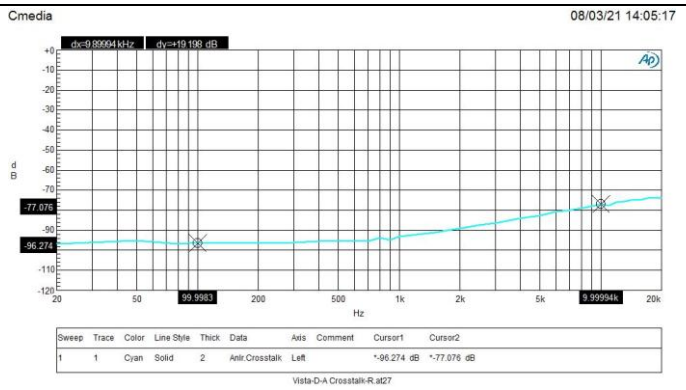
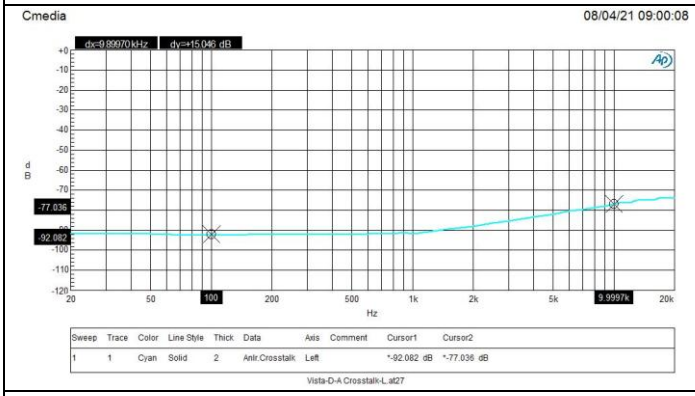
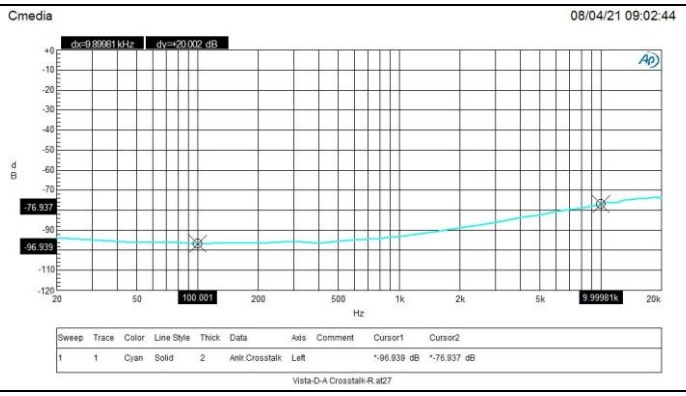
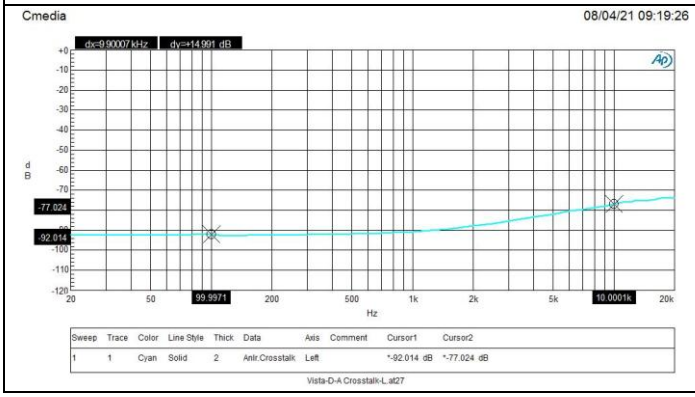
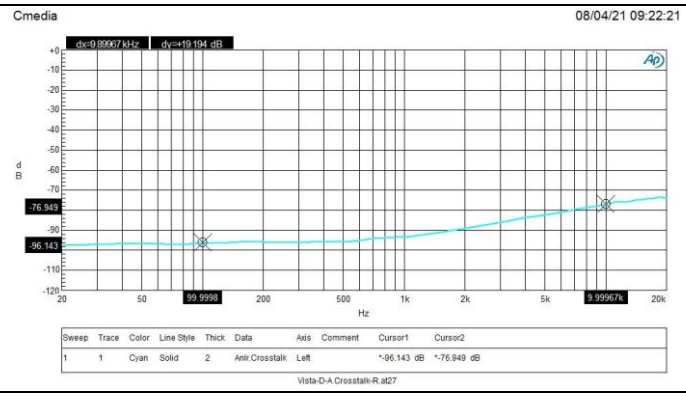
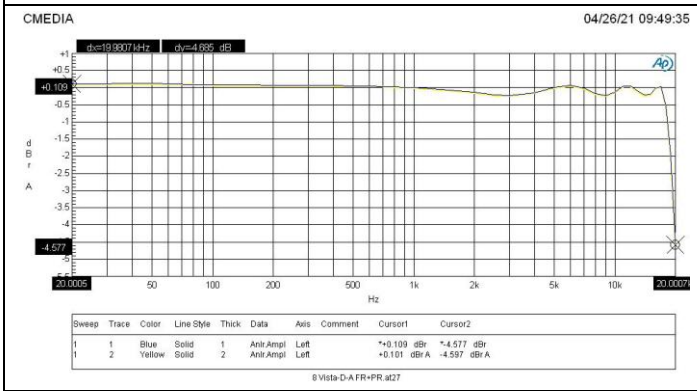
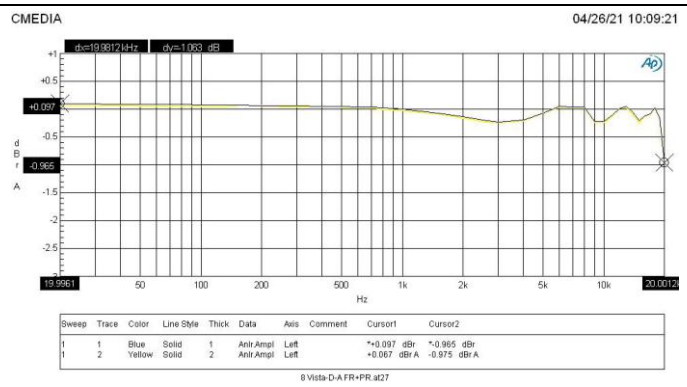
96K/24bits L	96K/24bits R
	
176.4K/32bits L	176.4K/32bits R
	
192K/32bits L	192K/32bits R
	

Figure 10：DAC 10KΩ loading,Frequency Response

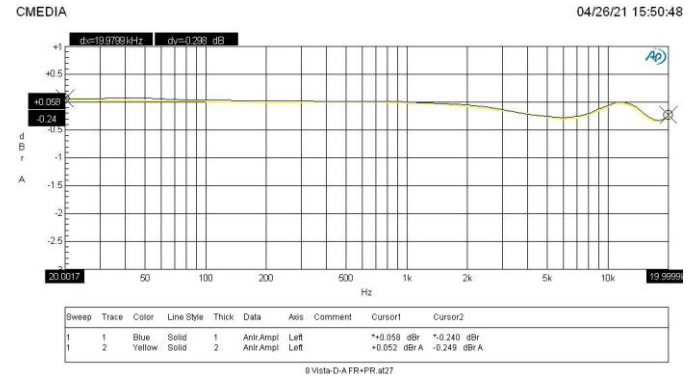
44.1K/16bits



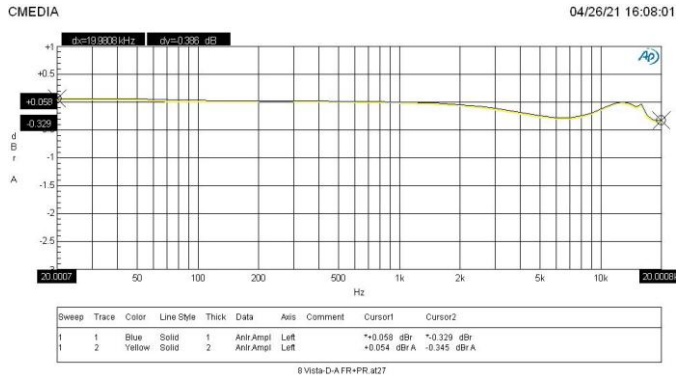
48K/16bits



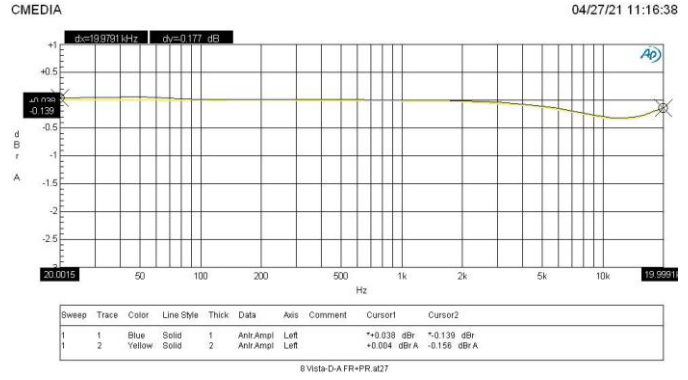
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

Figure 11：DAC 32Ω loading,Frequency Response

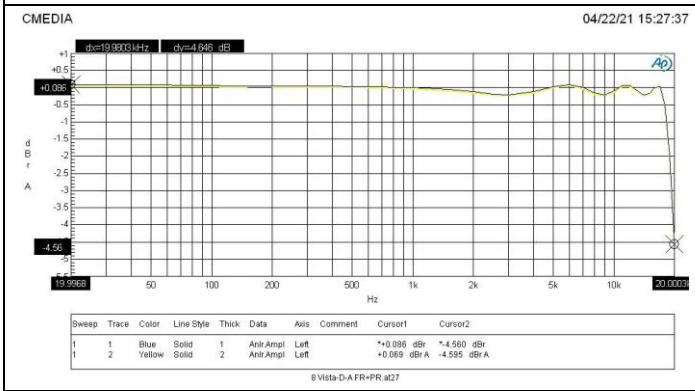
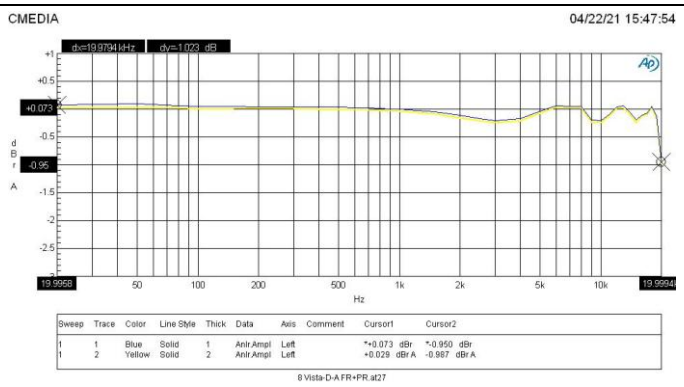
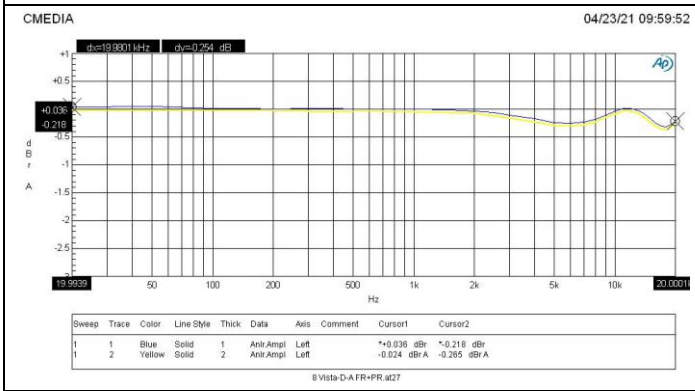
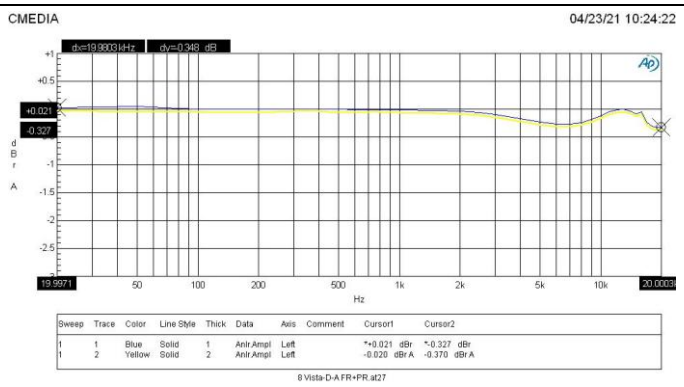
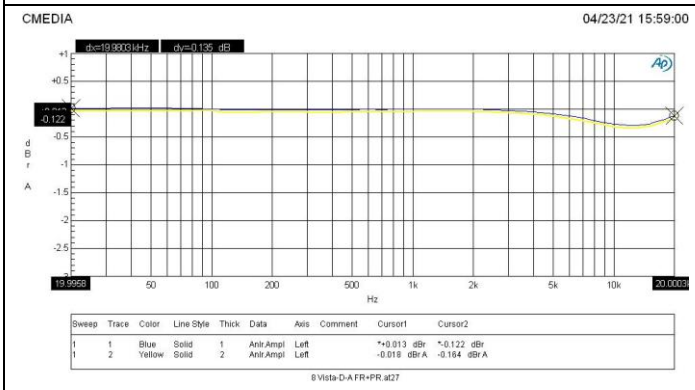
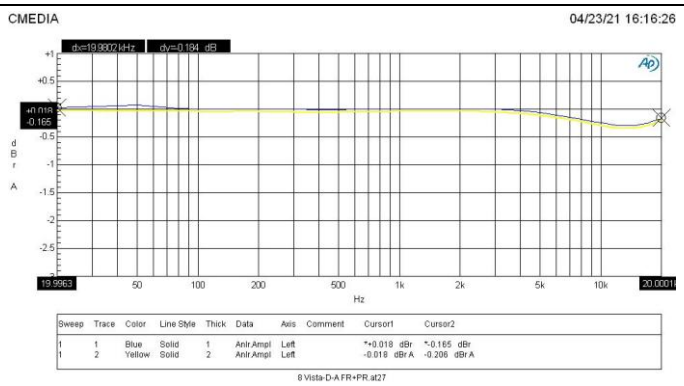
44.1K/16bits	48K/16bits
	
88.2K/24bits	96K/24bits
	
176.4K/32bits	192K/32bits
	

Figure 12：DAC 32Ω loading Cascade 33 Ω ,Frequency Response

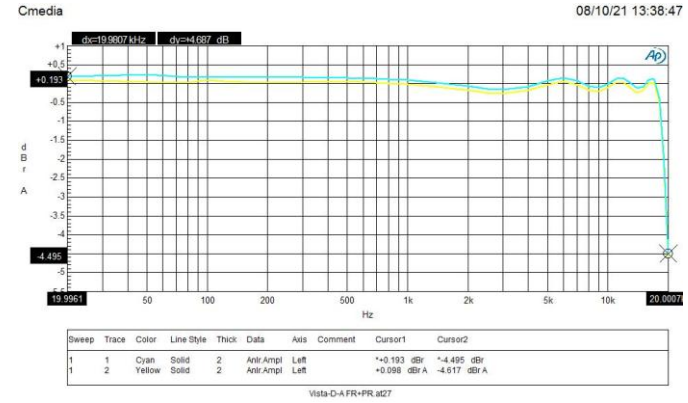
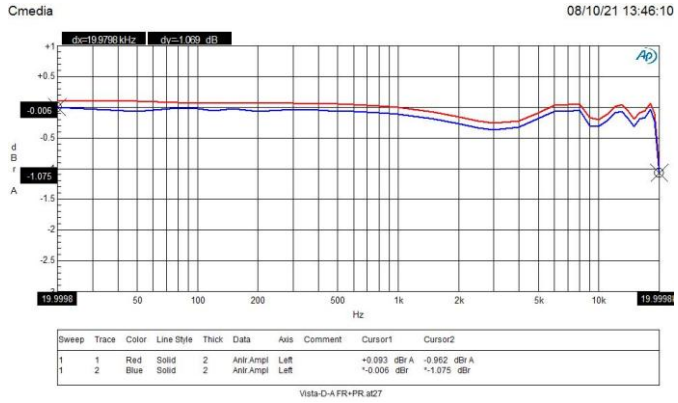
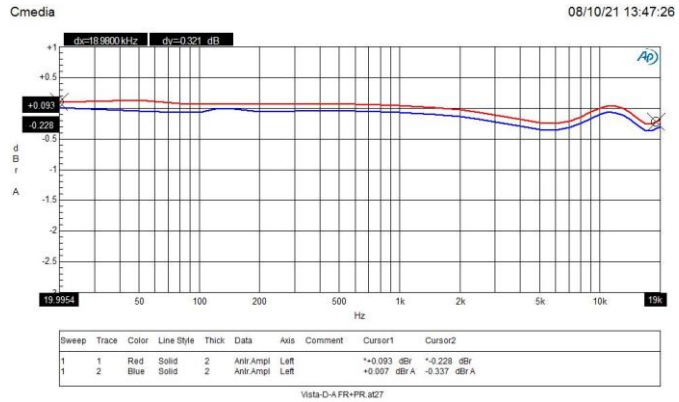
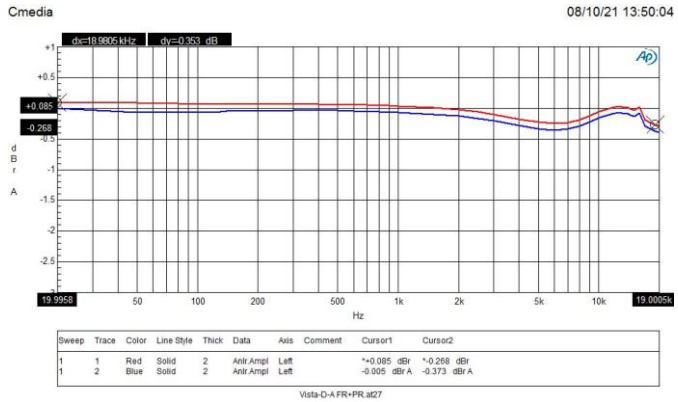
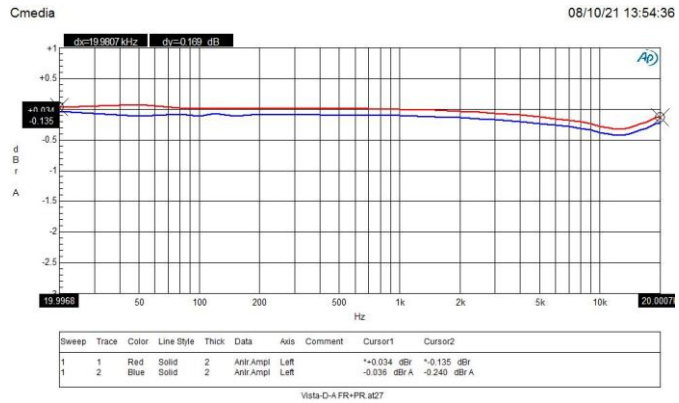
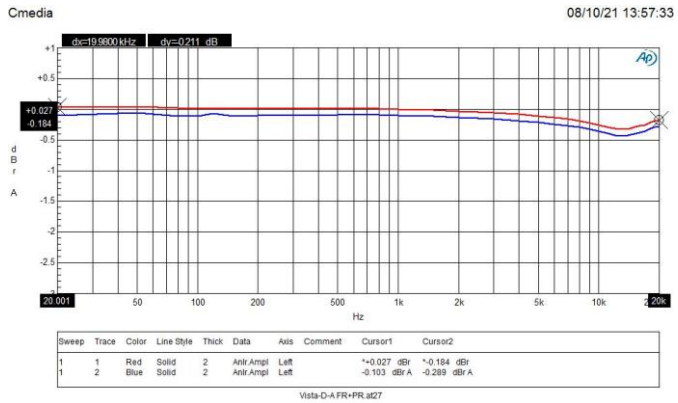
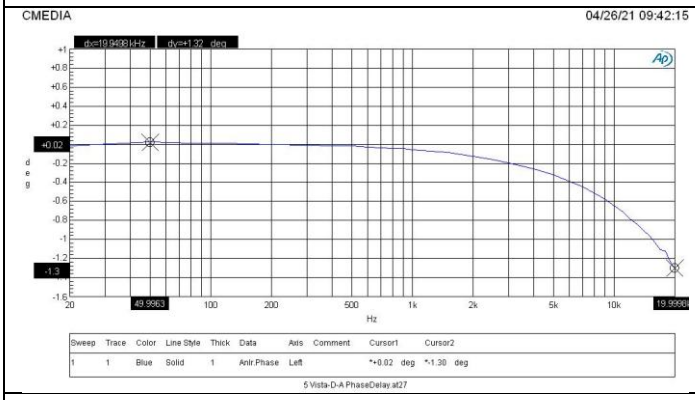
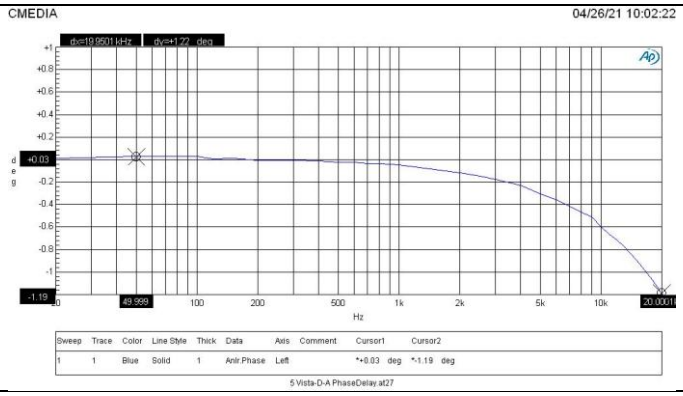
44.1K/16bits	48K/16bits
	
88.2K/24bits	96K/24bits
	
176.4K/32bits	192K/32bits
	

Figure 13：DAC 10KΩ loading, Interchannel phase delay

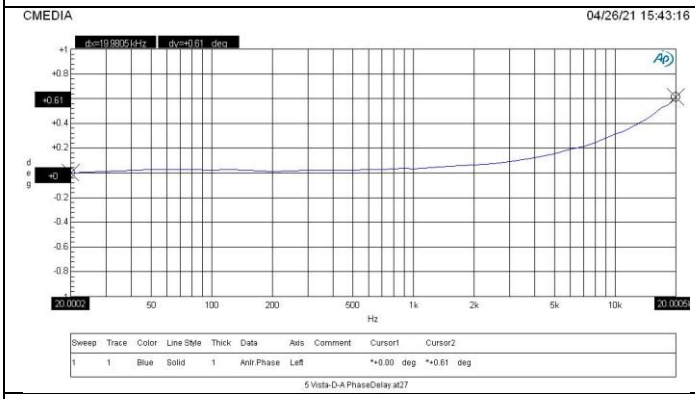
44.1K/16bits



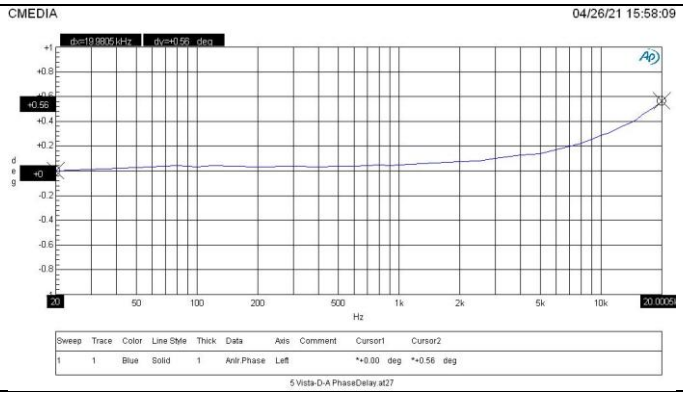
48K/16bits



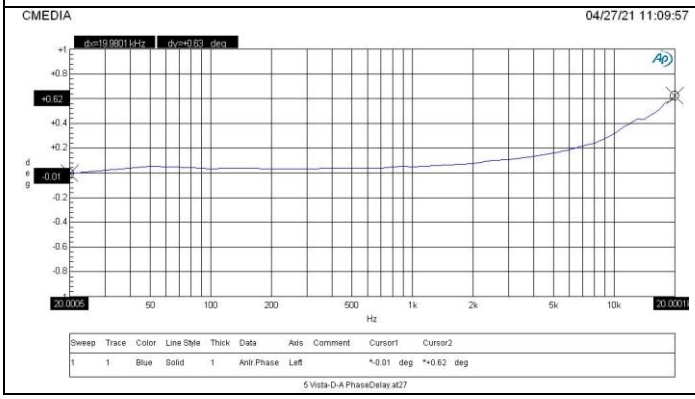
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

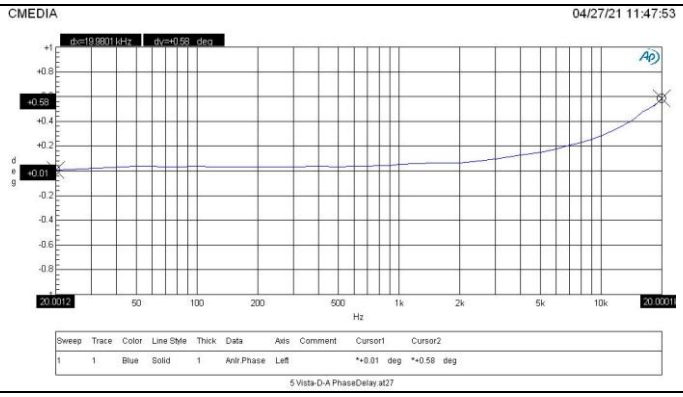
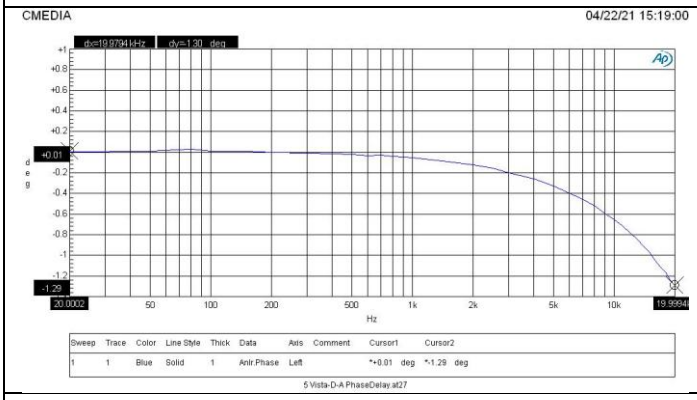
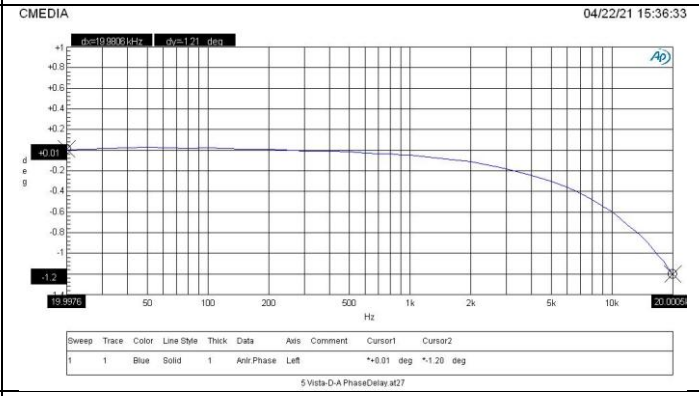


Figure 14：DAC 32Ω loading , Interchannel phase delay

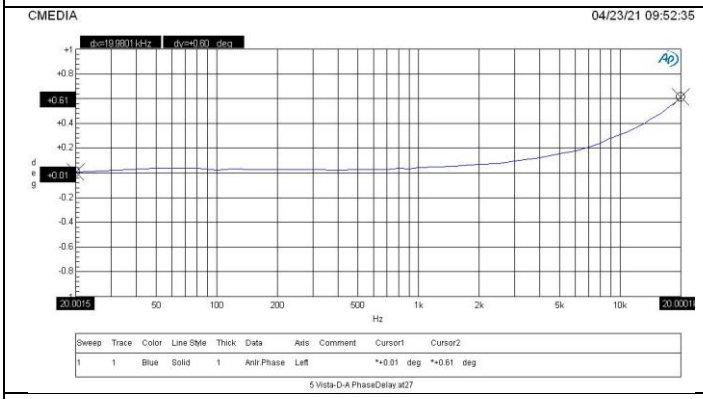
44.1K/16bits



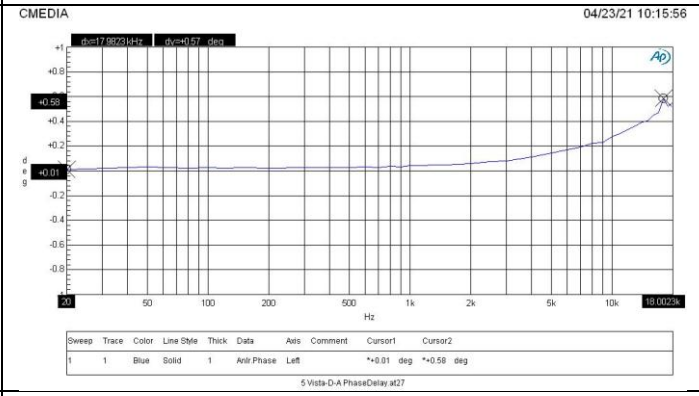
48K/16bits



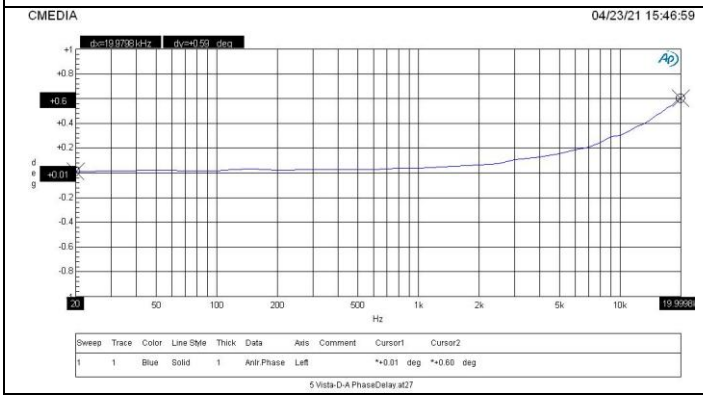
88.2K/24bits



96K/24bits



176.4K/32bits



192K/32bits

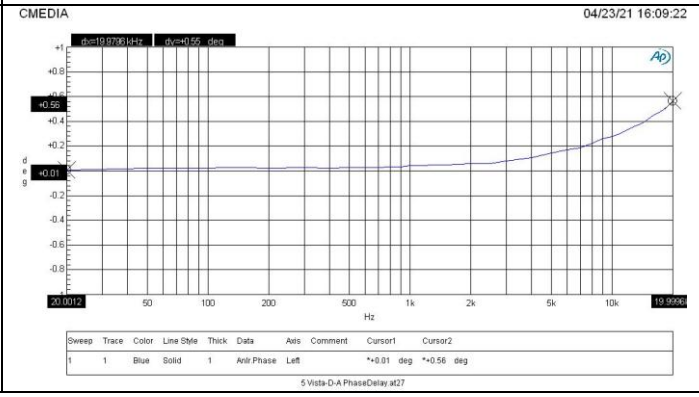
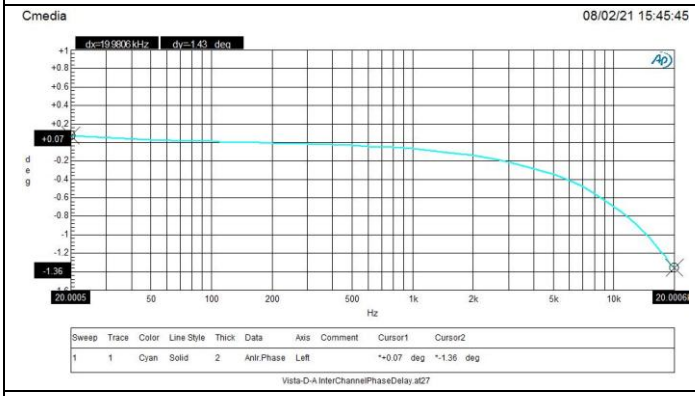
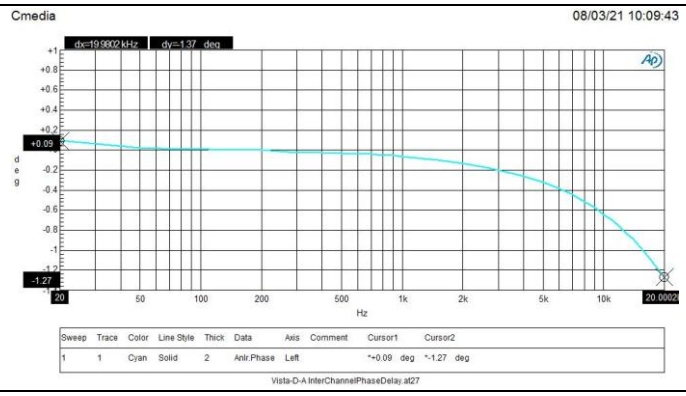


Figure 15：DAC 32Ω loading Cascade 33 Ω , Interchannel phase delay

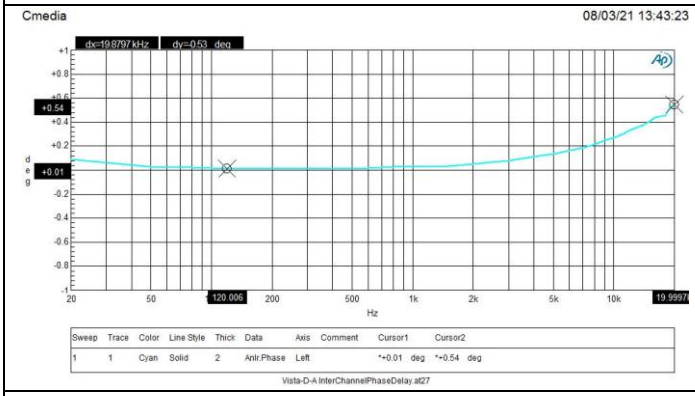
44.1K/16bits



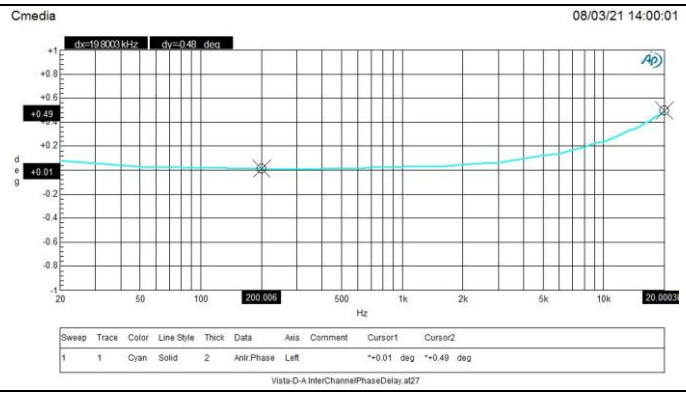
48K/16bits



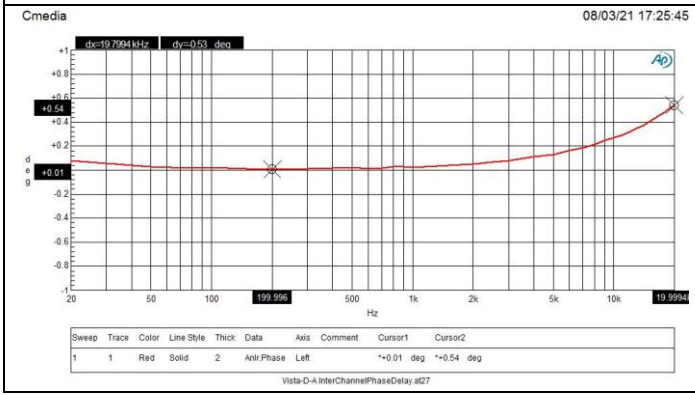
88.2K/24bits



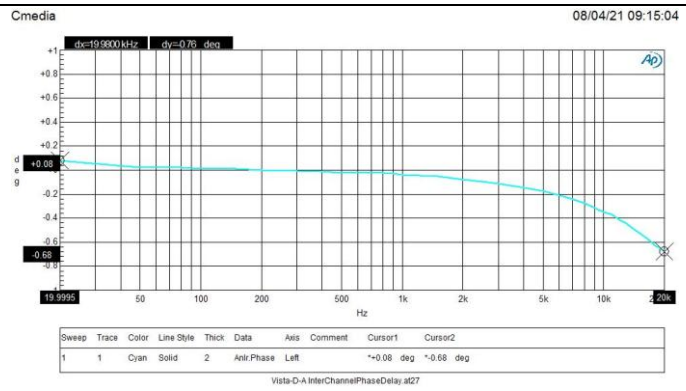
96K/24bits



176.4K/32bits



192K/32bits



8.2 ADC audio quality

TA=25℃, XD5V_XA5V = 4.3V, AGND =0V, 997Hz Sine-wave, measure bandwidth is 20Hz to 20kHz, Equalizer disable, AGC off, Mic Gain= 0dB,

Test Platform:HP EliteBook 840r G4 8G RAM , Windows 10

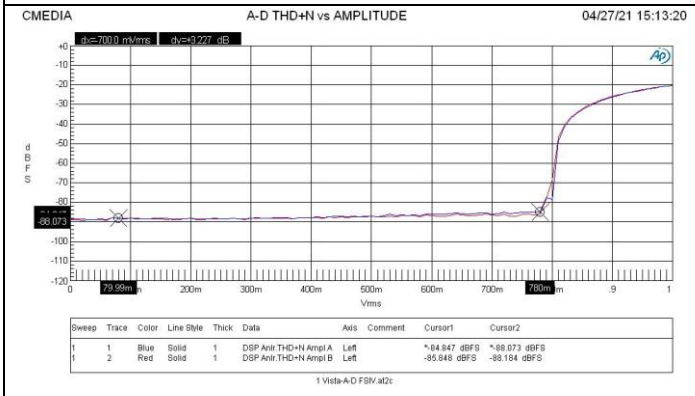
Items	Test Conditions		Test Values			Unit
			Min.	Typ.	Max.	
Full Scale Input Voltage (Fig16)	0dB Gain	48K/16bits	-	780	-	mVrms
	20dB Gain	48K/16bits	-	78	-	
Microphone Input Impedance	A-A Disable		-	20	-	K Ω
	With-A-A, Note 2		-	10	-	
THD+N With None Filter (1KHZ)	0dB Gain (Fig17)	44.1K/16bits	-	-87	-	dB
		48K/16bits	-	-87	-	
		96K/24bits	-	-88	-	
		192K/24bit	-	-90	-	
	20dB Gain (Fig18)	44.1K/16bits	-	-83	-	dB
		48K/16bits	-	-84	-	
		96K/24bits	-	-84	-	
		192K/24bit	-	-84	-	
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	0dB Gain	44.1K/16bits	-	-91.5	-	dB
		48K/16bits	-	-92.1	-	
		96K/24bits	-	-93.2	-	
		192K/24bit	-	-94.6	-	
	20dB Gain	44.1K/16bits	-	-87.5	-	dB
		48K/16bits	-	-87.4	-	
		96K/24bits	-	-87.8	-	
		192K/24bit	-	-88.0	-	
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	0dB Gain	44.1K/16bits	-	-91.6	-	dB
		48K/16bits	-	-92.4	-	
		96K/24bits	-	-93.6	-	
		192K/24bit	-	-94.8	-	
	20dB Gain	44.1K/16bits	-	-87.7	-	dB
		48K/16bits	-	-87.6	-	
		96K/24bits	-	-87.9	-	
		192K/24bit	-	-88.2	-	
Sampling Frequency Accuracy	0dB Gain	44.1K/16bits	-0.0065	-	0.0121	%
		48K/16bits	-0.0040	-	0.0092	
		96K/24bits	-0.0031	-	0.0078	
		192K/24bit	-0.0089	-	0.0043	
	20dB Gain	44.1K/16bits	-0.0016	-	0.0079	%
		48K/16bits	-0.0035	-	0.0081	
		96K/24bits	-0.0045	-	0.0074	
		192K/24bit	-0.0040	-	0.0105	

Note 2: A-A stands for Analog to Analog, it is Microphone input directly out to Headphone.

Channel Separation (L/R Cross-talk)	Sampling frequency		100	-	10K	HZ
	0dB Gain (Fig19)	44.1K/16bits	-121.0	-	-99.6	dB
		48K/16bits	-117.3	-	-97.3	
		96K/24bits	-117.2	-	-100.7	
		192K/24bit	-116.1		-103.8	
	20dB Gain (Fig20)	44.1K/16bits	-93.0	-	-57.0	dB
		48K/16bits	-94.0	-	-57.1	
		96K/24bits	-93.3	-	-57.6	
		192K/24bit	-90.4		-57.5	
Frequency Response (ref.:-20dB)	Band Edge		20	-	20K	HZ
	0dB Gain (Fig21)	44.1K/16bits	-20.3	-	-22.5	dB
		48K/16bits	-20.7	-	-21.0	
		96K/24bits	-22.1	-	-20.4	
		192K/24bit	-25.1		-20.3	
	20dB Gain (Fig22)	44.1K/16bits	-20.4	-	-24.1	dB
		48K/16bits	-20.5	-	-20.9	
		96K/24bits	-22.0	-	-20.5	
		192K/24bit	-25.2		-20.4	
Passband Ripple	0dB Gain	44.1K/16bits	-	0.23	-	dB
		48K/16bits	-	0.25	-	
		96K/24bits	-	0.25	-	
		192K/24bit	-	0.38	-	
	20dB Gain	44.1K/16bits	-	0.25	-	dB
		48K/16bits	-	0.26	-	
		96K/24bits	-	0.24	-	
		192K/24bit	-	0.20	-	
Interchannel phase delay	0dB Gain (Fig23)	44.1K/16bits	-	-0.01	-	deg
		48K/16bits	-	-0.01	-	
		96K/24bits	-	-0.07	-	
		192K/24bit	-	0.16	-	
	20dB Gain (Fig24)	44.1K/16bits	-	-0.01	-	deg
		48K/16bits	-	-0.02	-	
		96K/24bits	-	-0.06	-	
		192K/24bit	-	-0.14	-	

Figure 16：ADC Full Scale Input Voltage.

0dB 48K/16bits



20dB 48K/16bits

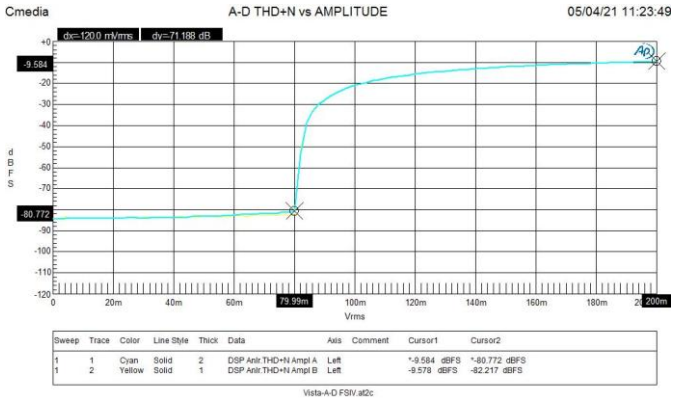
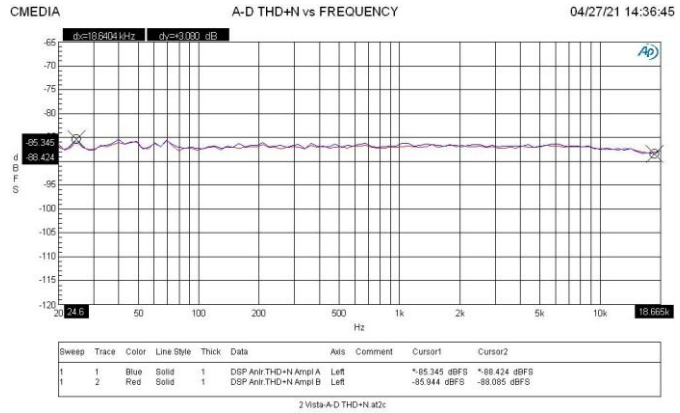
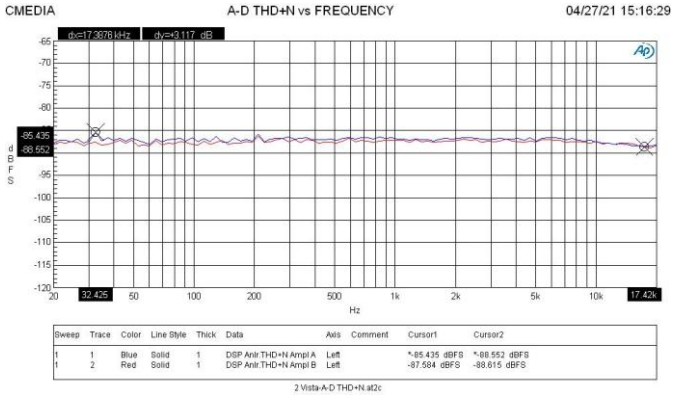


Figure 17：ADC THD+N 0dB Gain

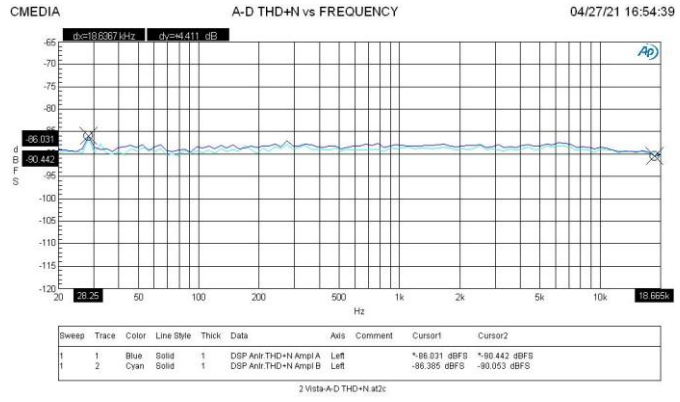
44.1K/16bits



48K/16bits



96K/24bits



192K/24bits

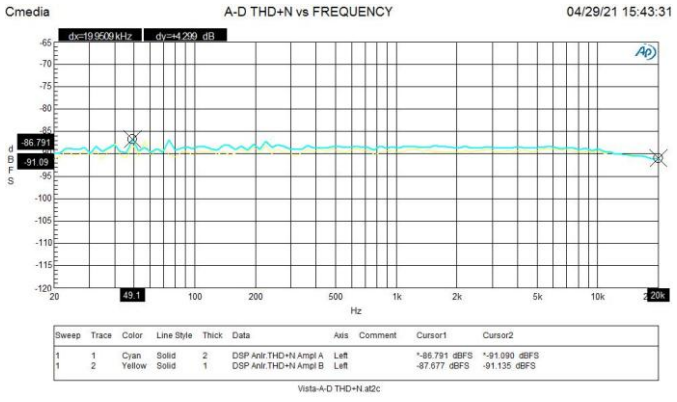


Figure 18：ADC THD+N 20dB Gain

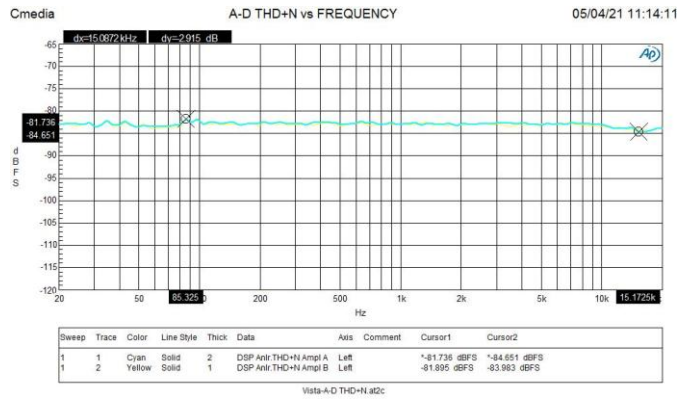
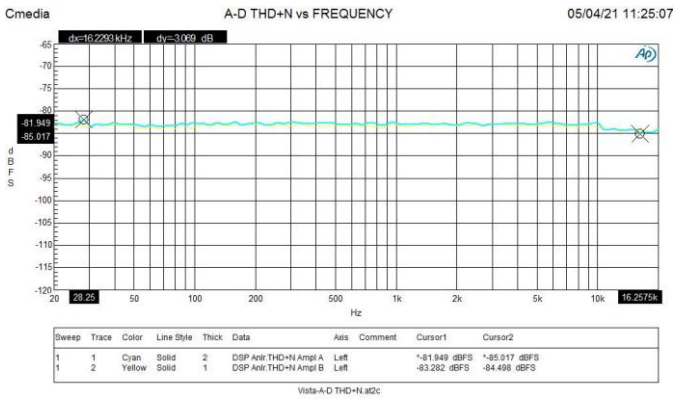
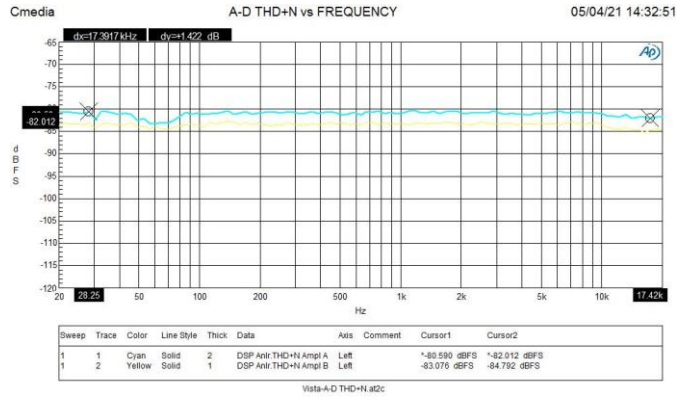
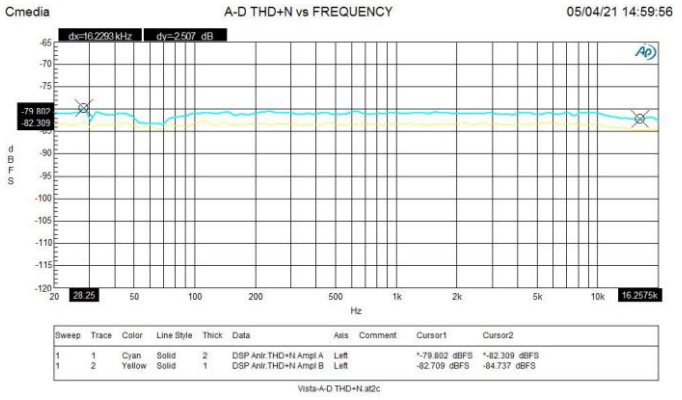
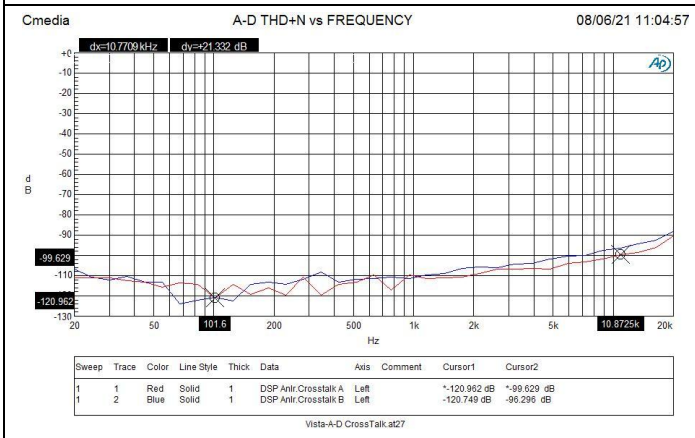
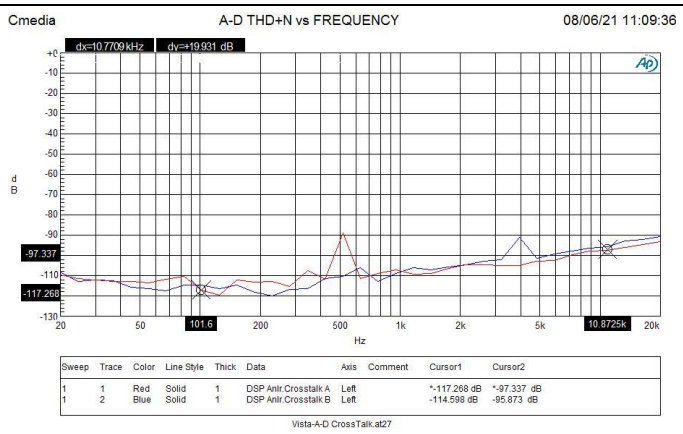
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 19：ADC Cross-talk 0dB Gain

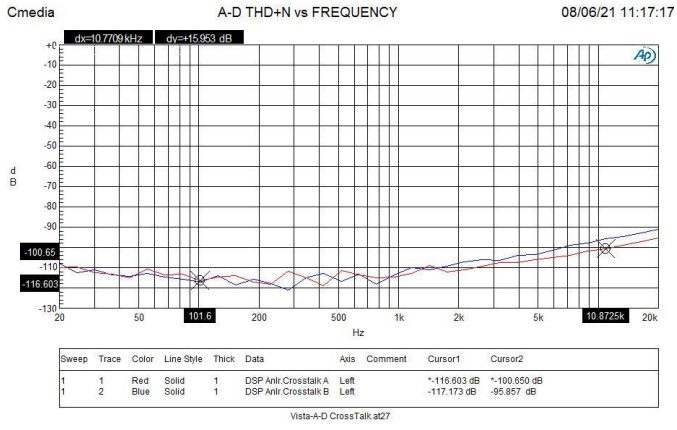
44.1K/16bits



48K/16bits



96K/24bits



192K/24bits

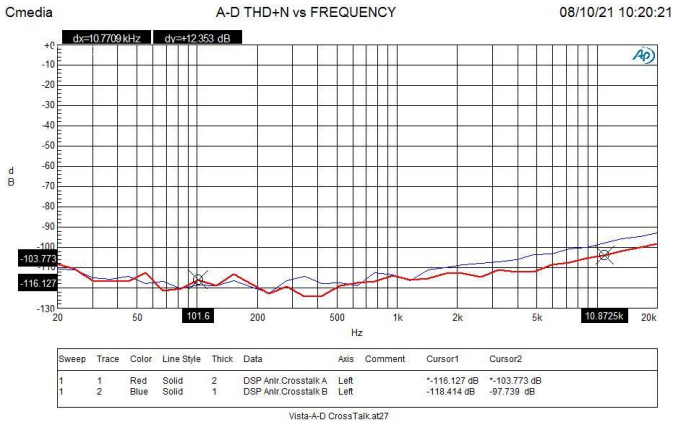
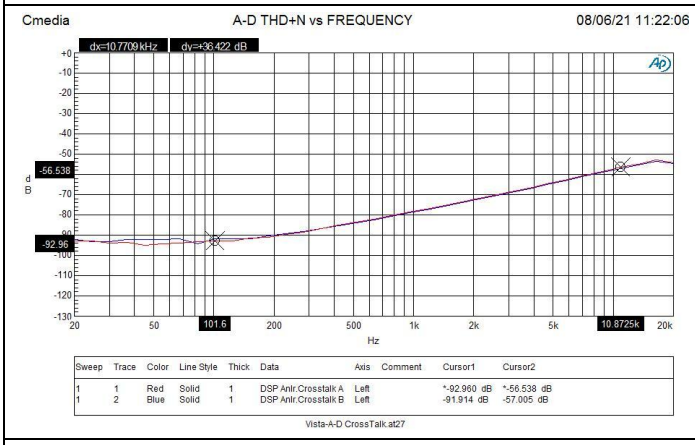
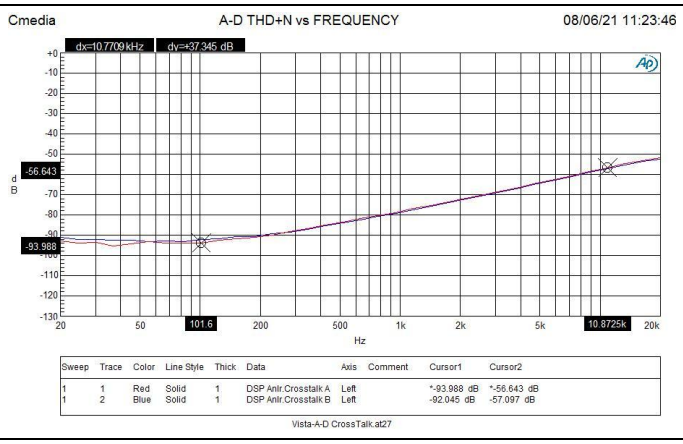


Figure 20：ADC Cross-talk 20dB Gain

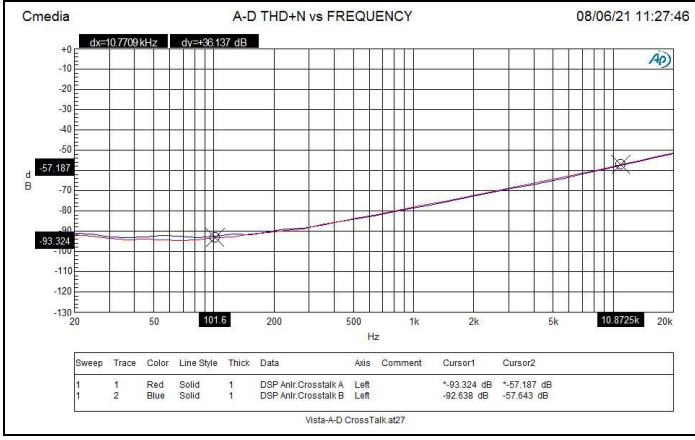
44.1K/16bits



48K/16bits



96K/24bits



192K/24bits

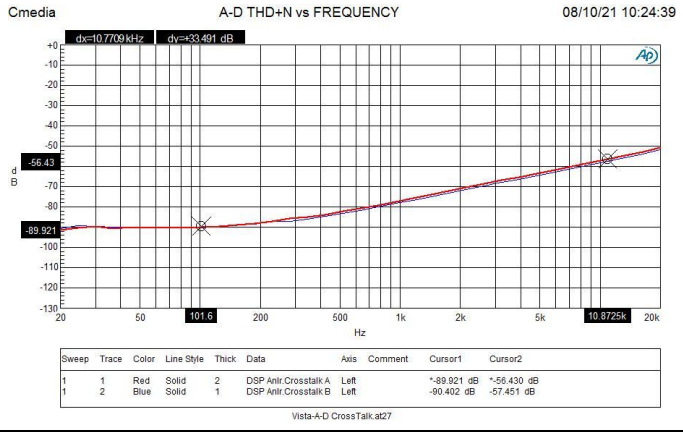


Figure 21：ADC Frequency Response 0dB Gain

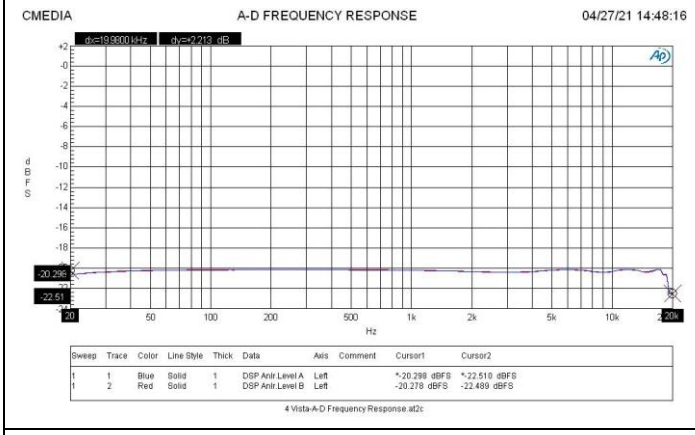
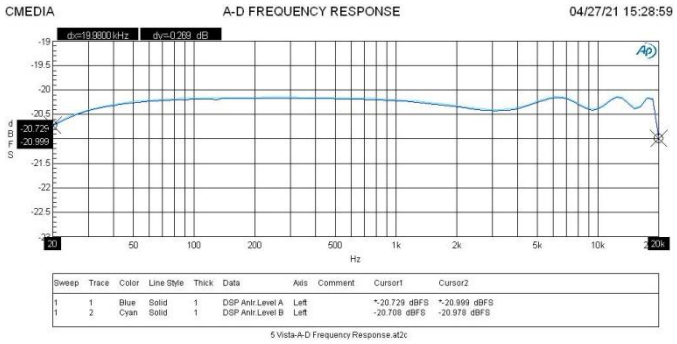
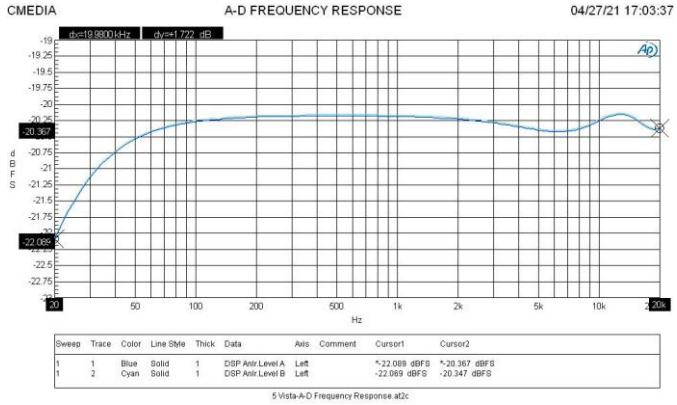
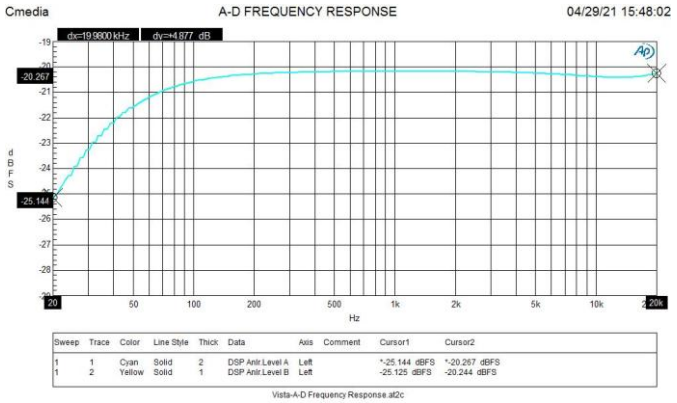
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 22：ADC Frequency Response 20dB Gain

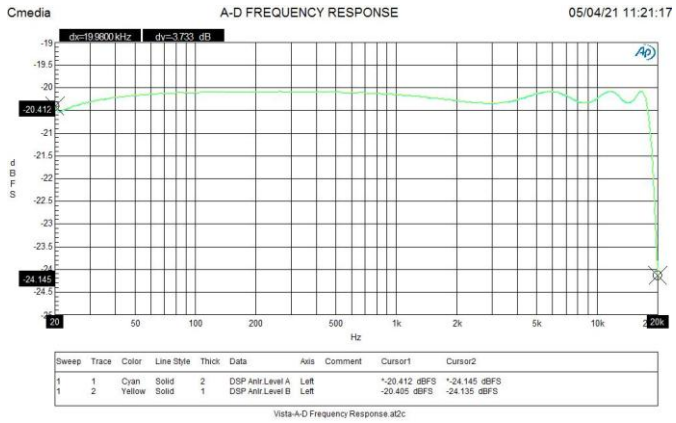
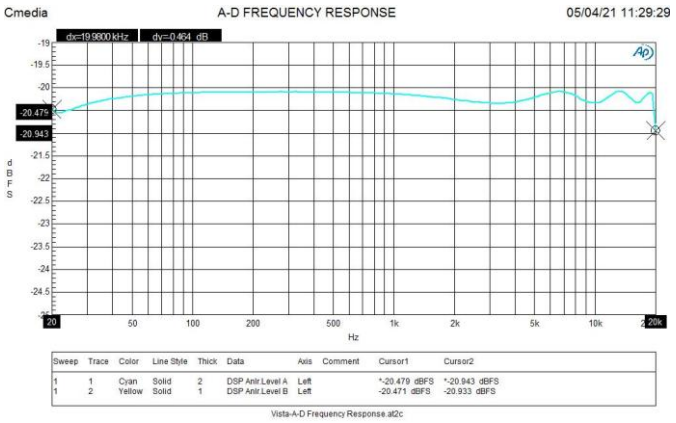
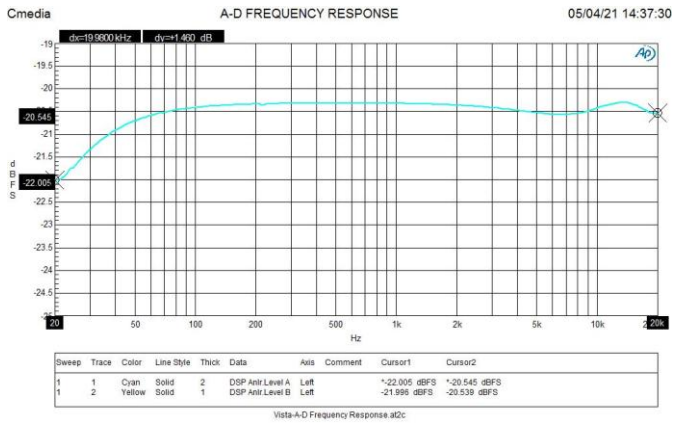
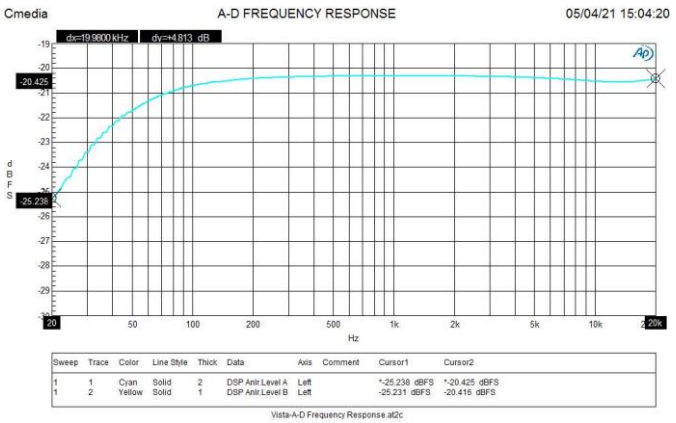
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 23：ADC Interchannel phase delay 0dB Gain

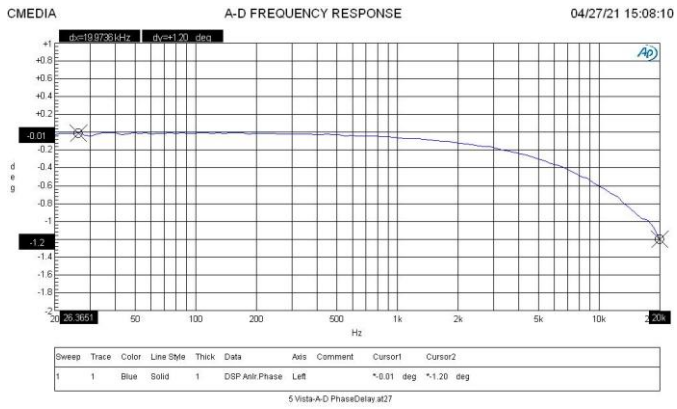
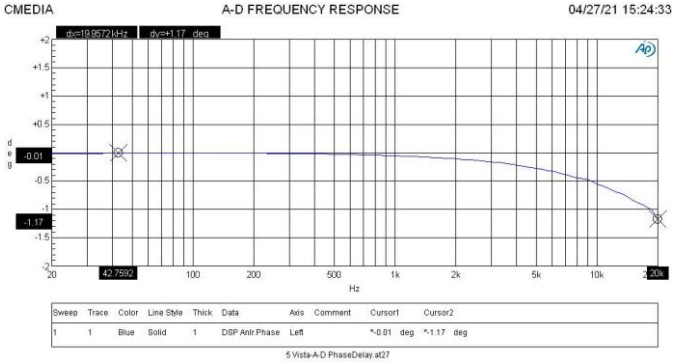
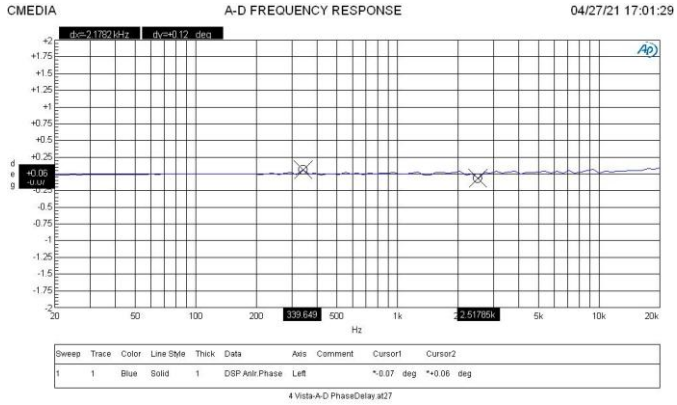
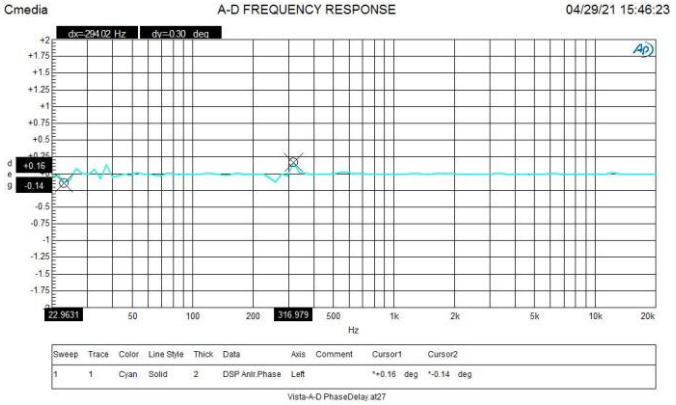
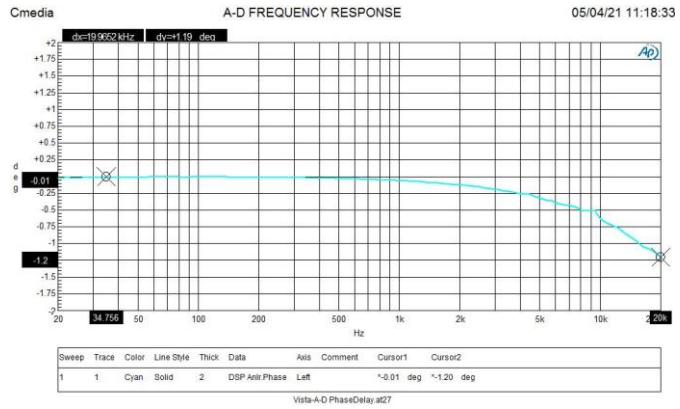
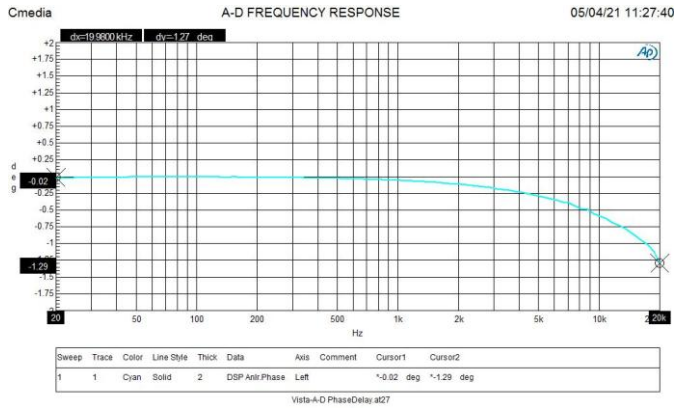
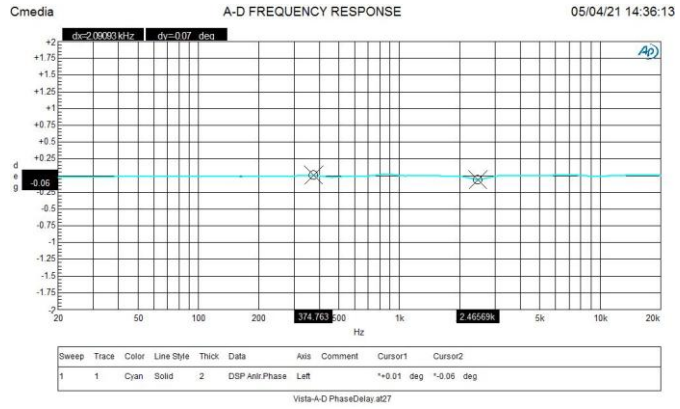
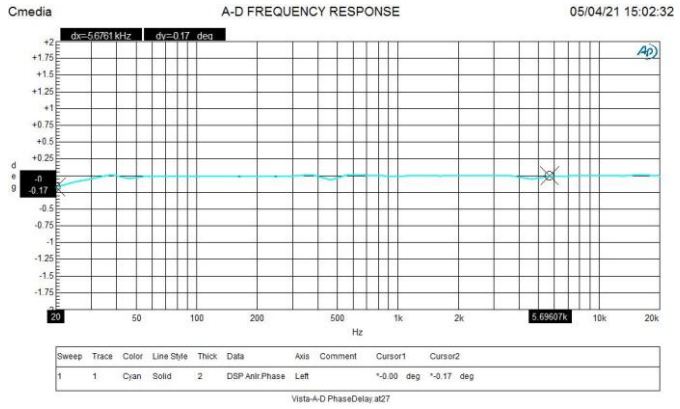
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 24：ADC Interchannel phase delay 20dB Gain

44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

8.3 Analog Monitoring / Side tone (A-A) path audio quality

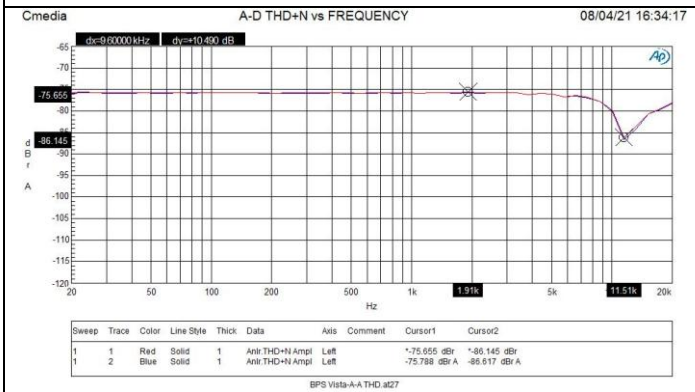
TA=25℃, XD5V_XA5V = 4.3V, AGND =0V, Microphone-In to Headphone-Out, 32ohms loading, Master Volume=0dB, Mic Gain=0dB, Typical Fs/Bit-depth=48KHz/24bit,

Test Platform:HP EliteBook 840r G4 8G RAM , Windows 10

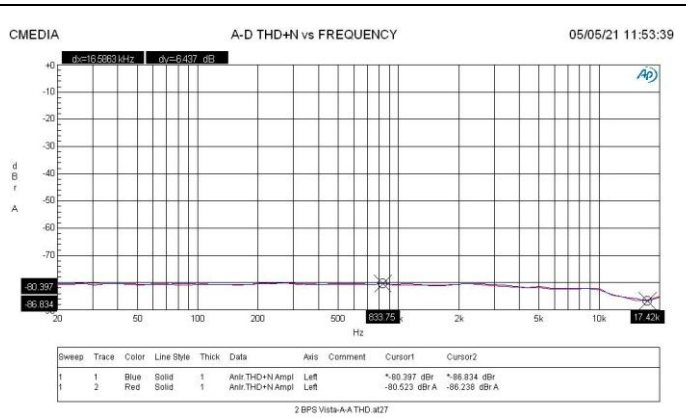
Items	Test Conditions		Test Values			Unit
			Min.	Typ.	Max.	
Full Scale Output Voltage	10KΩ loading		-	1060	-	mVrms
	32Ω loading		-	1030	-	
	32Ω loading with 33 ohm cascade		-	493	-	
THD+N With None Filter (Fig25)	10KΩ loading	0dBFS	-	-86.6	-	dB
		-3dBFS	-	-86.8	-	
	32Ω loading	0dBFS	-	-84.1	-	dB
		-3dBFS	-	-83.2	-	
	32Ω loading Cascade 33 ohm	0dBFS	-	-84.7	-	dB
		-3dBFS	-	-84.5	-	
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	10KΩ loading		-	-89.8	-	dB
	32Ω loading		-	-86.8	-	
	32Ω loading, Cascade 33 ohm		-	-81.5	-	
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	10KΩ loading		-	-89.9	-	dB
	32Ω loading		-	-86.9	-	
	32Ω loading, Cascade 33 ohm		-	-81.7	-	
Channel Separation (Cross-talk) (Fig26)	Sampling frequency		100	-	10K	HZ
	10KΩ loading		-96.9	-	-90.8	dB
	32Ω loading		-63.0	-	-64.8	
	32Ω loading, Cascade 33 ohm		-68.2	-	-68.0	
Frequency Response (ref.:-20dB) (Fig27)	Band Edge		20	-	20K	HZ
	10KΩ loading,		-20.1	-	-20.1	dB
	32Ω loading		-23.5	-	-22.2	
	32Ω loading, Cascade 33 ohm		-20.0	-	-21.0	
Passband Ripple	10KΩ loading		-	0.07	-	d
	32Ω loading		-	0.05	-	
	32Ω loading, Cascade 33 ohm		-	0.127	-	
Inter-Channel Phase Delay (Fig28)	10KΩ loading		-	0.03	-	deg
	32Ω loading		-	0.02	-	
	32Ω loading, Cascade 33 ohm		-	0.01	-	
Sampling Frequency Accuracy	10KΩ loading		-0.0114	-	0.0196	%
	32Ω loading		-0.0068	-	0.0078	
	32Ω loading, Cascade 33 ohm		-0.0059	-	0.0042	

Figure 25：A-A THD+N

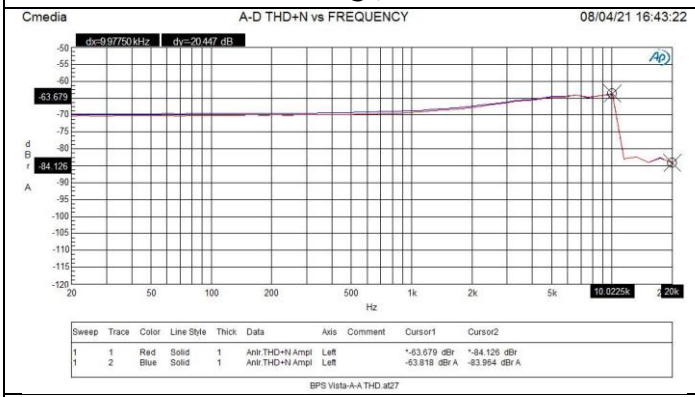
10KΩ loading ,0dB Gain



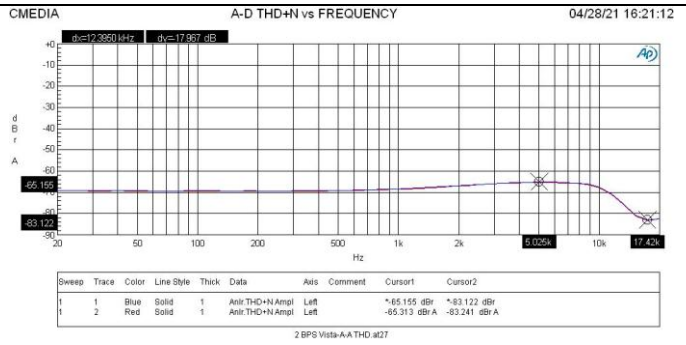
10KΩ loading ,-3dB Gain



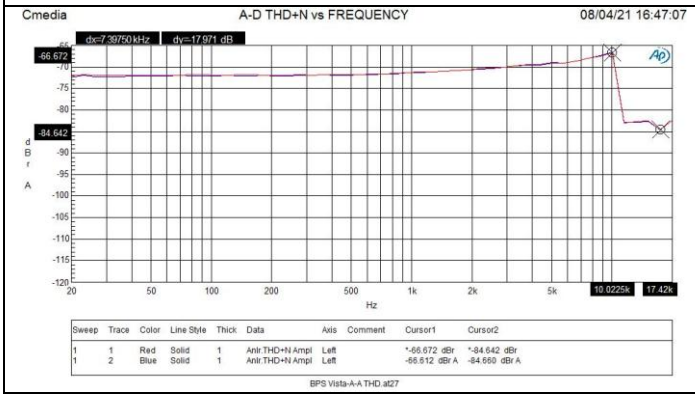
32Ω loading ,0dB Gain



32Ω loading ,-3dB Gain



32Ω loading loading Cascade 33Ω,0dB Gain



32Ω loading loading Cascade 33Ω,-3dB Gain

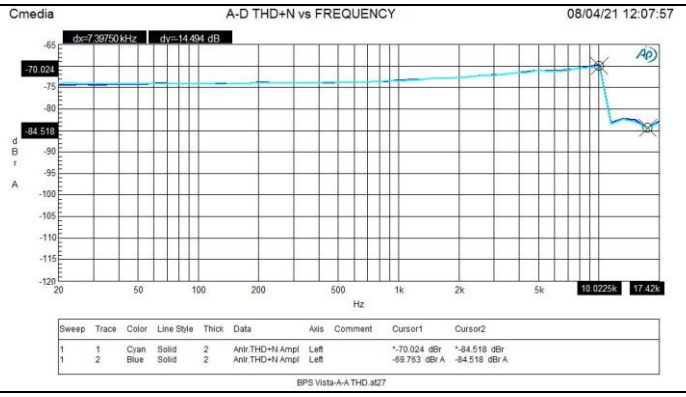


Figure 26：A-A Cross-talk

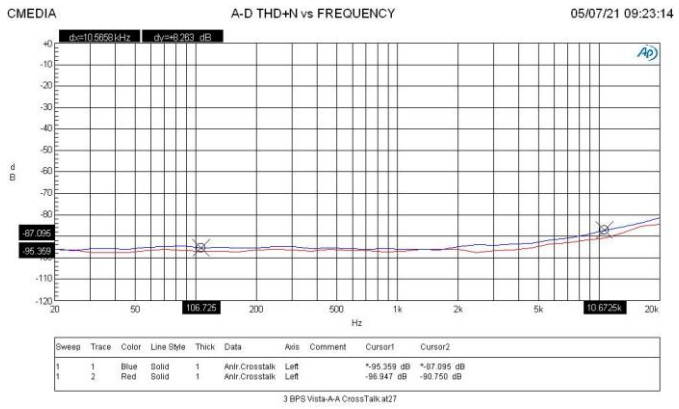
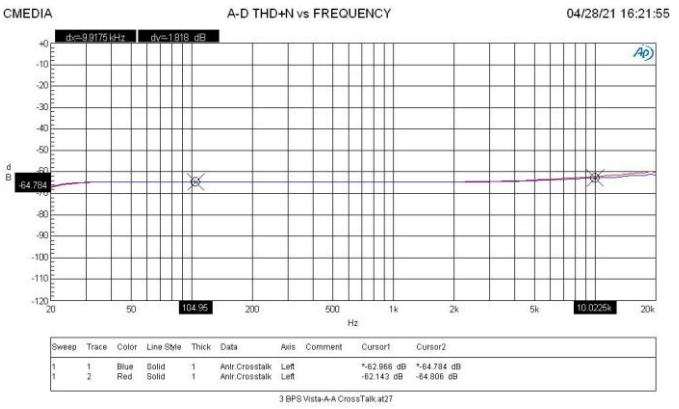
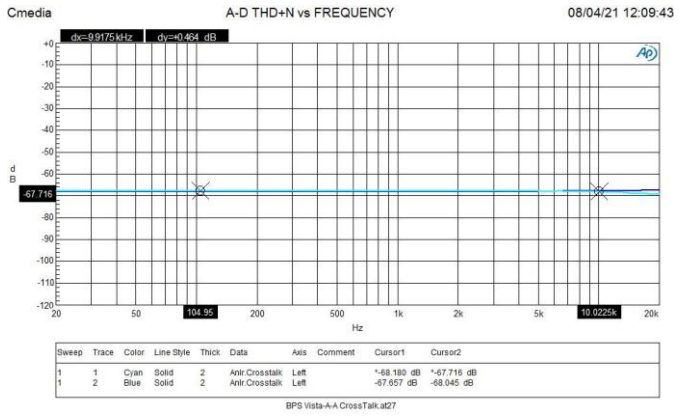
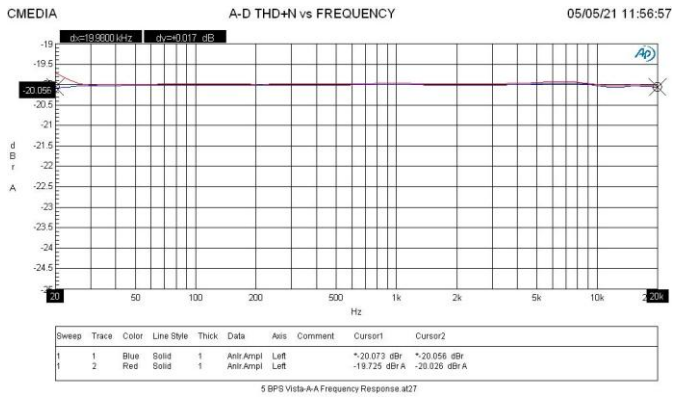
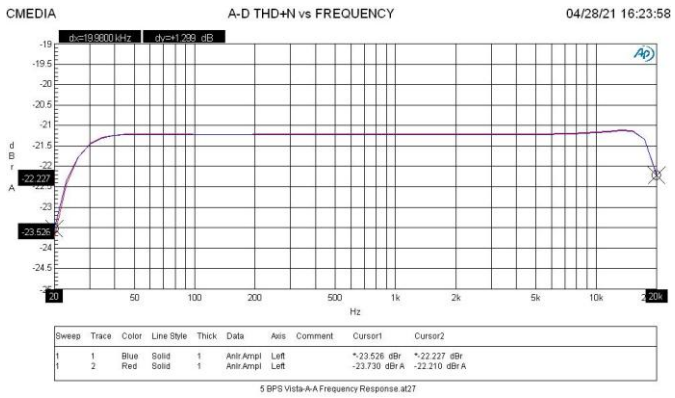
10KΩ loading	32Ω loading
	
32Ω loading loading Cascade 33 Ω	
	

Figure 27：A-A Frequency Response (ref.:-20dB)

10KΩ loading



32Ω loading



32Ω loading loading Cascade 33 Ω

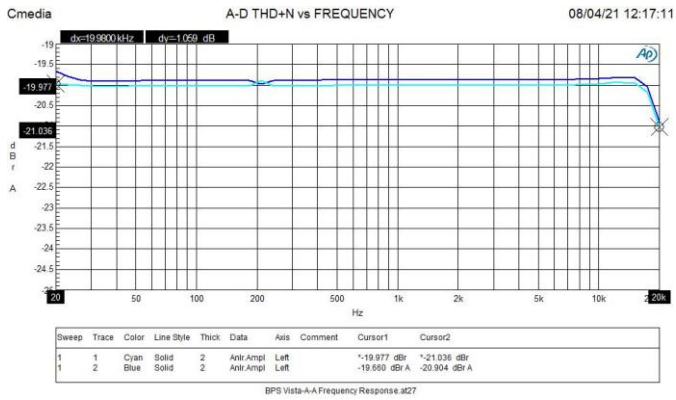
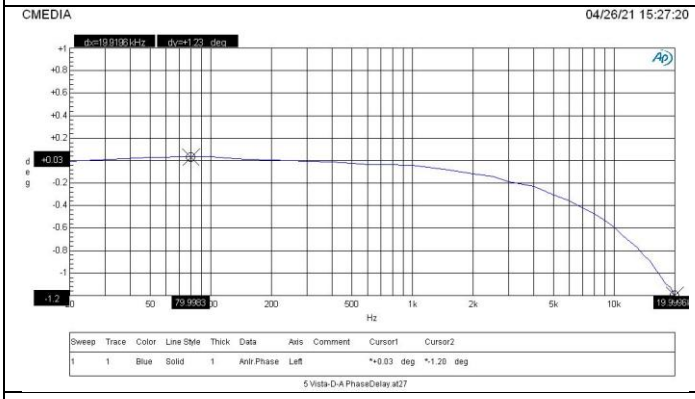
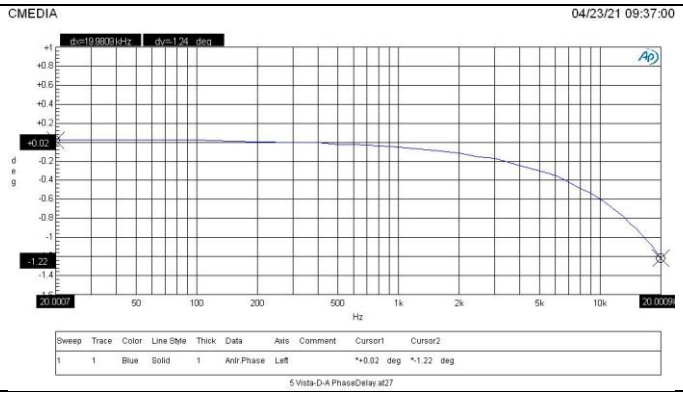
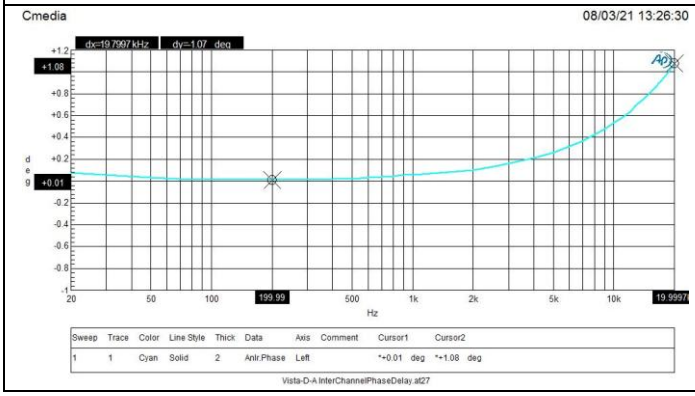
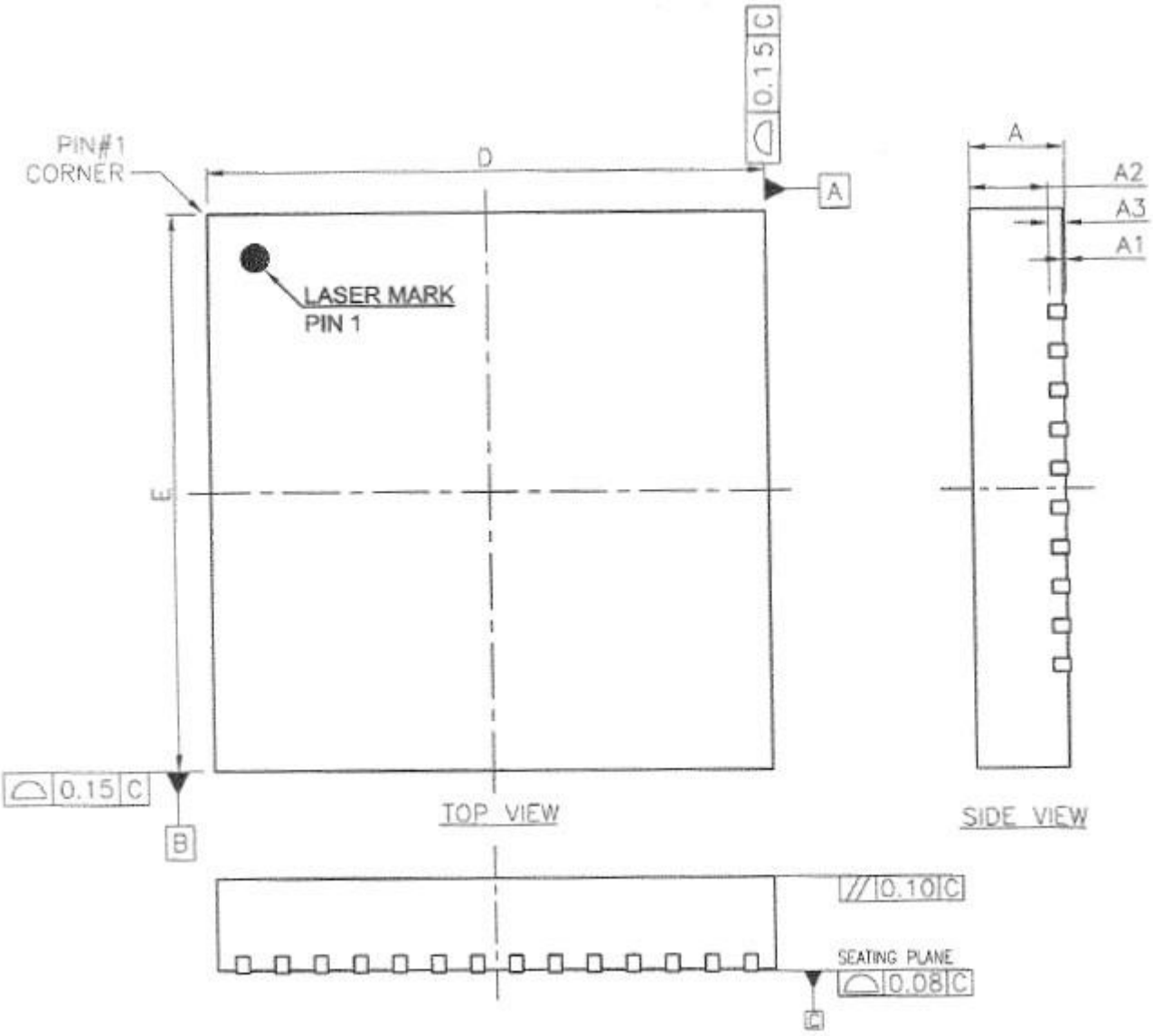


Figure 28：AA Inter-Channel Phase Delay

10KΩ loading	32Ω loading
	
32Ω loading loading Cascade 33 Ω	
	

9 Package Dimensions

9.1 QFN48 5mm x 5mm (10-14-10-14)

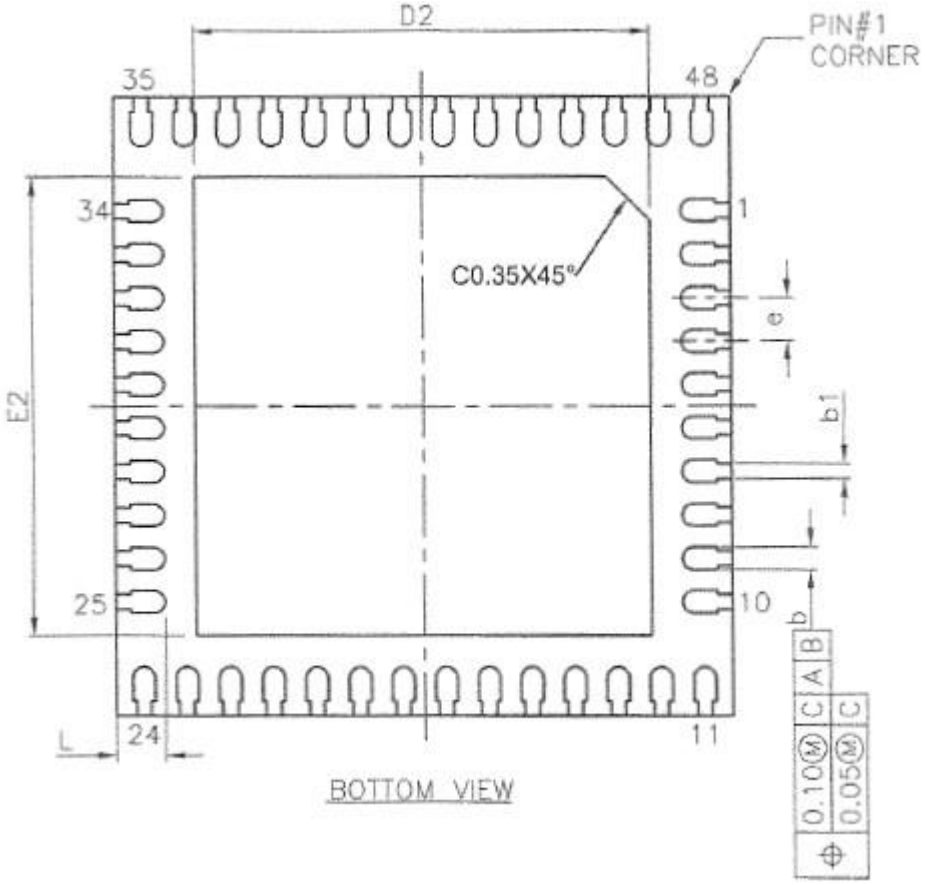


Top View

	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.65	0.70	0.75
Lead thickness	A3	0.15 REF.		
Body size	D	4.95	5.00	5.05
	E	4.95	5.00	5.05
Lead width	b	0.13	0.18	0.23
	b1	0.07	0.12	0.17
Exposed pad width	D2	3.65	3.70	3.75
Exposed pad length	E2	3.65	3.70	3.75
Lead pitch	e	0.35 BSC		
Lead length	L	0.35	0.40	0.45
Lead count	N	48L		

9.2 Recommended Land Pattern

PCB land pattern is recommended to fit the dimensions of the pad, please use the maximum value of the dimensions as reference for PCB layout. The dimensions for the ground plane are D2 by E2.



Symbol	Dimensions in mm		
	Minimum	Normal	Maximum
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
e		0.35 BSC	

Pad Size	Dimensions in mm		
	Minimum	Normal	Maximum
D2	3.65	3.70	3.75
E2	3.65	3.70	3.75
L	0.35	0.40	0.45

— End of Datasheet —

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