DS25M4AB

1.8V 128M-BIT

Serial Flash Memory with 4KB Sectors, Dual and Quad I/O SPI & QPI

Documents title

128M bit Serial Flash Memory with 4KB Sectors, Dual and Quad I/O SPI &QPI

Revision History

Revision No.	History	Draft date	Release date	Remark
0.0	Initial Draft	Sep.10.2018	Sep.12.2018	Preliminary
0.1	DTR read option change	Sep.17.2018	Sep.19.2018	
0.2	Modify some formats	Sep.17.2019	Sep.18.2019	
0.3	Modify P/N to keep consistent with others	Dec.03.2019	Dec.05.2019	
0.4	Typo Correction and Modified Driver Strength	Apr.03.2020	Apr.06.2020	
0.5	Add WLCSP PKG type	Sep.03.2020	Sep.05.2020	
0.6	Update PWR Up Timing	Oct.20.2020	Oct.22.2020	
0.7	Update WLCSP ball diameter etc	Mar.24.2021	Mar.25.2021	
0.8	Update LC bits setting & dummy description of DTR Read instruction	Jun.03.2021	Jun.07.2021	
0.9	Update tRES and align the max frequency	Jul. 06. 2021	Jul.10.2021	
1.0	Add automotive grade1 P/N and BGA24 pkg info	Dec. 05. 2022	Dec.08.2022	

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1. GENERAL DESCRIPTIONS

The DS25M4AB (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25M series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.65V to 1.95V power supply with current consumption as low as 13mA active and 1µA for power-down. All devices are offered in space- saving packages.

The DS25M4AB array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The DS25M4AB has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The DS25M4AB support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI) as well as Double Transfer Rate(DTR) : Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 216MHz for Dual I/O and 432 for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SPI Flash Memories**
  – DS25M4AB: 128M-bit / 16M-byte
  – Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  – Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  – Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  – QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  – Quad/QPI DTR(Double Transfer Rate) Read
- **Highest Performance Serial Flash**
  – 104MHz Single, Dual/Quad SPI clocks
  – More than 100,000 erase/program cycles
  – More than 20-year data retention
  – Burst Read with 8/16/32/64 Byte Wrap
- **Efficient “Continuous Read” and QPI Mode**
  – Continuous Read with 8/16/32/64-Byte Wrap
  – Quad Peripheral Interface (QPI) reduces instruction overhead
  – Allows true XIP (execute in place) operation
- **High performance program/erase speed**
  – Page program time: 0.7ms typical
  – Sector erase time: 50ms typical
  – 32KB Block erase time 150ms typical
  – 64KB Block erase time 300ms typical
  – Chip erase time: 40 seconds typical
- **Low Power Consumption**
  – Full voltage range: 1.65-1.95V
  – 18 mA maximum active read current
  – 20 µA maximum Deep power down current
- **Wide Temperature Range**
  – -40°C to +85°C operating range
  – -40°C to +125°C operating range
- **Flexible Architecture with 4KB sectors**
  – Uniform Sector/Block Erase (4K/32K/64K-Byte)
  – Program 1 to 256 byte per programmable page
  – Erase/Program Suspend & Resume
- **Advanced Security Features**
  – Software and Hardware Write-Protect
  – Power Supply Lock-Down and OTP protection
  – Top/Bottom, Complement array protection
  – 64-Bit Unique ID for each device
  – Support Serial Flash Discoverable Parameters (SFDP) signature
  – 3 sets of OTP lockable 256 byte security pages
  – Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  – 8-pin SOP 208-mil
  – 8-pad WSON 6x5-mm
  – 8-pin WLCSP
  – Contact Dosilicon for KGD and other options

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1. Pin Configuration SOP 208-mil

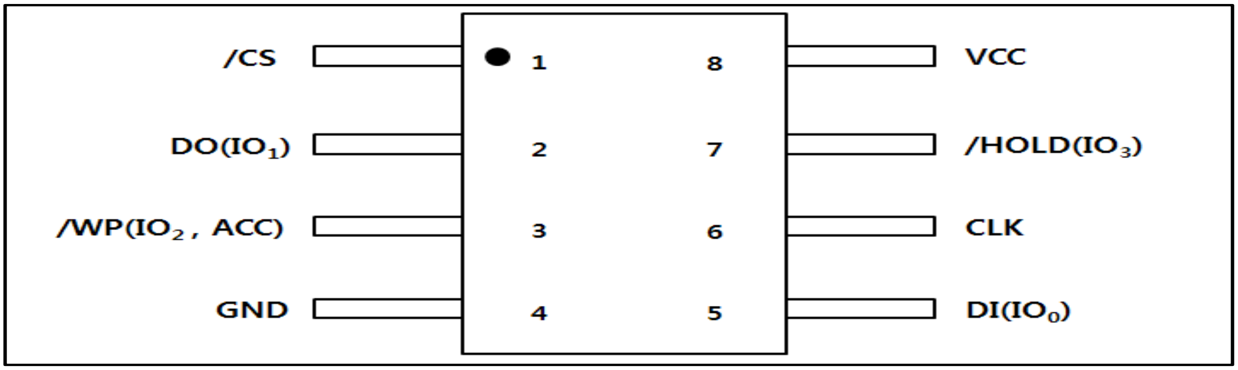

Figure 1a. DS25M4AB Pin Assignments, 8-pin SOP 208-mil

3.2. Pad Configuration WSON 6x5-mm

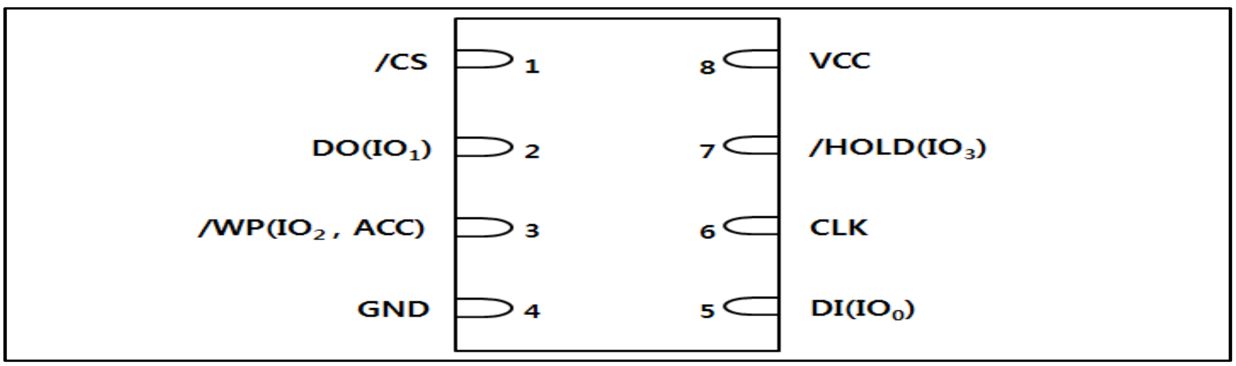

Figure 1b. DS25M4AB Pad Assignments, 8-pad WSON 6x5-mm

3.3. Pin Configuration 16Ball WLCSP(8 NC pins and 8 function pins inside)

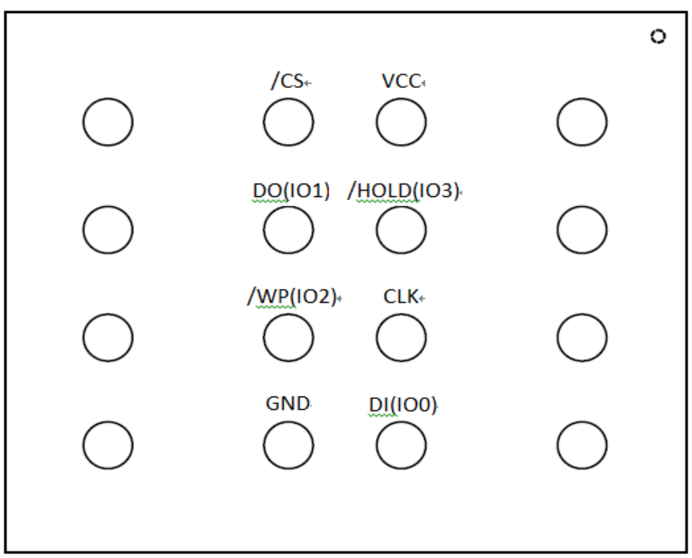

Figure 1c. DS25M4AB Pad Assignments, 16Ball WLCSP(Bottom View)

3.4. Pin Description SOP 208-mil, WSON 6x5-mm, WLCSP

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1. Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 44). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2. Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The DS25M4AB supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3. Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-b for the pin configuration of Quad I/O operation.

4.4. HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-b for the pin configuration of Quad I/O operation.

4.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6. Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration.

5. BLOCK DIAGRAM

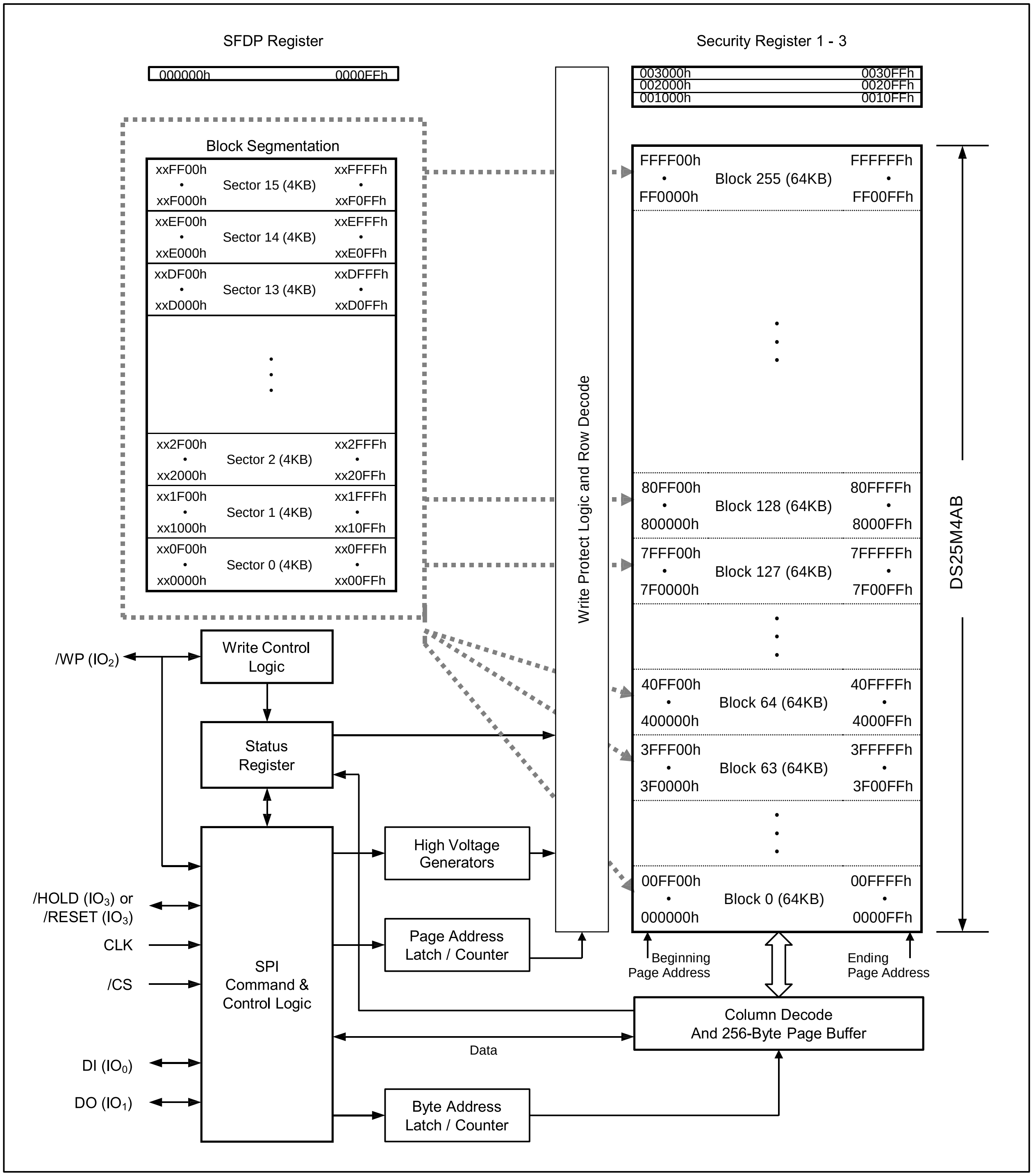

Figure 2. DS25M4AB Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1. SPI / QPI Operations

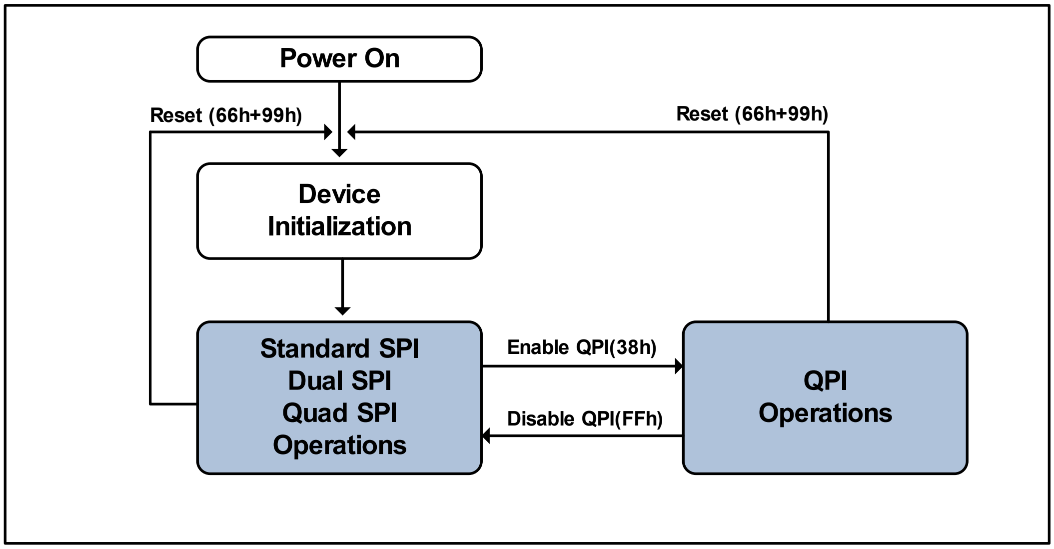

Figure 3. DS25M4AB Serial Flash Memory Operation Diagram

6.1.1. Standard SPI Instructions

The DS25M4AB is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2. Dual SPI Instructions

The DS25M4AB supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

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6.1.3. Quad SPI Instructions

The DS25M4AB supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, and “Word Read Quad I/O (E7h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non- volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4. QPI Instructions

The DS25M4AB supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

6.1.5. Quad / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, DS25M4AB introduces multiple DTR (Double Transfer Rate) Read instructions that support Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

6.1.6. Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the DS25M4AB operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.7. Software Reset & Hardware /RESET pin

The DS25M4AB can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the reset period.

For the WSON-8 package type, DS25M4AB can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (t_{RESET}*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (t_{RESET}*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.

6.2. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the DS25M4AB provides several means to protect the data from inadvertent writes.

6.2.1. Write Protect Features

- Device resets when V_{CC} is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

* Note: This feature is available upon special order. Please contact Dosilicon for details.

Upon power-up or at power-down, the DS25M4AB will maintain a reset condition while V_{CC} is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 44). While reset, all operations are disabled and no instructions are recognized. During power-up and after the V_{CC} voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the V_{CC} supply level at power-up until the V_{CC}-min level and t_{VSL} time delay is reached, and it must also track the V_{CC} supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Deep Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for DS25M4AB. The Read Status Register- 1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, output driver strength and power- up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1. Status Registers

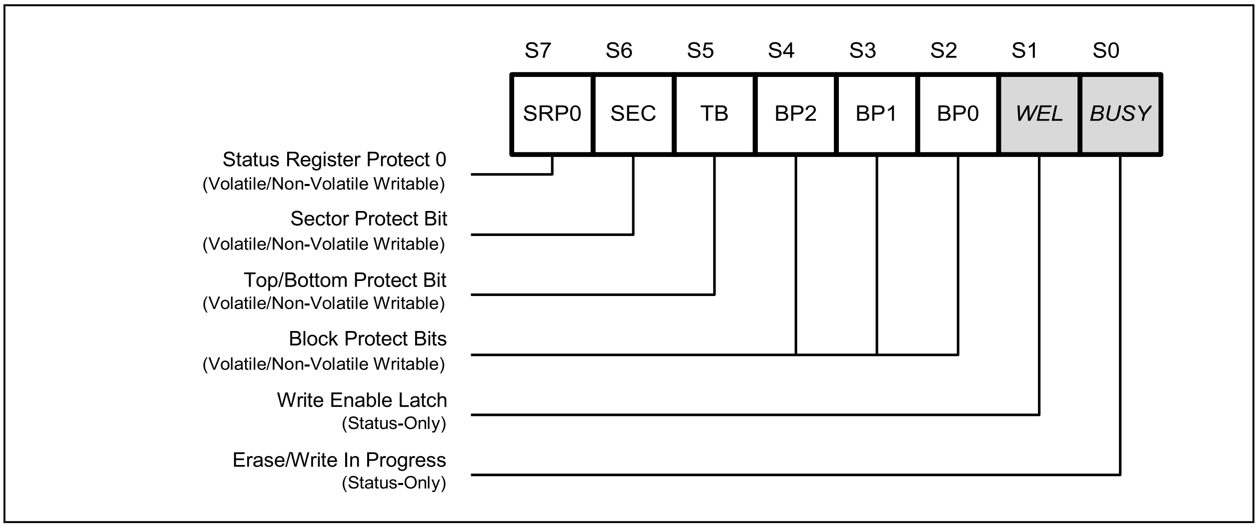

Figure 4a. Status Register-1

7.1.1. Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2. Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3. Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4. Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

7.1.5. Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6. Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7. Status Register Protect (SRP1, SRP0) – *Volatile/Non-Volatile Writable*

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available upon special order. Please contact Dosilicon for details.

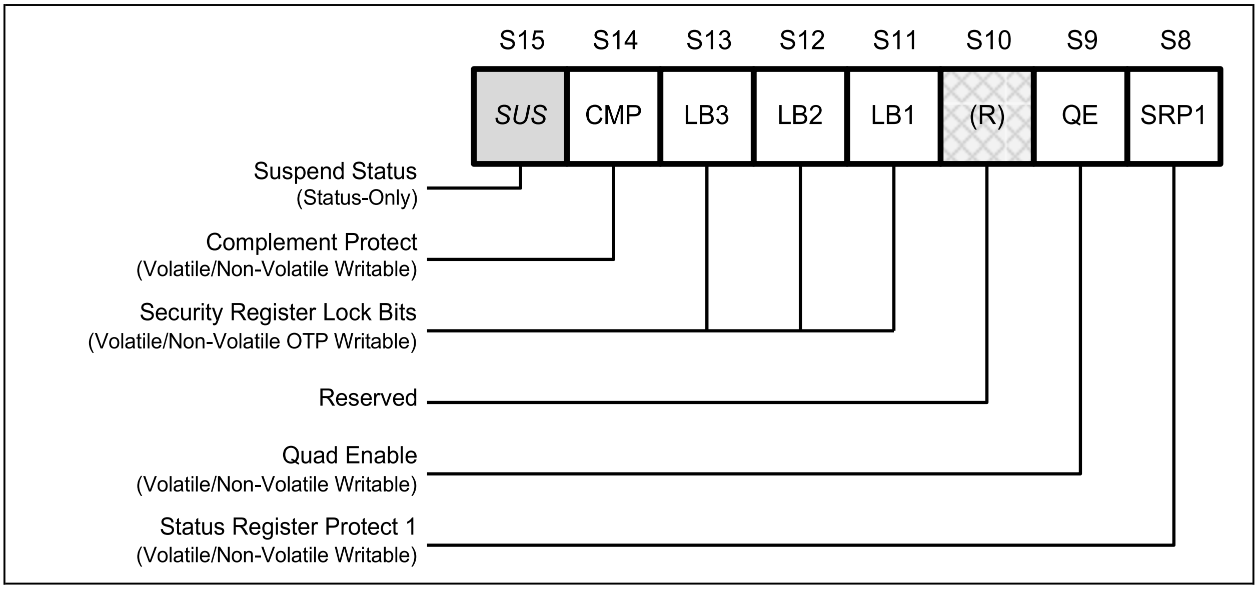

Figure 4b. Status Register-2

7.1.8. Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9. Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.10. Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state, the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored.

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

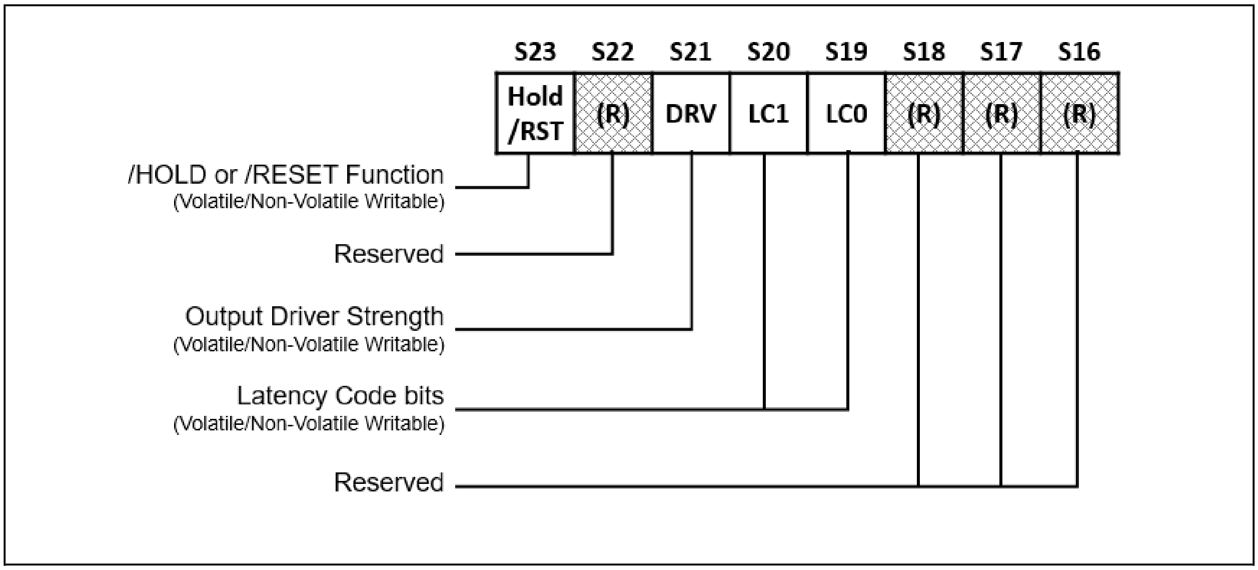

Figure 4c. Status Register-3

7.1.11. Output Driver Strength (DRV) – *Volatile/Non-Volatile Writable*

The DRV bit is used to determine the output driver strength for the Read operations.

DRV	Driver Strength
0	100%(Default)
1	75%

7.1.12. /HOLD or /RESET Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

7.1.13. Latency Code Bits (LC1, LC0) – Volatile/Non-Volatile Writable

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for DTR read command(EDh).

LC1, LC0	Dummy clock cycles	Quad ID DTR Read (MHz)
00 (default)	6	66
01	4	40
10	8	66
11	10	66

7.1.14. Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.1.15. DS25M4AB Status Register Memory Protection (CMP = 0)

STATUS REGISTER(1)					DS25M4AB (128M-BIT) MEMORY PROTECTION(3)			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h – FFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h – FFFFFFh	4KB	U - 1/4096
1	0	0	1	0	255	FFE000h – FFFFFFh	8KB	U - 1/2048
1	0	0	1	1	255	FFC000h – FFFFFFh	16KB	U - 1/1024
1	0	1	0	X	255	FF8000h – FFFFFFh	32KB	U - 1/512
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/4096
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/2048
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/1024
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/512

Notes:

1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

7.1.16. DS25M4AB Status Register Memory Protection (CMP = 1)

STATUS REGISTER[1]					DS25M4AB (128M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	0 thru 255	000000h - FFFFFFh	16MB	ALL
0	0	0	0	1	0 thru 251	000000h - FBFFFFh	16,128KB	Lower 63/64
0	0	0	1	0	0 thru 247	000000h – F7FFFFh	15,872KB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h - EFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h - DFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h - BFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h - 7FFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h - FFFFFFh	16,128KB	Upper 63/64
0	1	0	1	0	8 thru 255	080000h - FFFFFFh	15,872KB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h - FFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h - FFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h - FFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h - FFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 255	000000h – FFEFFFh	16,380KB	L - 4095/4096
1	0	0	1	0	0 thru 255	000000h – FFDFFFh	16,376KB	L - 2047/2048
1	0	0	1	1	0 thru 255	000000h – FFBFFFh	16,368KB	L - 1023/1024
1	0	1	0	X	0 thru 255	000000h – FF7FFFh	16,352KB	L - 511/512
1	1	0	0	1	0 thru 255	001000h – FFFFFFh	16,380KB	U - 4095/4096
1	1	0	1	0	0 thru 255	002000h – FFFFFFh	16,376KB	U - 2047/2048
1	1	0	1	1	0 thru 255	004000h – FFFFFFh	16,368KB	U -1023/1024
1	1	1	0	X	0 thru 255	008000h – FFFFFFh	16,352KB	U - 511/512

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the DS25M4AB consists of 41 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the DS25M4AB consists of 28 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 43. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1. Device ID and Instruction Set Tables

8.1.1. Manufacturer and Device Identification

		ID code	Instruction
Manufacturer ID	Dosilicon	E5h	90h, 92h, 94h, 9Fh
Device ID	DS25M4AB	17h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	42h	9Fh
Capacity Type ID	128M	18h	9Fh

8.1.2. Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	(0 – 7)	(8 – 15)	(16 – 23)	(24 – 31)	(32 – 39)	(40 – 47)	(48 – 55)
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Chip Erase	C7h/60h						
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						

8.1.3. Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0 – 7)**	**(8 – 15)**	**(16 – 23)**	**(24 – 31)**	**(32 – 39)**	**(40 – 47)**
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID63-UID0)
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Quad Input Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0, …(9)	D7-D0, …(3)
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(7)
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(9)
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0		
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0 – 7)**	**(8 – 11)**	**(12 – 15)**	**(16 – 19)**	**(20 – 23)**	**(24 – 27)**	**(28 – 31)**
Fast Read Dual I/O	BBh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0 – 7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**	**(14, 15)**	**(16, 17)**	**(18,19)**	**(20, 21)**	**(22, 23)**
Quad Page Program	33h	A23-A16	A15-A8	A7-A0	D7-D0, …	D7-D0, …	D7-D0, …	D7-D0, …	D7-D0, …
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W8-W0				
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Word Read Quad I/O(12)	E7h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6-10 / 6-8 / 6-12 / 6-14	Byte ..
Clock Number	**(0 – 7)**	**(8)**	**(9)**	**(10)**	**(11)**	**(12-16) / (12-14) / (12-18) / (12-20)**	**17/15/19/21**
DTR Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy (LC1-0 : 00 / 01 / 10 /11)	(D7-D0)

8.1.4. Instruction Set Table 3 (QPI Instructions)[14]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**	**(10, 11)**
Write Enable	06h					
Volatile SR Write Enable	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0)[2]				
Write Status Register-1[4]	01h	(S7-S0)[4]				
Read Status Register-2	35h	(S15-S8)[2]				
Write Status Register-2	31h	(S15-S8)				
Read Status Register-3	15h	(S23-S16)[2]				
Write Status Register-3	11h	(S23-S16)				
Chip Erase	C7h/60h					
Erase / Program Suspend	75h					
Erase / Program Resume	7Ah					
Deep Power-down	B9h					
Set Read Parameters	C0h	P7-P0				
Release Power down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)[2]	
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)		
Exit QPI Mode	FFh					
Enable Reset	66h					
Reset Device	99h					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0[9]	D7-D0[3]
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy[13]	(D7-D0)
Burst Read with Wrap[14]	0Ch	A23-A16	A15-A8	A7-A0	Dummy[13]	(D7-D0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6-10 / 6-8 / 6-12 / 6-14	Byte ..
Clock Number	**(0, 1)**	**(2)**	**(3)**	**(4)**	**(5)**	**(6-10) / (6-8) / (6-12) / (6-14)**	**11/9/13/15**
DTR Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy (LC1-0 : 00 / 01 / 10 /11)	(D7-D0)

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 8.2.5.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0) IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
9. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. Word Read Quad I/O data output format:
    IO0 = (x, x, D4, D0, D4, D0, D4, D0)
    IO1 = (x, x, D5, D1, D5, D1, D5, D1)
    IO2 = (x, x, D6, D2, D6, D2, D6, D2)
    IO3 = (x, x, D7, D3, D7, D3, D7, D3)
12. QPI Command, Address, Data input/output format:

CLK #	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*
IO0 =	C4,	C0,	A20,	A16,	A12,	A08,	A4,	A0,	D4,	D0,	D4,	D0
IO1 =	C5,	C1,	A21,	A17,	A13,	A09,	A5,	A1,	D5,	D1,	D5,	D1
IO2 =	C6,	C2,	A22,	A18,	A14,	A10,	A6,	A2,	D6,	D2,	D6,	D2
IO3 =	C7,	C3,	A23,	A19,	A15,	A11,	A7,	A3,	D7,	D3,	D7,	D3

13. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
14. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.
15. DTR Address, Data input/output format:

CLK #	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
IO0 =	A20,A16,	A12,A08,	A4,A0,	M4,M0,	x,x,	x,x,	x,x,	D4,D0,	D4,D0
IO1 =	A21,A17,	A13,A09,	A5,A1,	M5,M1,	x,x,	x,x,	x,x,	D5,D1,	D5,D1
IO2 =	A22,A18,	A14,A10,	A6,A2,	M6,M2,	x,x,	x,x,	x,x,	D6,D2,	D6,D2
IO3 =	A23,A19,	A15,A11,	A7,A3,	M7,M3,	x,x,	x,x,	x,x,	D7,D3,	D7,D3

8.2. Instruction Descriptions

8.2.1. Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

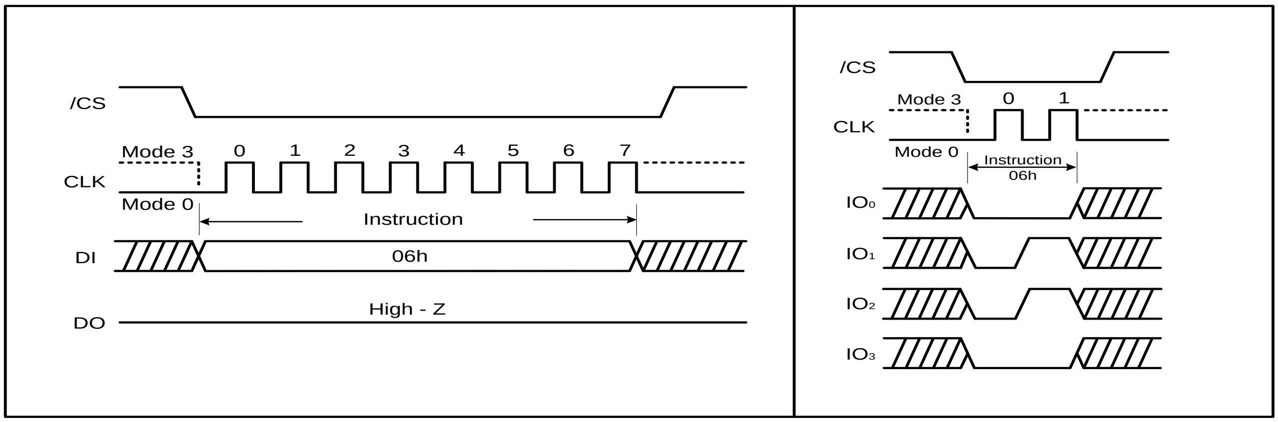

Figure 5. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

8.2.2. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

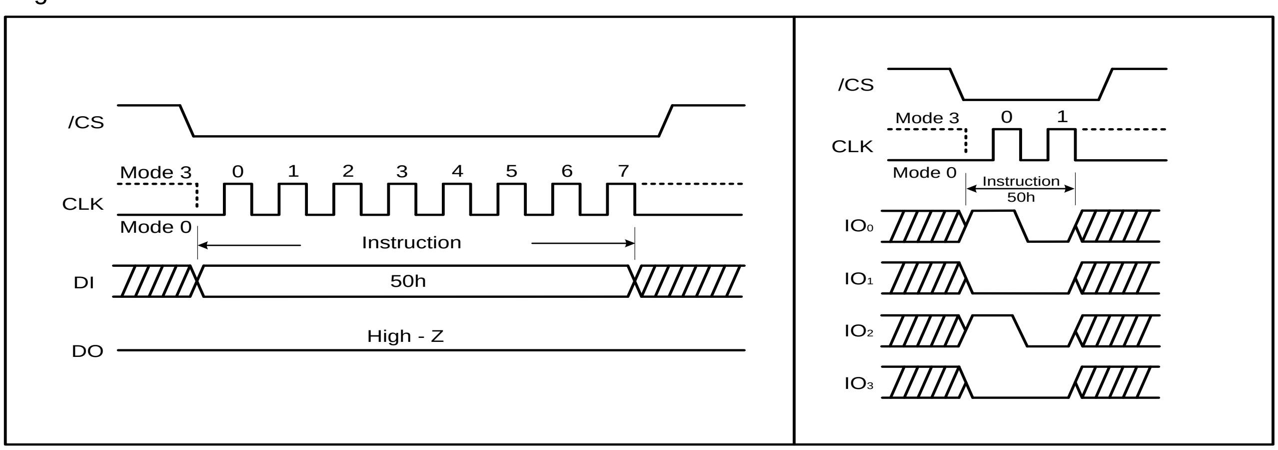

Figure 6. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

8.2.3. Write Disable (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

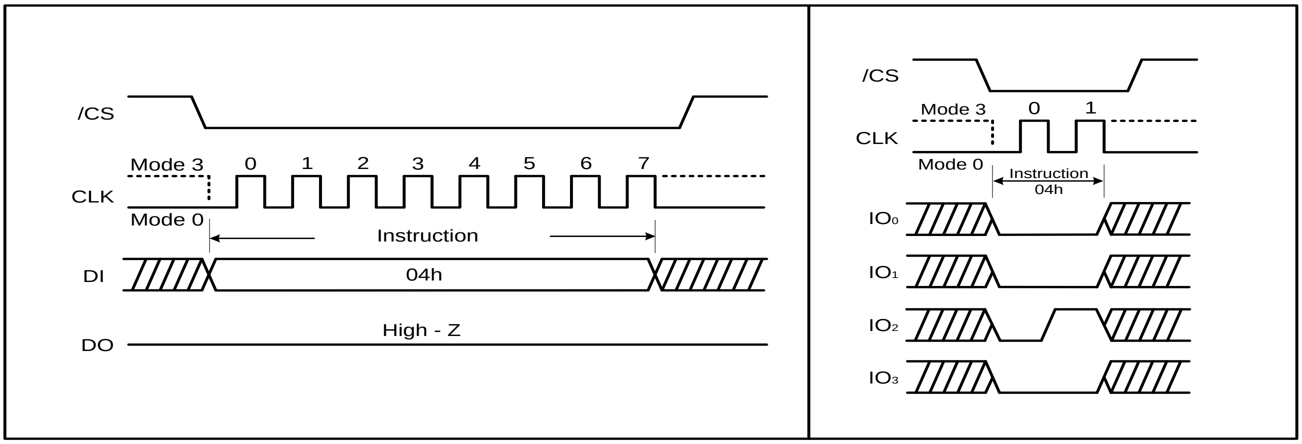

Figure 7. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

8.2.4. Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

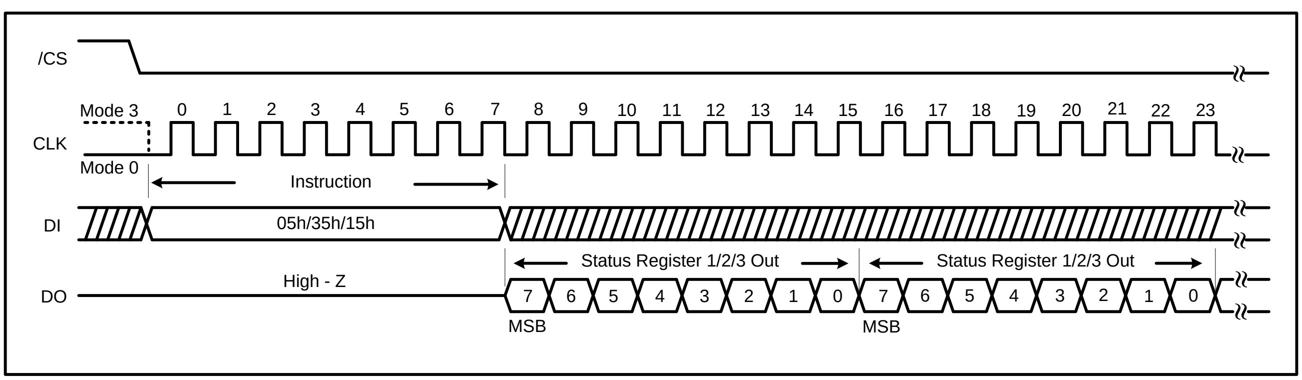

Figure 8a. Read Status Register Instruction (SPI Mode)

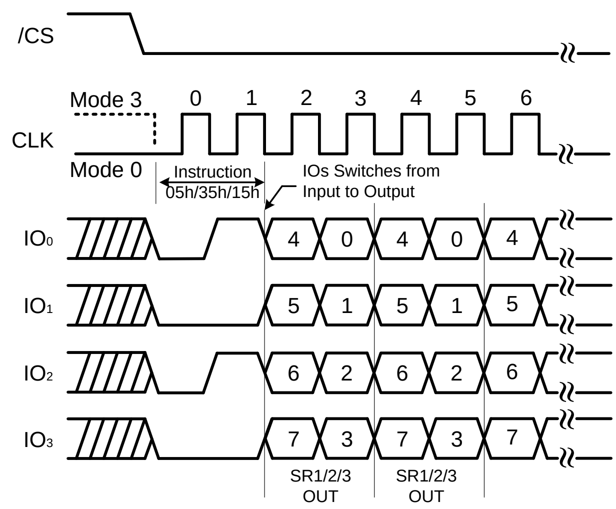

Figure 8b. Read Status Register Instruction (QPI Mode)

8.2.5. Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP0, SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register-2; HOLD/RST, DRV in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non- volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 9a & 9b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 7.1 for Status Register descriptions.

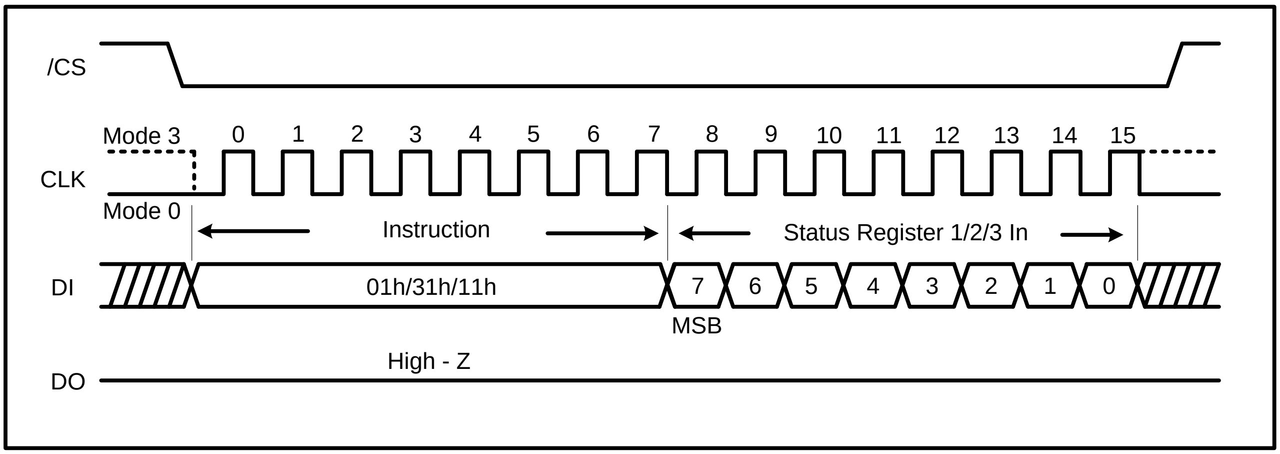

Figure 9a. Write Status Register-1/2/3 Instruction (SPI Mode)

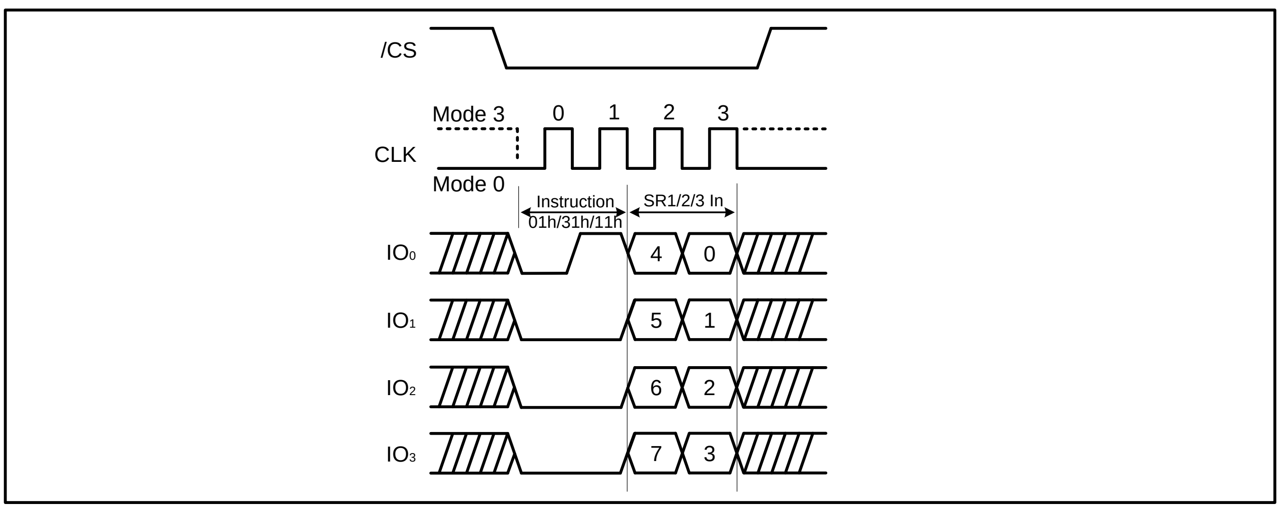

Figure 9b. Write Status Register-1/2/3 Instruction (QPI Mode)

The DS25M4AB is also backward compatible to Dosilicon's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 9c & 9d. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).

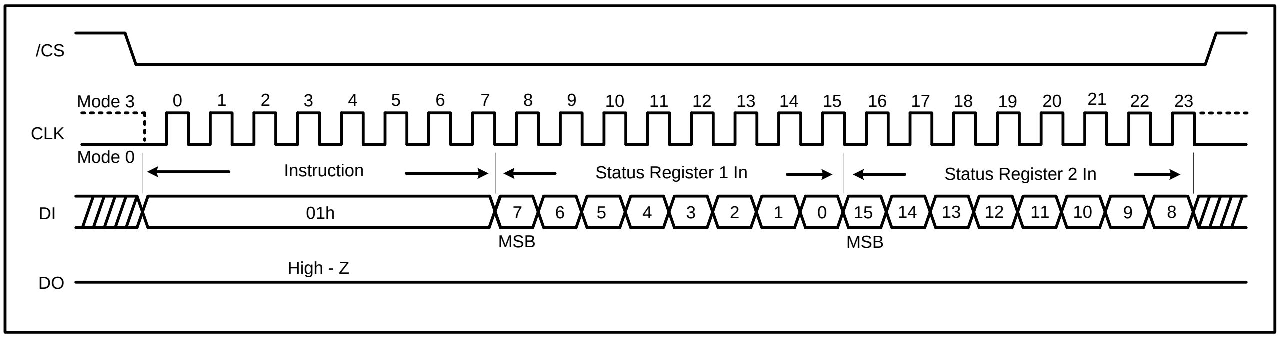

Figure 9c. Write Status Register-1/2 Instruction (SPI Mode)

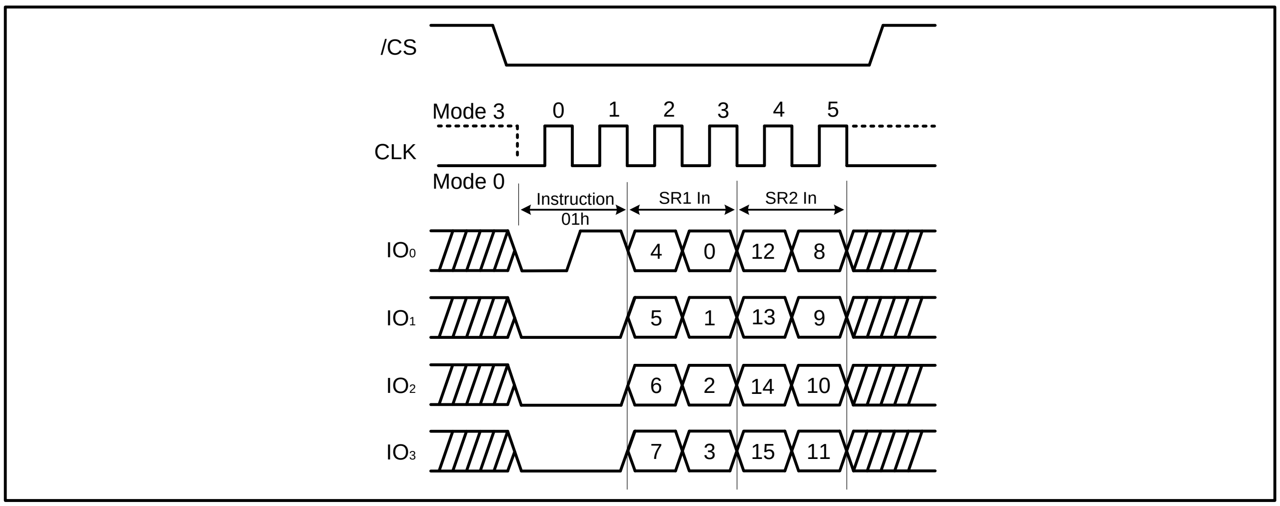

Figure 9d. Write Status Register-1/2 Instruction (QPI Mode)

8.2.6. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 10. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

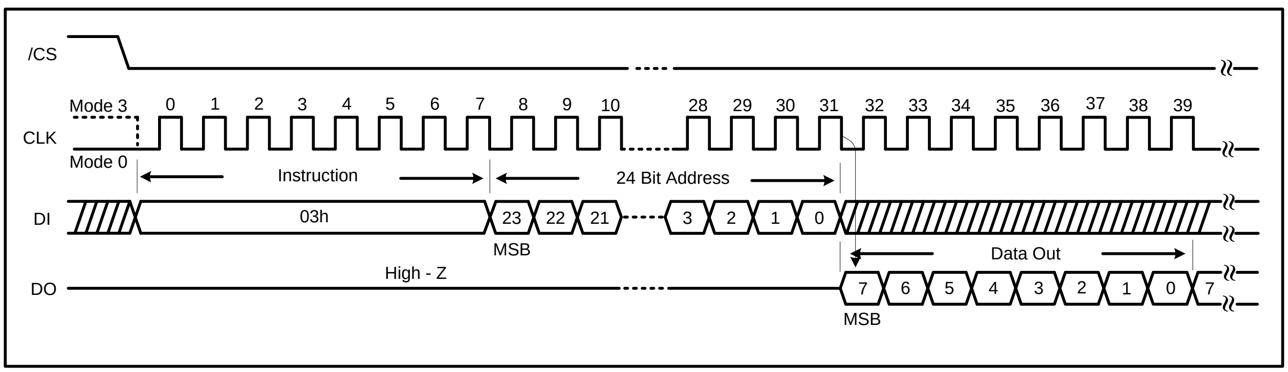

Figure 10. Read Data Instruction (SPI Mode only)

8.2.7. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

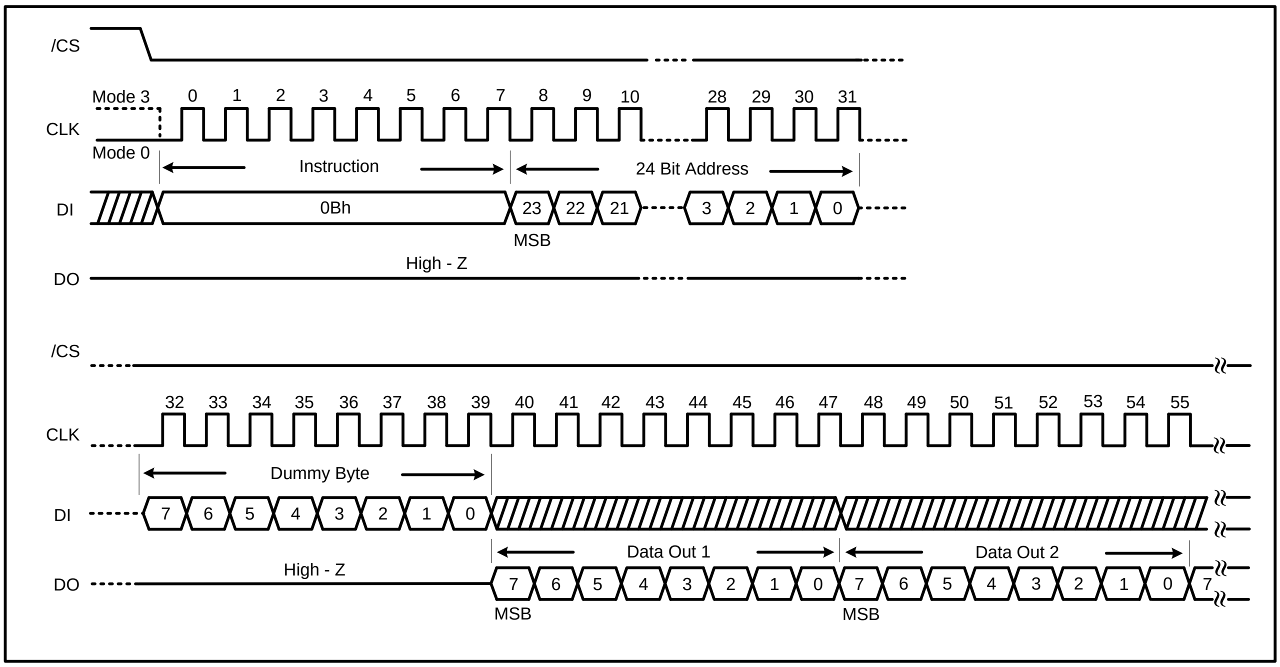

Figure 11a. Fast Read Instruction (SPI Mode)

8.2.8. Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

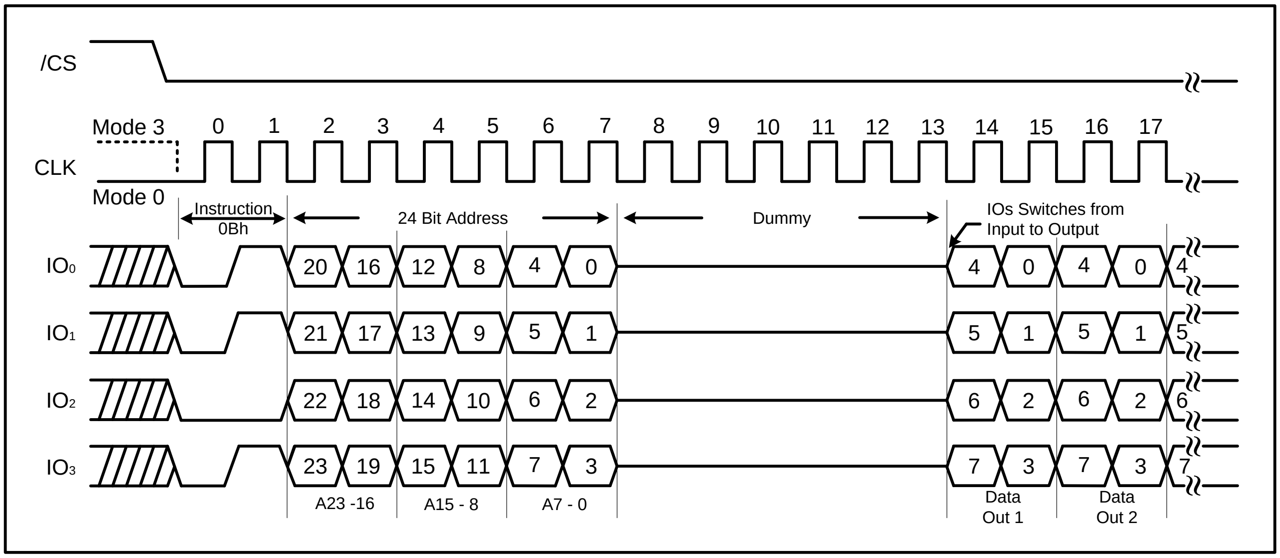

Figure 11b. Fast Read Instruction (QPI Mode)

8.2.9. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

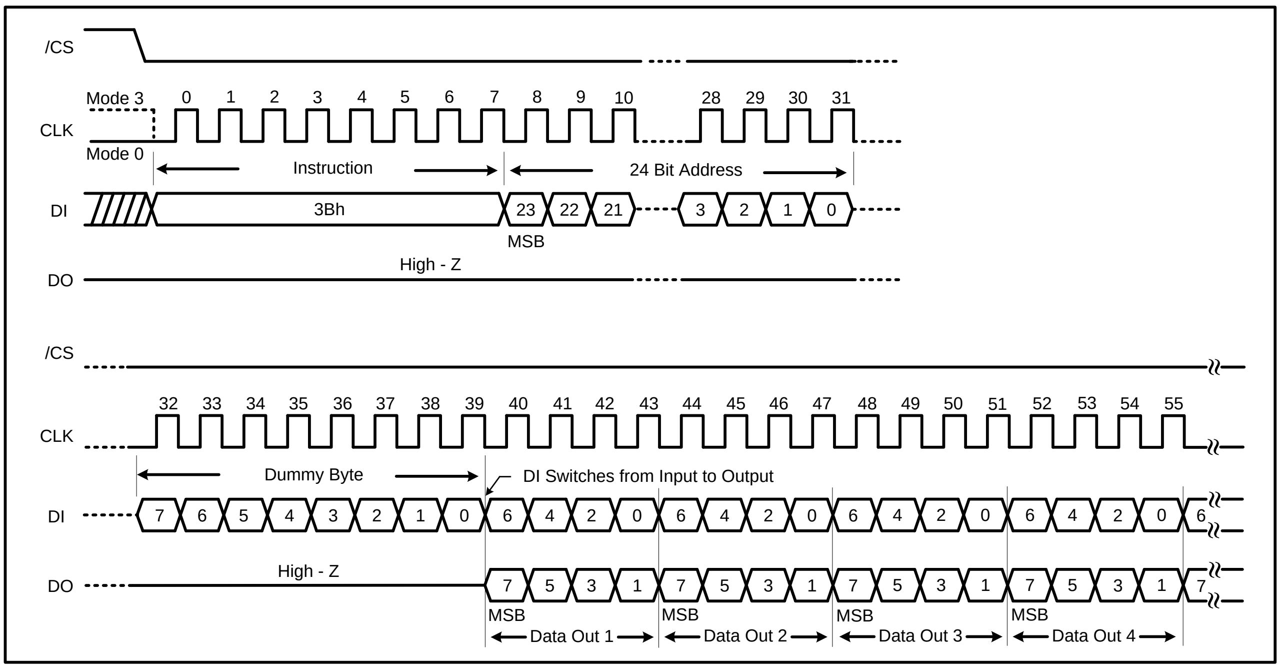

Figure 12. Fast Read Dual Output Instruction (SPI Mode only)

8.2.10. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 13. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

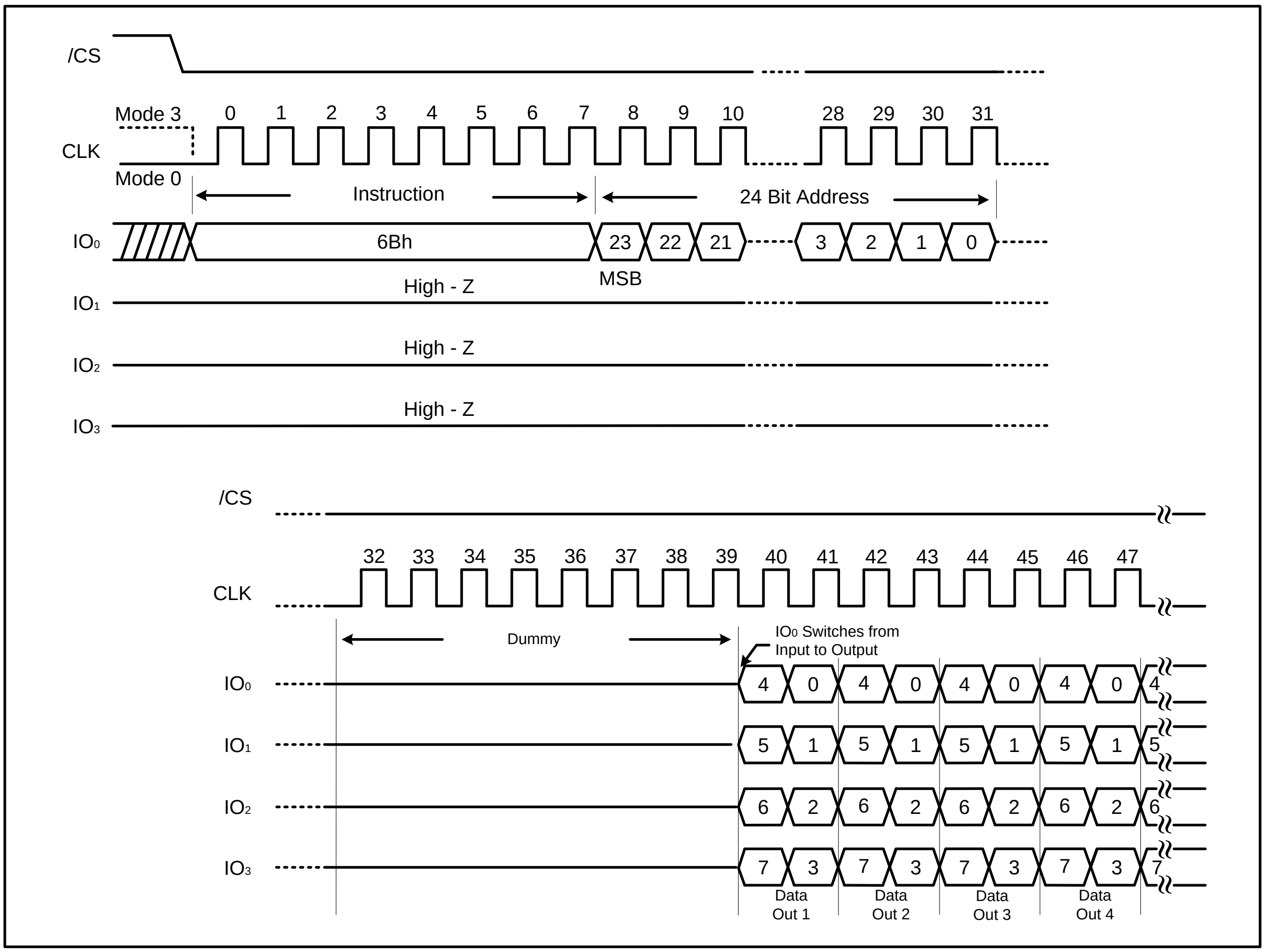

Figure 13. Fast Read Quad Output Instruction (SPI Mode only)

8.2.11. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

8.2.12. Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 14a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 14b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

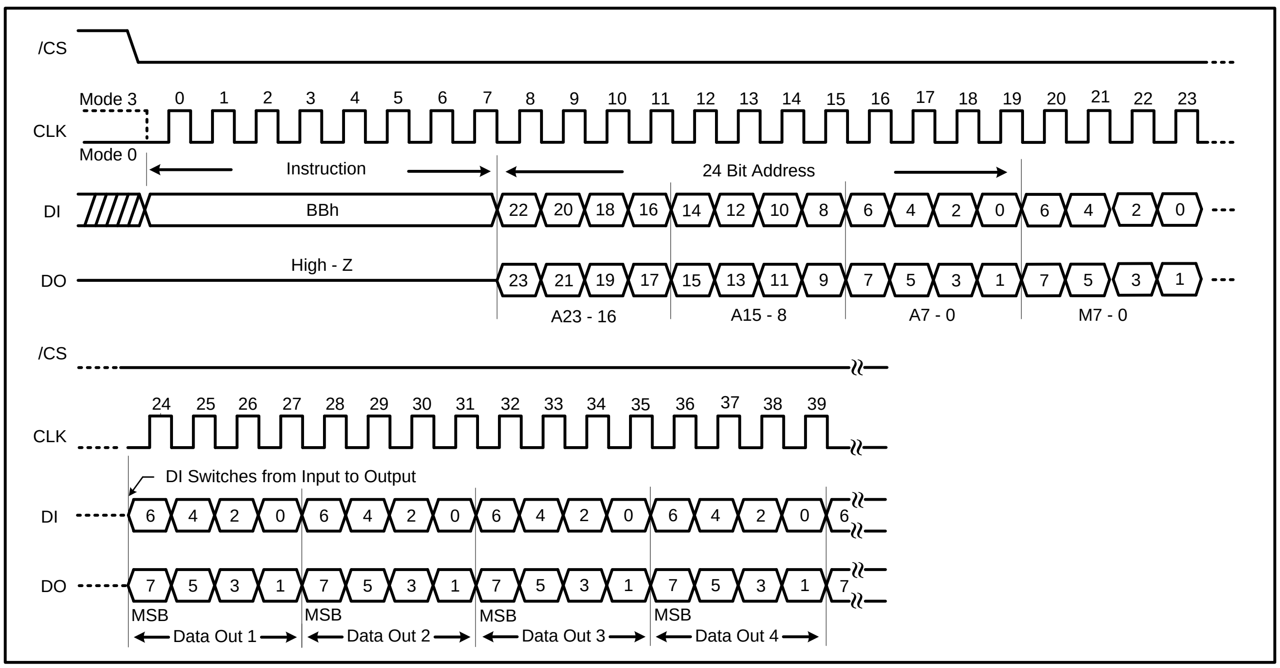

Figure 14a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

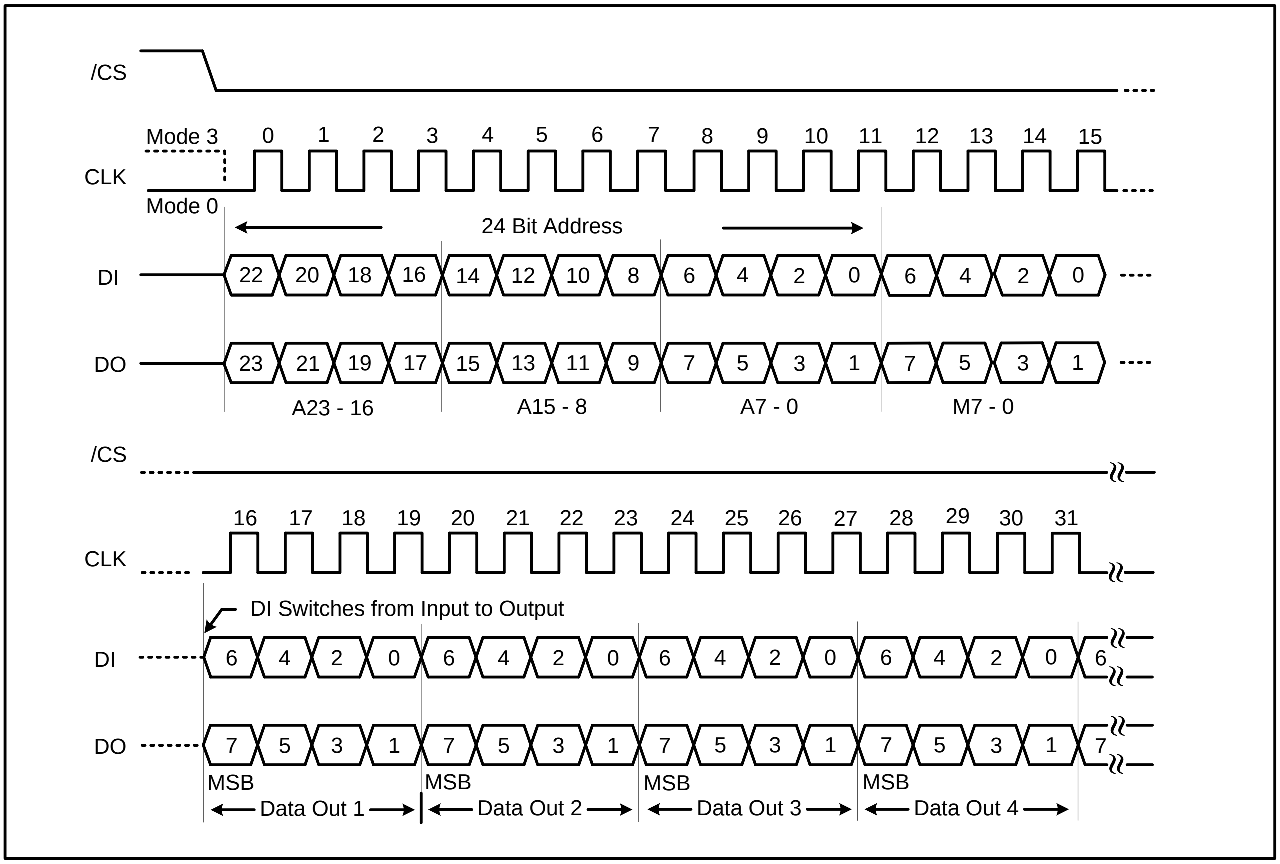

Figure 14b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

8.2.13. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

8.2.14. Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 15a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 15b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

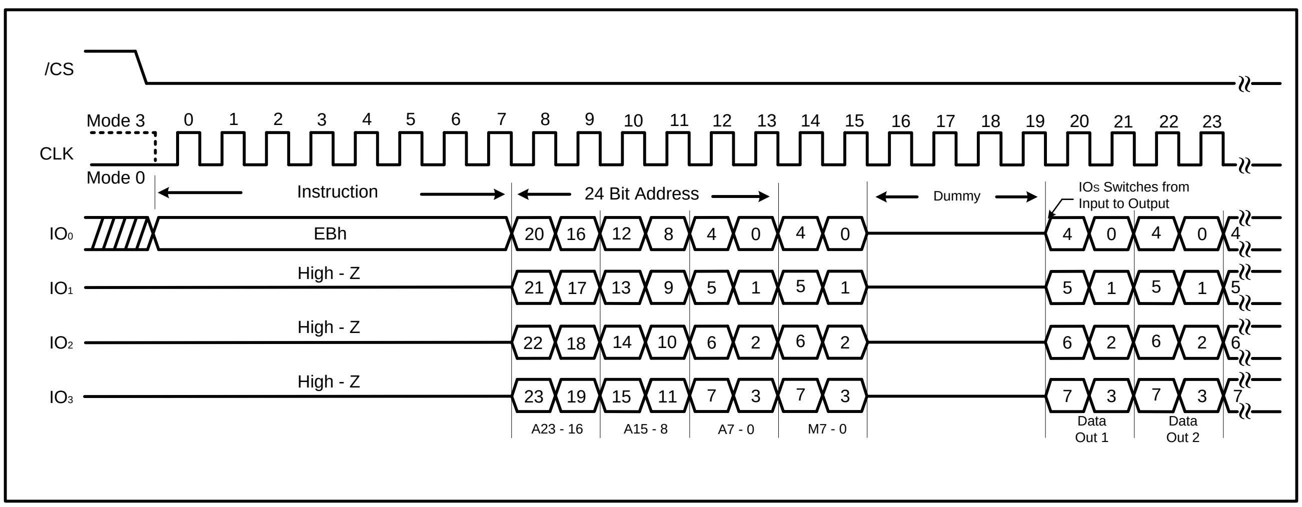

Figure 15a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

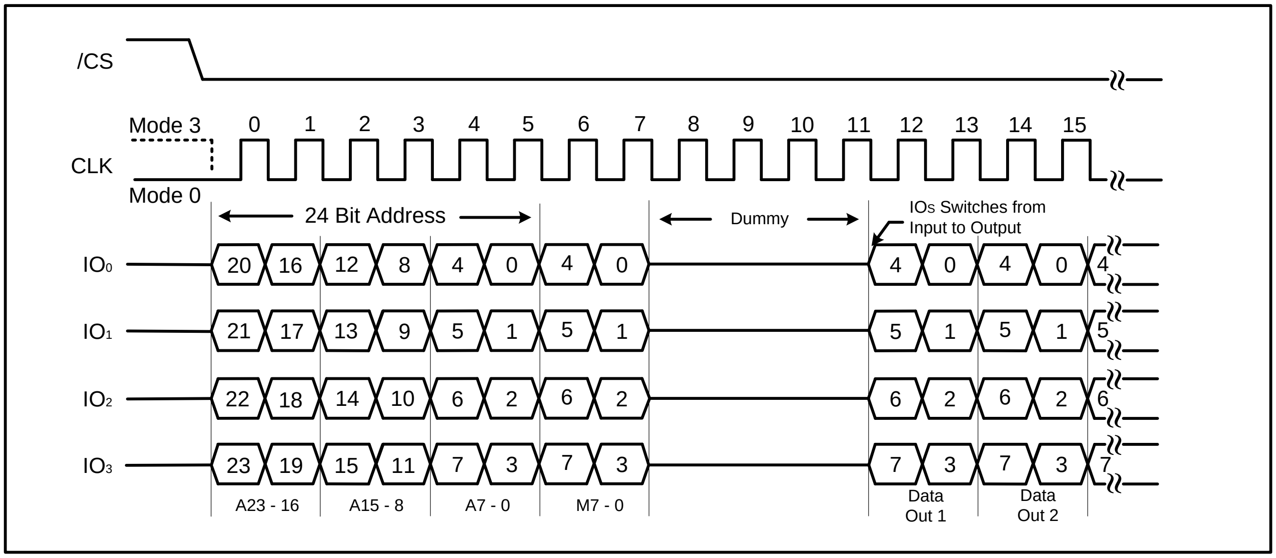

Figure 15b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

8.2.15. **Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section "Set Burst with Wrap" for detail descriptions.

8.2.16. **Fast Read Quad I/O (EBh) in QPI Mode**

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 15c. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used. Please refer to section "Burst Read with Wrap" for details.

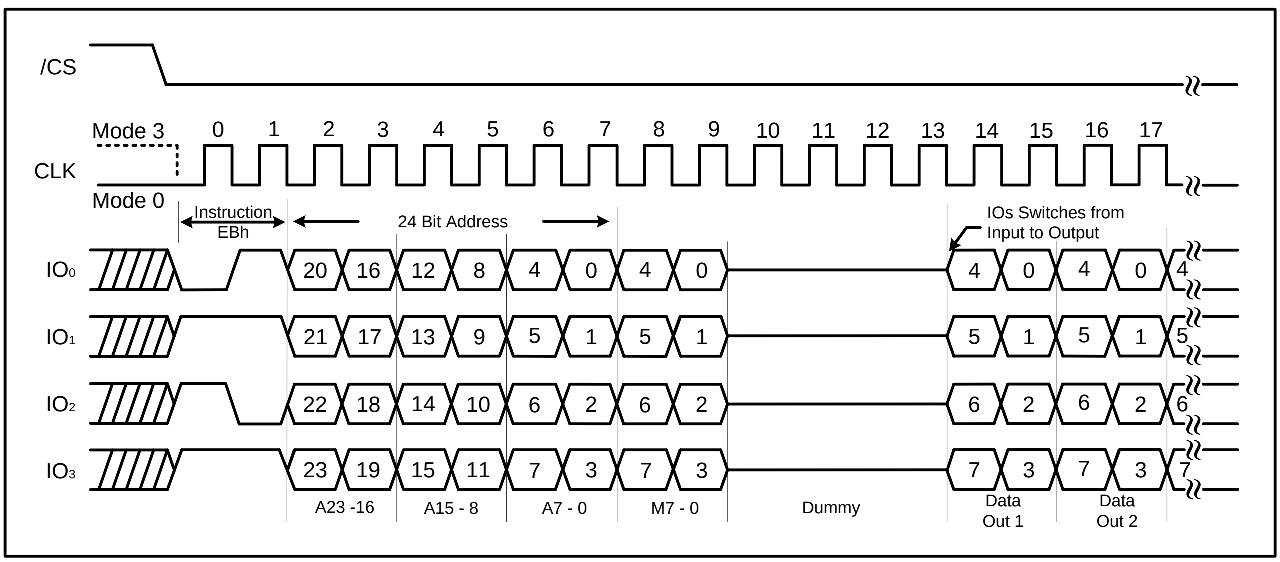

Figure 15c. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

8.2.17. Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

8.2.18. Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 16a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E7h instruction code, as shown in Figure 16b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

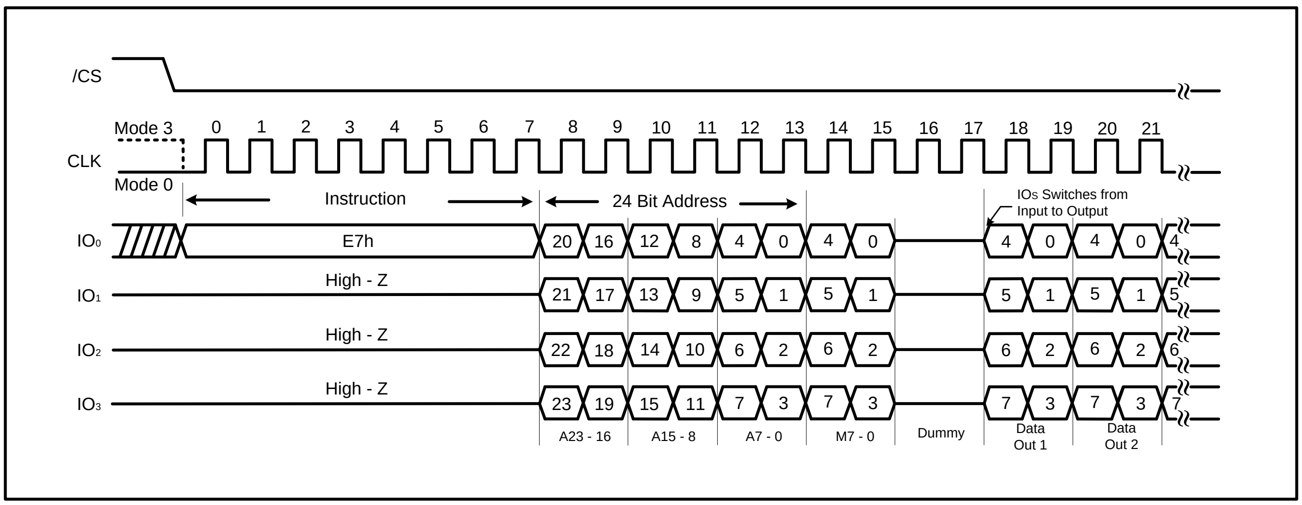

Figure 16a. Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

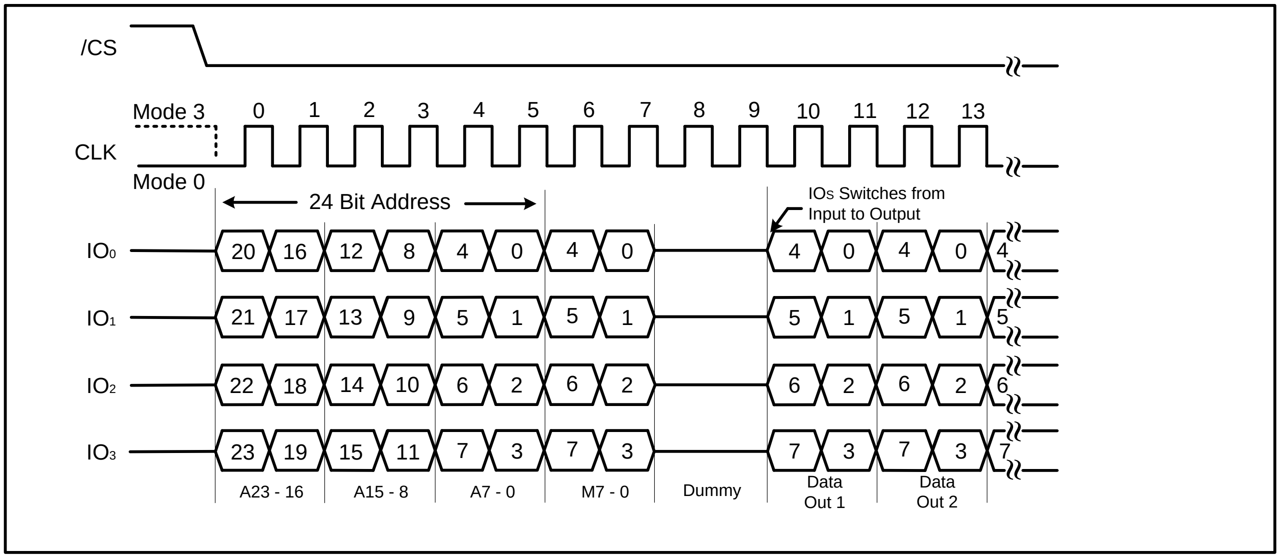

Figure16b. Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

8.2.19. Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See section "Set Burst with Wrap" for detail descriptions.

8.2.20. Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 17. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the “Burst Read with Wrap (0Ch)” instruction should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0h)” instruction. Refer to section “Set Read Parameters” and “Burst Read with Wrap” for details.

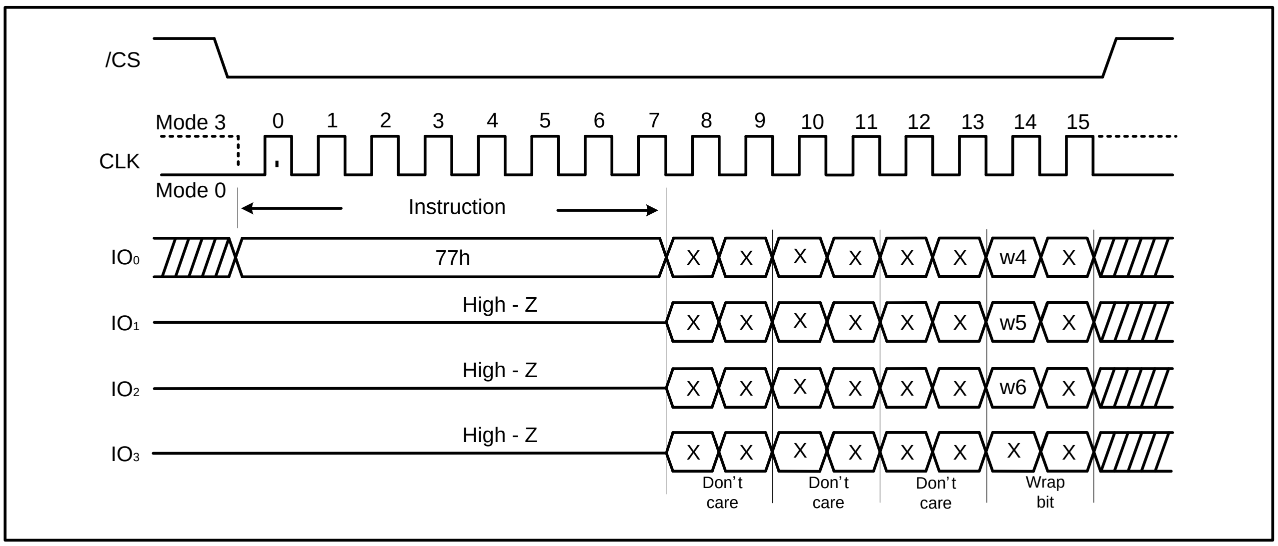

Figure 17. Set Burst with Wrap Instruction (SPI Mode only)

8.2.21. **DTR Read Quad I/O (EDh)**

The DTR Read Quad I/O instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of Status Register must be set to "1" before sending the DTR Read Quad I/O instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of CLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single DTR Read Quad I/O instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DTR Read Quad I/O instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Notes : Users need to set the dummy cycles and LC 1-0 bit according to the max clock frequency to use DTR read. Dummy contains the M7-0 bit.

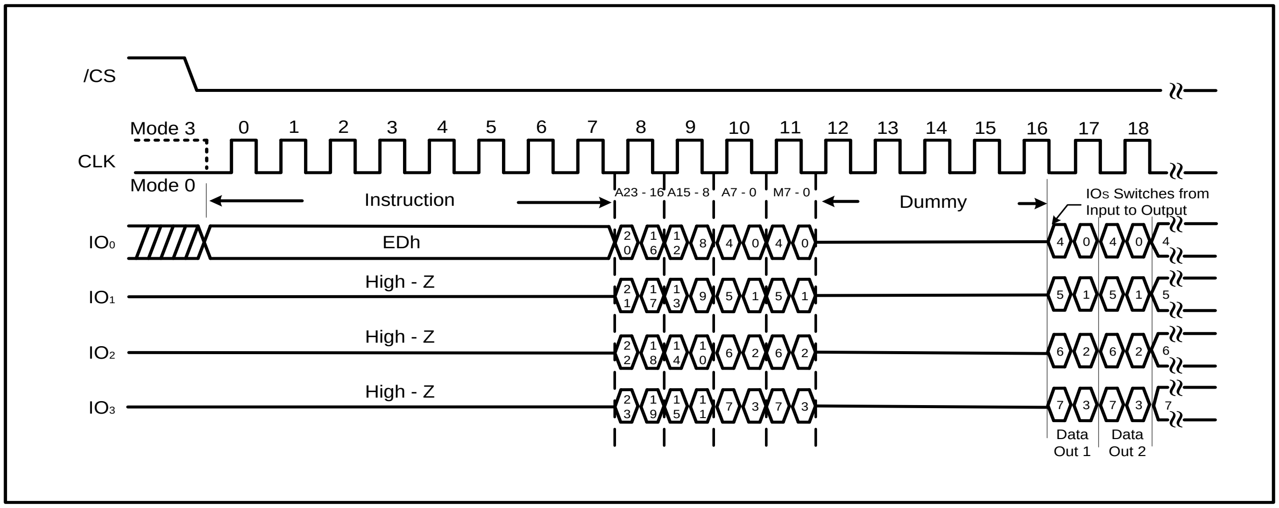

Figure17a. DTR Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, 66MHz SPI Mode, 6 dummy, LC1-0 = 00 in Status Register-3)

8.2.22. DTR Read Quad I/O with "Continuous Read Mode"

The DTR Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 18a. The upper nibble of the (M7-4) controls the length of the next DTR Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EDh instruction code, as shown in Figure 18b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

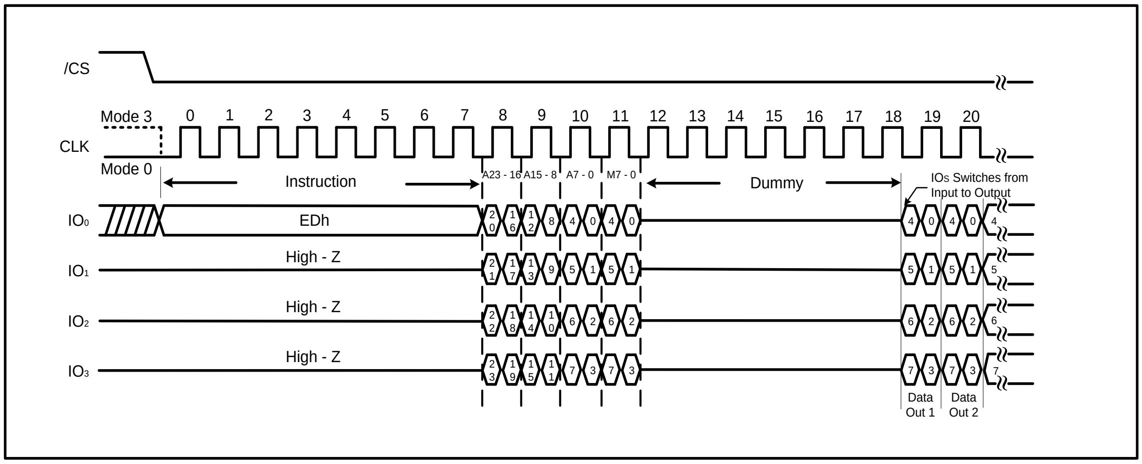

Figure18a. DTR Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, SPI Mode, 8 dummy, LC1-0 = 10 in Status Register-3)

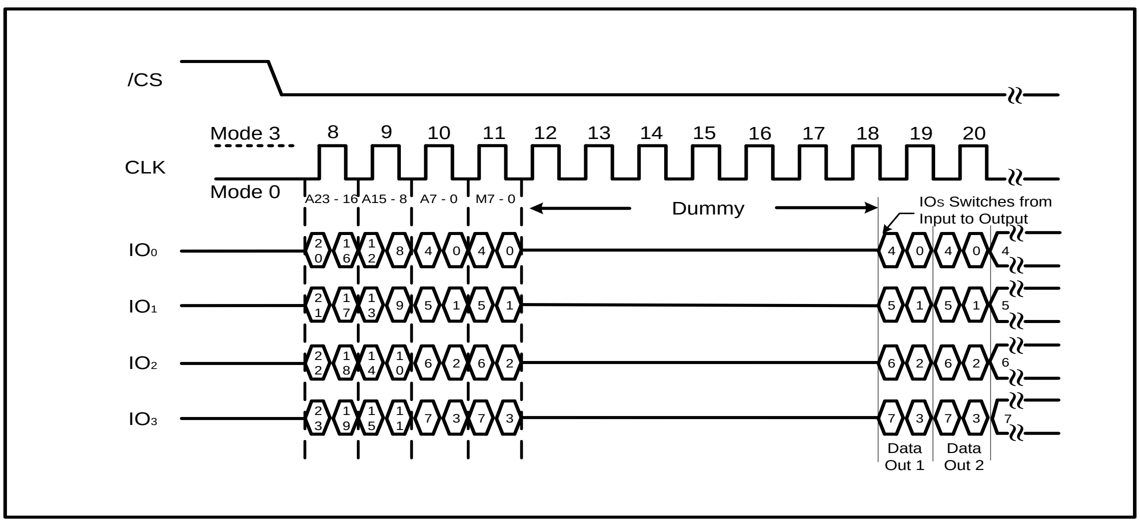

Figure18b. DTR Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode, 8 dummy, LC1-0 = 10 in Status Register-3)

8.2.23. DTR Read Quad I/O (EDh) in QPI Mode

The DTR Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 18c. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for DTR Read Quad I/O instruction. Please refer to the description on previous pages.

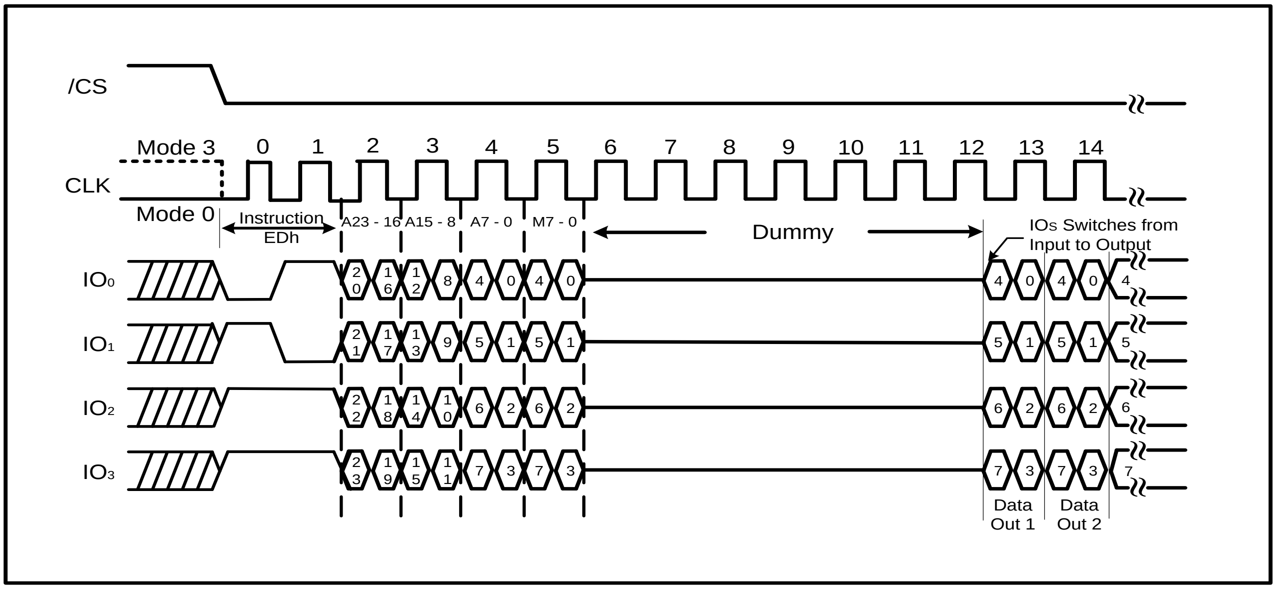

Figure18c. DTR Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, QPI Mode, 8 dummy, LC1-0 = 10 in Status Register-3)

8.2.24. **Page Program (02h)**

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 19.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

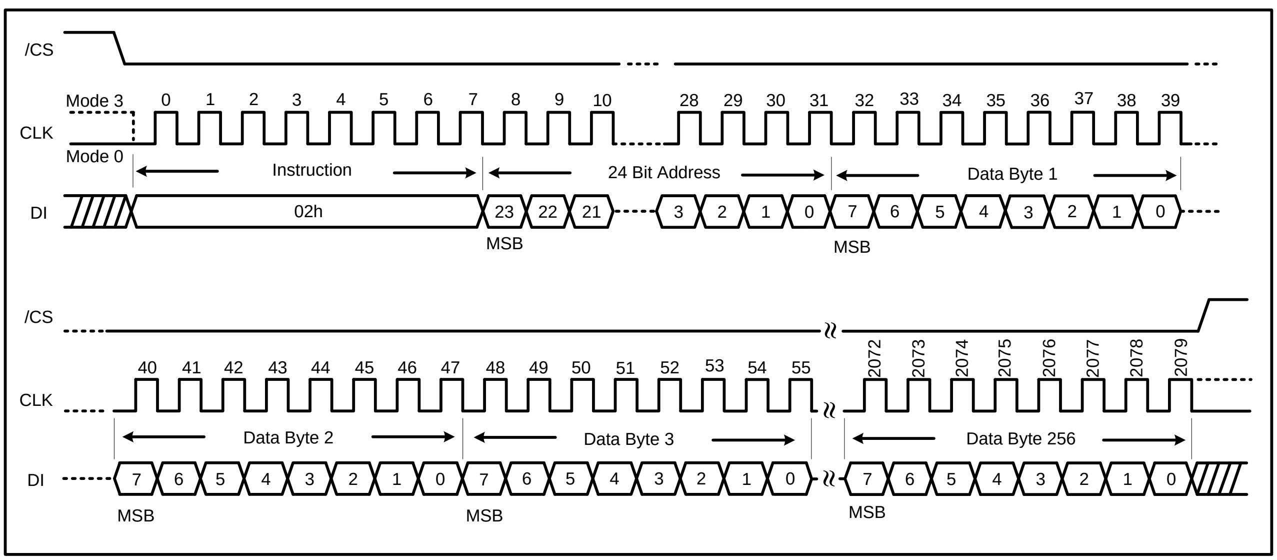

Figure 19a. Page Program Instruction (SPI Mode)

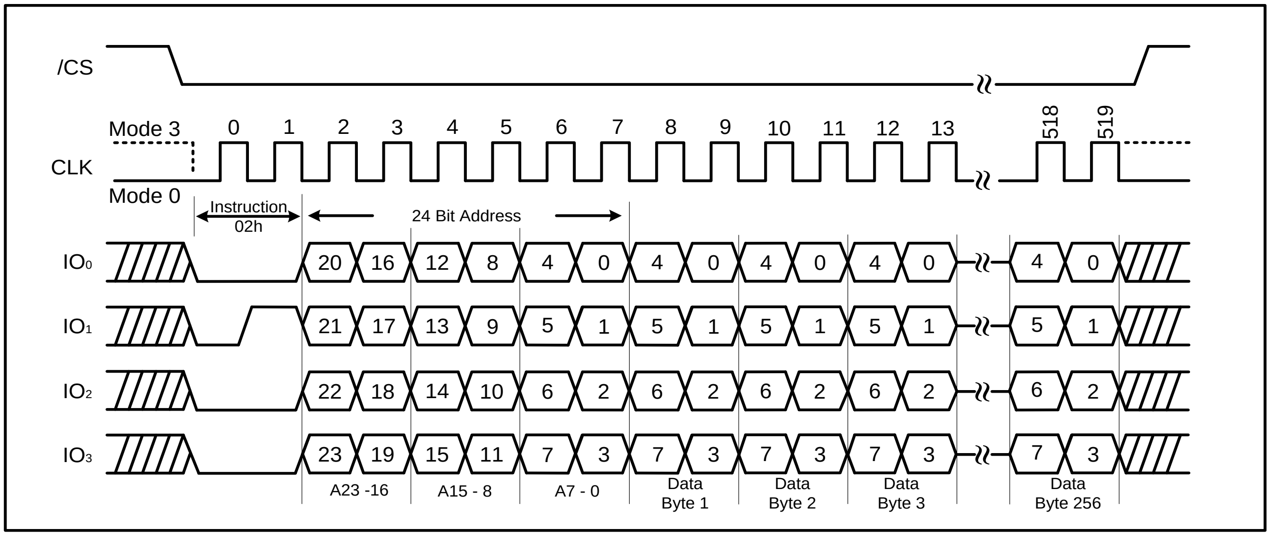

Figure 19b. Page Program Instruction (QPI Mode)

8.2.25. **Quad Input Page Program (32h)**

The Quad Input Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Input Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Input Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Input Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Input Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Input Page Program are identical to standard Page Program. The Quad Input Page Program instruction sequence is shown in Figure 20.

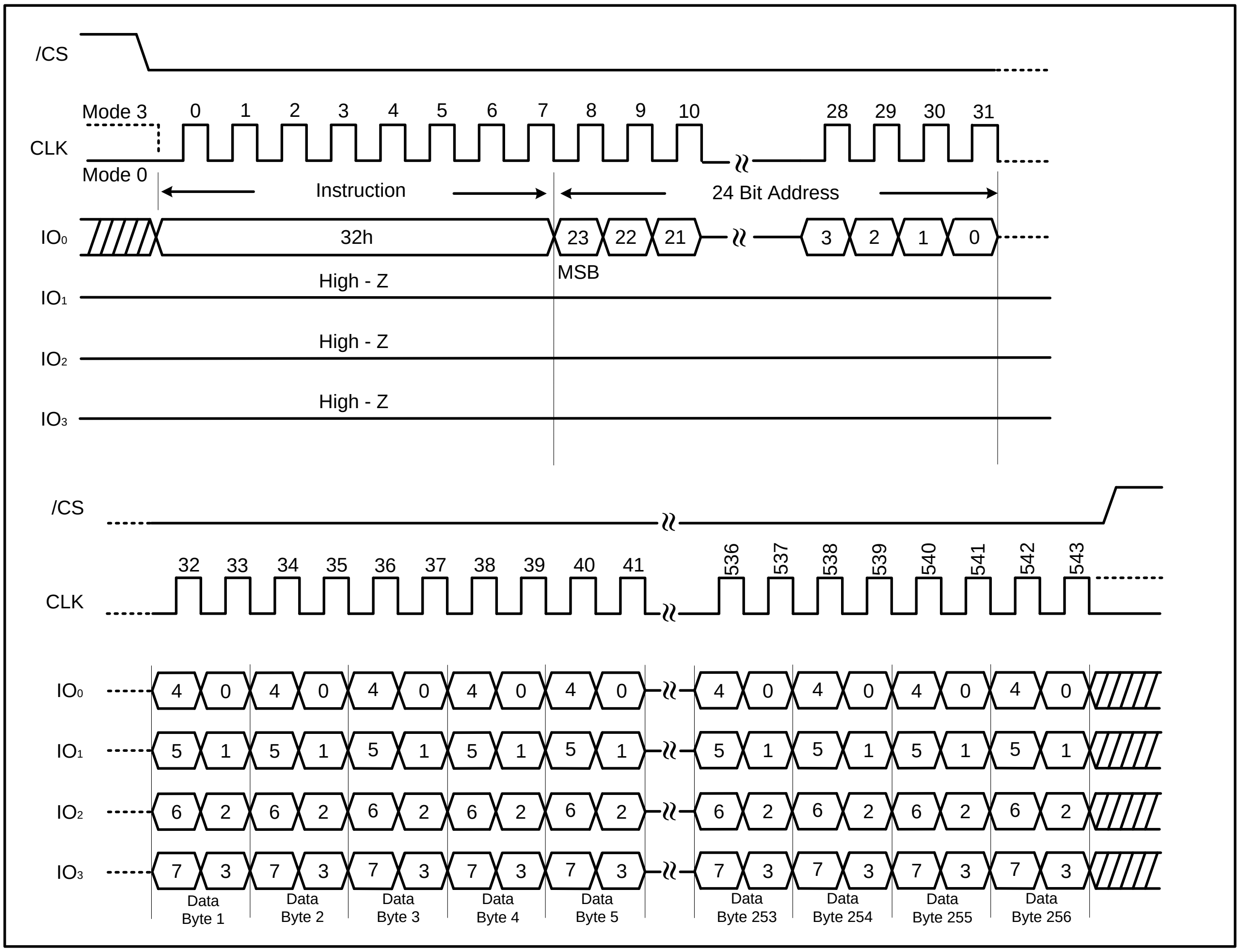

Figure 20. Quad Input Page Program Instruction (SPI Mode only)

8.2.26. Quad Page Program (33h)

The Quad Page Program (33h) instruction is similar to the Quad Input Page Program (32h) instruction except that address and data bits are both input and output through four pins IO_0, IO_1, IO_2 and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data. To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. The Quad Page Program instruction sequence is shown in Figure 21.

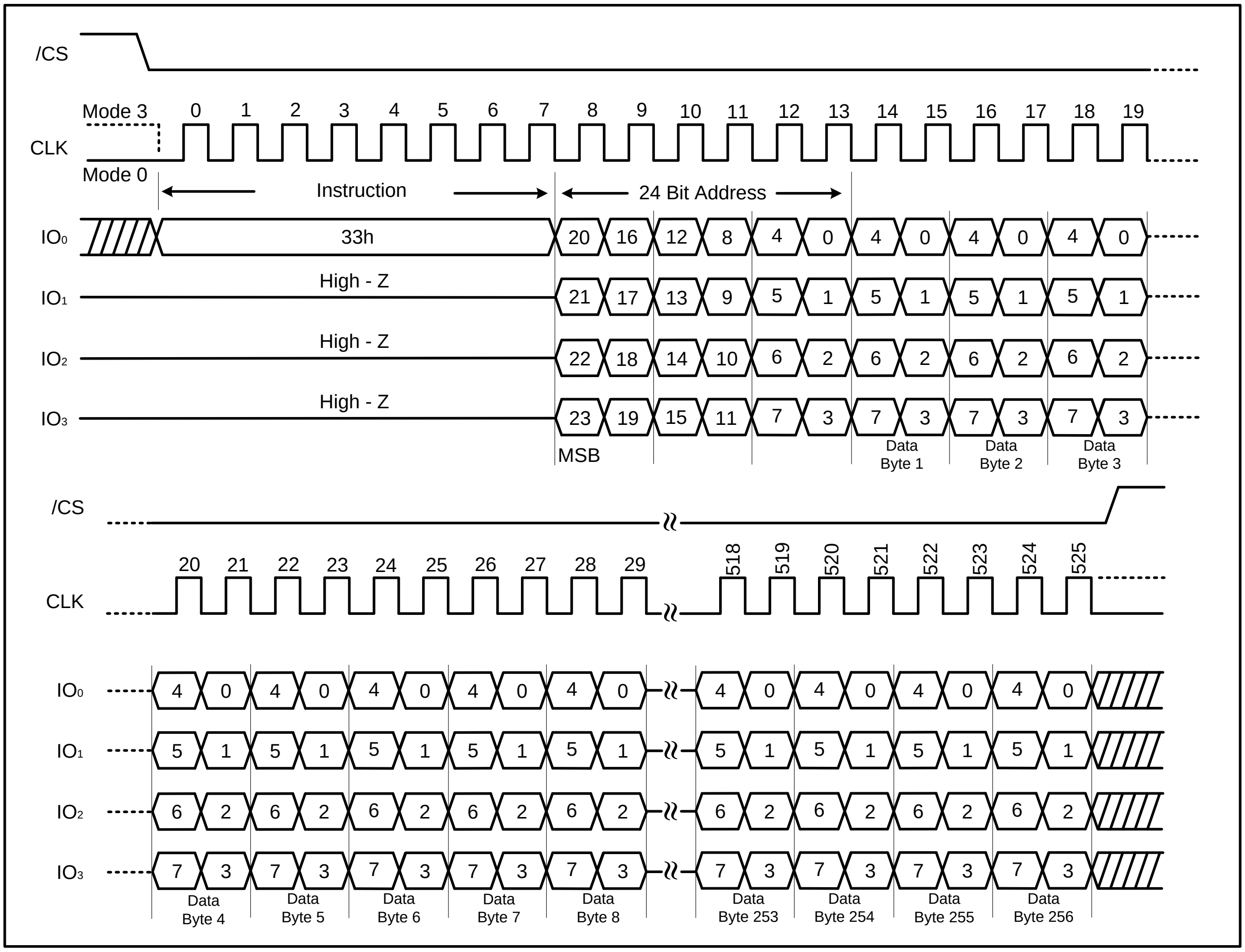

Figure 21. Quad Page Program Instruction (SPI Mode only)

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8.2.27. **Sector Erase (20h)**

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 22a & 22b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

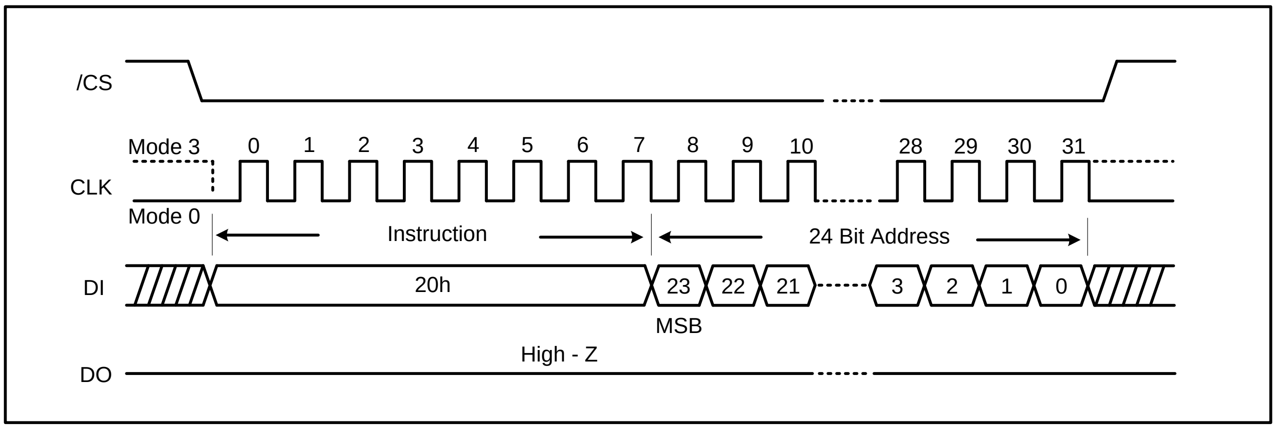


Figure 22a. Sector Erase Instruction (SPI Mode)

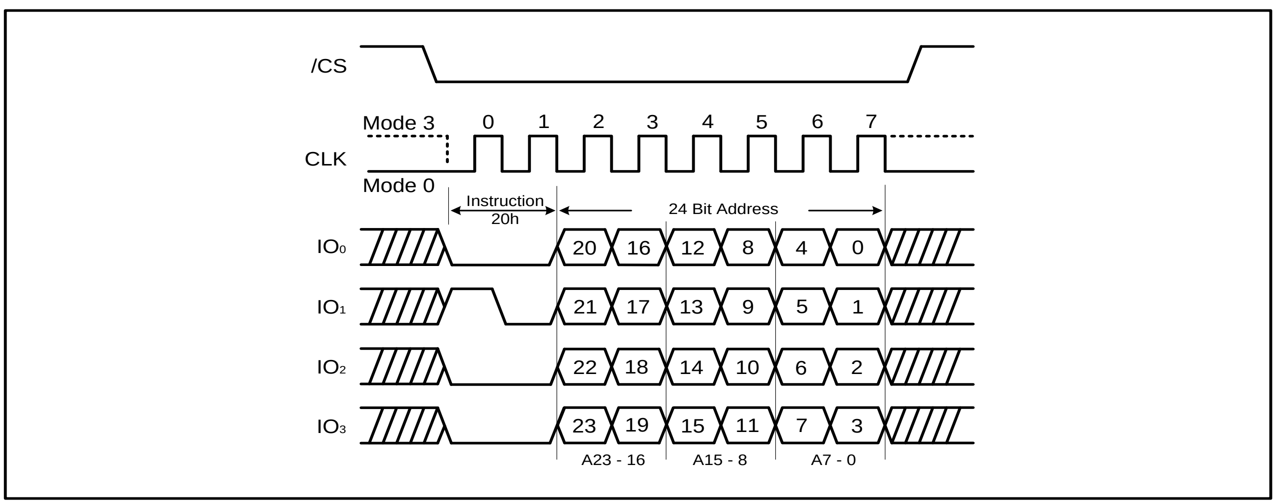


Figure 22b. Sector Erase Instruction (QPI Mode)

8.2.28. 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 23a &23b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

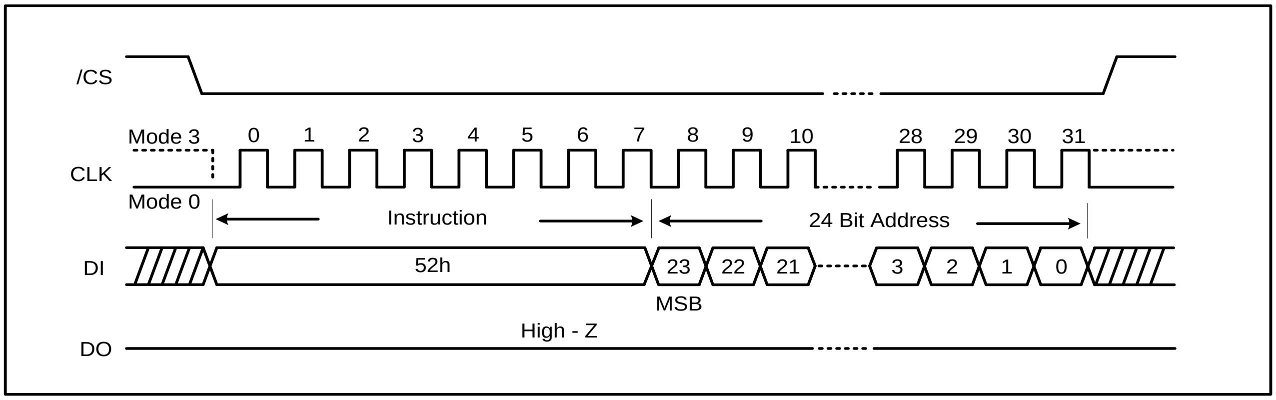


Figure 23a. 32KB Block Erase Instruction (SPI Mode)

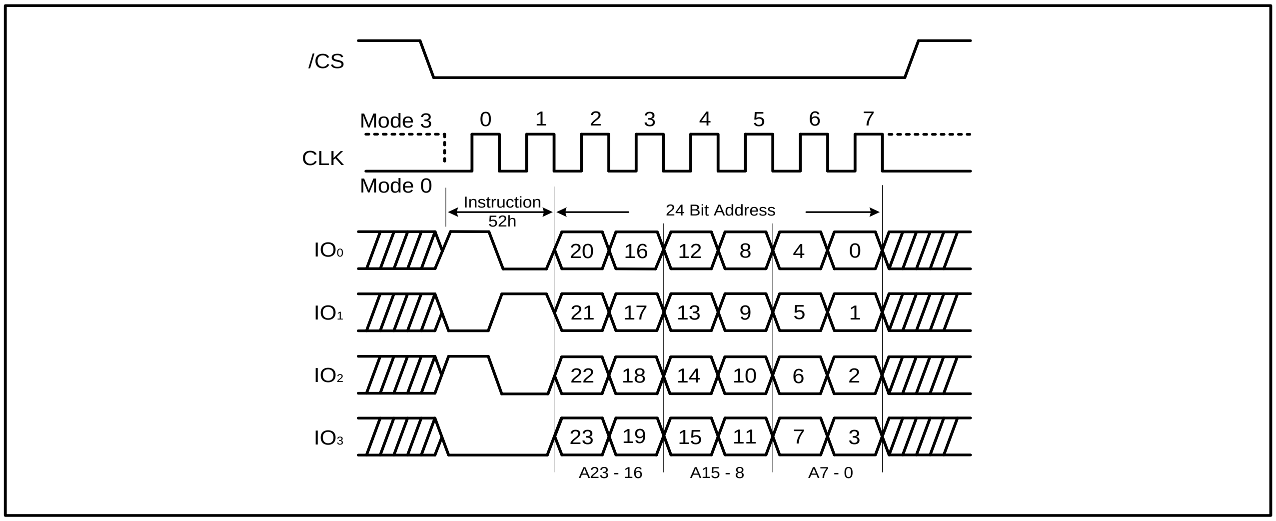


Figure 23b. 32KB Block Erase Instruction (QPI Mode)

8.2.29. 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 24a & 24b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

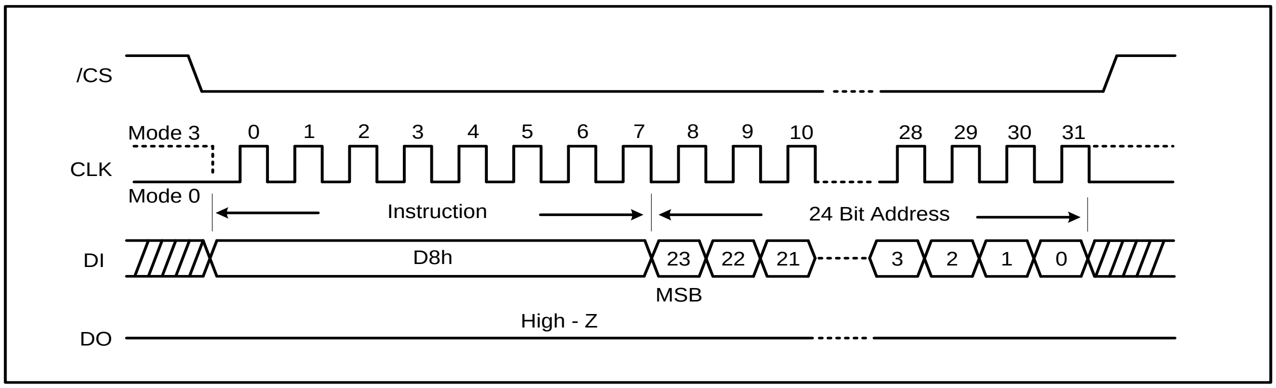


Figure 24a. 64KB Block Erase Instruction (SPI Mode)

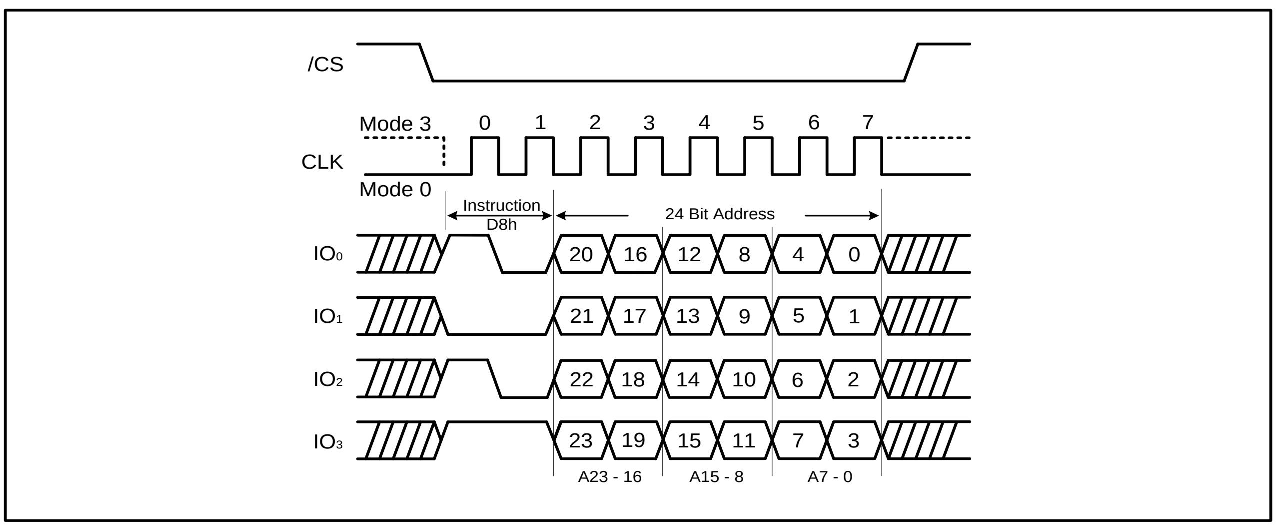


Figure 24b. 64KB Block Erase Instruction (QPI Mode)

8.2.30. Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 25.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

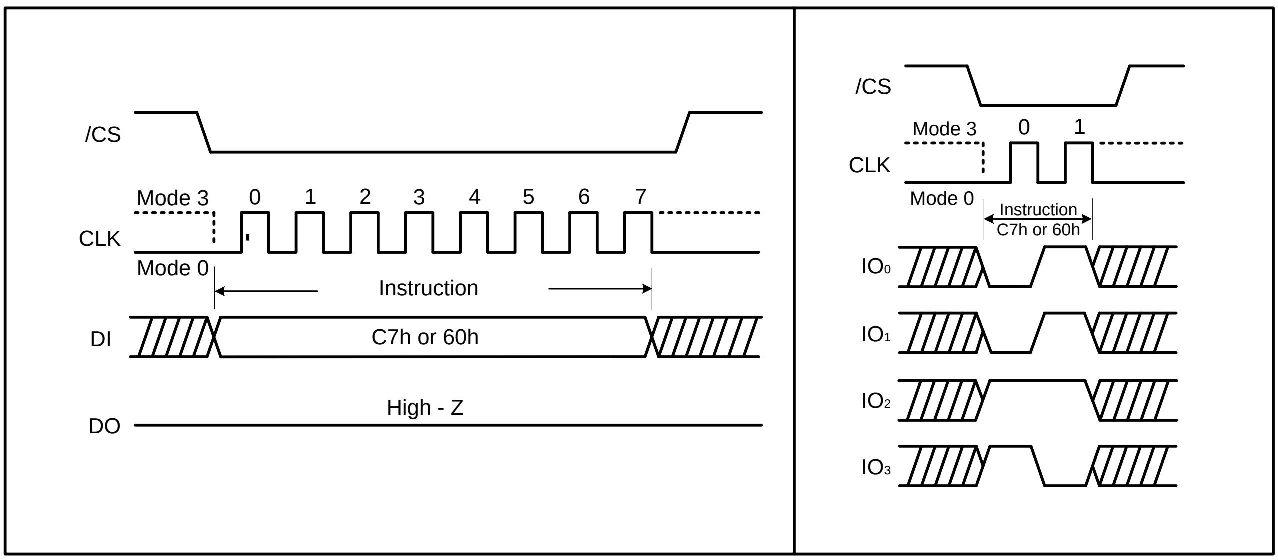


Figure 25. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

8.2.31. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction "75h", allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 26a & 26b.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instructions (01h, 31h, 11h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction "75h" will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of "t_{SUS}" (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within "t_{SUS}" and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction "75h" is not issued earlier than a minimum of time of "t_{SUS}" following the preceding Resume instruction "7Ah".

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

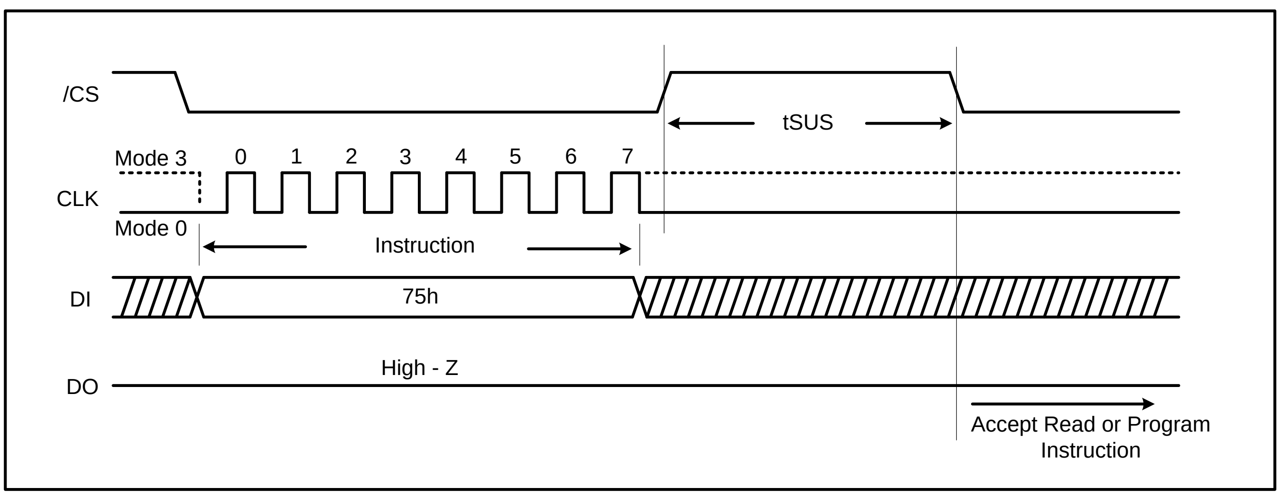


Figure 26a. Erase/Program Suspend Instruction (SPI Mode)

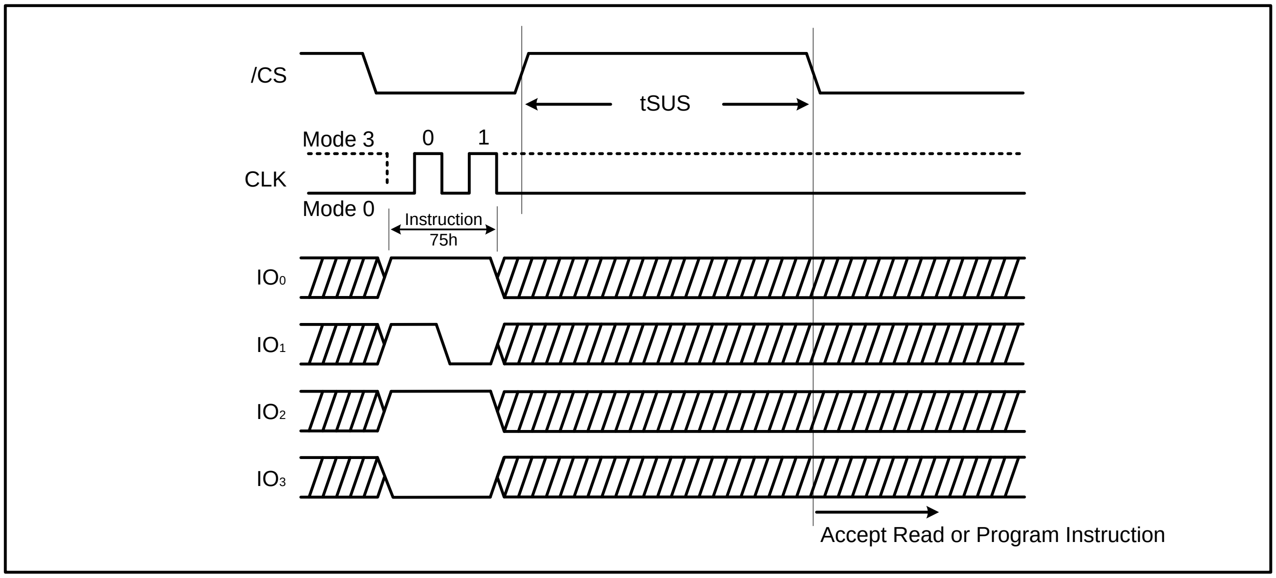


Figure 26b. Erase/Program Suspend Instruction (QPI Mode)

8.2.32. **Erase / Program Resume (7Ah)**

The Erase/Program Resume instruction "7Ah" must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction "7Ah" will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction "7Ah" will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 27a & 27b.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of "t_{SUS}" following a previous Resume instruction.

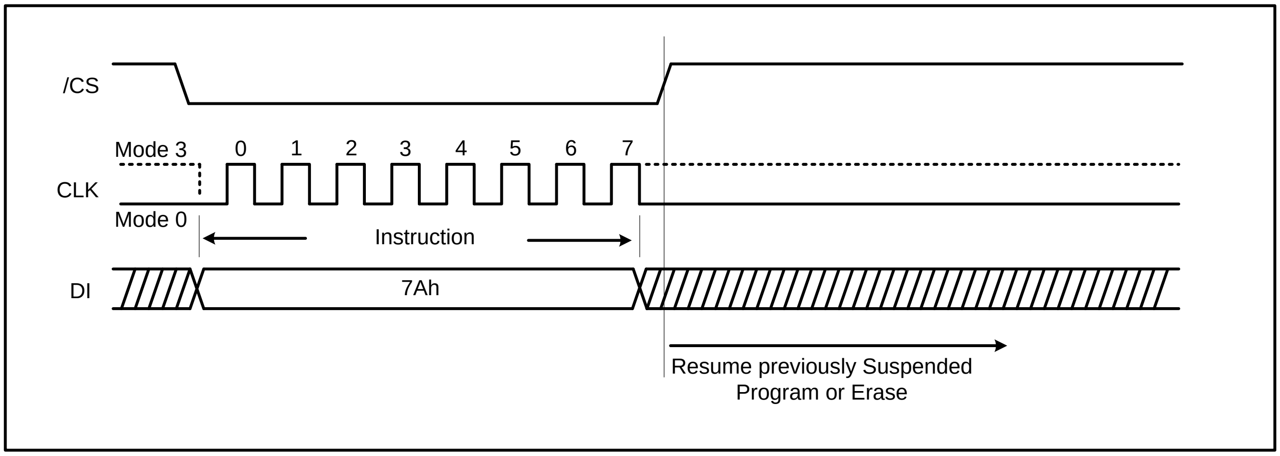


Figure 27a. Erase/Program Resume Instruction (SPI Mode)

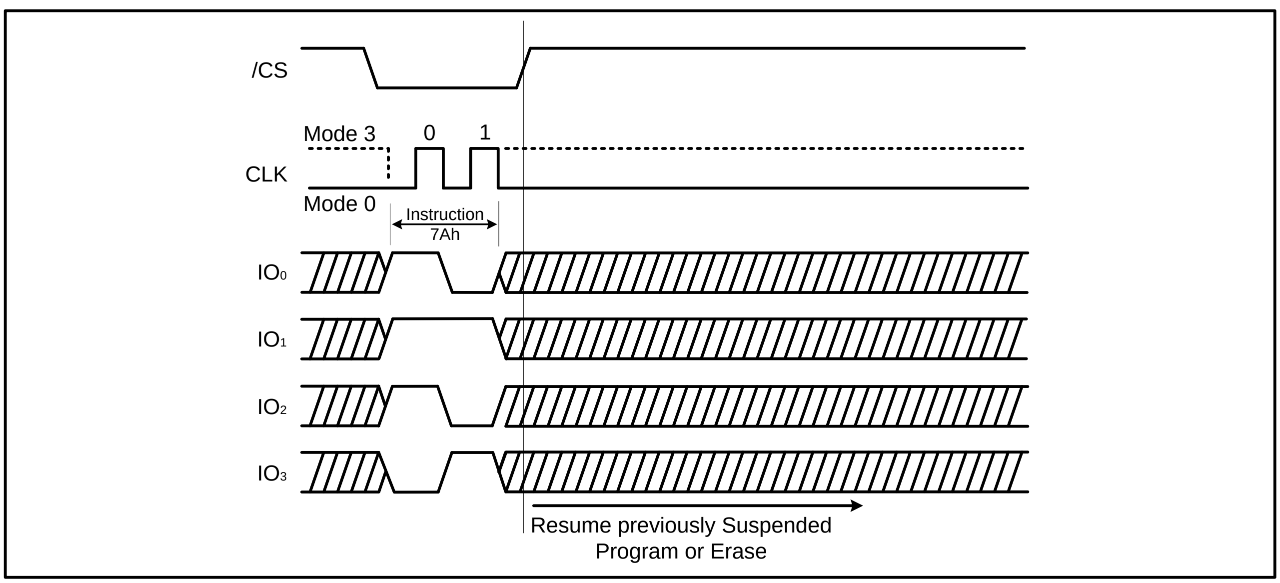


Figure 27b. Erase/Program Resume Instruction (QPI Mode)

8.2.33. Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 28a & 28b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power- down / Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Deep Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

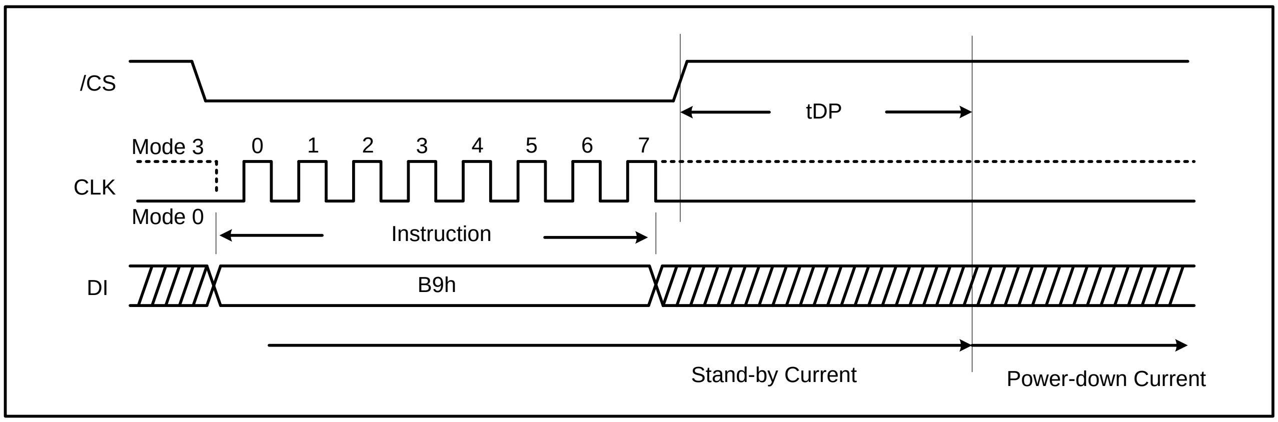


Figure 28a. Deep Power-down Instruction (SPI Mode)

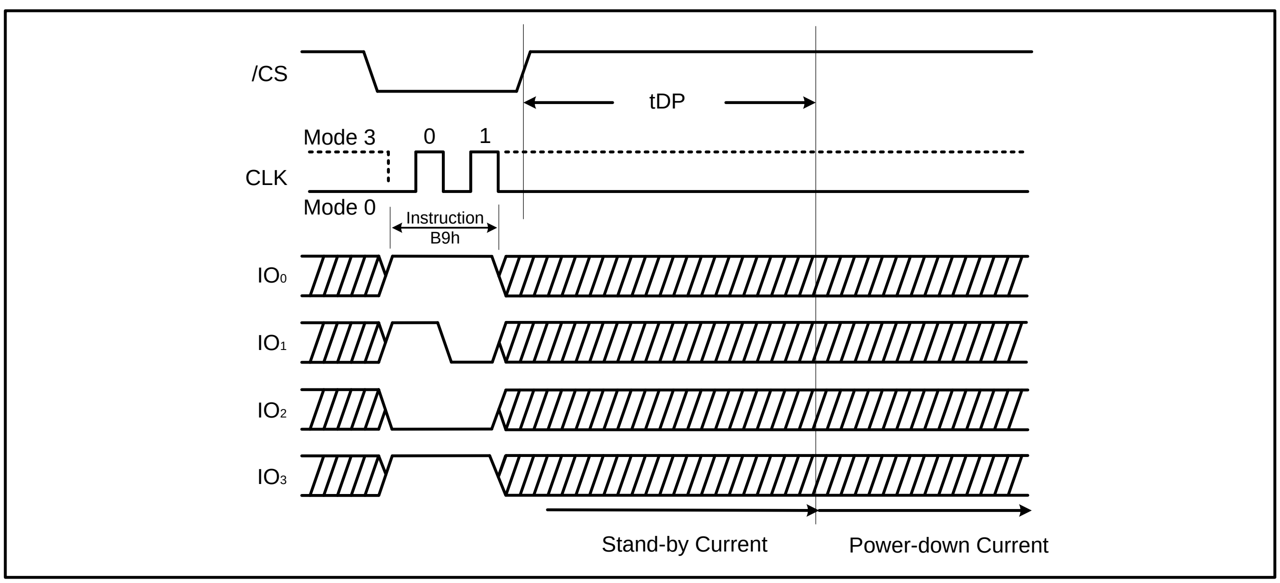


Figure 28b. Deep Power-down Instruction (QPI Mode)

8.2.34. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high as shown in Figure 29a & 29b. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the DS25M4AB is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 29c & 29d, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

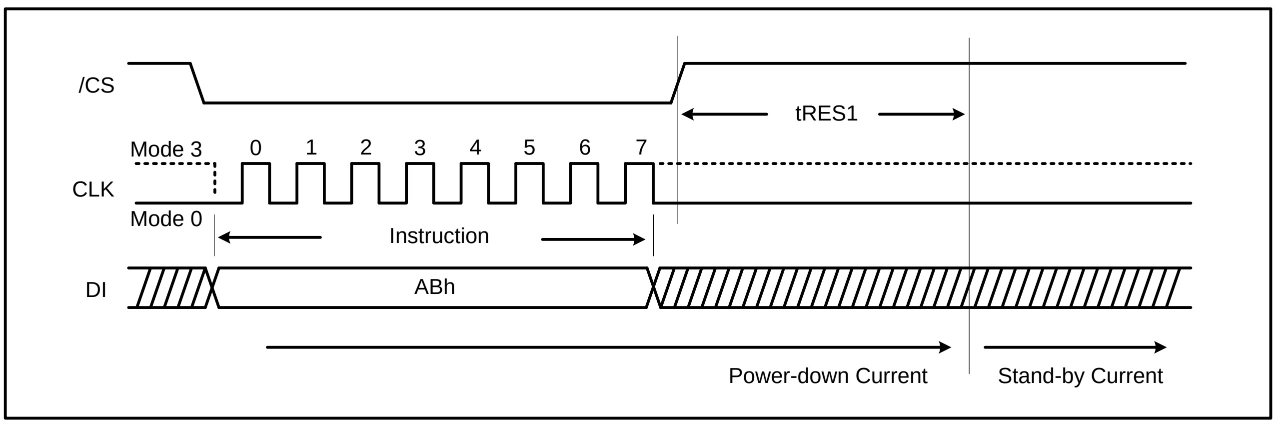


Figure 29a. Release Power-down Instruction (SPI Mode)

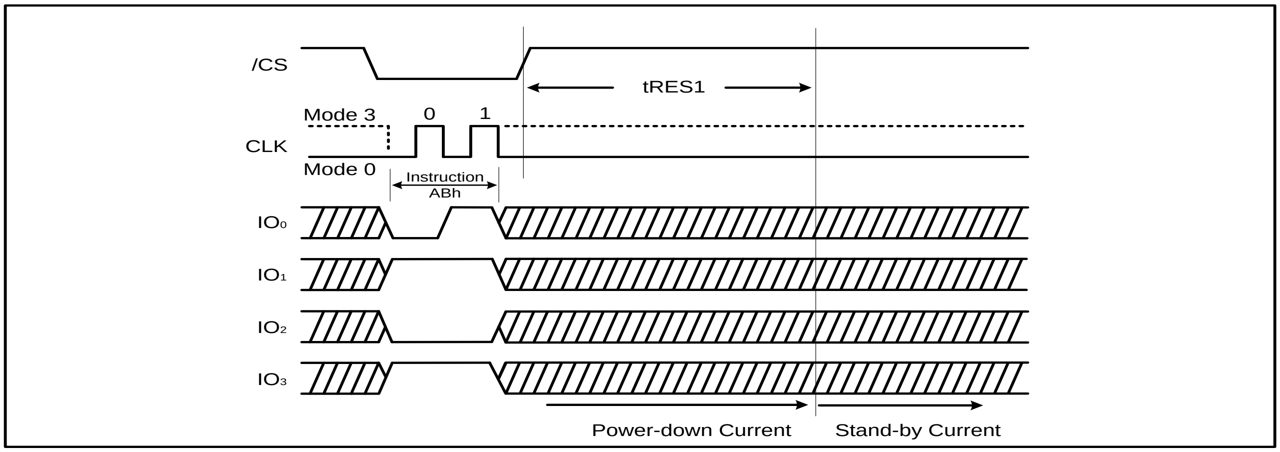


Figure 29b. Release Power-down Instruction (QPI Mode)

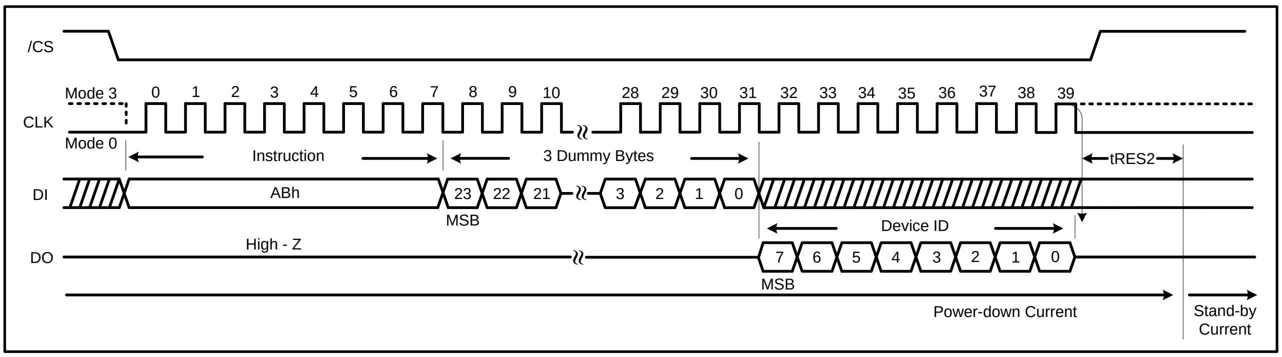


Figure 29c. Release Power-down / Device ID Instruction (SPI Mode)

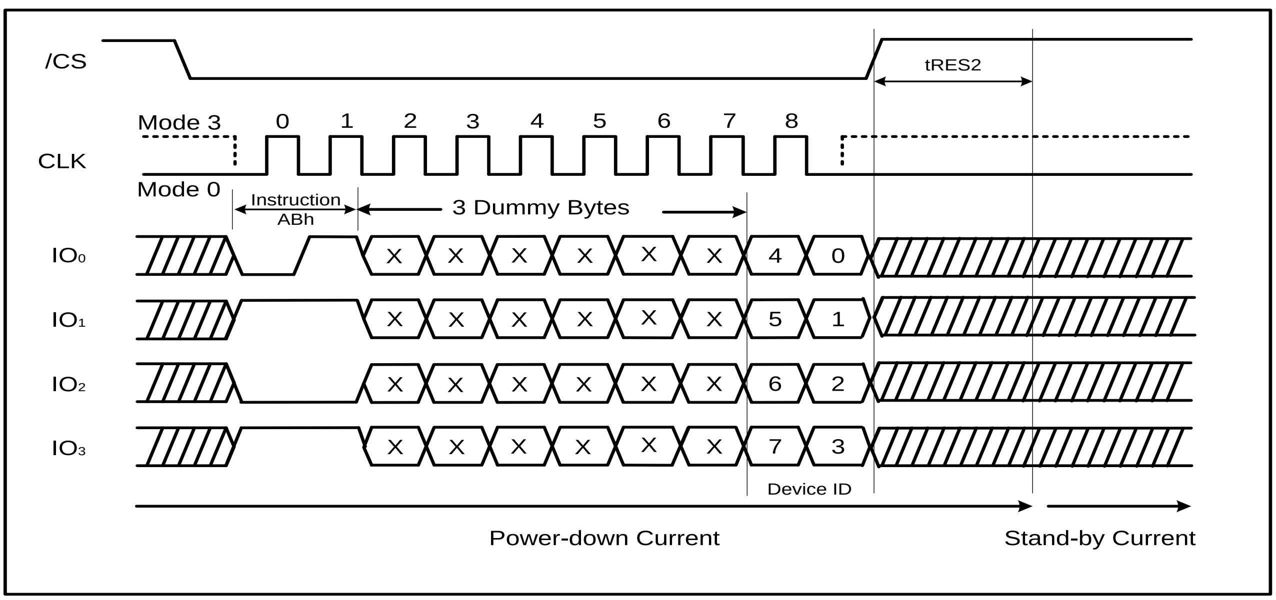


Figure 29d. Release Power-down / Device ID Instruction (QPI Mode)

8.2.35. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Dosilicon (E5h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 30. The Device ID values for the DS25M4AB are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

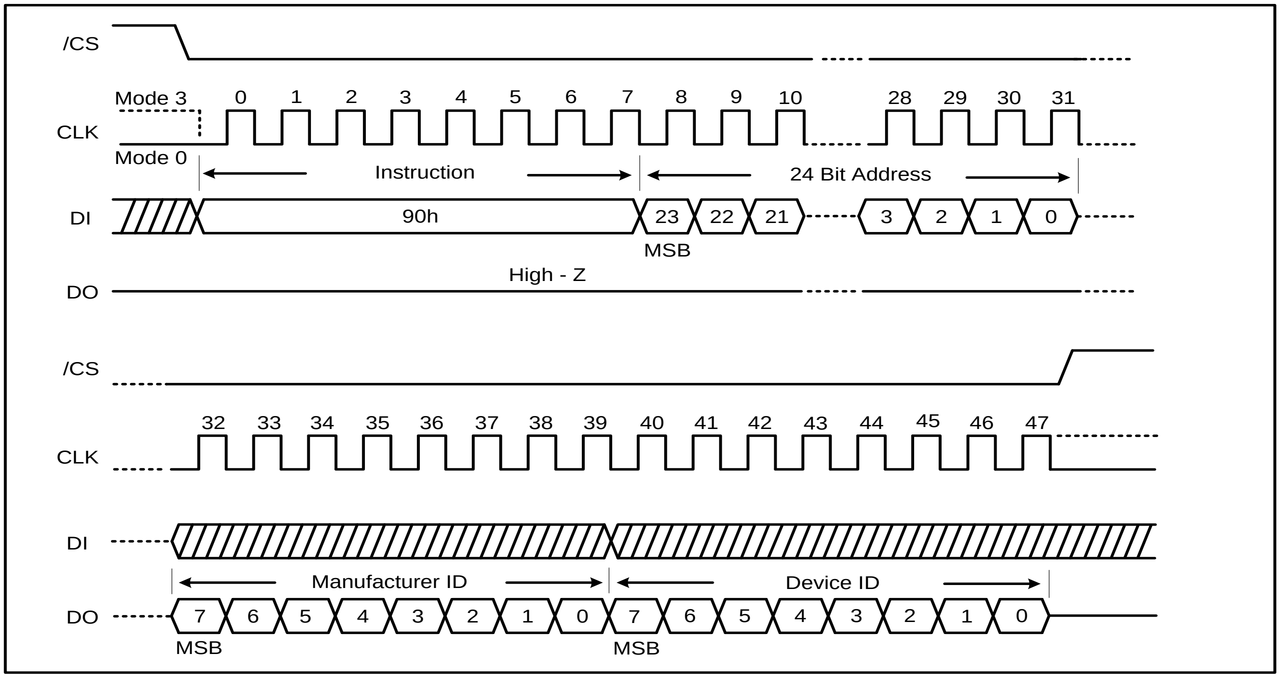


Figure 30a. Read Manufacturer / Device ID Instruction (SPI Mode)

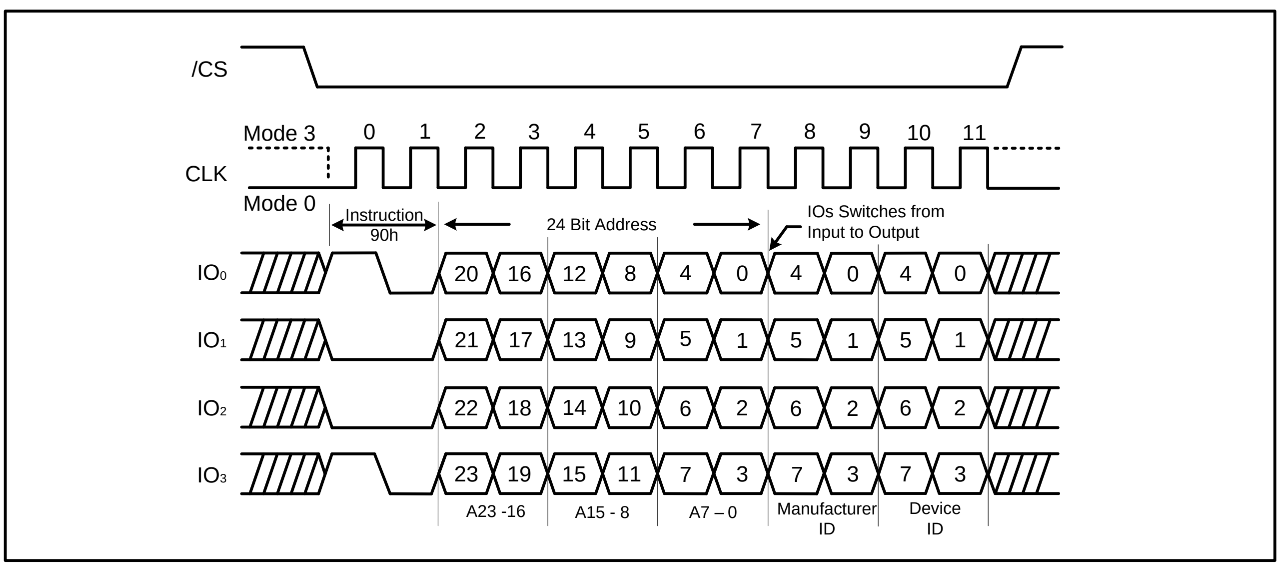


Figure 30b. Read Manufacturer / Device ID Instruction (QPI Mode)

8.2.36. Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Dosilicon (E5h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 31. The Device ID values for the DS25M4AB are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

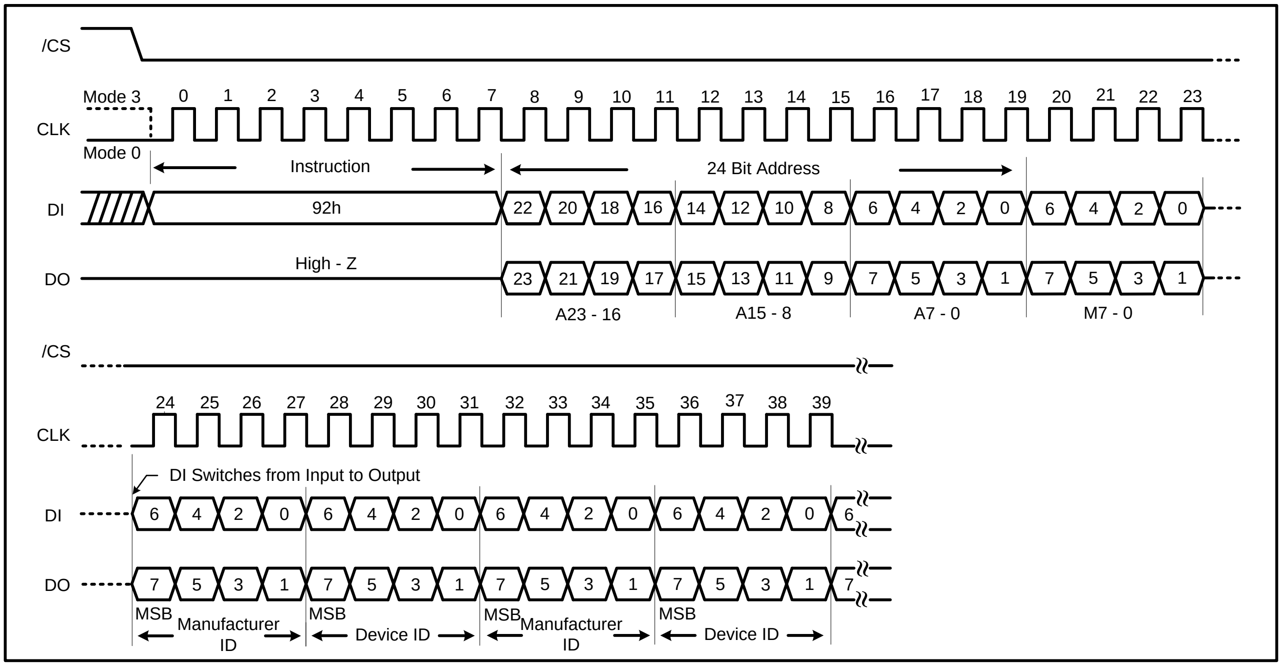


Figure 31. Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

Note:

The "Continuous Read Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

8.2.37. **Read Manufacturer / Device ID Quad I/O (94h)**

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Dosilicon (E5h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 32. The Device ID values for the DS25M4AB are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

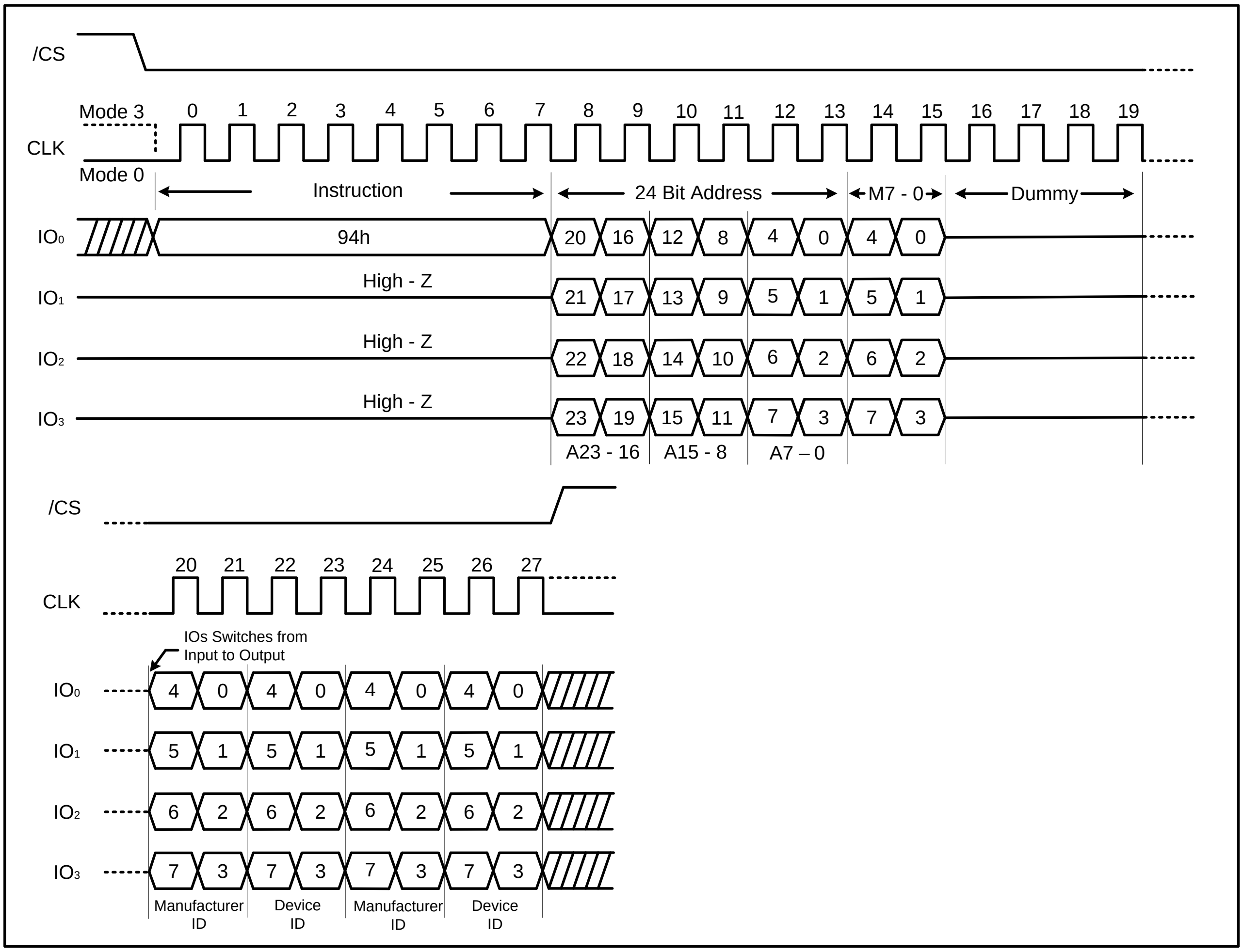


Figure 32. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

Note:

The "Continuous Read Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

8.2.38. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each DS25M4AB device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 33.

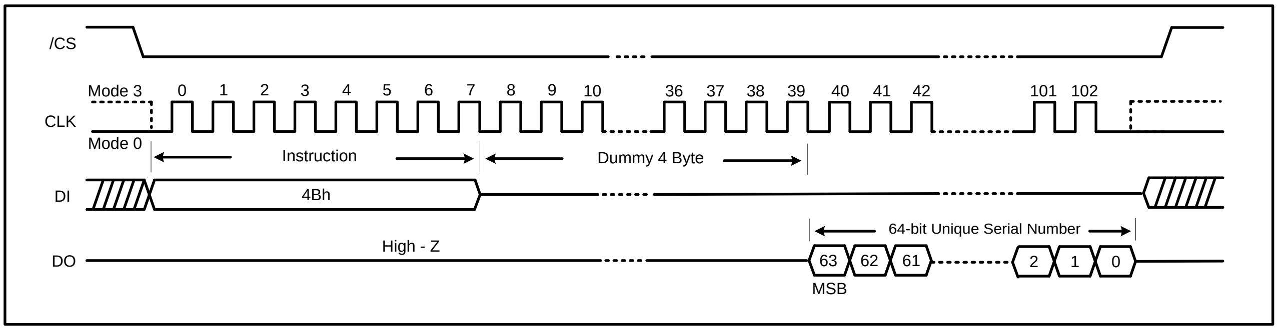


Figure 33. Read Unique ID Number Instruction (SPI Mode only)

8.2.39. **Read JEDEC ID (9Fh)**

For compatibility reasons, the DS25M4AB provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code "9Fh". The JEDEC assigned Manufacturer ID byte for Dosilicon (E5h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 34a & 34b. For memory type and capacity values refer to Manufacturer and Device Identification table.

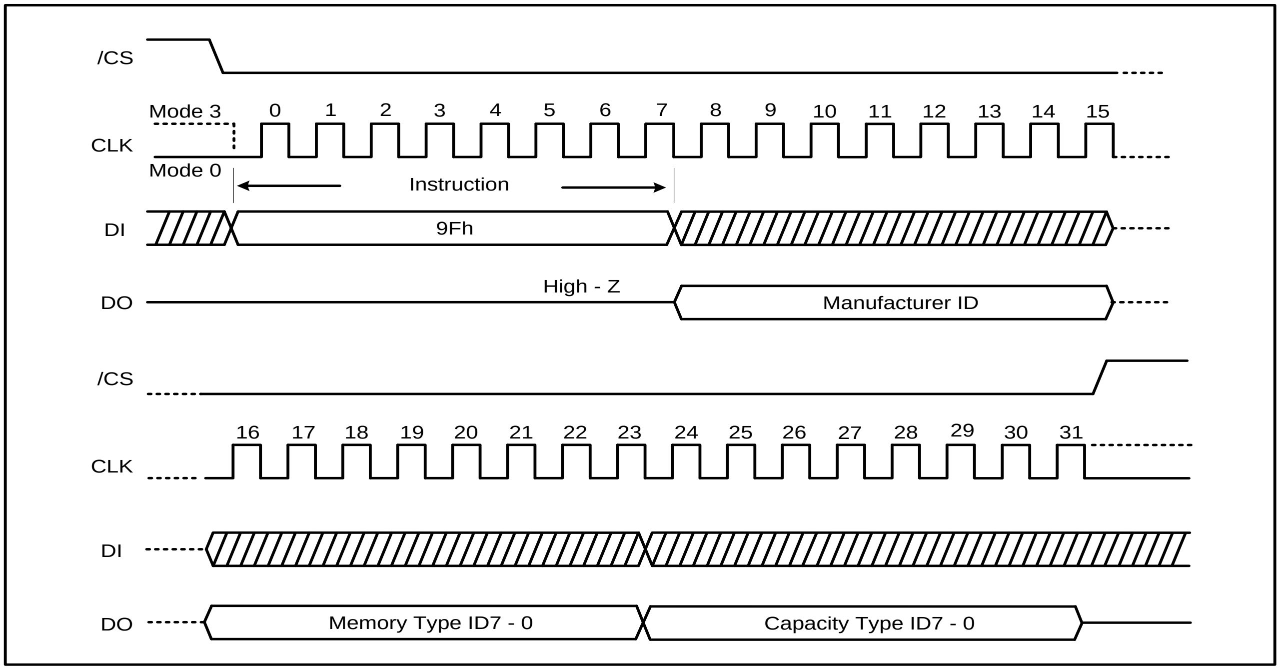


Figure 34a. Read JEDEC ID Instruction (SPI Mode)

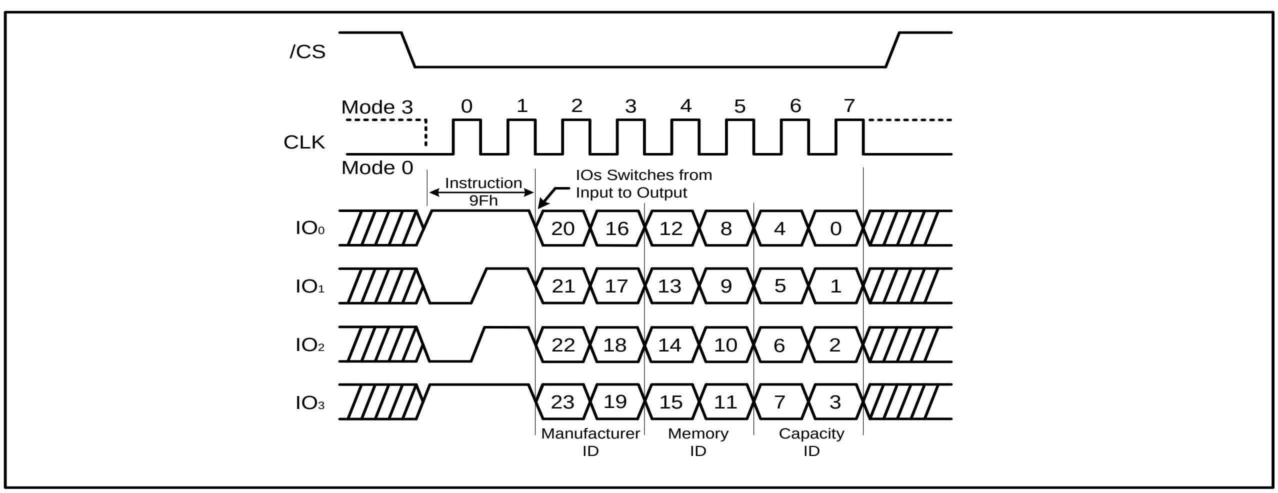


Figure 34b. Read JEDEC ID Instruction (QPI Mode)

8.2.40. Read SFDP Register (5Ah)

The DS25M4AB features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 35. For SFDP register values and descriptions, please refer to the Dosilicon Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

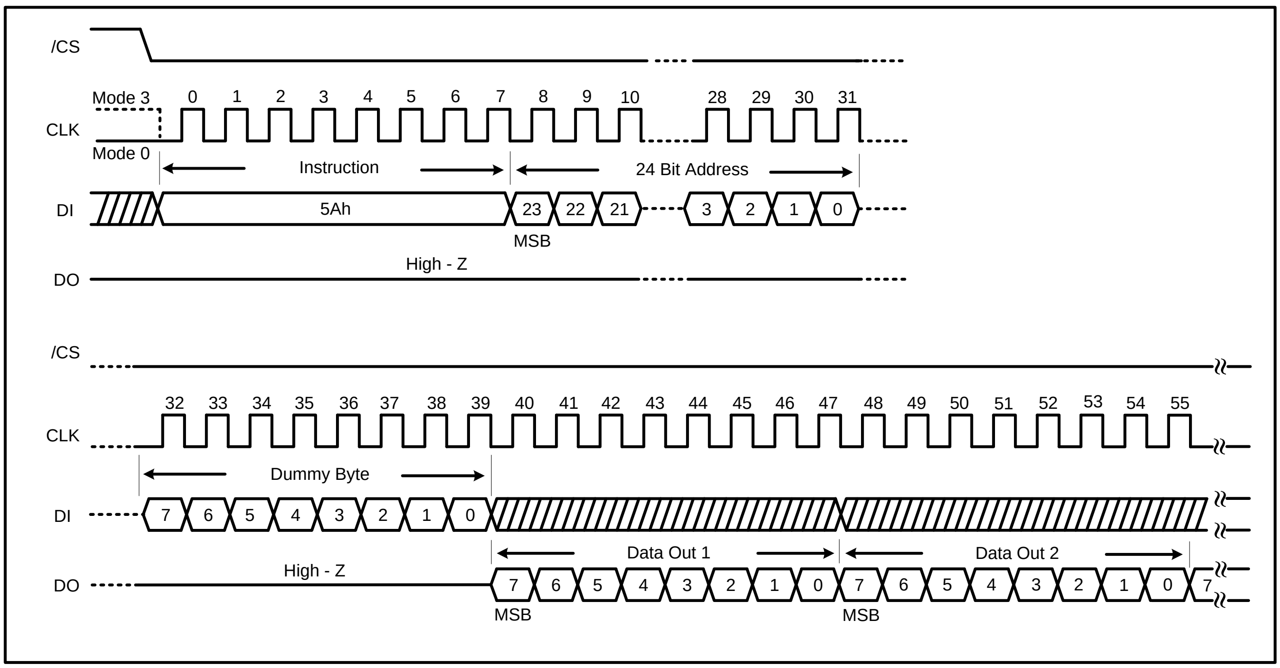


Figure 35. Read SFDP Register Instruction Sequence Diagram

8.2.41. **Erase Security Registers (44h)**

The DS25M4AB offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don't Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don't Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don't Care

The Erase Security Register instruction sequence is shown in Figure 36. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 7.1.8 for detail descriptions).

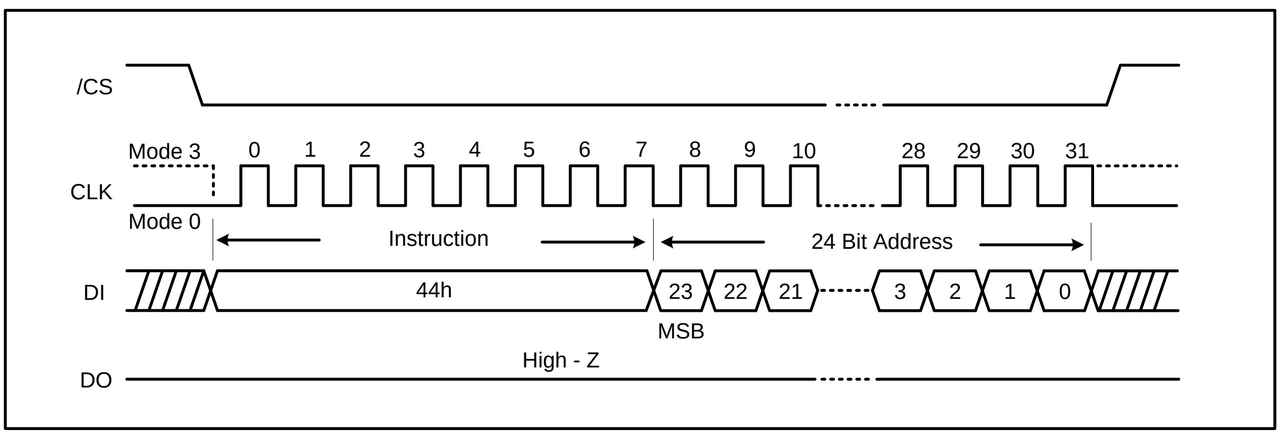


Figure 36. Erase Security Registers Instruction (SPI Mode only)

8.2.42. Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 37. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See Section “Security Register Lock Bits(LB3, B2, LB1) for detail descriptions).

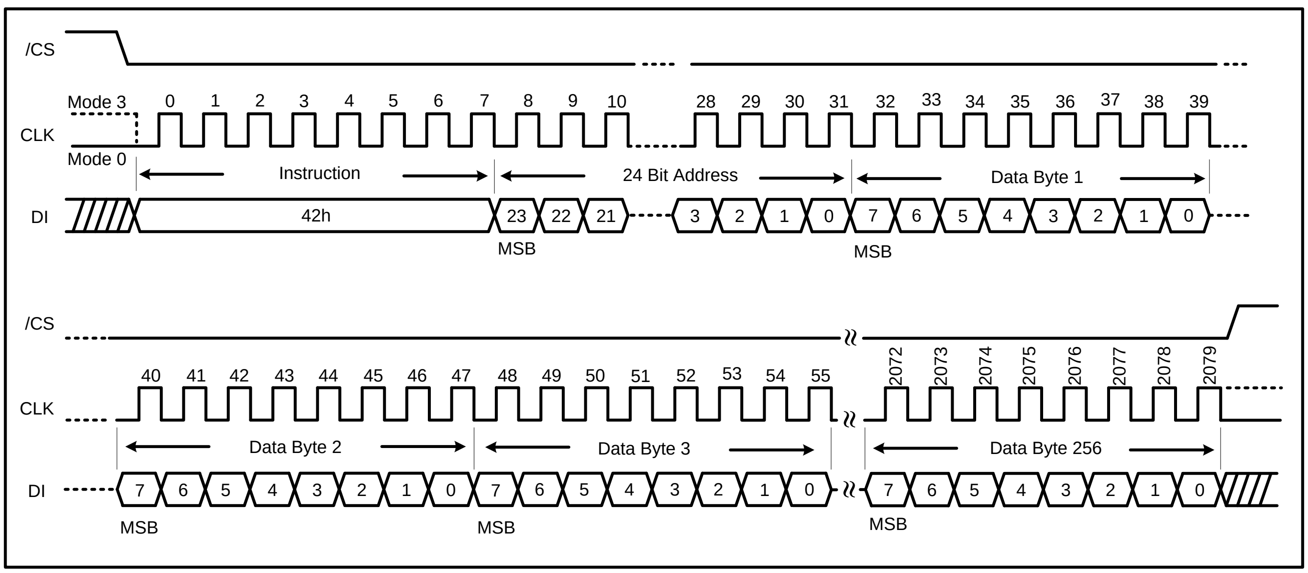


Figure 37. Program Security Registers Instruction (SPI Mode only)

8.2.43. Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 38. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

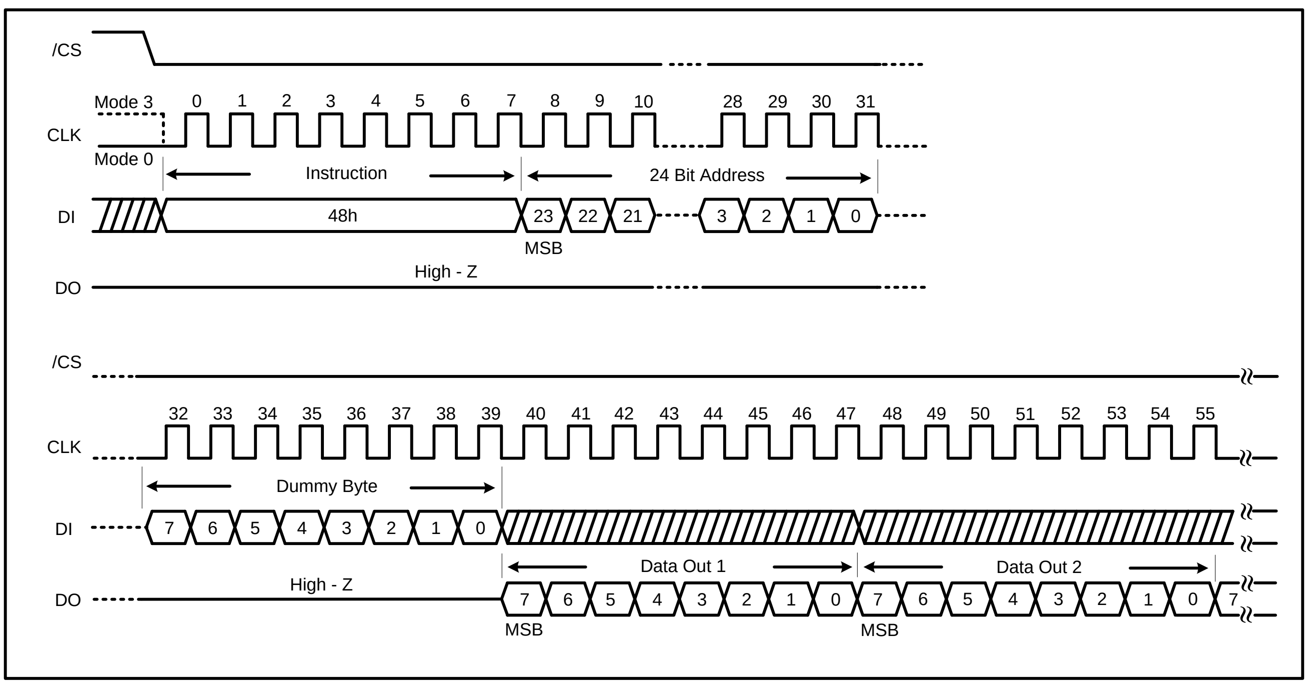


Figure 38. Read Security Registers Instruction (SPI Mode only)

8.2.44. **Set Read Parameters (C0h)**

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” instructions, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” instruction.

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction Table 1-2 for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2. The number of dummy clocks is only programmable for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ.	P1 – P0	WRAP LENGTH
0 0	2	40MHz	0 0	8-byte
0 1	4	80MHz	0 1	16-byte
1 0	6	104MHz	1 0	32-byte
1 1	8	104MHz	1 1	64-byte

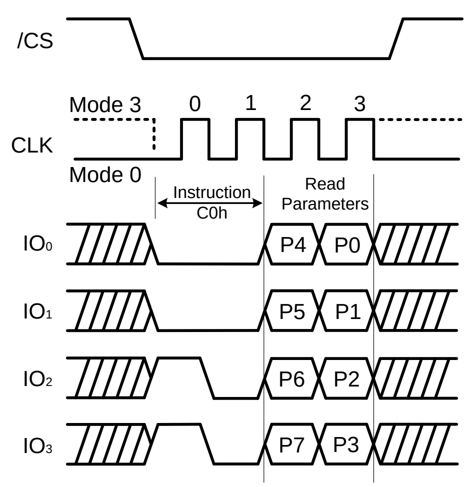


Figure 39. Set Read Parameters Instruction (QPI Mode only)

8.2.45. Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

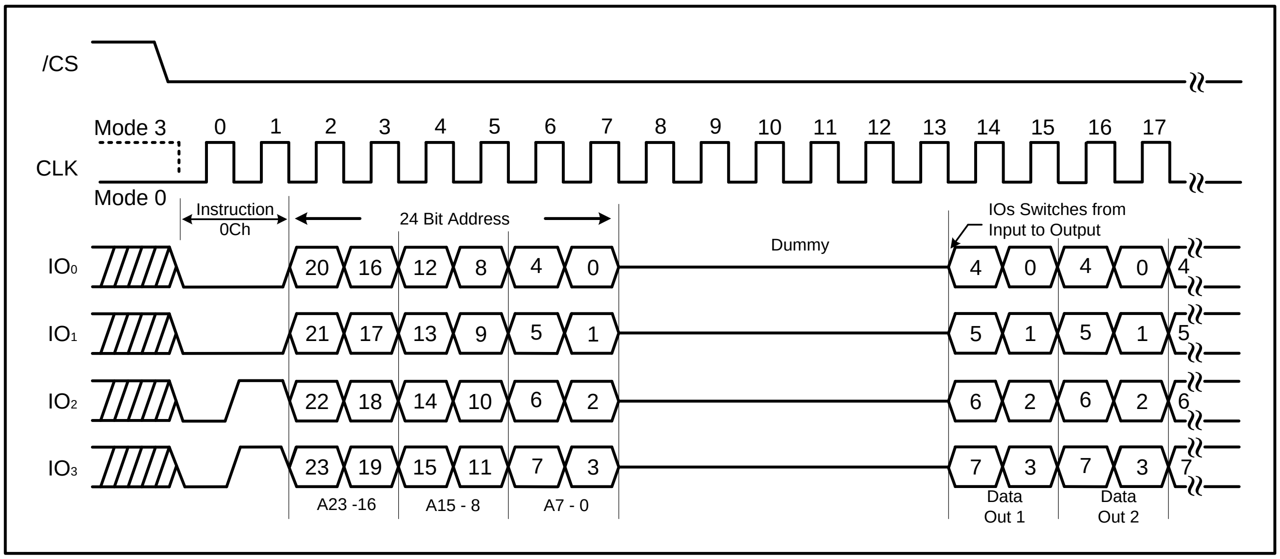


Figure 40. Burst Read with Wrap Instruction (QPI Mode only)

8.2.46. Enter QPI Mode (38h)

The DS25M4AB support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Dosilicon serial flash memories. See Instruction Set Table 1-3 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 3 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

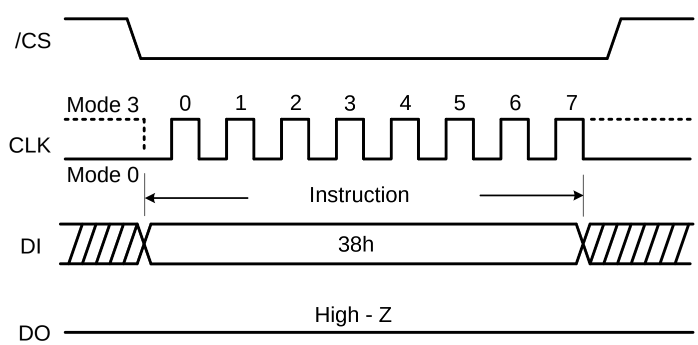


Figure 41. Enter QPI Instruction (SPI Mode only)

8.2.47. Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

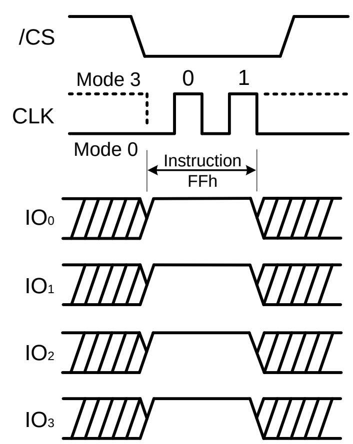


Figure 42. Exit QPI Instruction (QPI Mode only)

8.2.48. **Enable Reset (66h) and Reset Device (99h)**

Because of the small package and the limitation on the number of pins, the DS25M4AB provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

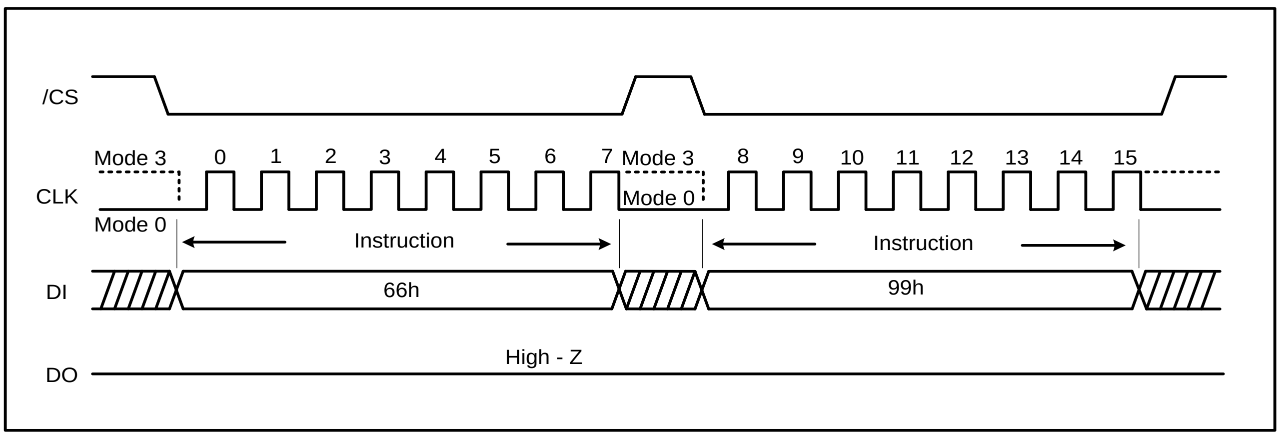


Figure 43a. Enable Reset and Reset Instruction Sequence (SPI Mode)

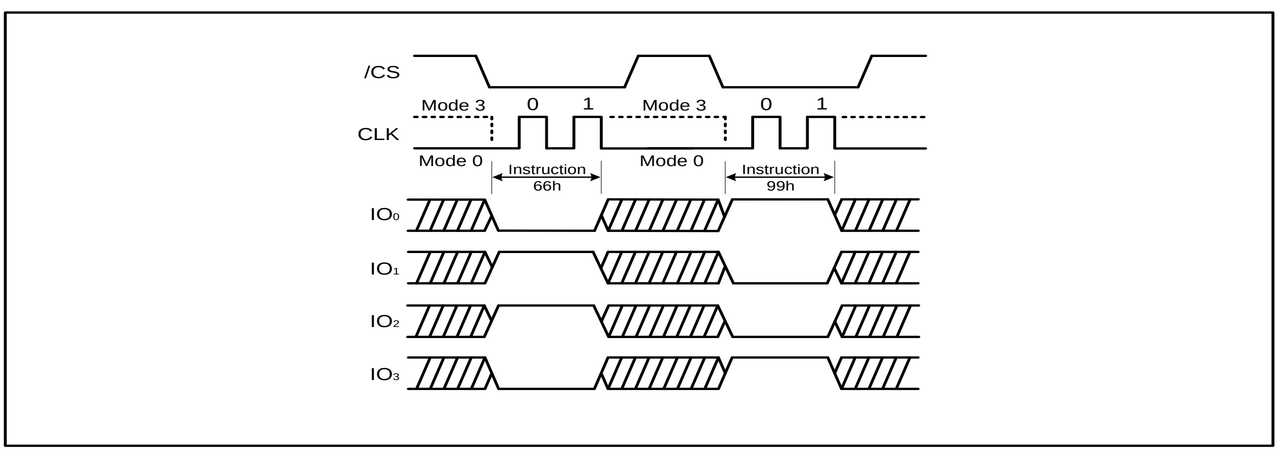


Figure 43b. Enable Reset and Reset Instruction Sequence (QPI Mode)

9. ELECTRICAL CHARACTERISTICS

9.1. Absolute Maximum Ratings (1)(2)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to VCC+0.4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	℃
Lead Temperature	TLEAD(3)		See Note (3)	℃
Electrostatic Discharge Voltage	VESD(2)	Human Body Model	–2000 to +2000	V

Notes:

1.This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

2.JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

3.Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.

9.2. Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC (1)	FR = 104MHz, fR = 50MHz	1.65	1.95	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
Ambient Temperature, Operating	TA	Industrial	–40	+125	°C

Note:

1.VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

9.3. Power-Up Power-Down Timing and Requirements(1)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to Device Operation	t_{VSL}	1.5		ms
Write Inhibit Threshold Voltage	V_{WI}	1.0	1.4	V

Note: 1. These parameters are characterized only.

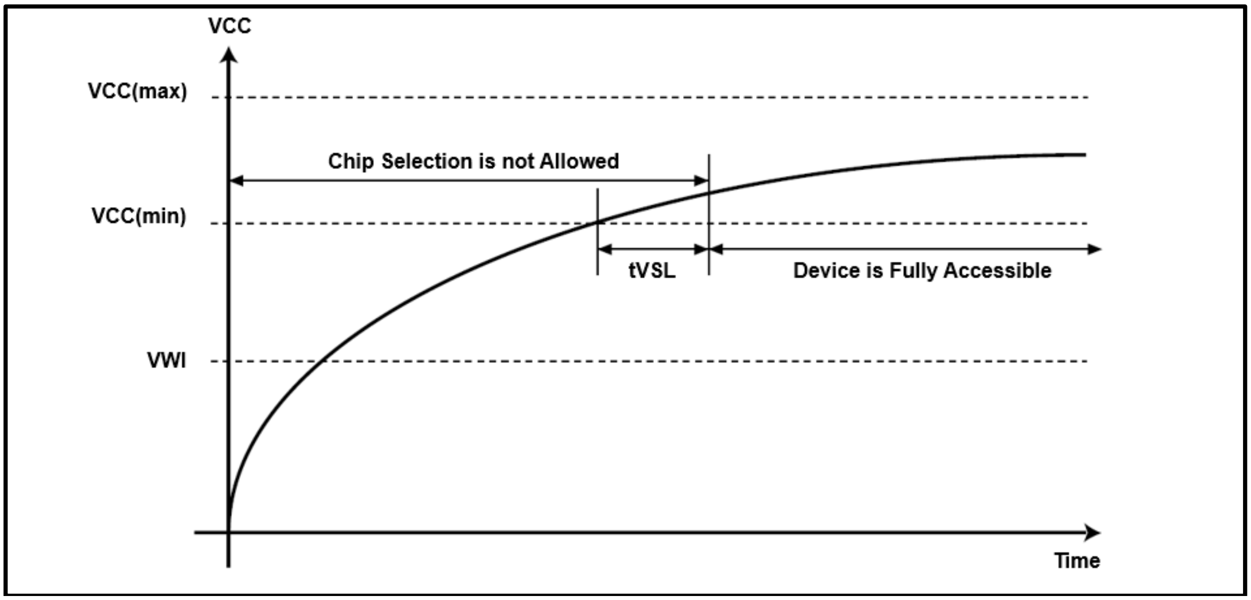


Figure 44a. Power-up Timing and Voltage Levels

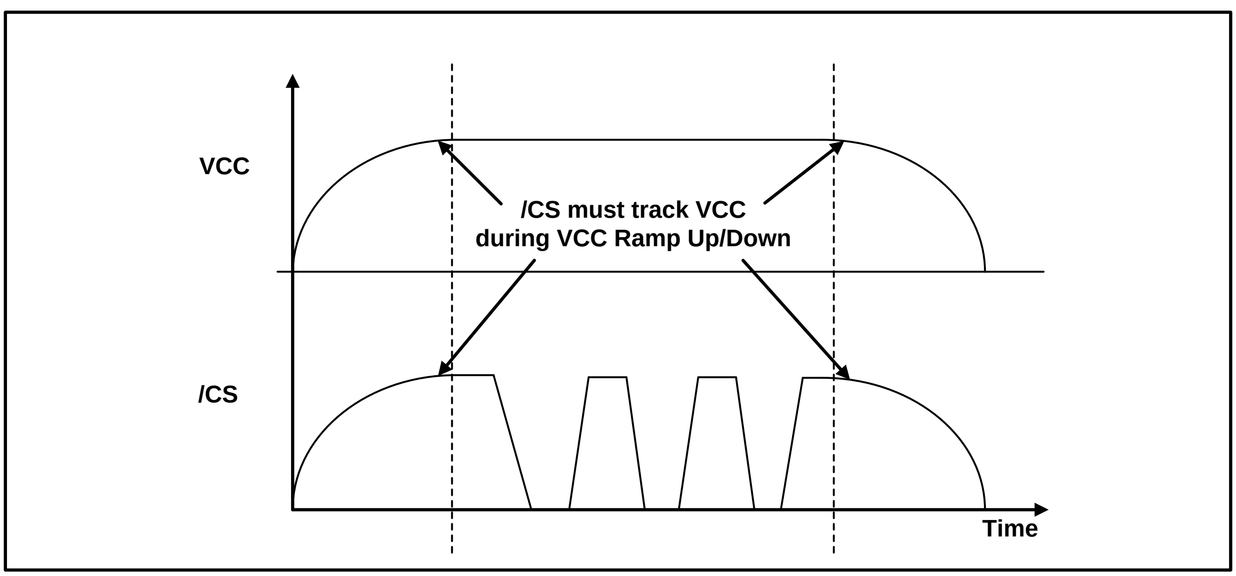


Figure 44b. Power-up, Power-Down Requirement

9.4. DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = V_{CC}, V_{IN} = GND or VCC		10	50	µA
Deep Power-down Current	I_{CC2}	/CS = VCC, V_{IN} = GND or V_{CC}		1	20	µA
Operating Current (Read)	I_{CC3}	CLK = 0.1 VCC / 0.9 V_{CC} at 104MHz, DQ = open(1,2,4 I/O)		13	18	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 50MHz, DQ = open(1,2,4 I/O)		11	16	mA
Operating Current (PP)	I_{CC4}	CS# = V_{CC}		16	20	mA
Operating Current (WRSR)	I_{CC5}	CS# = V_{CC}		8	12	mA
Operating Current (SE,BE)	I_{CC6}	CS# = V_{CC}		16	20	mA
Operating Current (CE)	I_{CC7}	CS# = V_{CC}		16	20	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC -0.2			V

9.5. AC Measurement Conditions(1)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

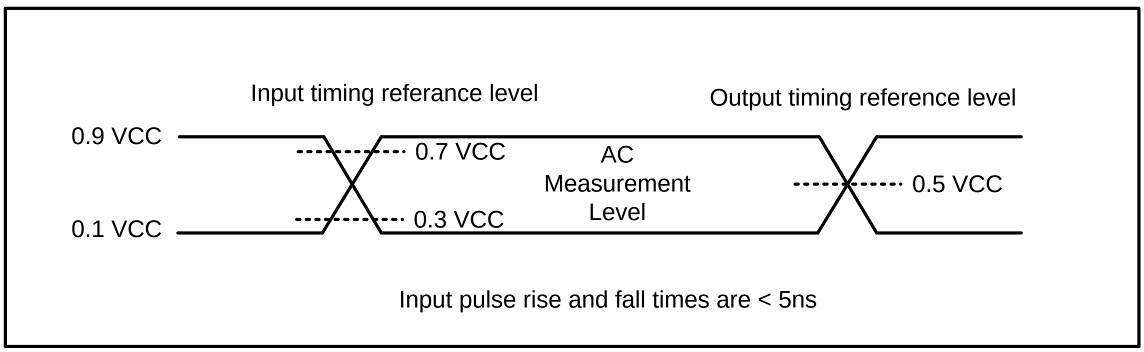


Figure 45. AC Measurement I/O Waveform

9.6. AC Electrical Characteristics(5)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Serial Clock Frequency for: FAST_READ, QPP, PP, SE, HBE, BE, DP, RES, WREN, WRDI, WRSR, RDSR, RDID, Dual Output Fast Read, Dual I/O Fast Read	fc	f_{C1}	D.C.		104	MHz
Serial Clock Frequency for: Quad Output, Quad I/O Fast Read, Quad I/O Word Read and Burst Read	fc	f_{C2}	D.C.		104	MHz
Serial Clock Frequency for Quad I/O DTR Read	fc	f_{C3}	D.C		66	MHz
Clock frequency for Read	f_R		D.C.		50	MHz
Clock High, Low Time except DTR Read	t_{CLH1}, t_{CLL1}(1)		4			ns
Clock High, Low Time for DTR Read	t_{CLH2}, t_{CLL2}(1)		5.6			ns
Serial Clock Rise Time (Slew Rate)	t_{CLCH}(2)		0.1			V/ns
Serial Clock Fall Time (Slew Rate)	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		5			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		5			ns
/CS Deselect Time (for Read)	t_{SHSL1}	t_{CSH}	15			ns
/CS Deselect Time (for Erase or Program or write)	t_{SHSL2}	t_{CSH}	30			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			6	ns
Clock Low to Output Valid for 30pF	t_{CLQV}	t_V			7	ns
Clock Low to Output Valid for 15pF	t_{CLQV}	t_V			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns

Continued – next page AC Electrical Characteristics (cont'd)

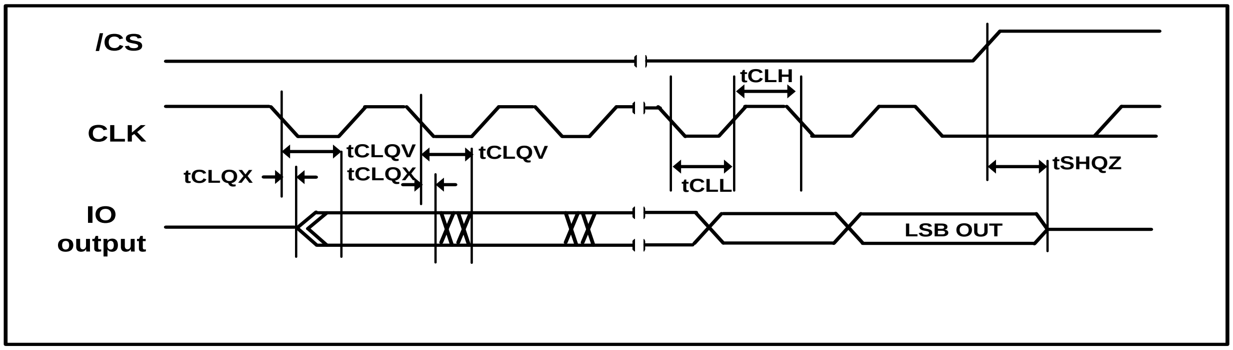
AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			6	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			6	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				30	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				30	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device	t_{RESET}(2)(4)		1			µs
Write Status Register Time	t_W			10	30	ms
Page Program Time	t_{PP}			0.7	3	ms
Sector Erase Time (4KB)	t_{SE}			50	300	ms
Block Erase Time (32KB)	t_{BE1}			0.15	0.9	s
Block Erase Time (64KB)	t_{BE2}			0.3	1.8	s
Chip Erase Time	t_{CE}			40	100	s
Software Reset Latency (WIP = write operation)	t_{SR}				28	µs
Software Reset Latency (WIP = not in write operation)	t_{SR}				0	µs

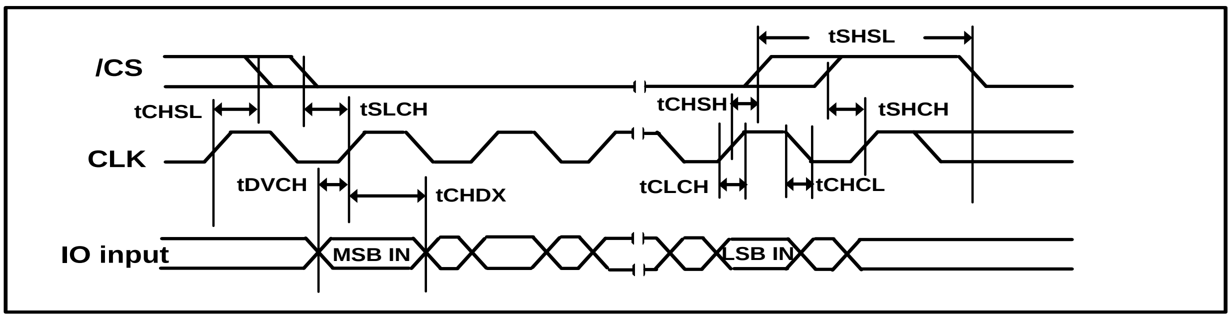
Notes:

1.Clock high + Clock low must be less than or equal to 1/fC.
2.Value guaranteed by design and/or characterization, not 100% tested in production.
3.Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).
4.It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.

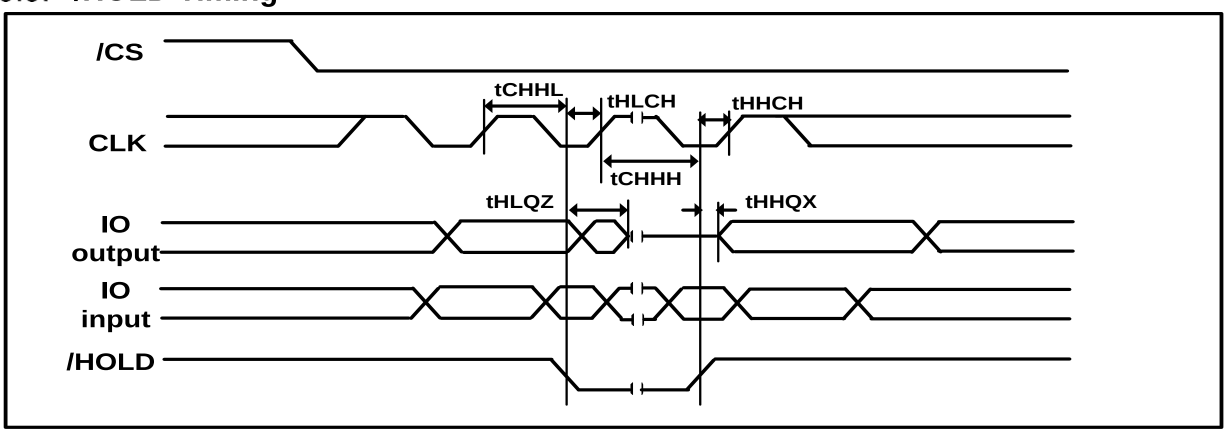
9.7. Serial Output Timing



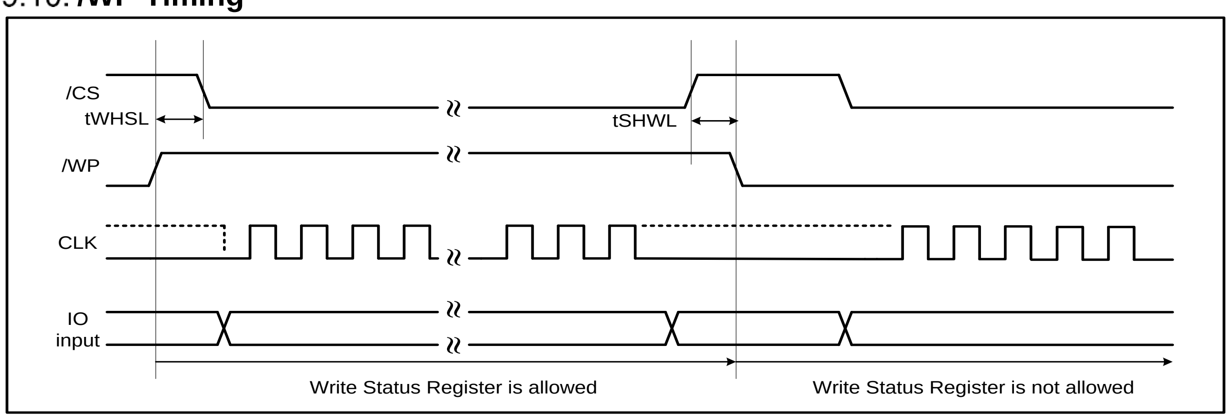
9.8. Serial Input Timing



9.9. /HOLD Timing

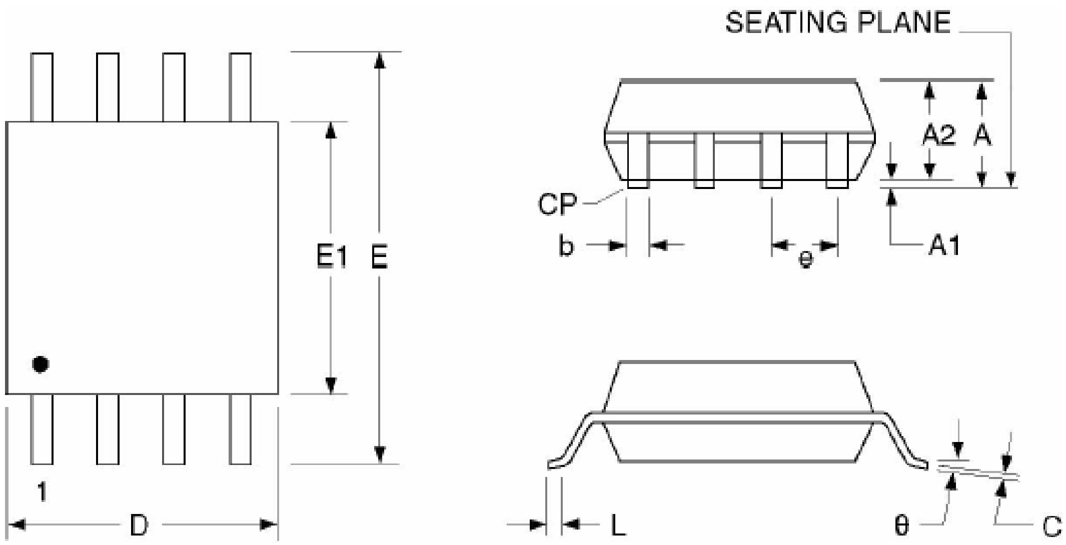


9.10. /WP Timing



10. PACKAGE SPECIFICATIONS

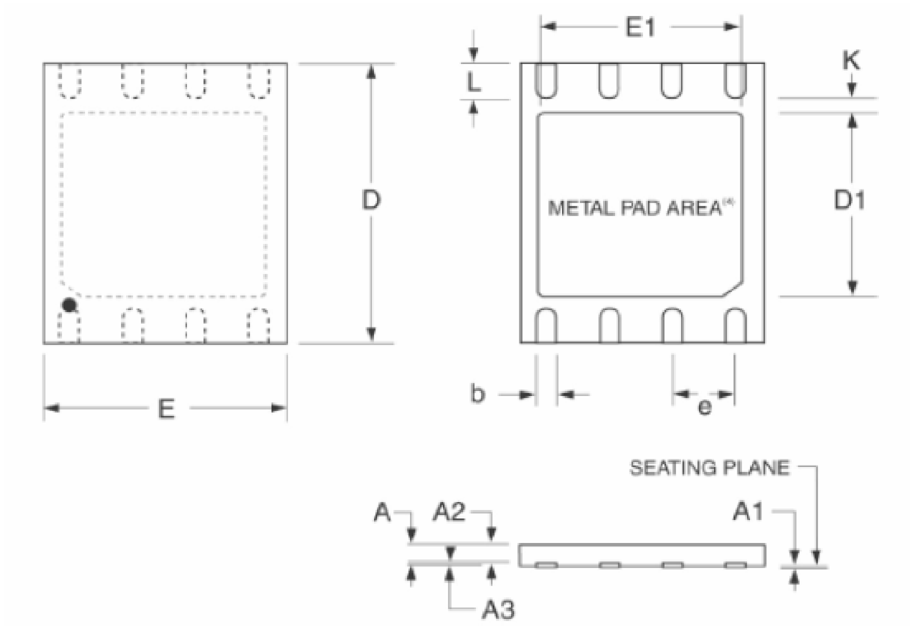
10.1. 8-Pin SOP 208-mil



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
B	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	1.27 BSC			0.050 BSC		
L	0.50	0.65	0.80	0.020	0.026	0.031
Θ	0˚	-	8˚	0˚	-	8˚
Seating Plane	-	-	0.10	-	-	0.004

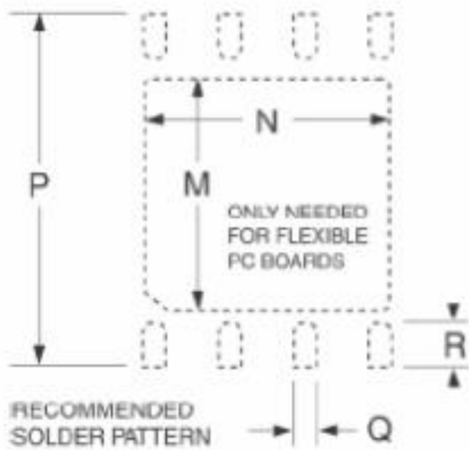
Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

10.2. 8-contact 6x5 WSON



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.25	4.30	4.35	0.1673	0.1692	0.1712
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

10.3. 8-contact 6x5 WSON (cont'd)



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
SOLDER PATTERN						
M		3.40			0.1338	
N		4.30			0.1692	
P		6.00			0.2360	
Q		0.50			0.0196	
R		0.65			0.0255	

Notes:

1. Advanced Packaging Information; please contact Dosilicon Co., Ltd. for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB bias under the pad.

10.4. **8-pin WLCSP**

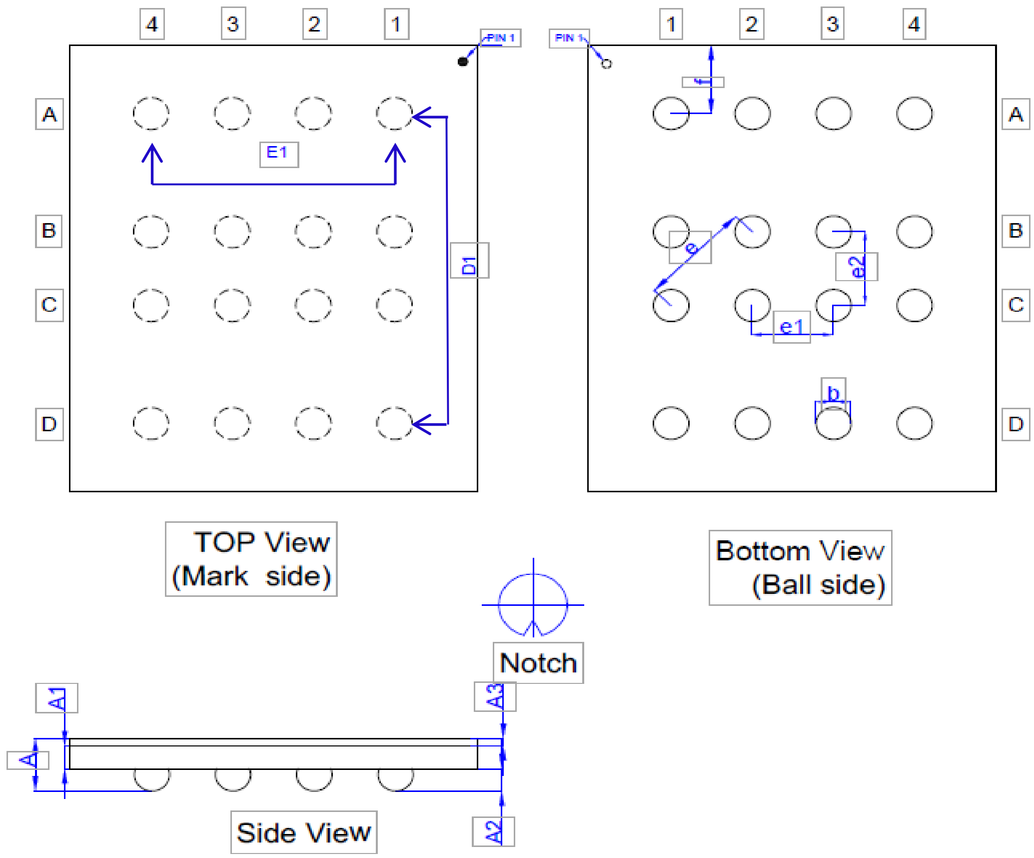
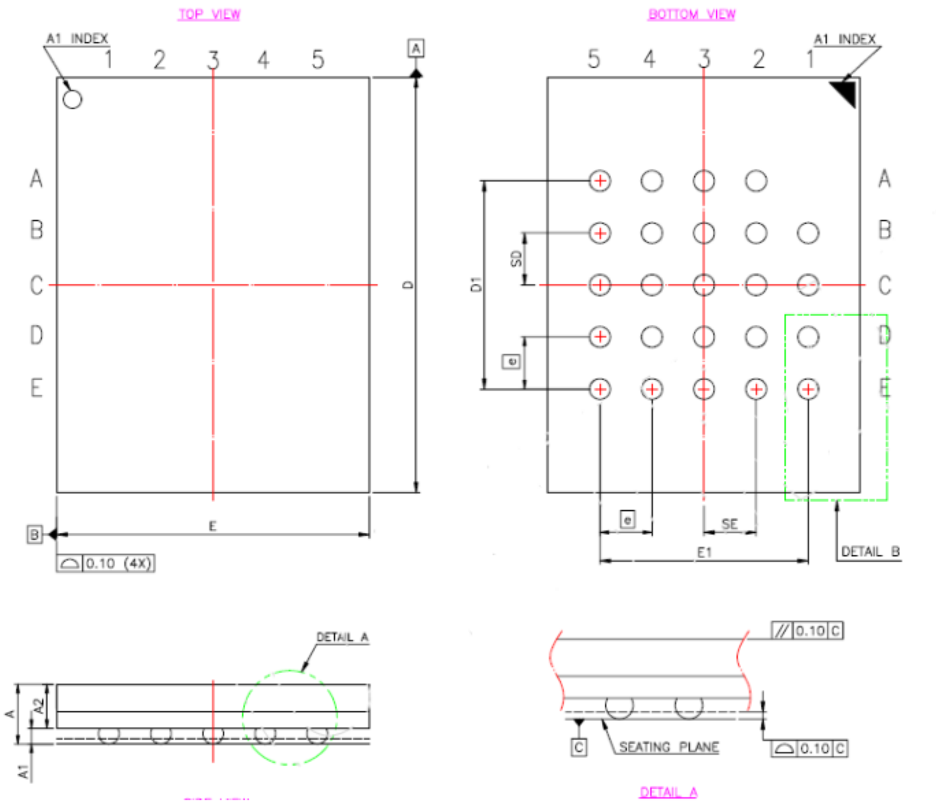


Table: Package Dimension				
Parameter	Symbol	Nominal(um)	Min(um)	Max(um)
Package Height	A	485	450	520
Package Body Thickness	A1	295	265	325
Ball Height	A2	165	145	185
BSC	A3	25		
Dimension x	E1	1500		
Dimension y	D1	2100		
Ball pitch	e	707.11 REF		
Ball pitch	e1	500		
Ball pitch	e2	500		
Ball Diameter	b	300	270	330
Ball Count		16 ea		

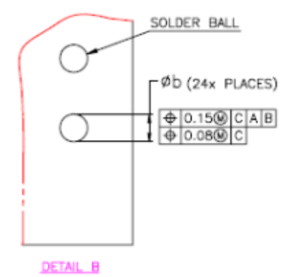
Note:
Please contact Dosilicon for full dimension information

10.5. **BGA24**



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.25	0.30	0.35
A2	—	0.79	—
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.



11. ORDERING INFORMATION

DS XXXXXX - XXXXX X

Dosilicon Memory

Product Family
25 : SPI

Organization
Q : Quad (2.7V ~ 3.6V)
M : Quad (1.65V ~ 1.95V)
W : Quad (1.65V ~ 3.6V)

Device Depth
04 : 4M
08 : 8M
16 : 16M
32 : 32M
64 : 64M
4A : 128M
4B : 256M
4S : 256M (2stack)

Generation
A : 1st
B : 2nd
C : 3rd

Speed
50 : 50Mhz
85 : 85Mhz
1A : 104Mhz
13 : 133Mhz

Packing Type
T : Tube (Standard)
R : Tape and Reel
Blank : Tray
* Package NO Marking

Business Package Type
0 : 8 Contact 4x4 USON 0.55t 0.4ld
1 : 8 Pin 208 mil SOIC
2 : 16 Pin 300 mil SOIC
3 : 8 Pin 300 mil PDIP
4 : 8 Contact 6x5 WSON
5 : 8 Pin 150 mil SOIC
6 : 8 Contact 8x6 WSON
7 : 8 Pin VSOP
8 : 24ball TFBGA
9 : 9 Contact 6x5 WSON
U : 8 Contact 3x2 USON 0.55t 0.35ld
X : 8 Contact 3x2 USON 0.55t 0.45ld
S : 8 Contact 3x3 USON 0.55t 0.4ld
N : 8 Contact 3x4 USON 0.55t 0.6ld
T : 8 Contact 3x2 USON 0.45t 0.45ld
Y : 8 Contact 3x4 USON 0.45t 0.6ld
R : 8 Contact 4x4 USON 0.45t 0.4ld
W : Wafer
M : Bumped Wafer
L : WLCSP

Core / IO Voltage
A : 3.0V / 3.0V
B : 1.8V / 1.8V
C : 1.65V ~ 3.6V

Temperature
I: Industrial (-40°C~85°C)
J : Industrial Plus (-40°C~105°C)
A1: Automotive/AEC-Q100 Grade1 (-40°C~125°C)