CX2001

GPS BT FM combo device

Features

- High co-existence and co-habitation performance with each subsystem working simultaneously at high performance
- Small dimensions: 3.80 x 4.07 x 0.6 (mm) in 85-ball WLCSP package with 0.4 mm pitch
- Minimal number of standard external components
- Shared clock and supply inputs for all functions
- Single-ended antenna ports
- Support for 1.8 V and direct Vbatt connection
- HCI commands to control all subsystems over the same shared UART interface
- System interfaces: UART, SPI, PCM, I2S, control interfaces, FM analog audio output, WLAN ePTA, and WiMAX PTA.
- Audio DSP: embedded BT wide band speech SBC codec, A2DP SBC stereo encoding and L2CAP encapsulation to reduce host processing and power consumption
- Direct loop-through mode from FM Rx audio to BT A2DP
- Application footprint on PCB <50mm^2 with less than 10 externals components

GPS features

- Advanced proprietary multipath algorithms for robust low-dropout tracking in indoor and outdoor urban canyons
- GSM, WCDMA and CDMA control plane aGPS assistance data standards
- SUPL user plane aGPS assistance data
- Exceeds 3GPP and TIA performance requirements
- -165 dBm low sensitivity limit for tracking (GPS), -161 dBm for acquisition (aGPS)
- Cold start 2 seconds aGPS and 38 seconds autonomous GPS (typical)
- Measurement engine with a search capacity of 35000 correlators
- 14 search and three track channels used to track up to 47 individual satellite signals
- Support the 1PPS industry standard interface

Bluetooth features

- Full compliance with Bluetooth specification version 4.0 (including Bluetooth Low Energy)
- Output power of up to 13 dBm
- -92 dBm sensitivity in basic rate
- Low power consumption: 140 µA (sniff), 12.4 mA (HV3) and 9.2 mA (2-EV3) in master modes

FM TX/RX features

- Embedded (loop) antenna support for FM TX/RX
- True worldwide FM RX band support (70 - 108 MHz), for wire antenna with single application
- FM TX on dual FM channel (with RDS AF list) for robust FM transmission
- R(B)DS modulator/demodulator and encoder/decoder compliant with EN 62106
- FM TX: up to 120 dBµV output power
- FM RX: 1.1 μV_{EMF} sensitivity and 7 μV_{EMF} RDS sensitivity
- Low power consumption: 12.6 mA in FM RX mode, 11.1 mA on 1.8 V and 3.8 mA on 2.5 V in FM TX mode

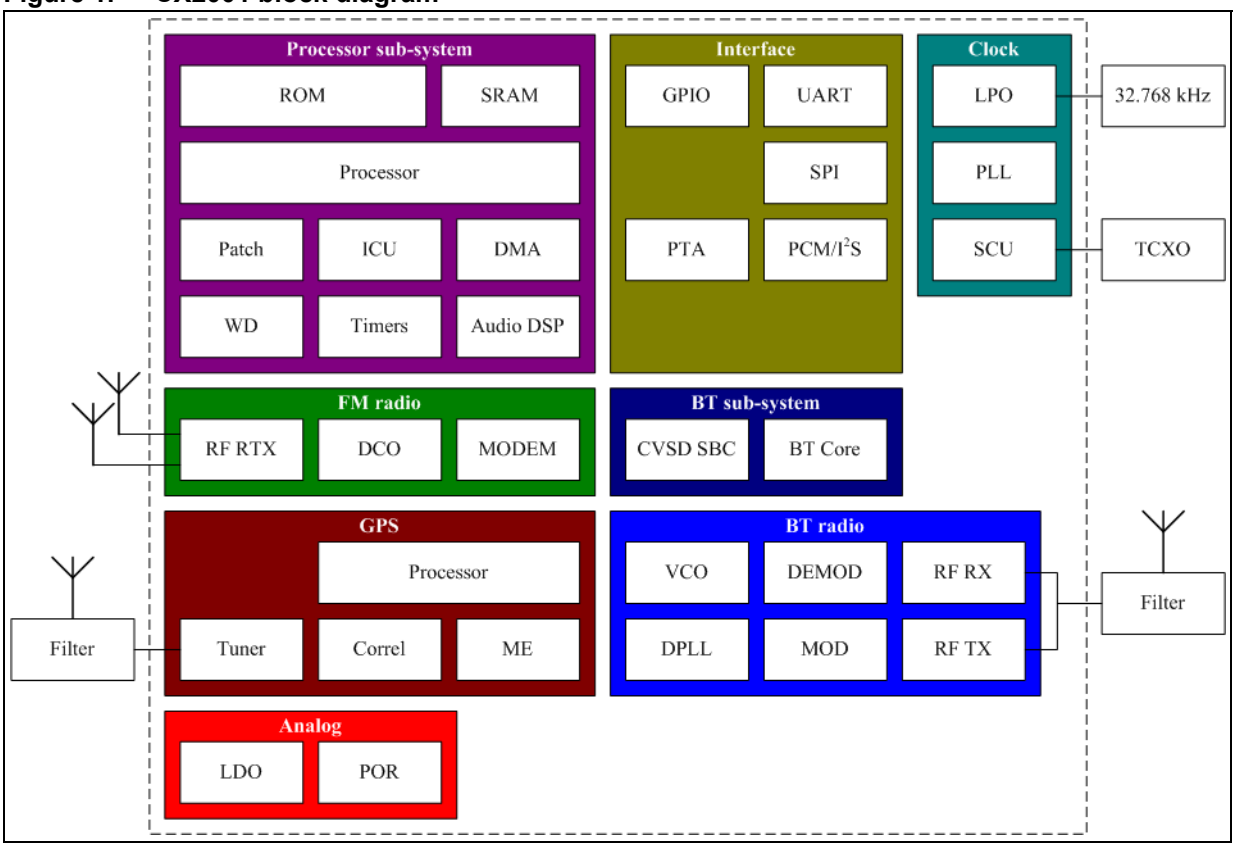
1 Overview and block diagram

The CX2001 is a monolithic combo integrating GPS Measurement Engine (ME), Bluetooth and Bluetooth Low Energy (BLE) and FM TX/RX. It is manufactured in 45 nm CMOS technology and provided in a WLCSP package. The CX2001 is optimized for best in class power consumption with a very high level of integration.

The CX2001 needs a low number of external components making integration in mobile applications easy.

1.1 Block diagram

Figure 1. CX2001 block diagram



The CX2001 is a monolithic GPS, BT+BLE and FM TX/RX controller in one WLCSP package and has a common HCI interface for all these subsystems.

The complete system is operated from a single 1.8 V nominal supply or from VBAT or from a combination of those. Separate ground connections are provided to reduce parasitic coupling effects.

The CX2001 combines:

- a GPS receiver with its measurement engine.
- a BT+BLE transceiver and core including a CVSD transcoder and supporting wide band speech SBC transcoding, as well as A2DP SBC stereo encoding.
- a FM TX/RX RDS radio with sound processing and RDS data handling.

The CX2001 is also integrating the industry standard ARM CortexM3 micro-controller with low power consumption feature, as well as ROM and SRAM memories. The communication with the external host is handled using the HCI (UART or SPI).

The CX2001 supports several industry standard interfaces such as UART, PCM, I2S, and SPI. It is designed to be used for BT wireless links operating in the ISM band (2400 MHz to 2483.5 MHz) without interfering with the FM band (70 MHz to 108 MHz) or the GPS L-band (1575.42 MHz).

The CX2001 provides maximum interface configuration flexibility and each interface can be used for multiple applications. The multiplexing of the interfaces is presented in *[10.]*

The CX2001 provides several data and voice paths configurations, which together with the audio DSP, allow to off-load the host processor and to support the different application use cases. Descriptions about these paths and off-loading capabilities are available in *[11.]*

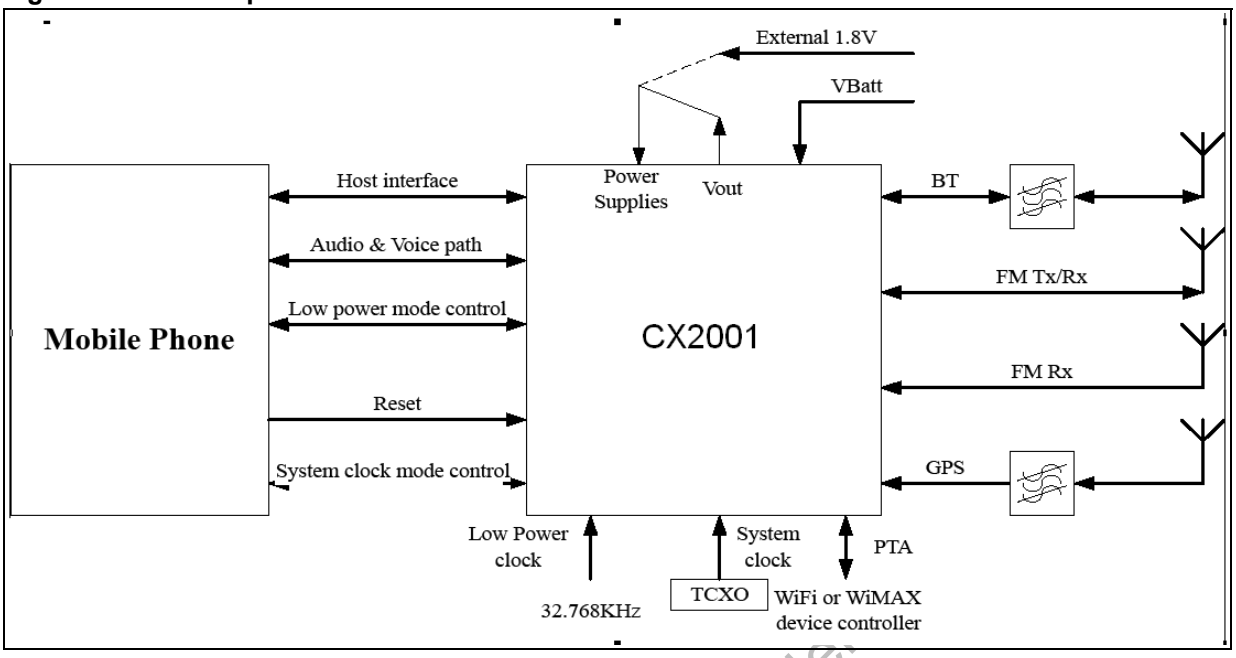
- The CX2001 is designed to provide optimal power consumption. As detailed in *Section 1.1.1*, the architecture allows each subsystem to be switched ON and OFF or to be put in a low power mode, depending on the use case. The ARM core subsystem controls the interfaces usage. The detailed power architecture and power modes description can be found in *Section 1.4*.
- The CX2001 architecture has been designed to optimize the application footprint and integration into a mobile phone. Requiring 10 external components (including the TCXO and its components) together with its small package, the total application footprint is less than 50 mm^2 for a PCB layout. To further ease the integration, all of the RF inputs are designed for single ended antenna connections. The CX2001 device meets coexistence requirements performance for cellular, DVB-H, WLAN, WiMax, WUSB and other standards as described in *Section 1.8.8*. The CX2001 uses three clocks inputs: a system clock, cellular reference clock, and a low power clock (see *Section 1.6*).

The design choices such as coexistence and cohabitation architecture, clock architecture, debug architecture, supply architecture, have all been defined keeping in mind the scalability goal, and are built with the ARM Cortex M3 as the central control point.

1.1.1 Typical application

A typical application is shown in *Figure 2*. The (a)GPS subsystem provides the accurate positioning information. In a mobile phone application, the BT link is the medium for headset to communicate together on an ad-hoc basis. The FM subsystem is useful to listen to radio stations or may be used to send music through, for example, a car radio system.

Figure 2. Mobile phone - hardware overview



The CX2001 can be supplied either from a regulated 1.8 V supply voltage or either from a 3.6 V battery.

The host communicates with the CX2001 using either the UART or SPI interface. Each interface complies to the BT HCI H:4 standard.

The static and dynamic parameters are stored on the mobile phone side and are provided to the CX2001 using factory settings.

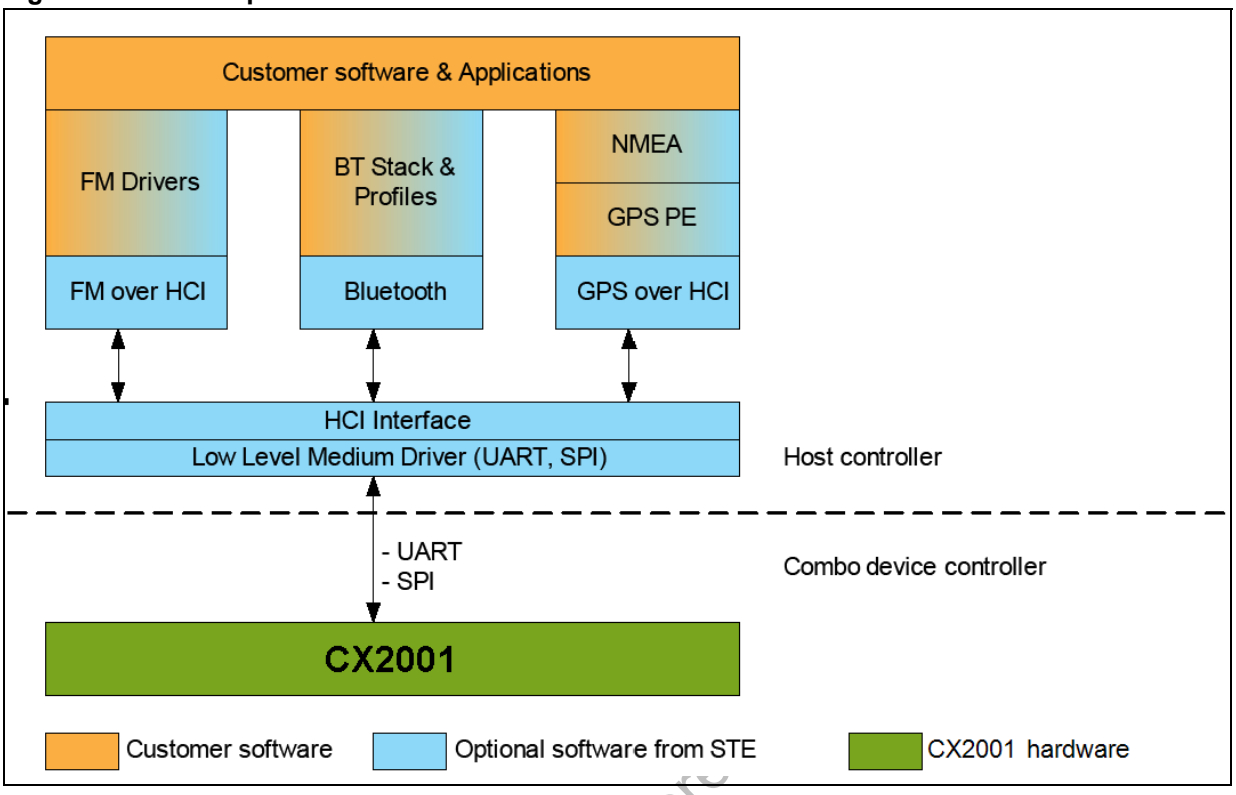
The audio and voice path is using either the PCM, I2S1, or I2S2 interface to carry BT SCO and eSCO, as well as FM stereo RX and TX data and BT stereo data for A2DP. Next to this, the FM stereo RX can use the analog audio output interface. BT A2DP can also be sent over HCI.

A system clock request signal is provided to manage the system clock coming from the Host platform. The system clock request signal may be shared with multiple sources. The low power clock is used to manage the CX2001 low power modes.

The WiFi or WiMAX co-existence is managed using enhanced Packet Traffic Arbitration (ePTA) algorithm, which follows the guidelines of the IEEE 802.15.2 recommended practice. The two systems exchange their real-time RF activity as medium access requests, completing this reporting with additional status information. The ePTA arbitration engine inside the WLAN device can make medium access decisions on a case by case basis based on all available information.

The diagram (*Figure 3*) presents the software partitioning between the host and the CX2001 part. The GPS, BT, and FM communicate with the host through the HCI interface. This HCI interface supports specific commands reference to command and transport layer specification to support both GPS and FM subsystem, next to the BT subsystem.

Figure 3. Mobile phone - software overview



1.2 Electrical specifications

1.2.1 Limiting values

Stressing the device above the rating listed in *Table 1: Limiting values* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the recommended operating conditions section of this document is not implied.

Table 1. Limiting values (1) (2)

Symbol	Parameter	Conditions	Min	Max	Unit
VDDIO1	I/O1 supply voltage		-0.5	2.75	V
VDDIO2	I/O2 supply voltage		-0.5	2.75	V
VDD_x	Core supply voltage	@ 1.8 V	-0.5	2.75	V
V_{PINIOx}	Input voltage on any VDDIOx(3) pin with respect to VSS		-0.5	V_{DDIOx} + 0.5	V
VBAT	Battery supply voltage		-0.5	+6.0	V
T_{stor}	Storage temperature		-40	125	°C
V_{GPS_RFIN}	Input DC voltage on pin GPS_RFIN		-0.3	+0.6	V

Table 1. Limiting values (continued)(1) (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{FM_WANT}	Input DC voltage on pin FM_WANT		-0.5	+0.5	V
$V_{BT\_RF\_TRX}$	Input DC voltage on pin BT_RF_TRX		-0.1	+0.1	V

1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. In accordance with the absolute maximum rating system (IEC 60134).
3. VDDIOx corresponds to VDDIO1 and VDDIO2

1.2.2 Recommended operating conditions

Table 2. General operating conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{amb}	Operating ambient temperature device meets all specifications		-30	-	+85	°C
P_D	Power Dissipation	T_{amb} = -30°C to 85°C	-	-	600	mW

Table 3. Power supply (1)(2)(3)(4) (5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VBAT	Regulator input supply voltage VBAT low level = 2.75 V ± 5% VBAT high level = 3.25 V ± 5%		2.3(6)	3.6	4.8(7)	V
VDD_DIG	Digital supply voltage		1.7	1.8	1.9	V
VDD_GPS	GPS analog supply voltage		1.7	1.8	1.9	V
VDDA_FM	FM analog supply voltage		1.7	1.8	1.9	V
VDD_FM_PA	FM TX power amplifier supply voltage		1.7	1.8/2.5	2.60	V
VDD_BT_RF	BT analog supply voltage		1.7	1.8	1.9	V
VDD_BT_PA	BT power amplifier supply voltage		1.7	1.8	1.9	V
VDDIOx	I/O1 and I/O2 supply voltage		1.65	1.8	1.9	V
VOUT(8)	Regulator output supply voltage		1.7	1.8	1.9	V

1. See *Section 1.4* for explanation on power supply domains
2. For 1,8 V, the supply ripple below 1.5 MHz will be < 25 mVpp (standby/PFM mode)
3. For 1,8 V, the supply ripple from 1.5 MHz to 5 MHz will be < 25 mVpp (PWM mode)
4. For 1,8 V, the supply ripple above 5 MHz will be < 5 mVpp, further decreasing with 20 dB/decade
5. For VBAT, the supply ripple will be < 400 mV, starting from 2.7 V (hence the 2.3 V min specified)
6. Below VBAT low level, the embedded VDD_FM_PA LDO output is reduced to 1.8 V and the FM TX output is limited to the value indicated in *Table 37*.

7. Up to 4.8 V maximum for continuous operation, 4.8 V to 5.0 V for 250 seconds cumulative over lifetime, 5.0 V to 5.5 V for 10 s cumulative over lifetime
8. This supply will only be used to supply the CX2001 1.8 V parts

Table 4. TCXO power supply

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD_TCXO	TCXO supply voltage		1.74	1.83	1.92	V
$I_{TCXOmax}$	Maximum current a TCXO can draw from this supply		-	-	10	mA

Table 5. Low power clock(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{lpo_clk}	LPO clock voltage	Square wave: V_{IH}	0.7	-	V_{DDIO1}	V
		Square wave: V_{IL}	0	-	0.2	V
V_{lpo_Hys}	Input hysteresis voltage		0.1 x V_{DDIO}	-	-	V
F_{lpo_clk}	LPO clock frequency		-	32.768	-	kHz
F_{lpo_acc}	LPO clock frequency accuracy		-250	-	250	ppm
$t_{Dutycycle}$	LPO clock duty cycle		30	-	70	%
t_{jitter}	Short term jitter	6 sigma standard deviation of 1000 consecutive periods	-25	-	25	ns

1. Low power clock input does not require external series capacitor.

Table 6. System clock input (SYS_CLK)(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_{osc_in}	Input capacitance on SYS_CLK		2	-	4.5	pF
R_{osc_in}	Input resistance on SYS_CLK		30	100	-	kΩ
$T_{sys\_stability}$	Stabilization time for input clock in number of system clock cycles(2)		-	-	65535	cycles
T_{sys_start}	Turn on time	Within 10 ppm of final frequency	-	-	100	µs
T_{sys_stop}	Turn off time	To reach power down current	-	-	50	ns
V_{sys_clk}	System clock voltage swing (square or sine wave)		0.4	-	VDD_TXCO	Vpp
F_{sys_clk}	System clock frequency		19.2, 26, 38.4, 52			MHz

Table 6. System clock input (SYS_CLK)(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{sys_acc}	System clock frequency accuracy		-0.5	-	0.5	ppm
$PhiN_{2.4G}$	Phase noise for CX2001 standalone or combo with 2.4GHz (3)	@ 1 Hz	-	-	-55	dBc/Hz
		@ 10 Hz	-	-	-80	dBc/Hz
		@ 100 Hz	-	-	-105	dBc/Hz
		@ 1 kHz	-	-	-125	dBc/Hz
		@ 10 kHz	-	-	-134	dBc/Hz
		@ 100 kHz	-	-	-139	dBc/Hz
$PhiN_{combo5G}$	Phase noise for combo with 5 GHz WLAN (using SYS_CLK_OUT) (3)	@ 1 Hz	-	-	-55	dBc/Hz
		@ 10 Hz	-	-	-80	dBc/Hz
		@ 100 Hz	-	-	-105	dBc/Hz
		@ 1 kHz	-	-	-130	dBc/Hz
		@ 10 kHz	-	-	-146	dBc/Hz
		@ 100 kHz	-	-	-148	dBc/Hz

1. SYS_CLK input is internally AC coupled, external series capacitor is not required.
2. After SYS_CLK_REQ or VDD_TCXO active, the CX2001 waits for a stable system clock on SYS_CLK during this number of cycles. SYS_CLK clock response to TCXO being turned on (or SYS_CLK_REQ) should have 90% amplitude levels within 10% of the programmed counter delay not to affect wrong timing of this wait time.
3. For a TCXO with frequency of 26 MHz

Table 7. External reference clock (EXT_REF_CLK)(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{EXT\_REF\_CLK}$	External reference clock voltage swing (square or sine wave)		0.4		VDD_IO1	Vpp
$f_{EXT\_REF\_CLK}$	External reference clock		19.2, 26, 38.4			MHz

1. EXT_REF_CLK input is internally AC coupled, external series capacitor is not required.

Table 8. System clock output (SYS_CLK_OUT)(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{sys_clk}	System clock frequency		19.2	-	52	MHz
Vol		20 pF, 10 kΩ			0.45	V
Voh		20 pF, 10 kΩ	V_{DD_TCXO} - 0.45		-	V

Table 8. System clock output (SYS_CLK_OUT)(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$PhiN_{SYSCLK\ OUT\_2.4G}$	Phase noise(2)	@ 1 Hz	-	-	-55	dBc/Hz
		@ 10 Hz	-	-	-80	dBc/Hz
		@ 100 Hz	-	-	-105	dBc/Hz
		@ 1 kHz	-	-	-124	dBc/Hz
		@ 10 kHz	-	-	-133	dBc/Hz
		@ 100 kHz	-	-	-138	dBc/Hz
$PhiN_{SYSCLK\ OUT\_5G}$	Phase noise (3)	@ 1 Hz	-	-	-55	dBc/Hz
		@ 10 Hz	-	-	-80	dBc/Hz
		@ 100 Hz	-	-	-105	dBc/Hz
		@ 1 kHz	-	-	-128	dBc/Hz
		@ 10 kHz	-	-	-142	dBc/Hz
		@ 100 kHz	-	-	-145	dBc/Hz

1. SYS_CLK_OUT output frequency is equal to the frequency of SYS_CLK.
2. For a TCXO with frequency of 26 MHz meeting the conditions of PhiN2.4G in *Table 6*
3. For a TCXO with frequency of 26 MHz meeting the conditions of PhiNcombo5G in *Table 6*

Table 9. I/O pins(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input levels						
VIH	High level input voltage		0.65 x VDDIO	-	VDDIO + 0.3	V
VIL	Low level input voltage		-0.3	-	0.35 x VDDIO	V
VHYS	Input hysteresis voltage		0.1 x VDDIO	-	-	V
Output levels (GPIO[0] – GPIO[5], GPIO[8] – GPIO[20], GPS_ANT_SEL, GPS_LNA_EN)						
VOH	High level output voltage	IOH @ 7.2mA	VDDIO – 0.4V	-		V
VOL	Low level output voltage	IOL @ 7.3mA	-	-	0.4	V
Output levels (GPIO[6] – GPIO[7])						
VOH	High level output voltage	IOH @ 1mA	0.9 x VDDIO	-		V
VOL	Low level output voltage	IOL @ 1mA	-	-	0.1 x VDDIO	V
Rise and fall times						
tr	Low to high rising time	RLOAD = 15pF	1.6	-	5	ns
tf	High to low falling time	RLOAD = 15pF	1.6	-	5	ns

1. Applicable for all digital control signals and programmable pins (supplied by VDDIO1 or VDDIO2) as stated in *Table 12: Pinning information*, except otherwise stated in *Section 1.8: Interfaces*.

1.2.3 Thermal characteristics

Table 10. Package thermal resistance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{JA}	Junction-to-air thermal resistance	JEDEC (JESD-51 series)	-	48	-	°C/W
T_{JC}	Junction-to-case thermal resistance		-	32.4	-	°C/W

1.2.4 System power consumption

Table 11 contains the power consumption of the full system. Power consumption of the subsystems are detailed in the subsystems' chapters.

Table 11. System power consumption(1)

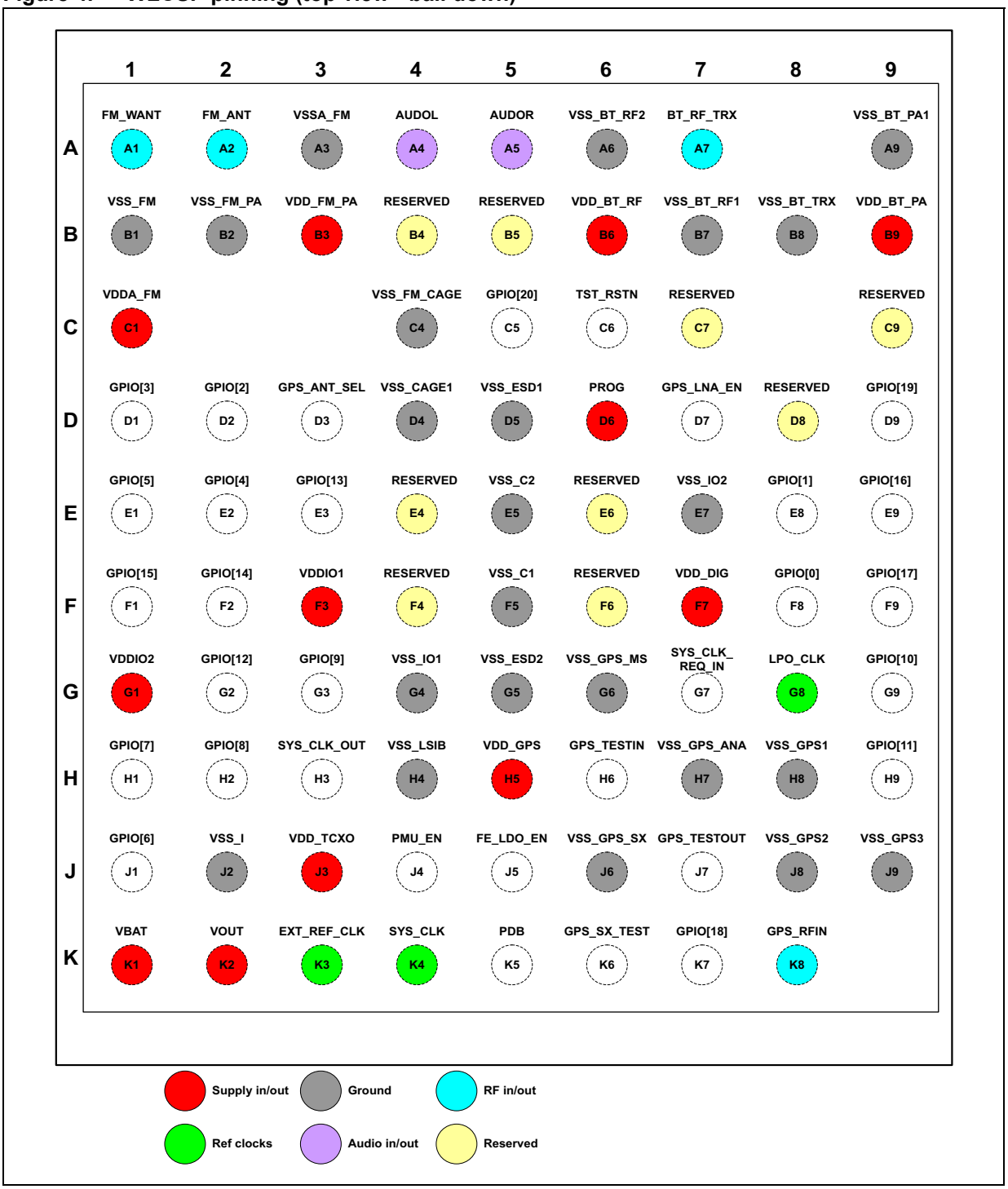
Symbol	Parameter	Condition		Typ.	Max.	Unit
I_{Off}	System Off mode, power supply architecture 1 (*Figure 5*) and power supply architecture 2 (*Figure 6*)	FE LDO = off System clock = off LPO clock = on PDB pin = low Memories are cleared VDDIOx = on 1.8 V = on VBAT = on	-	4	-	µA
I_{Sleep}	System Deep Sleep mode, power supply architecture 1 (*Figure 5*)	FE LDO = off System clock = off LPO clock = on PDB pin = high ARM sub system in eco mode FM and GPS sub system Off	-	72	-	µA
	System Deep Sleep mode, power supply architecture 2 (*Figure 6*)	FE LDO = eco mode System clock = off LPO clock = on PDB pin = high ARM sub system in eco mode FM and GPS sub system Off	-	95	-	µA
I_{Peak}	System maximum peak current	From VBAT (as in power supply architecture 2)		260	360(2)	mA
		From VBAT (as in power supply architecture 1)			8(2)	mA
		From 1.8 V (as in power supply architecture 1)			350	mA
I_{IO}	VDDIO1 + VDDIO2		-	-	0.25	mA
I_{TCXO}	TCXO current, when TCXO supplied via VBAT(3)		-	1.5	-	mA

1. VDDIOx, VDD_x, VDD_BT_RF, VDD_BT_PA, VDDA, VDD_FM_PA, VDD_GPS = 1.8 V; Temperature = 25 °C unless otherwise specified.
2. Over a 11 ns period. Hard current limit of 500 mA on VBAT.
3. Dependent on which specific TCXO component is used in the application.

1.3 Pin information

1.3.1 Pinning

Figure 4. WLCSP pinning (top view - ball down)



1.3.2 Pin description

Table 12. Pinning information

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
Clocks								
K4	SYS_CLK	Int. LDO	I	Input	System clock input		Input	
H3	SYS_CLK_OUT	Int. LDO	O	Output	System clock output (state: if SYS_CLK_REQ_IN = 0 ==> SYS_CLK_OUT = PD, if SYS_CLK_REQ_IN = 1 ==> SYS_CLK_OUT = driven)			
G8	LPO_CLK	VDDIO1	I	Input	Low power clock input		Input	
K3	EXT_REF_CLK	VDDIO1	I		GPS cellular clock		High-Z	
Digital control signals								
K5	PDB	VDDIO1	I	Input	LDO power down input		Input PD	
J5	FE_LDO_EN	VDDIO1	I	Input	Enable the internal LDO to generate 1.8 V from VBAT		Input	
J4	PMU_EN	VDDIO1	O	Output	Enable the external DC/DC 1.8 V power supply		High-Z	
D3	GPS_ANT_SEL	VDDIO1	O		GPS antenna selection		Output PD	
D7	GPS_LNA_EN	VDDIO1	O		GPS LNA enable		Output PD	
G7	SYS_CLK_ REQ_IN	VDDIO1	I	Input	System clock request input		Input PD	
Digital programmable pins								
F8	GPIO[0]	VDDIO1	I/O	Progr.	PCM/I2S1 data input/output	DA_IP	High-Z	
					I2S2 data output	SDO_I2S2		
					WLAN coexistence	PTA_RF_ CONFIRMN		
E8	GPIO[1]	VDDIO1	I/O	Progr.	PCM/I2S1 data input/output	DB_IP	High-Z	
					I2S2 data input	SDI_I2S2		
					WLAN coexistence	PTA_ STATUS		

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
D2	GPIO[2]	VDDIO1	I/O	Progr.	UART clear to send (HCI)	CTS_UART	Input PU	
					I2S2 data write sync	WS_I2S2		
D1	GPIO[3]	VDDIO1	I/O	Progr.	UART request to send (HCI)	RTS_UART	Input PU	RTS_UART
					I2S2 data output	SDO_I2S2		
					System clock request output	SYS_CLK_REQ		
E2	GPIO[4]	VDDIO1	I/O	Progr.	UART transmit data output (HCI)	TXD_UART	Input PU	
					I2S2 data clock	SCK_I2S2		
E1	GPIO[5]	VDDIO1	I/O	Progr.	UART receive data input (HCI)	RXD_UART	Input PU	RXD_UART
					I2S2 data input	SDI_I2S2		
J1	GPIO[6]	VDDIO2	I/O	Progr.	PCM/I2S1 data input/output	DB_IP	Hi-Z	
					I2S2 data input	SDI_I2S2		
H1	GPIO[7]	VDDIO2	I/O	Progr.	PCM/I2S1 frame sync	FSC_IP	Hi-Z	
					I2S2 data write sync	WS_I2S2		
H2	GPIO[8]	VDDIO2	I/O	Progr.	PCM/I2S1 data clock	DCLK_IP	Input PD	
					I2S2 data clock	SCK_I2S2		
					WLAN coexistence	PTA_RF_ CONFIRMN		
G3	GPIO[9]	VDDIO2	I/O	Progr.	PCM/I2S1 data input/output	DA_IP	Input PD	
					I2S2 data output	SDO_I2S2		
					WLAN coexistence	PTA_STATUS		
G9	GPIO[10]	VDDIO1	I/O	Progr.	Power mode request to wake-up external PMU	SYS_PWR_RE Q	Input PD	
					SPI transfer request (HCI)	INT_SPI_E		

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
H9	GPIO[11]	VDDIO1	I/O	Progr.	System clock request output	SYS_CLK_REQ	Output PD	SYS_CLK_REQ
					I2S2 data output	SDO_I2S2		
					BT request to wake-up host	HOST_WAKE_UP		
G2	GPIO[12]	VDDIO1	I/O	Progr.	SPI data output (HCI)	MISO_SPI_E	Input PD	
					I2S2 data output	SDO_I2S2		
					PCM/I2S1 data input/output	DA_IP		
					Disable the BT transmitter	BT_TX_DISABLE		
E3	GPIO[13]	VDDIO1	I/O	Progr.	SPI chip selection (HCI)	CS_SPI_E	Input PD	CS_SPI
					I2S2 data write sync	WS_I2S2		
					PCM/I2S1 frame sync	FSC_IP		
F2	GPIO[14]	VDDIO1	I/O	Progr.	SPI data clock (HCI)	CLK_SPI_E	Input PD	CLK_SPI
					I2S2 data clock	SCK_I2S2		
					PCM/I2S data clock	DCLK_IP		
F1	GPIO[15]	VDDIO1	I/O	Progr.	SPI data input (HCI)	MOSI_SPI_E	Input PD	MOSI_SPI
					I2S2 data input	SDI_I2S2		
					PCM/I2S1 data input/output	DB_IP		
E9	GPIO[16]	VDDIO1	I/O	Progr.	reserved	reserved	Input PD	
					PCM/I2S1 frame sync	FSC_IP		
					I2S2 data write sync	WS_I2S2		
					WLAN coexistence	PTA_FREQ		
					Host request to wake-up GPS	HOST_GPS_WAKE_UP		
					Disable the BT transmitter	BT_TX_DISABLE		

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
F9	GPIO[17]	VDDIO1	I/O	Progr.	reserved	reserved	Input PD	
					PCM/I2S1 data clock	DCLK_IP		
					I2S2 data clock	SCK_I2S2		
					WLAN coexistence	PTA_REQUEST		
					GPS request to wake-up host	GPS_HOST_ REQ		
K7	GPIO[18]	VDDIO1	I/O	Progr.	One pulse per second output	PULSE_OUT	Input PD	
					GPS cellular ref clock request for calibration	GPS_CAL_REQ		
					SPI flow control (HCI)	FLOW_SPI_E		
					Disable the BT transmitter	BT_TX_ DISABLE		
D9	GPIO[19]	VDDIO1	I/O	Progr.	GPS blanking input	EXT_DUTY_ CYCLE	Input PD	
C5	GPIO[20]	VDDIO1	I/O	Progr.	GPS cellular frame timing reference	EXT_FRM_ SYNCH	Input PD	
Antenna interfaces								
A1	FM_WANT	N/A	I/O		FM single ended wired antenna			
A2	FM_ANT	N/A	I/O		FM single ended embedded antenna			
B1	VSS_FM		-		FM antenna ground			
A7	BT_RF_TRX	N/A	I/O		BT single ended antenna			
B8	VSS_BT_TRX		-		BT antenna ground			
K8	GPS_RFIN	N/A	I		GPS single ended antenna			
FM analog audio interface								
A4	AUDOL	VDDA_FM	O		Left analog audio output		Disabled	

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
A5	AUDOR	VDDA_FM	O		Right analog audio output		Disabled	
Battery supply								
K1	VBAT		I		Regulator input 3.6 V			
K2	VOUT		O		Regulator output 1.8 V			
J2	VSS_I		-		Front end LDO ground			
Digital supply								
F7	VDD_DIG		I		Digital supply			
F3	VDDIO1		I		General purpose IO supply			
G1	VDDIO2		I		General purpose IO supply			
J3	VDD_TCXO		O		External TCXO power supply		Output	
F5	VSS_C1		-		Digital core ground General purpose IO ground			
E5	VSS_C2		-		Digital core ground General purpose IO ground			
G4	VSS_IO1		-		General purpose IO ground			
E7	VSS_IO2		-		General purpose IO ground			
H4	VSS_LSIB		-		System clock ground			
GPS subsystem supply								

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
H5	VDD_GPS		I		GPS RF supply	See application notes on layout requirements		
H7	VSS_GPS_ANA		-		GPS analog ground			
G6	VSS_GPS_MS		-		GPS mixed signal ground			
J6	VSS_GPS_SX		-		GPS synthesizer ground			
H8	VSS_GPS1		-		GPS internal LNA regulator ground			
J8	VSS_GPS2		-		GPS cold ground			
J9	VSS_GPS3		-		GPS cold ground			
BT subsystem supply								
B6	VDD_BT_RF		I		BT analog supply			
B9	VDD_BT_PA		I		BT power amplifier supply			
B7	VSS_BT_RF1		-		BT analog ground			
A6	VSS_BT_RF2		-		BT analog ground			
A9	VSS_BT_PA1		-		BT power amplifier ground			
FM subsystem supply								
C1	VDDA_FM		I		FM analog supply			
B3	VDD_FM_PA		I		FM power amplifier supply			
A3	VSSA_FM		-		FM analog ground			
B2	VSS_FM_PA		-		FM power amplifier ground			
Protection								
D4	VSS_CAGE1		-		CAGE ground			
D5	VSS_ESD1		-		ESD shield ground			
G5	VSS_ESD2		-		ESD shield ground			
C4	VSS_FM_CAGE		-		FM ESD shield ground			

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
Other pins								
C6	TST_RSTN	VDDIO1	I	Input	Test pin, to be connected to VDDIO1		Input PU	
D6	PROG	N/A	I		Must be set to GND in customer application		Input	
H6	GPS_TESTIN	VDD_GPS	I		Enable ST-Ericsson test mode usage Must be set to GND in customer application		Disabled	
J7	GPS_TESTOUT	VDD_GPS	O		Enable ST-Ericsson test mode usage Must be unconnected in customer application		Disabled	
K6	GPS_SX_TEST	VDD_GPS	O		Enable ST-Ericsson test mode usage Must be unconnected in customer application		Disabled	
D8	RESERVED		I	Input	Must be set to GND		Input	
B4	RESERVED				Unconnected in customer application			
B5	RESERVED				Unconnected in customer application			
C7	RESERVED				Unconnected in customer application			
C9	RESERVED				Unconnected in customer application			
E4	RESERVED				Unconnected in customer application			

Table 12. Pinning information (continued)

Pin	Pin name	Supply	I/O	Type	Description and alternate function		Power Off state(1)	Default function after Power Off
E6	RESERVED				Unconnected in customer application			
F4	RESERVED				Unconnected in customer application			
F6	RESERVED				Unconnected in customer application			

1. Without any firmware nor software initialization ion and during PDB = “0”. Refer to *Figure 7: Start-up and reset state diagram* for more information.

1.4 Power supply

1.4.1 Platform power supply architecture

The CX2001 supports different platform power supply architectures. *Figure 5* and *Figure 6* give two examples of possible power supply architectures, more details can be found in the hardware user manual *[10.]*.

Figure 5. Platform power supply architecture 1

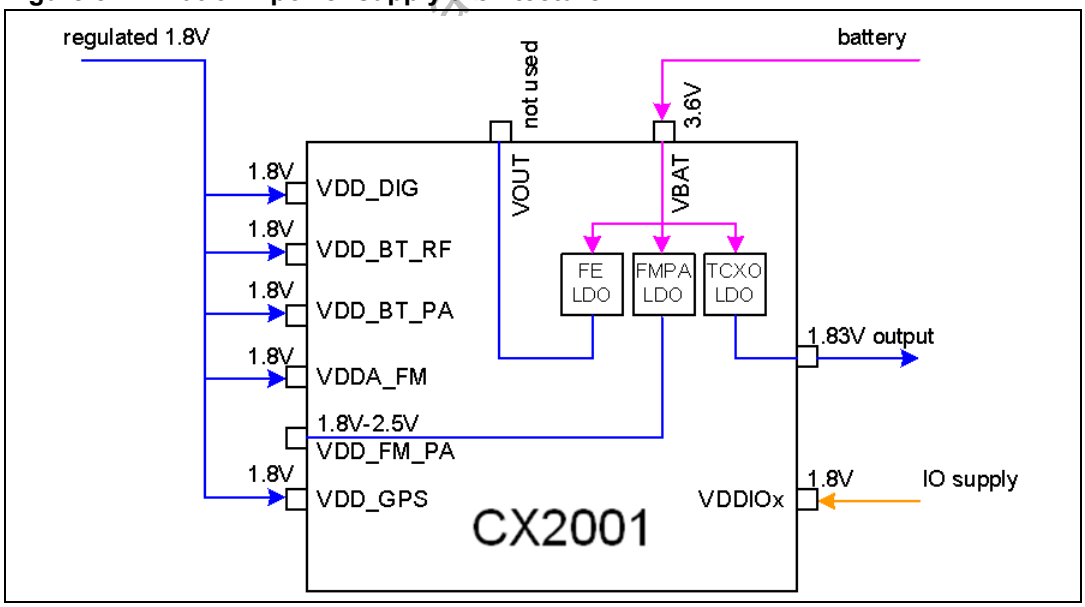
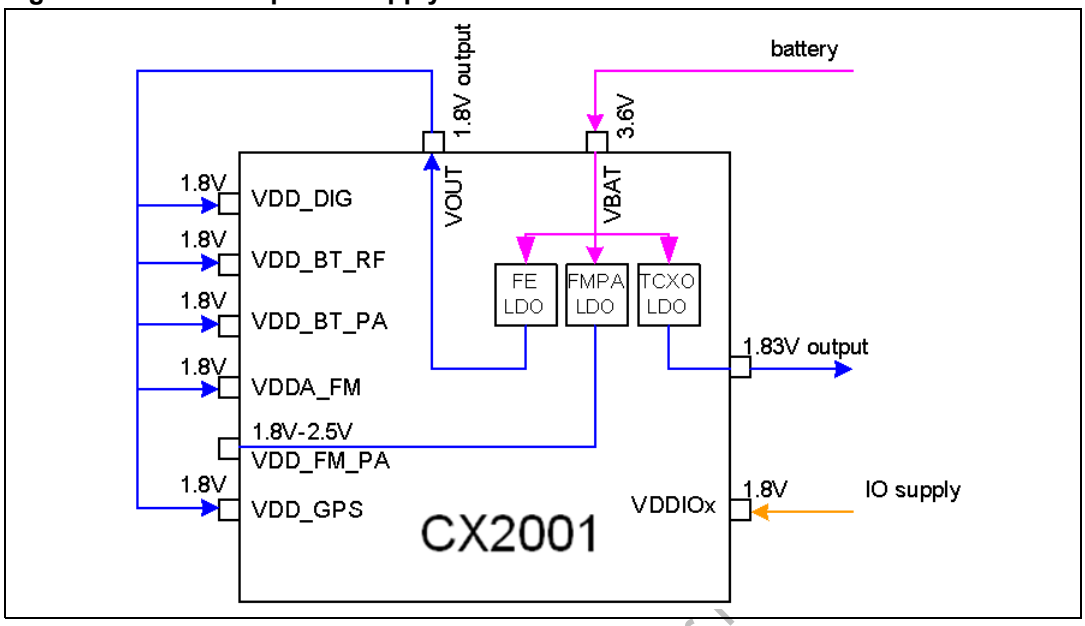


Figure 6. Platform power supply architecture 2



Battery connect

The typical value for VBAT is 3.6 V. VBAT can be used for three functionalities:

- Supply a first LDO that has an output voltage of 1.8 V (at pin VOUT), which is connected to all CX2001 input power supply pins, except for the FM TX PA. As shown in the architecture 2 of *Figure 6*.
- Supply a second LDO that has an output voltage of 2.5 V (except when VBAT is below 2.75 V, then the output is 1.8 V), and is used to supply the FM TX PA. As shown both in architecture 1 of *Figure 5* and architecture 2 of *Figure 6*.
- Supply a third LDO that has a 1.83 V output that can be used to enable and supply the external TCXO. As shown both in architecture 1 of *Figure 5* and architecture 2 of *Figure 6*.

The battery voltage needs to be connected to the VBAT pin in any possible configuration, in order to supply the CX2001 internal system clock buffers.

System supply

The typical value for the system supply is 1.8 V. This 1.8 V can come from a pre-regulated supply from the platform (*Figure 5*). Alternatively the 1.8 V can come from the output (via pin VOUT) of the CX2001 internal LDO, supplied by VBAT (*Figure 6*).

1.8 V is supplied at pins VDD_DIG, VDDA_FM, VDD_GPS, VDD_BT_RF, VDD_BT_PA.

FM TX PA supply

The typical value for the FM TX PA supply is 2.5 V. This 2.5 V is generated from the output of a CX2001 internal LDO, supplied by VBAT. In that case, the output power of the FM TX is the level indicated in *Table 37*. When VBAT is below 2.75 V, the internal LDO generates 1.8 V and the output power of the FM TX is reduced to the level defined in *Table 37*.

Alternatively the FM TX PA can also be supplied from a pre-regulated 2.5 V or 1.8 V supply. The output power of the FM TX can be found in *Table 37*.

IO supply

The typical value for the IO supply is 1.8 V. This is supplied at pins VDDIO1 and VDDIO2.

1.4.2 Power-on reset

In order to reset correctly the digital cores, there is a Power-on Reset (PoR) unit monitoring the LDO core supply voltage domain.

A PDB input pad is available, as a package pin, to power-up and reset the device. This mechanism enables/disables the voltage regulator and controls the state retention on I/Os

1.4.3 External SMPS control

The CX2001 supports the control of an external Switched Mode Power Supply (SMPS) that can generate the 1.8 V for the system supply.

For this, the PMU_EN signal is available. It is a buffered signal of the PDB signal. The PMU_EN is open drain output, therefore a wired-OR function may be implemented on the PCB if desired. When inactive, the PMU_EN signal is high-Z. This control logic is powered by VDDIO1.

Additionally the SYS_PWR_REQ output signal (available on a GPIO) from the CX2001 may be configured by software to control the mode of the external SMPS.

1.5 Power modes

In the different device and subsystem (GPS, BT, and FM) states, the power and clocks are managed to lower the power consumption depending on the application use case. *Table 13* gives an overview of which clocks are used.

Table 13. Power modes

Application use case	System clock(1)	LPO clock
GPS normal / sleep	Used	Used
GPS coma	Stopped	Used
GPS deep coma	Stopped	Used
BT active	Used	Used
BT sleep	Stopped	Used
BT off	Stopped	Stopped
FM power up / memory load	Used	Used
FM standby	Stopped	Stopped
FM power down	Stopped	Stopped

1. Clock is only stopped if also the other subsystems do not need the clock

The states for the system and different subsystems (GPS, BT, and FM) are given below.

The CX2001 system can be in following states

- Power Off: PDB = 0
- System Active: at least one of the subsystems (GPS, BT, and FM) is active
- System Deep Sleep: all the device subsystems (GPS, BT, and FM) are disabled or in low power mode
- System Off: PDB = 0, after System Active mode, same as Power Off, except that the state of the IOs is defined based on the platform requirements.

GPS can be in one of the following states depending on the GPS operation mode:

- GPS Normal: Receiving the GPS signal
- GPS Sleep: Not receiving a GPS signal for a given time under control of the host, but keeping accurate time from TCXO
- GPS Coma/Deep Coma: GPS subsystem disabled by the host, allowing restart without patch and parameter download, time maintained from the LPO
- GPS Shutdown: GPS IP disabled over HCI

BT can be in one of the following states depending on the BT operation mode:

- BT Active: Sending or receiving data
- BT Sleep: Idle period between active periods
- BT Off: BT subsystem disabled by the host

FM can be in one of the following states depending on the FM operation mode:

- FM Power Up: FM active RX or TX
- FM Memory Load: FM firmware download
- FM Standby: FM paused, for example: to handle incoming call
- FM Power Down: FM subsystem disabled by the host

1.6 Clocks

1.6.1 Overview

There are two clock sources: the system clock is used in normal operations while the low power clock is used for both normal operation and low power operations.

In Active mode, the system clock is mandatory when using the GPS, and/or BT subsystems.

The low power clock is used to keep the enabled system subsystems (GPS and BT) running during their low power mode. It is also used for the automatic system clock frequency detection.

1.6.2 System clock

The CX2001 provides a single ended system clock input for all integrated subsystems (GPS, BT, and FM). This system clock input can come from a TCXO, which is included in the reference design. Or the system clock input can come from the Host and the clock specification need to meet CX2001 requirement.

When the system clock comes from an external TCXO, the TCXO is directly supplied from the VDD_TCXO pin, and can be controlled by switching on/off the VDD_TCXO supply.

When the system clock is supplied by the Host, the clock is requested by the SYS_CLK_REQ output.

The system clock request output signal is available from two GPIOs:

- GPIO[11] where SYS_CLK_REQ is active high, and can be configured as wired OR or push-pull.
- GPIO[03] where SYS_CLK_REQ is active low, and can be configured as wired NAND or push-pull.

Since the range of frequencies supported is wide, from 19.2 MHz to 52 MHz, the CX2001 includes the capability to automatically detect the system clock frequency.

The system clock input accepts the following frequencies (see *Table 14*).

Table 14. System clock frequencies

System clock frequency (MHz)
19.2
26
38.4
52

Since the system clock input is AC coupled, there is no need for an external coupling capacitor as long as the requirements on the voltage swing are met (see *Table 5*).

System clock output

The TCXO may serve as the single clock source for the overall application. For this the CX2001 provides a system clock output, SYS_CLK_OUT which can be used by other functions in the application. The enable control is done by the SYS_CLK_REQ_IN signal, which is ORed with the internal system clock request. The SYS_CLK_OUT is available even if the CX2001 is disabled by PDB control (VBAT and VDDIO1 need to be supplied). The SYS_CLK_OUT functionality can be disabled from the Host using factory settings.

1.6.3 Low power clock

The low power clock is used in normal operation for clock synchronization while in low power mode, it is used to keep the GPS and BT sub-systems timing.

The low power clock is to be provided on the low power clock input (LPO_CLK), as a 32.768 kHz square wave clock input.

1.7 Reset (cold start) and start-up

1.7.1 Reset conditions

The device is reset (cold start) from the following conditions:

- Power-on start-up
  After applying the power supply voltage, nothing happens as long as the PDB pin is kept at low level (“0”). When the PDB pin goes to high level (“1”), the reset condition is met. This powers up the device and causes a power on reset.
- PDB pin
  The PDB pin can be used to asynchronously reset the device.

1.7.2 Start-up conditions

Figure 7 presents the device start-up phases.

When the system starts up, it goes through a power-on reset where the system clock is requested by both the SYS_CLK_REQ output signal and VDD_TCXO. Following this power-on reset, the system waits for a stable system clock by counting a number of clock cycles, whilst the system is still kept in reset. Once the system clock is stable, a synchronous reset for a fixed number of system clock cycles keeps the system in reset, until the system is ready to go in the System Enable state

In System Enable state, the device automatically detects the system clock frequency, and enables the UART and SPI HCI interfaces. An automatic detection on these interfaces is then performed to select the one used by the host. The CX2001 detects which HCI interface is used by the Host, at the moment the host starts transmitting one command of a limited set of HCI commands on one of the HCI interfaces. More information can be found in the software user manual *[11.]*. Once the HCI interface has been detected, the device goes into the System Active state.

In the System Active state, the host has to configure the device further. This is, to download patch file (BT and ARM-SS) and static settings file. Following reset, by default GPS and FM are in power down, BT is active or in power down depending on the static settings file. The different device subsystems (GPS, BT, and FM) can be enabled or disabled separately.

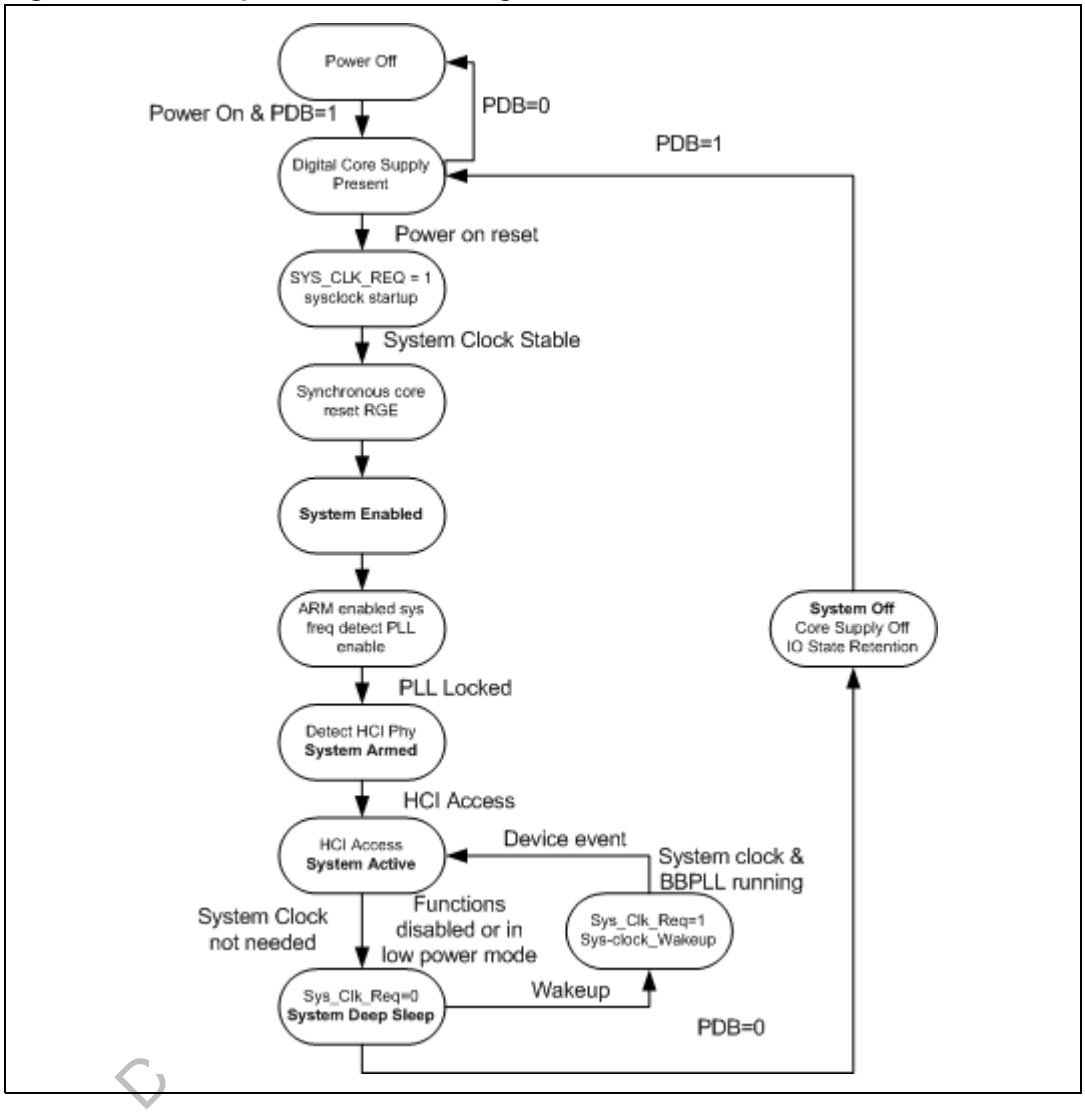
As long as one of the device subsystems (GPS, BT, and FM) is enabled and active, the device stays in the System Active state. When all the device subsystems (GPS, BT and FM) are disabled or in low power mode, the device goes into the System Deep Sleep state. In the System Deep Sleep state, only the low power clock is used and the power supplies are managed to reduce the power consumption. Waking up from the System Deep Sleep state can be triggered from an internal device event (for example, BT Sniff beacon) or by the Host via the HCI.

Once the device is in the System Deep Sleep state and all device subsystems (GPS, BT, and FM) are disabled, the device can be put in the System Off state to reduce consumption even further (for example, this mode is used when all device subsystems are disabled from the host). In the System Off state, the IOs can be configured by the host to keep a pull-up, pull-down, or high-Z state retention configuration to not interfere with the rest of the application, and all the internal clocks are switched-off while SYS_CLK_OUT functionality is still operational.

The System Off state is entered via a Host software request and via the PDB pin assertion to a low level. Then, going back to the System Active mode requires the PDB pin to be asserted to a high level. Following the high level on PDB, the CX2001 goes through the

system reset. Upon system reset, patch and configuration information need to be download. More information can be found in the CX2001 software user manual *[11.]*.

Figure 7. Start-up and reset state diagram



1.8 Interfaces

1.8.1 Programmable I/Os interfaces

After reset, the ARM enables the UART and SPI HCI interfaces. To limit disturbances, not all IOs will be enabled. Once the HCI interface is detected, the other HCI interface is disabled. All other IOs will be enabled by software after Host configuration.

1.8.2 Control signals

Table 15. Control signals

Signal	Direction	Function
PDB	input	Power Down Bar. When 0, the CX2001 is powered down.
SYS_CLK_REQ	output	Signal that requests the system clock only when needed to allow power saving.
SYS_CLK_REQ_IN	input	Signal that allows the sharing of the system clock between several devices on a board without the need of external components for the control of the enable of this clock.
VDD_TCXO	output	Powering and enabling an external TCXO
FE_LDO_EN	input	Enable signal of the CX2001 Front End LDO to generate 1.8 V from VBAT
PMU_EN	output	PMU_EN pad is the buffered signal of the PDB signal. When PDB is high, CX2001 will issue the enable signal for the SMPS.
SYS_PWR_REQ	output	SYS_PWR_REQ configured by CX2001 software to control the mode of the external SMPS (for example, PWM/PFM mode).
GPS_ANT_SEL	output	When the platform has multiple antennas, this pin can be used to switch to the other antenna.
GPS_LNA_EN	output	Optionally an external LNA can be used, this signal enables/disables this external LNA.
GPS_CAL_REQ	output	With GPS_CAL_REQ, the GPS can ask to get the platform clock on the pin EXT_REF_CLK. This clock is then used to tune the TCXO.
EXT_REF_CLK	input	With GPS_CAL_REQ, the GPS can ask to get the platform clock on the pin EXT_REF_CLK. This clock is then used to tune the TCXO.
EXT_DUTY_CYCLE	input	GPS blanking input
EXT_FRM_SYNCH	input	GPS cellular frame timing reference input

1.8.3 UART interface

The implemented UART interface is an asynchronous serial interface used for the GPS/BT/FM control and data transfer.

Features

The following features are supported:

- 1-bit start generation
- 8-bits character size
- 1-bit stop generation
- No parity generation and detection
- Programmable standard baud rates from 38.4 kBaud to 1.8432 MBaud + additional baud rates for fast data transfer from 2.5 MBaud up to 4.92 MBaud
- RTS/CTS handshake

Interface description

The UART interface consists of four wires:

- TXD_UART to transmit the data
  The data is driven according to the local clock and features programmed.
- RXD_UART to receive the data
  The data is read according to the local clock and features programmed.
- CTS_UART to indicate receiver is ready
  This signal is active at low level and indicates the external modem it is ready to accept transmitted data via RXD_UART.
- RTS_UART to indicate transmitter is ready
  This signal is active at low level and asks to the external modem if it is allowed to sent data on it's TXD_UART.

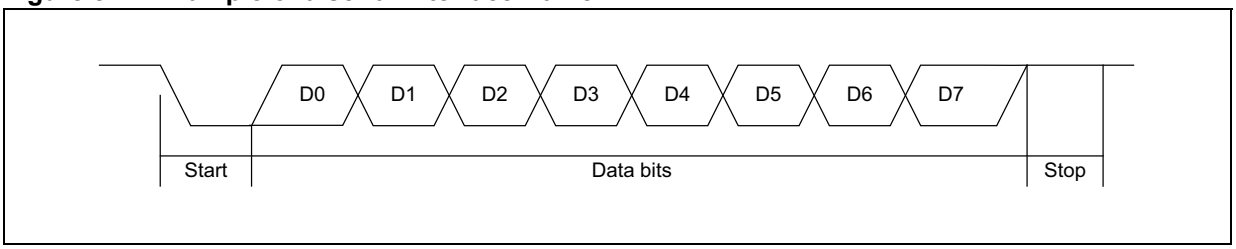
The data size handled is 8 bit. The supported endianness is LSB first.

Operations

The UART uses the modem signals Clear To Send (CTS) and Request To Send (RTS) for a handshake between the devices at both sides of the serial line. The notation for the signals is from the Data Terminal Endpoint (DTE) point of view (i.e. the device at the other side of the serial line has to be configured as Data Communication Equipment (DCE)).

An example of a frame for a protocol with one start bit ('0'), 8 data bits (LSB first), no parity, and one stop bit ('1') is shown in *Figure 8*.

Figure 8. Example of a serial interface frame



Baud rates

The CX2001 supports a wide range from standard to high baud rates as listed *Table 16*.

The CX2001 startup baud rates are 120 kBaud and 115.2 kBaud.

Supported baud rates

Table 16 lists the baud rates supported by the CX2001.

Table 16. Supported baud rates

Baud rates (bps)		
4,950,000		1,800,000
4,920,000		1,500,000
4,860,000		1,444,400
4,800,000		1,000,000
4,050,000		921,600
4,000,000		750,000
3,692,300		162,500
3,690,000		120,000
3,600,000		115,200
3,250,000		81,250
3,000,000		60,000
2,000,000		38,400
1,843,200		

Timing

The UART interface complies with the timing characteristics indicated in *Table 17*.

Figure 9. UART interface timing

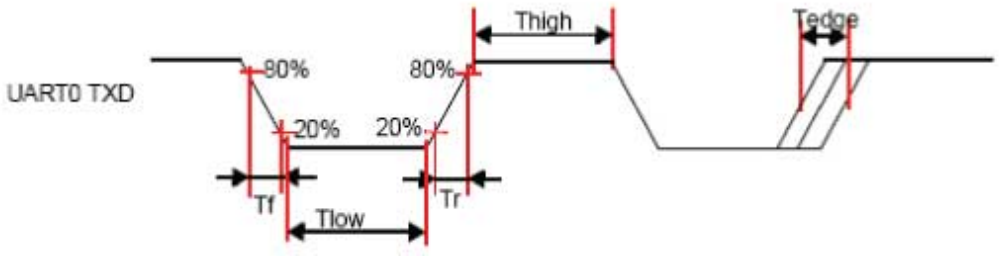


Figure 10. UART0 RXD timing

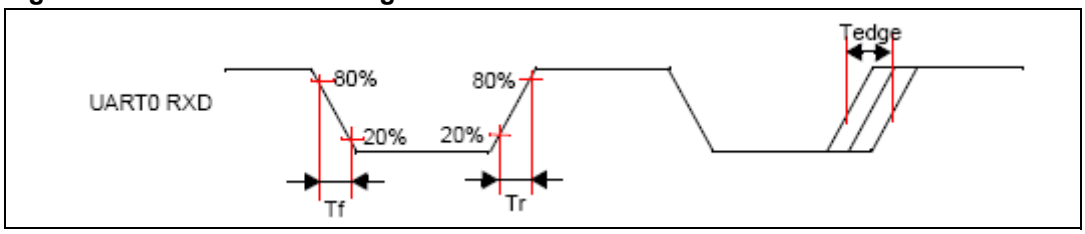


Table 17. UART timing

Symbol	Parameter	Min	Typ	Max	unit
Tlow	TXD output high time	90	-	107	% of Tbaudrate
Thigh	TXD output low time	90	-	107	% of Tbaudrate
Tedge	TXD error on any edge position compared to ideal baud rate position	-8	-	8	% ideal TbaudRate
Tr	TXD output rise time (15pF load)	1.5	-	5	ns
Tf	Output fall time (15pF load)	1.5	-	5	ns

Table 18. UART RXD timing

Symbol	Parameter	Min	Typ	Max	unit
Tedge	RXD error on any edge position compared to ideal baud rate position	-10	-	+10	% ideal TbaudRate
Tr	RXD input rise time	-	-	15	ns
Tf	RXD input fall time	-	-	15	ns

1.8.4 SPI interface

The implemented SPI interface is a synchronous serial interface used for the GPS/BT/FM control and data transfer.

Interface description

The SPI interface consists of five wires + one optional wire:

- CS_SPI to select the device before data exchange
  This signal is driven by the host and is active at low level during each SPI frame.
- CLK_SPI to clock the data
  It is active for a multiple of data length cycles during SPI transfer. The clock is driven by the host, and can also be active outside the SPI frame selection, for example, when the CX2001 is integrated into a multiple slaves architecture scenario.
- MOSI_SPI to receive the data
  Master sets data on the negative edge of the clock, while the slave samples it on the positive edge of the clock.
- MISO_SPI to transmit the data
  Slave sets data on the negative edge of the clock, while the master samples it on the

positive edge of the clock.
When the chip select signal is inactive, this pin is set to the tristate mode.

- INT_SPI to indicate a data transmission request
  The signal is managed from the slave (i.e. the CX2001) and is used to request a SPI transfer to the master. This signal is active at high level, thus implies the host shall be level sensitive.
- FLOW_SPI to control the incoming data flow (optional)
  The CX2001 uses this signal to indicate its reception buffer is ready to receive data.

The data size handled is 16-bits. The supported endianness is either the MSW first (but LSW first is also possible) or the MSB first (but LSB first is also possible).

Operations

The CX2001 supports only the slave role in half-duplex mode. The SPI data length, endianness (byte or bit usage) and flow control are configurable, and the host may change it via the SPI configuration register usage.

The host can send only one H4 packet per SPI transfer. However, the device supports the packet based flow control.

The maximum operating frequency of the SPI bus is 52 MHz.

The CX2001 may use the flow control capability to inform the host about its reception capability. This indication is available to the host via three ways:

- MISO_SPI signalization using the time between CS_SPI activation and CLK_SPI positive edge.
- Register reading
- FLOW_SPI

In half duplex operation, only the slave or master can transfer data at a given time (i.e. data sent by the receiving device is ignored by the transmitting device). All transfers start with the master sending a 2 bytes command field (=2 words) to indicate the transfer direction: read or write. In case of a read transfer, data moves from slave to master, while for a write transfer data moves from master to slave. During a read access, the 2 words sent by the slave are filling character (0xFF). During a write access, the slave sends only filling characters (0xFF). The master will ignore the filling characters sent by the slave.

Caution: The master can send only one H4 packet per SPI transfer.
The CX2001 can not request a write transfer.
Although supported, the master requesting a read transfer does not match a standard mobile phone application.

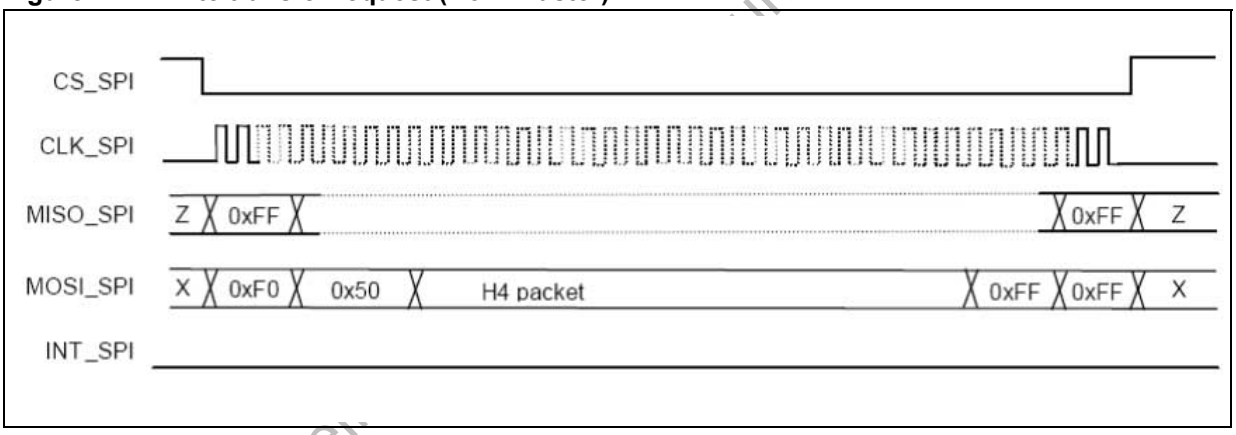
Table 19. SPI command words

1st command word	2nd command word	Purpose
0xF0		Write transfer command
	0x50	Reserved for future usage
0x80		Read transfer command
	0x50	Reserved for future usage
0x20		Sleep command
	0xFF	Reserved for future usage
0x40		WakeUp command
	0xFF	Reserved for future usage

- Master initiates a write transfer

The master can initiate a transfer to the slave at any time. It activates the chip select, the clock, and sends the write command words followed by the H4 packet and eventual filling characters as shown by *Figure 11*. The slave receives the H4 packet and filling characters until the transfer is completed. The completeness of the SPI transfer is indicated via de-assertion of the CS_SPI signal.

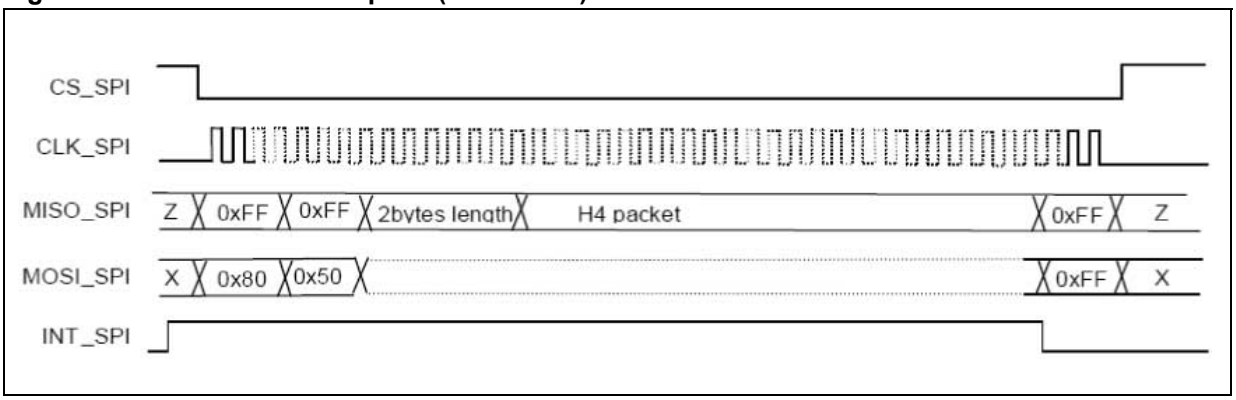
Figure 11. Write transfer request (from master)



- Slave initiates read transfer

The slave can request a read transfer at any time by setting the INT_SPI interrupt line. When ready to receive, the master asserts signals as mentioned previously (see *Figure 12*). The slave de-asserts the INT_SPI during the last byte transfer. Due to the internal 32-bit operation, the slave always sends data sized as a multiple of 4 bytes. This means that up to three filling characters may be sent. However, the host can also de-assert the CS_SPI signal before reading all the filling characters from the device (because of H4 packet length real-time analysis). In this case, the slave flushes the remaining filling characters and sets the INT_SPI signal to the low level immediately (< 1 data clock cycle).

Figure 12. Read transfer request (from slave)



- Sleep and wakeup command

Next to the read and write commands, the SPI interface supports sleep and wakeup commands. Both are 2 words long. The sleep command is 0x20FF and the wakeup command is 0x40FF. Each of these commands triggers a specific interrupt internally to the CX2001, so the software can take appropriate actions.

Timing

The SPI interface complies with the timing characteristics indicated in *Table 20*.

Figure 13. SPI interface timing

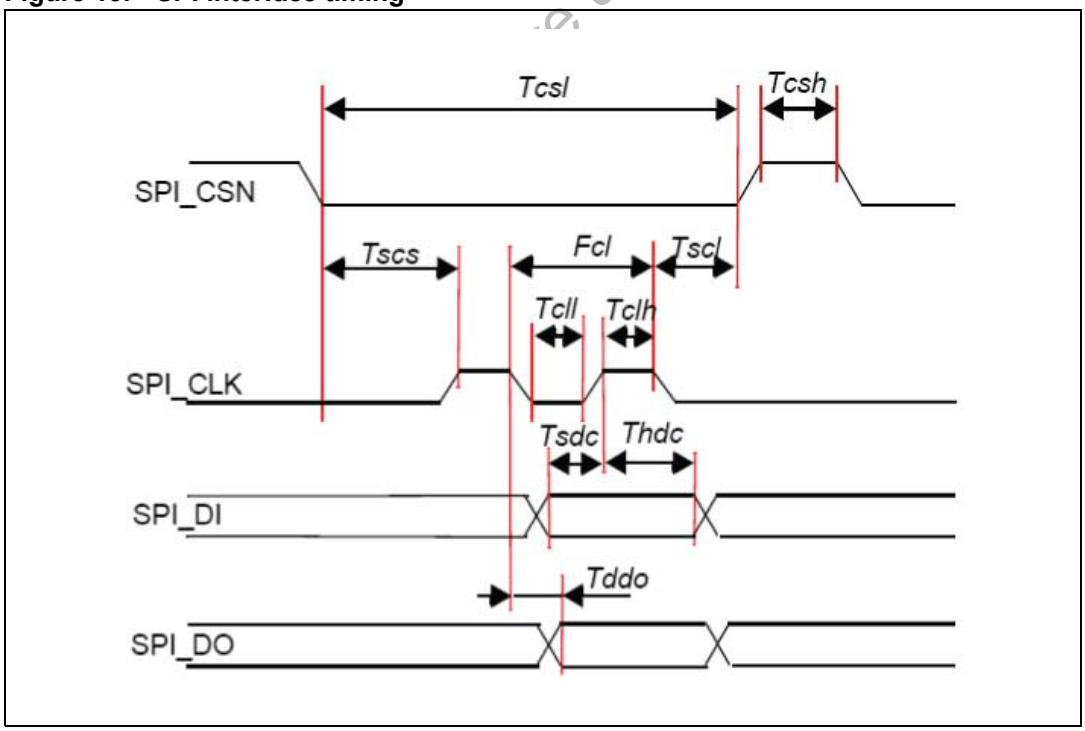


Table 20. SPI timing(1)

Symbol	Parameter	Min	Typ	Max	unit
Fcl	spi_clk frequency	1	-	52	MHz
Tclh	spi_clk high time	9	-	-	ns
Tcll	spi_clk low time	9	-	-	ns
Tcsh	high time of spi_csn	1 x Tcl	-	-	ns
Tcsl	low time of spi_csn	9 x Tcl	-	-	ns
Tscs	set-up time spi_csn low to spi_clk high	1 x Tcl	-	-	ns
Tscl	set-up time spi_clk low to spi_csn high	Tcl / 2	-	-	ns
Tsdc	set-up time spi_di valid to spi_clk high	50	-	-	ns
Thcd	hold time spi_di valid from spi_clk high	50	-	-	ns
Tddo	delay from spi_clk falling edge to spi_do valid	-	-	250	ns

1. Tcl = 1 / Fcl

1.8.5 PCM/I2S1 interface

The implemented PCM/I2S1 interface is a synchronous serial interface used for the transfer of voice/audio samples with full duplex capabilities. The PCM/I2S1 interface can also be used as audio interface when the CX2001 is running the BT A2DP.

A standard application may be running BT (Wideband) speech and/or FM stereo transmission/reception, between the CX2001 and an external device (for example, host system or codec).

Interface description

The PCM/I2S1 interface consists of four wires:

- FSC_IP is used to synchronize the slave device regarding data exchange.
  FSC_IP signal is driven from the master and is an active pulse at high level. Its position is configurable. FSC_IP is used as word select in I2S mode.
- DCLK_IP is used to clock the data
  The activity duration depends on the way the PCM interface is used. The clock is driven from the master.
- DA_IP and DB_IP are used to transmit/receive respectively data A and B.

The PCM/I2S1 interface supports both the PCM and I2S timing. The I2S1 is compatible with the I2S specification, see *[9.]*.

Operations

The CX2001 supports both master and slave modes. In both modes, several configurations for the PCM clock and frame frequencies are supported as given in *Table 21*. When configured in master mode, PCM/I2S1 [I2S] interface can generate any clock frequency from 128 kHz to 4800 kHz. Typical supported frequencies are 128, 256, 512, 1024, 1536, 2000, 2048, 2400, 3072 kHz but other values are also possible.

The PCM interface is able to carry two streams with different sample frequencies multiplexed on a single PCM frame (for example, a 32-bit left and right at 48 kHz audio stream and a 8 kHz BT voice stream). This allows the simultaneous transfer of both BT SCO and FM or both BT SCO and BT A2DP over the same PCM frame.

This is achieved according to the following principle:

- The FSC_IP frequency, slave mode used, is the highest of the two stream sample frequencies;
- A *ratio_value* features the frequency ratio of the two sampling frequencies. By convention, for the stream having the smaller sampling frequency:
  The output data is repeated over *ratio_value* PCM frames.
  The input data is expected once every *ratio_value* PCM frames.

Table 21. PCM frame duration in number of PCM clock cycles (master and slave modes)

DCLK_IP [kHz] / FSC_IP [kHz]	128	256	512	768	1024	1411.76	1536	2000	2048	2400	2823.52	3072	4800 (1) (2)	Up to 26000
8	16	32	64	96	128	-	192	250	256	300	-	384	-	-
16	8(3)	16(4)	32	48	64	-	96	125	128	150	-	192	-	-

Table 21. PCM frame duration in number of PCM clock cycles (master and slave modes)

DCLK_IP [kHz] / FSC_IP [kHz]	128	256	512	768	1024	1411.76	1536	2000	2048	2400	2823.52	3072	4800 (1) (2)	Up to 26000
32	-	-	-	-	-	-	-	-	-	-	-	-	-	-
44.1	-	-	-	-	-	32	-	-	-	-	64	-	-	-
48	-	-	-	16	-	-	32	-	-	50	-	64	100	-
Up to 500	-	-	-	-	-	-	-	-	-	-	-	-	-	>=32(1)

1. Slave mode only.
2. Clock frequency to support both FM audio (left and right channels) and BT-SCO (two channels) or both BT-A2DP and BT SCO.
3. Only one 8-bits slot (A-law, µ-law voice channel) is allowed.
4. Only one 16-bits slot (one PCM linear 16-bit voice channel) is allowed.

In PCM framing mode, a PCM frame starts with the PCM synchronization pulse. The position of this PCM synchronization pulse is programmable as either the first (*Figure 14*) or the last (*Figure 15*) bit of the frame. The number of PCM clock cycles between two PCM synchronization pulses defines the PCM frame duration. There are up to four active slots supported within a PCM frame.

Each active PCM slot can be either 8 or 16 bits wide. For each slot, the slot start time relative to FCS_IP can be programmed in PCM clock cycles. The timing of the PCM slots must be such that slot 0 is always located before slot 1. It is, however, possible to only use for example slot 1 and not slot 0. The DCLK_IP activity can be programmed to be active until the last data bit, or can be continuously active over the whole PCM frame. The PCM data in and data out can, per active slot, be programmed to be mapped on DA_IP or DB_IP.

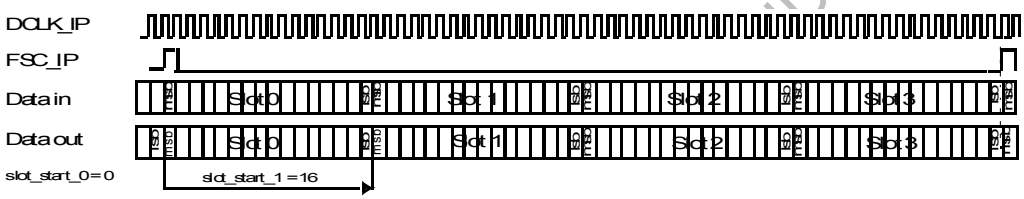
Figure 15 shows example of a PCM frame. The PCM frame starts with FSC_IP followed by the PCM slots. In this example, the PCM frame consists of four PCM slots, the first one (slot 0) is 16 bits wide and starts at PCM bit 1, the second one is 16 bits wide and start at PCM bit 17, and so on.

If pcm_clk > 16,000 kHz, CX2001 will not use the last slot/bits in the PCM frame.

The examples are as follows:

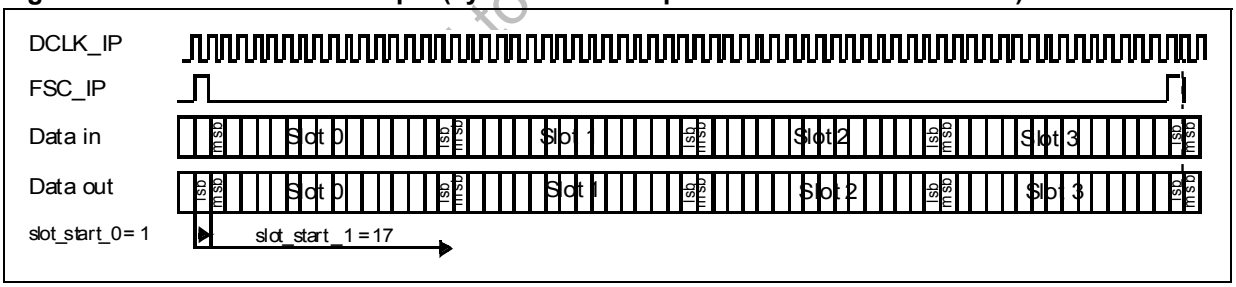
1. PCM frequency is 16 MHz or below , pcm_sync frequency is 500 kHz and frame period is 32,
   slot 0 active
   slot 1 active starting at 16 position
2. PCM frequency is 26 MHz, pcm_sync frequency is 500 kHz and frame period is 52,
   slot 0 active
   slot 1 active starting at 16 position
3. PCM frequency is 19.2 MHz, pcm_sync frequency is 492.3 kHz and frame period is 39,
   slot 0 active
   slot 1 active starting at 16 position
4. PCM frequency is 19.8 MHz, pcm_sync frequency is 495 kHz and frame period is 40,
   slot 0 active
   slot 1 active starting at 16 position

Figure 14. PCM transfer example (synchronization pulse is first bit of the frame)



1. *slot_start_0* = 0, first data bit of slot 0 occurs within the same DCLK_IP cycle as FSC_IP rising edge.
2. *slot_start_1* = 16.

Figure 15. PCM transfer example (synchronization pulse is last bit of the frame)



1. *slot_start_0* = 1, first data bit of slot 0 occurs 1 DCLK_IP cycle after FSC_IP rising edge.
2. slot_start_1 = 17

As it is important to synchronize the voice path, there are several configurations as outlined below:

- Bluetooth master and PCM master
  In this case, the voice path is synchronized.
- Bluetooth master and PCM slave
  In this case, the voice path is synchronized.
- Bluetooth slave and PCM master
  In this case, the voice path is synchronized. The PCM timing is synchronized to the

Bluetooth timing. Due to the synchronization, PCM clock cycles within the PCM frame may be stretched or shortend.

- Bluetooth slave and PCM slave
  In this case, there is no voice path synchronization and, depending on the drift between the PCM slave and the Bluetooth slave timings, a PCM sample is lost or duplicated.

Timing

In PCM framing mode, the PCM synchronization pulse is a one PCM clock cycle pulse. The received PCM data are sampled on the falling edge of the DCLK_IP, whilst the PCM data to send are output on the rising edge of DCLK_IP.

The PCM interface is defined according to the timing indicated in *Figure 16*. In slave mode, data is sampled using the clock edges as shown in *Figure 17*.

In I2S1 mode, synchronization is performed using FSC_IP as word select signal. The received I2S1 data are sampled on the rising edge of DCLK_IP, whilst the PCM data to send are output on the falling edge of DCLK_IP.

Figure 16. PCM interface timing (master mode)

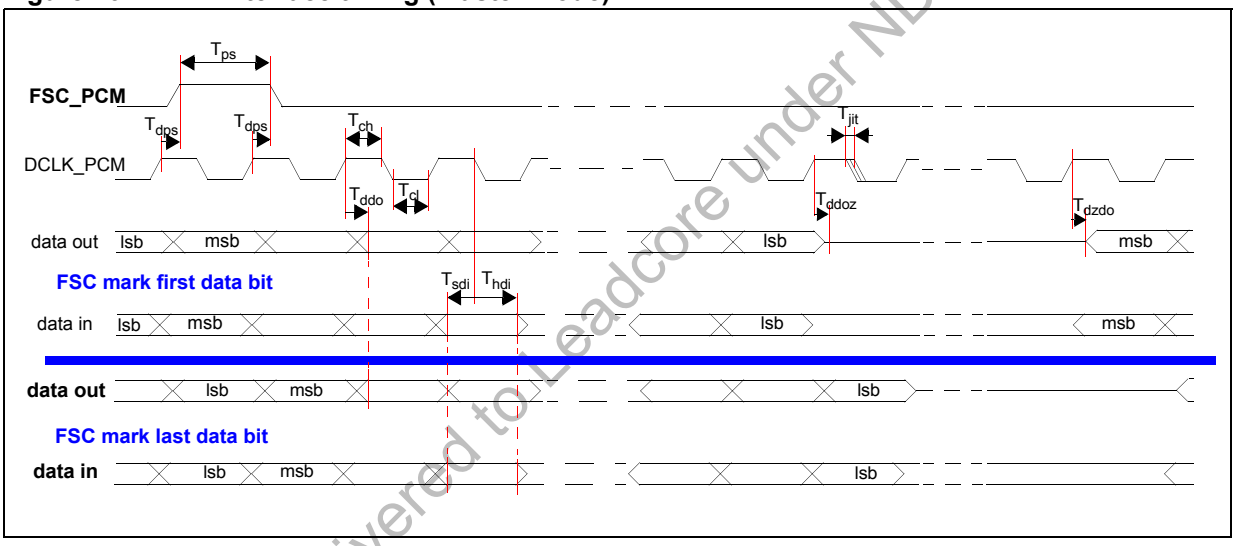


Table 22. PCM master timing

Symbol	Parameter	Min	Typ	Max	Unit
Tps	FSC_IP high time	260	-	-	ns
Tch	DCLK_IP(1) high time	130	-	-	ns
Tcl	DCLK_IP(2) low time	130	-	-	ns
Tjit	DCLK_IP jitter	-	-	62.5	ns
Tdps	Delay from DCLK_IP rising edge to FSC_IP edge	-	-	50	ns
Tddo	Delay from DCLK_IP rising edge to dataout transition	-	-	50	ns
Tdzdo	Delay from DCLK_IP rising edge and dataout High-Z to dataout valid	-	-	50	ns
Tddoz	Delay from DCLK_IP rising edge to dataout High-Z	-	-	50	ns

Table 22. PCM master timing (continued)

Symbol	Parameter	Min	Typ	Max	Unit
Thdi	Hold time from DCLK_IP falling edge to datain transition	50	-	-	ns
Tsdi	Set-up time of datain to DCLK_IP falling edge	50	-	-	ns

1. Max DCLK_IP high/low time and FSC_IP high time corresponds to DCLK_IP at 128 kHz.
2. Min DCLK_IP high/low time and FSC_IP high time corresponds to DCLK_IP at 3072 kHz.

Figure 17. PCM interface timing (slave mode)

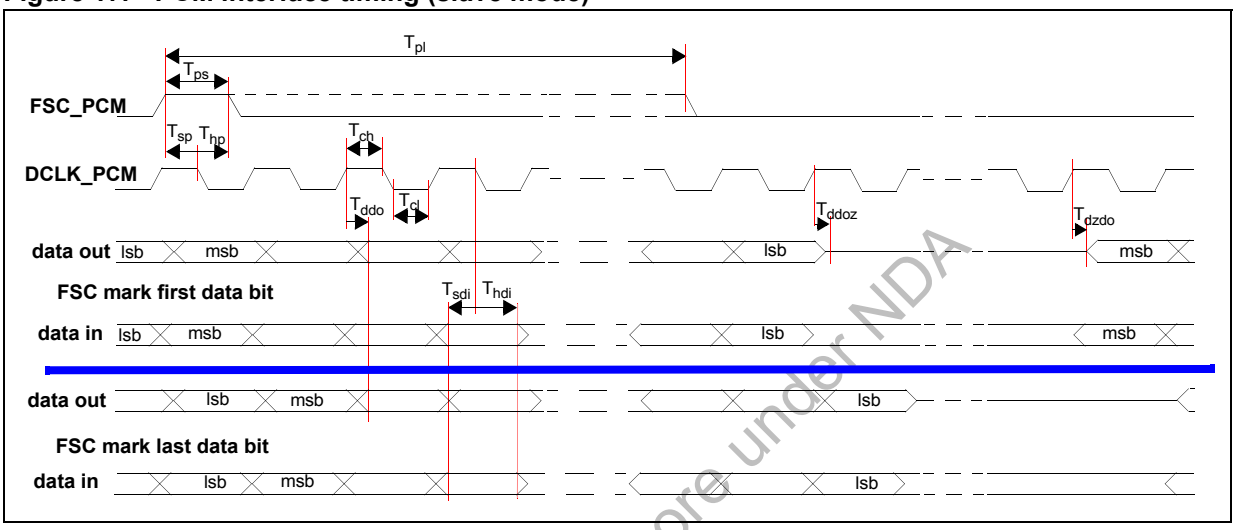


Table 23. PCM slave timing

Symbol	Parameter	Min	Typ	Max	unit
Tps	Short FSC_IP high time(1)(2)	$T_{clkburst}$	-	T_{128kHz}	ns
Tpl	Long FSC_IP high time	$T_{clkburst}$	-	$(N-1)^{(3)}$ (T_{128kHz})	ns
Tch	DCLK_IP high time	$T_{clkburst}/2$	-	-	ns
Tcl	DCLK_IP low time	$T_{clkburst}/2$	-	-	ns
Tsp	Set-up time from FSC_IP to DCLK_IP falling edge	10	-	-	ns
Thp	Hold time from DCLK_IP falling edge to FSC_IP	10	-	-	ns
Tddo	Delay from DCLK_IP rising edge to Dataout transition	-	-	20	ns
Tdzdo	Delay from *DCLK_IP* rising edge and dataout High-Z to dataout valid	-	-	20	ns
Tddoz	Delay from *DCLK_IP* rising edge to dataout High-Z	-	-	20	ns
Thdi	Hold time from *DCLK_IP* falling edge to datain transition	20	-	-	ns
Tsdi	set-up time of datain to *DCLK_IP* falling edge	20	-	-	ns

1. $T_{clkburst}$ is actually expected to be 16 MHz nominal ±20 ppm.
2. Other *DCLK_IP* input frequencies in between 128 kHz (featured by the period T_{128kHz}) to 4.8 MHz are actually expected to be f nominal ±20 ppm.
3. N represents the number of PCM clock cycles in a PCM frame.

1.8.6 Second I2S interface: I2S2

This I2S2 interface is a synchronous serial interface used for the transfer of voice/audio samples with full duplex capabilities (BT) or half duplex (FM).

The I2S2 interface can also be used as audio interface when the CX2001 is running the BT A2DP.

A standard application may be running BT (Wideband) speech or FM stereo transmission or reception, between the CX2001 and an external device (for example, host system or codec).

Interface description

The I2S2 interface consists of four wires:

- WS_I2S2 to select the data channel
  This signal is driven from the master and is active during all the channel selection. A low level selects the left channel, while a high level selects the right channel. This signal is continuously running when the interface is enabled.
- SCK_I2S2 to clock data
  The clock is driven from the master and it is continuously running when the interface is enabled.
- SDI_I2S2 and SDO_I2S 2 to respectively receive/transmit data
  Data is driven on the negative edge and read on the positive edge of the clock.

The data size handled is 16-bits. The supported bit ordering is MSB first, left justified.

Operations

The CX2001 supports both master and slave modes together with mono and stereo types as listed in *Table 23*. In both modes, several configurations for the I2S word selection and clock rates are supported as given in *Table 24*. When configured in master mode, the PCM/I2S2 [I2S] interface can generate any clock frequency from 128 kHz to 4800 kHz. Typical supported frequencies are 128, 256, 512, 1024, 1536, 2000, 2048, 2400, 3072 kHz but other values are also possible.

In stereo mode, the left and right data are transferred. In mono mode, the same data is output twice.

Table 24. I2S2 audio interface mode

I2S2-bus usage	Mode	Type	Direction
FM stereo transmission or BT A2DP	Master	Stereo	Uni-directional data input
FM stereo transmission or BT A2DP	Slave	Stereo	Uni-directional data input
FM stereo reception	Master	Stereo	Uni-directional data output
FM stereo reception	Slave	Stereo	Uni-directional data output
BT SCO	Master	Stereo left only	Bi-directional data
BT SCO	Slave	Stereo left only	Bi-directional data

Enabling or disabling the I2S2 interface usage is done via a host command. When disabled, the IO state is configurable to high-Z state, pull-up, pull-down, driven “1”, driven “0”.

Caution: For BT A2DP audio data and FM stereo audio data, it is provided at 48 kHz or 44.1 kHz. BT SCO handling is programmable, SCO channel 0 can be mapped on the left channel as indicated in *Table 24*.
In FM stereo handling or BT A2DP through WS_I2S2 signal indication, low level to indicate the left channel while high level is to indicate right channel.

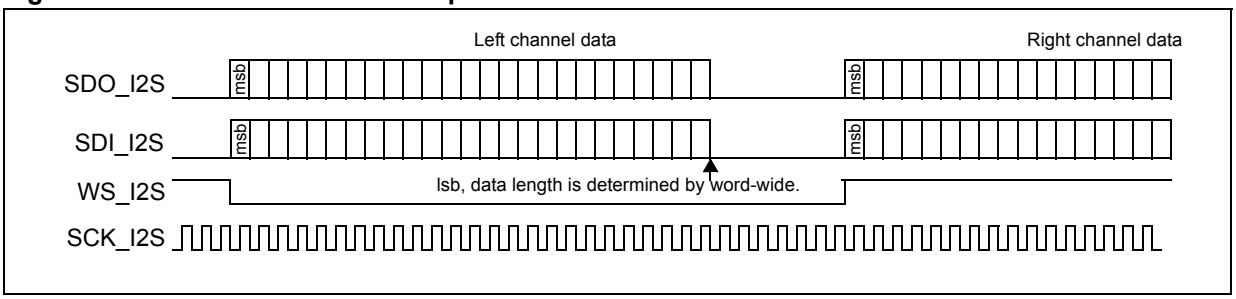
Table 25. I2S2 frame modes and rates

CLK [kHz]	WS [kHz]	Description
256	8	8 kHz, 32*FS, 32-bit/frame
512	16	16 kHz, 32*FS, 32-bit/frame
	8	8 kHz, 64*FS, 64-bit/frame
768	16	16 kHz, 48*FS, 48-bit/frame
	8	8 kHz, 96*FS, 96-bit/frame
1024	16	16 kHz, 64*FS, 64-bit/frame
	8	8 kHz, 128*FS, 128-bit/frame
1536	48	48 kHz, 32*FS, 32-bit/frame
	16	16 kHz, 96*FS, 96-bit/frame
	8	8 kHz, 192*FS, 192-bit/frame
2048	16	16 kHz, 128*FS, 128-bit/frame
	8	8 kHz, 256*FS, 256-bit/frame
2400	16	16 kHz, 150*FS, 150-bit/frame
	8	8 kHz, 300*FS, 300-bit/frame
3072	48	48 kHz, 64*FS, 64-bit/frame
	16	16 kHz, 192*FS, 192-bit/frame
	8	8 kHz, 384*FS, 384-bit/frame
1411.2	44.1	44.1 kHz, 32*FS, 32-bit/frame
	22.05	22.05 kHz, 64*FS, 64-bit/frame
2822.4	44.1	44.1 kHz, 64*FS, 64-bit/frame
	22.05	22.05 kHz, 128*FS, 128-bit/frame
16000(1)	up to 500	up to 16000 kHz, 32-bit/frame in slave mode only

1. Only 16-bit word width is supported

Figure 14 shows an example of an I2S2-bus frame.

Figure 18. I2S2-bus transfer example



Timing

In master mode, the I2S2 interface is defined according to the timing indicated in *Figure 19*. In slave mode, data is sampled using the clock edges as shown in *Figure 20*.

Figure 19. I2S2 master timing

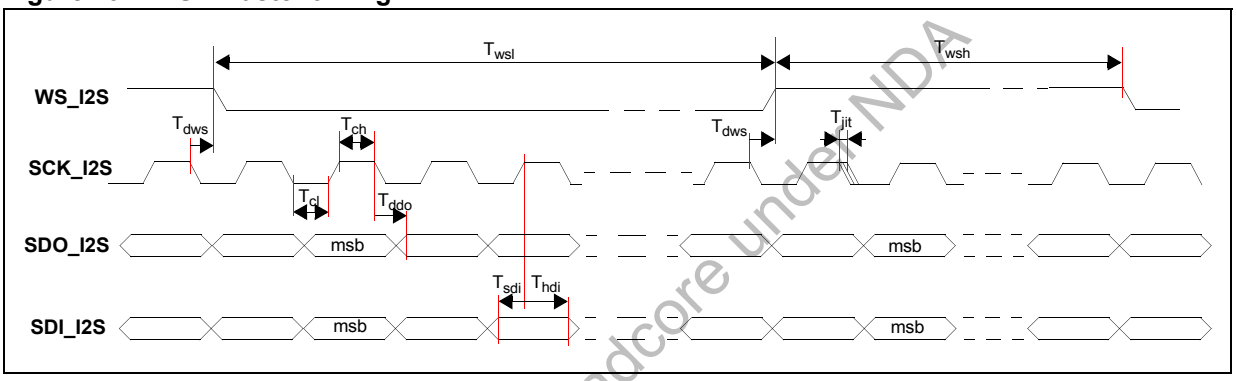


Table 26. I2S2 master timing

Symbol	Parameter	Min	Typ	Max	unit
Twsh	WS_I2S2 high time(1) (2)	16	-	-	SCLK_I2S2 cycles
Twsl	WS_I2S2 low time	16	-	-	SCLK_I2S2 cycles
Tch	SCK_I2S2 high time	125	-	-	ns
Tcl	SCK_I2S2 low time	125	-	-	ns
Tjit	SCK_I2S2 jitter	-	-	65	ns
Tdws	Delay from SCK_I2S2 falling edge to WS_I2S2 edge	-	-	50	ns
Tddo	Delay from SCK_I2S2 falling edge to SDO_I2S2 transition	-	-	50	ns
Tdzdo	Delay from SCK_I2S2 falling edge and SDO_I2S2 High-Z to SDO_I2S2 valid	-	-	50	ns
Tddoz	Delay from SCK_I2S2 falling edge to SDO_I2S2 High-Z	-	-	50	ns

Table 26. I2S2 master timing (continued)

Symbol	Parameter	Min	Typ	Max	unit
Thdi	Hold time from SCK_I2S2 rising edge to SDI_I2S2 transition	50	-	-	ns
Tsdi	Set-up time of SDI_I2S2 to SCK_I2S2 rising edge	50	-	-	ns

1. Max SCK_I2S and WS_I2S high/low time corresponds to SCK_I2S at 128 kHz.
2. Min SCK_I2S and WS_I2S high/low time corresponds to SCK_I2S at 3072 kHz.

Figure 20. I2S2 slave timing

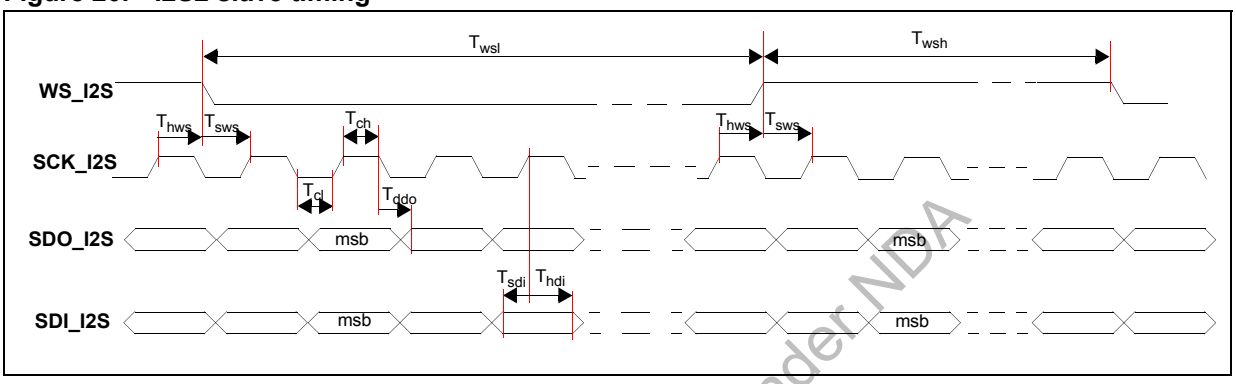


Table 27. I2S2 slave timing

Symbol	Parameter	Min	Typ	Max	unit
Twsh	WS_I2S2 high time	16	-	-	SCLK_I2S2 cycles
Twsl	WS_I2S2 low time	16	-	-	SCLK_I2S2 cycles
Tch	SCK_I2S2 high time	25	-	-	ns
Tcl	SCK_I2S2 low time	25	-	-	ns
Tsws	Set-up time from WS_I2S transition to SCK_I2S2 rising edge	20	-	-	ns
Thws	Hold time from SCK_I2S rising edge to WS_I2S2 transition	20	-	-	ns
Tddo	Delay from SCK_I2S2 falling edge to SDO_I2S2 transition	-	-	20	ns
Tdzdo	Delay from SCK_I2S2 falling edge and SDO_I2S2 High-Z to SDO_I2S2 valid	-	-	20	ns
Tddoz	Delay from SCK_I2S2 falling edge to SDO_I2S2 High-Z	-	-	20	ns
Thdi	Hold time from SCK_I2S2 rising edge to SDI_I2S2 transition	20	-	-	ns
Tsdi	set-up time of SDI_I2S2 to SCK_I2S2 rising edge	20	-	-	ns

1.8.7 Analog audio interface

The audio analog interface consists of two wires: AUDOL and AUDOR to receive the analog signal. These signals are used to receive the stereo analog audio from the FM RX.

The CX2001 supports output analog signals level as characterized in *Table 38*.

1.8.8 WLAN/WiMAX co-existence interface

The WLAN co-existence interface connects up to four wires between the CX2001 and the WLAN controllers. This interface is used to arbitrate the 2.4 GHz ISM band access to avoid interference between the BT and WLAN technologies when the distance between them is less than 50 cm (collocated scenario). Several priority algorithms have been implemented to maximize flexibility and efficiency when managing the priority handling.

The time division multiplexing and the priority mechanism combination avoids interferences due to packet collision. It also maximizes the 2.4 GHz ISM bandwidth usage for both devices while preserving the link quality.

The functionality of the wired connection depends on the selected algorithm, as explained below and summarized in *Table 28*.

The CX2001 supports four algorithms to provide efficient and flexible simultaneous functionality between the two technologies in collocated scenario:

- Algorithm 1:
  It is a PTA/ePTA (enhanced Packet Traffic Arbitration) based co-existence algorithm defined in accordance with the IEEE 802.15.2 recommended practice and proprietary features *[8.]*.
- Algorithm 2:
  The WLAN which is the master, indicates to the CX2001 when not to operate to prevent simultaneous access to the air interface, using only one signal connection.
- Algorithm 3:
  The CX2001 which is the master, indicates to the WLAN controller when not to operate to prevent simultaneous access to the air interface, using only one signal connection.
- Algorithm 4:
  Depending on host decision, the CX2001 or the WLAN controller is the master, using two signals connection.

The algorithm selection and the priority handling tuning are done via vendor specific HCI commands. By default, the algorithm 1 is used.

In the CX2001, the IO mapping of this interface (i.e. up to four wires) are fixed and assigned as indicated in *Table 28*.

Table 28. Co-existence signals assignment

Direction	Algo. 1	Algo. 2	Algo. 3	Algo. 4
BT -> WLAN	PTA_RF_REQUEST	Not used	WLAN_RF_NOT_ ALLOWED	WLAN_RF_NOT_ ALLOWED
BT -> WLAN	PTA_STATUS	Not used	Not used	Not used
BT -> WLAN	PTA_FREQ	Not used	Not used	Not used
WLAN -> BT	PTA_RF_CONFIRMN	BT_RF_NOT_ ALLOWED	Not used	BT_RF_NOT_ ALLOWED

Algorithm 1: PTA/ePTA (Packet Traffic Arbitration)

This co-existence algorithm allows dynamic bandwidth allocation to the two devices (for example, the full bandwidth can be allocated to the BT controller when the WLAN controller does not require any access).

The ePTA algorithm implements a major enhancement compared to the PTA algorithm by adding serial messages transfer over the same 4-wire interface. These messages take place to inform each other about the ongoing BT and WLAN traffic properties and to improve the scheduling and decision making on granting PTA signals.

When BT wants to perform a transaction, it indicates this to the WLAN device (RF_REQUEST). BT indicates whether the request is high or low priority (PRIO), whether the request is for a periodic packet (P) and whether it is a TX or RX activity (TX/RX). BT also indicates with a 6 bits linkID (L0-L6) for which BT link this request is done. The WLAN can associate this linkID with the information gathered in the serial messages send by BT over the same four wires. For BR/EDR, a transaction can be a TX/RX or a RX/TX combination, inquiry, paging, inquiry, and page scan. While for BLE a transaction can be a combination of advertising, scan request and scan response, or a scan (which can be cut in chunks with programmable length) or a TX/RX or RX/TX in connected state.

Figure 21. PTA/ePTA timing

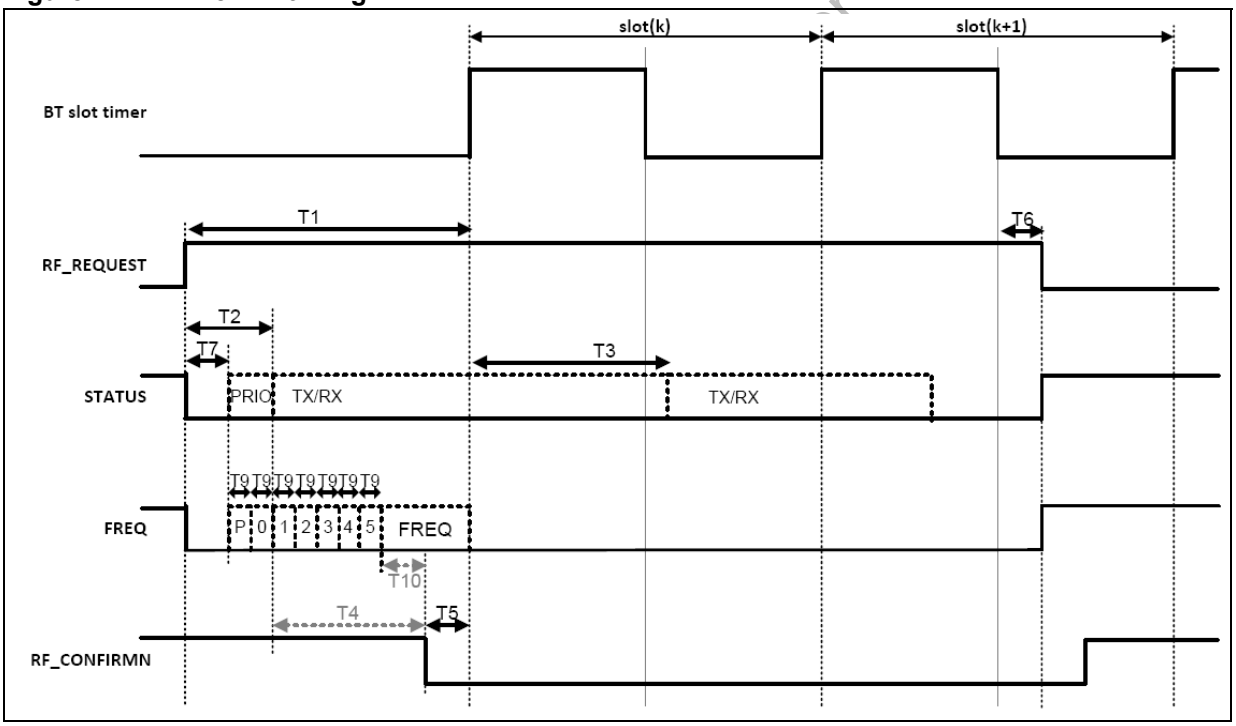


Table 29. PTA/ePTA timing

Parameter	Min (µs)	Max (µs)	Description
T_1	100	200	PTA_RF_REQUEST will be asserted before the medium is required.
T_2	0	20	The PTA_STATUS signal indicates the priority of a transaction for the duration of [T2-T7] after RF_ACTIVE is asserted. After T_2 PTA_STATUS line MAY indicate TX/RX mode of the subsequent slot(s).
T_3	360	475	If the PTA_STATUS signal will convey TX/RX mode, the PTA_STATUS signal shall be set to reflect the RX/TX mode for the slot N, T3 before the start of slot N.
T_4	-	160	For reference only.
T_5	75	-	If WLAN wishes to prevent a BT transmission, then it must de-assert (logic high) the PTA_RF_CONFIRMN signal at least 75 µs before the start of the BT transmit slot. The BT device will sample the PTA_RF_CONFIRMN signal T_5 (or shortly after) before the start of the transmit slot to determine whether transmit is allowed. Whenever PTA_RF_REQUEST is asserted, WLAN will not change the PTA_RF_CONFIRMN inside the T_5 window prior to start of a TX slot.
T_6	0	15.5	PTA_RF_REQUEST will be de-asserted within 25 µs after last RX or TX activity of the transaction has ended.
T_7	0	1	The PTA_STATUS signal will indicate priority of the signal no later than 1us after PTA_RF_REQUEST is asserted
T_9	1	10	On the PTA_FREQ line, the periodicity bit P and the 6 bits of the linkID are present for T9.
T_{10}	5	72	For reference only.

WiMax co-existence interface

The WiMax co-existence interface connects a single wire between the CX2001 and the WiMax controllers. The goal of the WiMax PTA implementation is to protect the traffic in the WiMax licensed bands adjacent to both ends the 2.4 GHz ISM band used by the Bluetooth.

The WiMax disable pin is interpreted as a systematic request to immediately shut down any ongoing or scheduled RF TX activity on the Bluetooth side. The WiMax system should assert this pin each time the WiMax RX activity takes place. The disable pin is directly connected to the BT radio control and BT TX shutdown happens in less than 20 µs.

1.8.9 GPS RF interface

The GPS receiver uses a single ended 50 Ω SAW filter.

More details can be found in CX2001 hardware user manual *[10.]*.

1.8.10 BT RF interface

The Bluetooth transceiver has an on-chip balun and hence uses a single ended 50 Ω bandpass filter.

More details can be found in CX2001 hardware user manual *[10.]*.

1.8.11 FM RF interface

FM embedded antenna

The CX2001 supports an FM embedded antenna, implemented as an inductive loop connected to FM_ANT. This antenna can be used for both FM TX and FM RX.

A filter between the antenna and the FM_ANT pin is needed to filter out FM TX out of band components. This filter consists of an inductor and a capacitor.

FM wire antenna

The CX2001 also supports an FM wire antenna, connected through an inductor to FM_WANT. The inductor value and Q factor are important to reach good sensitivity. The FM wire antenna can only be used for FM RX.

More details can be found in CX2001 hardware user manual *[10.]*

1.9 HCI interface

The CX2001 implements a common HCI interface to control the GPS, BT, and FM subsystems, which supports the H:4 “HCI UART transport layer” protocol *[6.]* by means of:

- the BT-SIG standard commands for the BT subsystem.
- vendor specific commands for GPS, BT, and FM subsystems.

The HCI interface applies an arbitration mechanism (round-robin priority) to serve all the subsystems (GPS/BT/FM) when used simultaneously.

The HCI interface (UART and SPI) supports low power modes. The system deep sleep mode is entered when allowed by the host. The HCI wake-up mechanism is used to wake-up the device.

1.9.1 H4 UART Transport Layer

The HCI transport layer supported on the UART is the H4 transport layer defined by the SIG *[6.]*. The HCI UART transport layer assumes that the UART communication is free from line errors.

For UART, the CX2001 allows to use either 115.2 kBaud or 120 kBaud. After the startup phase, this Baud rate can be modified on the fly via a vendor specific HCI command.

For UART, the HCI flow control is implemented, but there is not software flow control (i.e. XON/XOFF), inside the firmware.

The support for hardware handshaking (i.e. CTS/RTS) can not be disabled.

Enter and exit the low power modes are supported (For more details, refer to *[11.]*):

- H4 UART: using UART_RXD and UART_RTS.

The UART interface is defined in *Section 1.8.3*.

1.9.2 H4 SPI transport layer

The HCI transport layer supported on the SPI is the H4 transport layer defined by the SIG *[6.]*. The HCI SPI transport layer assumes that the SPI communication is free from line errors.

In addition, a messaging protocol is defined for controlling the Deep Sleep mode entry and wake-up. Three messages are defined: SLEEP, WAKEUP, and WOKEN. For details, refer to *[11.]*.

One way to enter and exit the low power modes is supported (For details, refer to *[11.]*):

- Enhanced H4 SPI: using SPI_INT and the SPI in band signaling.

The SPI interface is defined in *Section 1.8.4*.

1.10 Multimedia features

Because of its ultra low power audio DSP, the CX2001 offers efficient offloading to reduce the host computation needs and to optimize overall platform power.

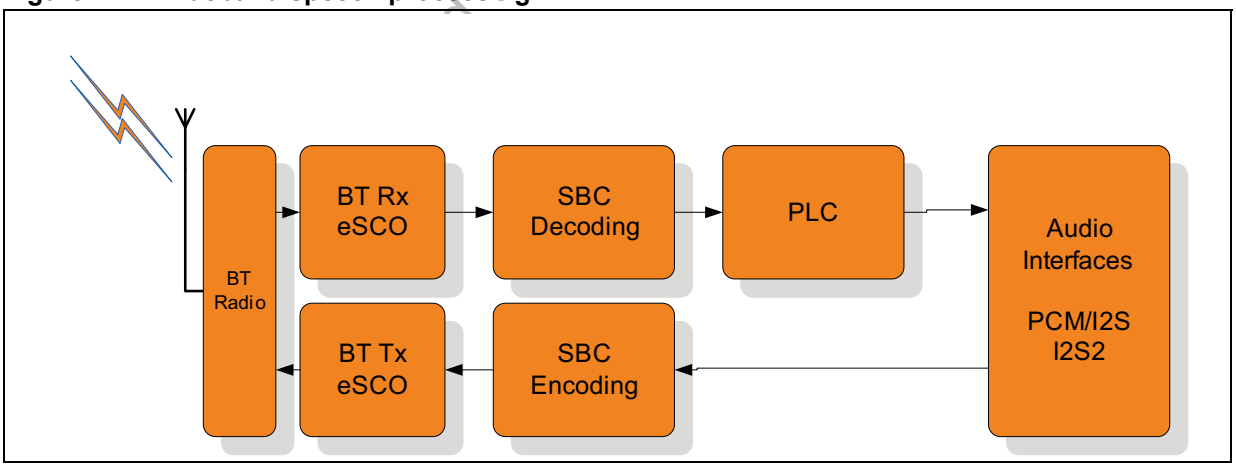
1.10.1 Wideband speech support

The CX2001 embeds support of SBC encoding and decoding for Wideband speech. The whole processing is performed internally and does not require dedicated processing from the host side.

Raw audio samples (16 bit at 16 kHz) are transferred over PCM/I2S interface and all the necessary processing, such as SBC codec and encapsulation in (e)SCO packets is handled internally is the CX2001.

A packet loss concealment algorithm allows improving the received voice quality in case of difficult BT link conditions.

Figure 22. Wideband speech processing



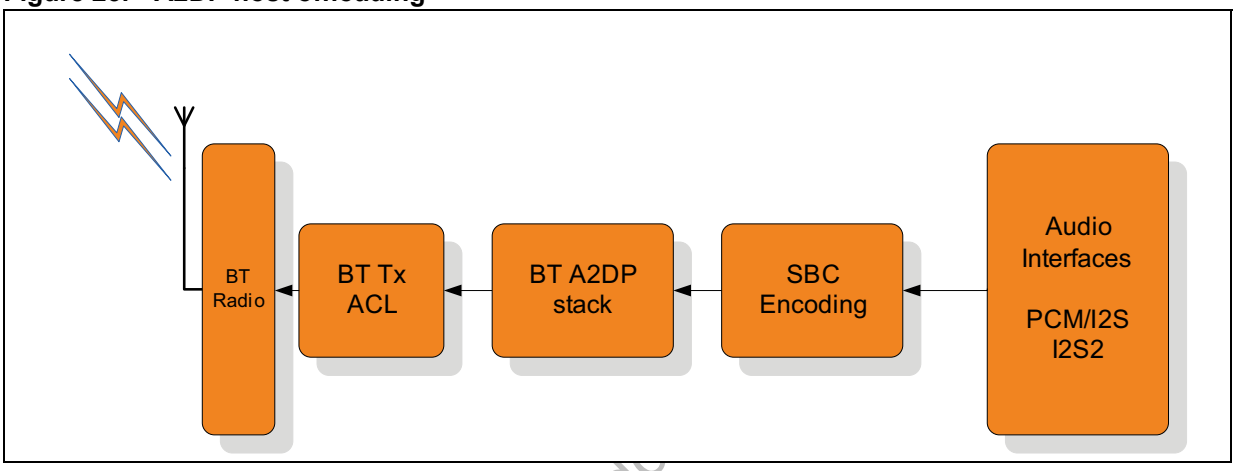
1.10.2 SBC host offloading for A2DP

BT A2DP offloading can also be performed with audio data transferred from the host over PCM or I2S. This slightly reduces the processing needs at the host side for A2DP streaming (becomes similar to playback with wired headset).

In that mode, the host sends stereo audio data samples (44.1 or 48 kHz) to the CX2001. This data is encoded locally using SBC and encapsulated in A2DP and L2CAP frames for sending over the air.

Data can be transferred in burst mode over the PCM or I2S interface to achieve significant host power consumption improvements during A2DP playback.

Figure 23. A2DP host offloading



1.10.3 Direct loopback of FM Rx to BT link

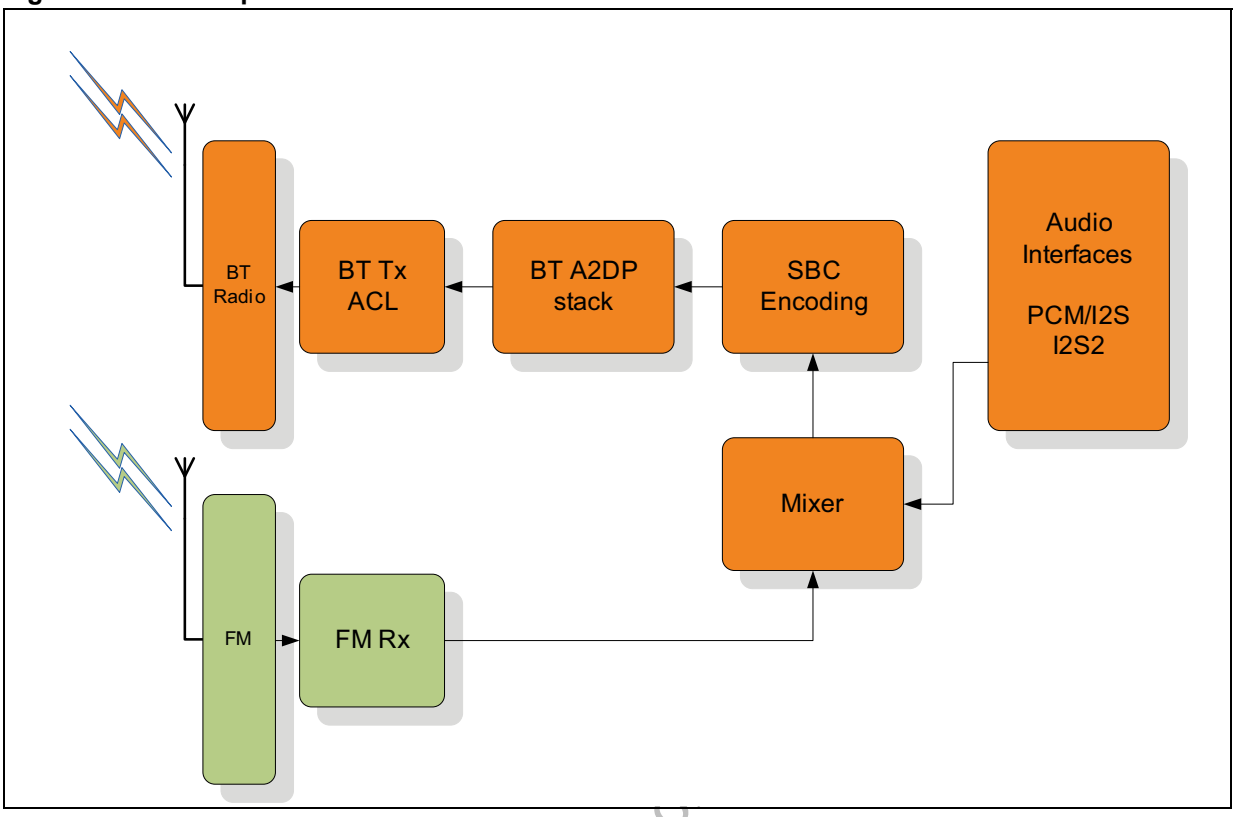
The CX2001 implements the streaming of FM radio over a BT A2DP or an eSCO link without any involvement of the host during the streaming. This leads to a drastic reduction of the power consumptions as the host can stay continuously in sleep mode.

All the necessary processing that is normally done in the host is handled inside the CX2001. This includes SBC encoding and A2DP/L2CAP framing.

Ring tone or system sounds generated from the host can be seamlessly mixed with the FM-RX audio-stereo data sent over BT. The audio tone is received over the audio interface (PCM/I2S1 or I2S2) and is mixed with the FM RX signal that is then SBC-encoded by the CX2001. Mixer is capable of detecting the presence of a tone and initiates the mixing automatically.

Mixing parameters are fully configurable (fade-in/out timings and main/background music levels) to provide optimal audio performances.

Figure 24. FM loopback over BT A2DP



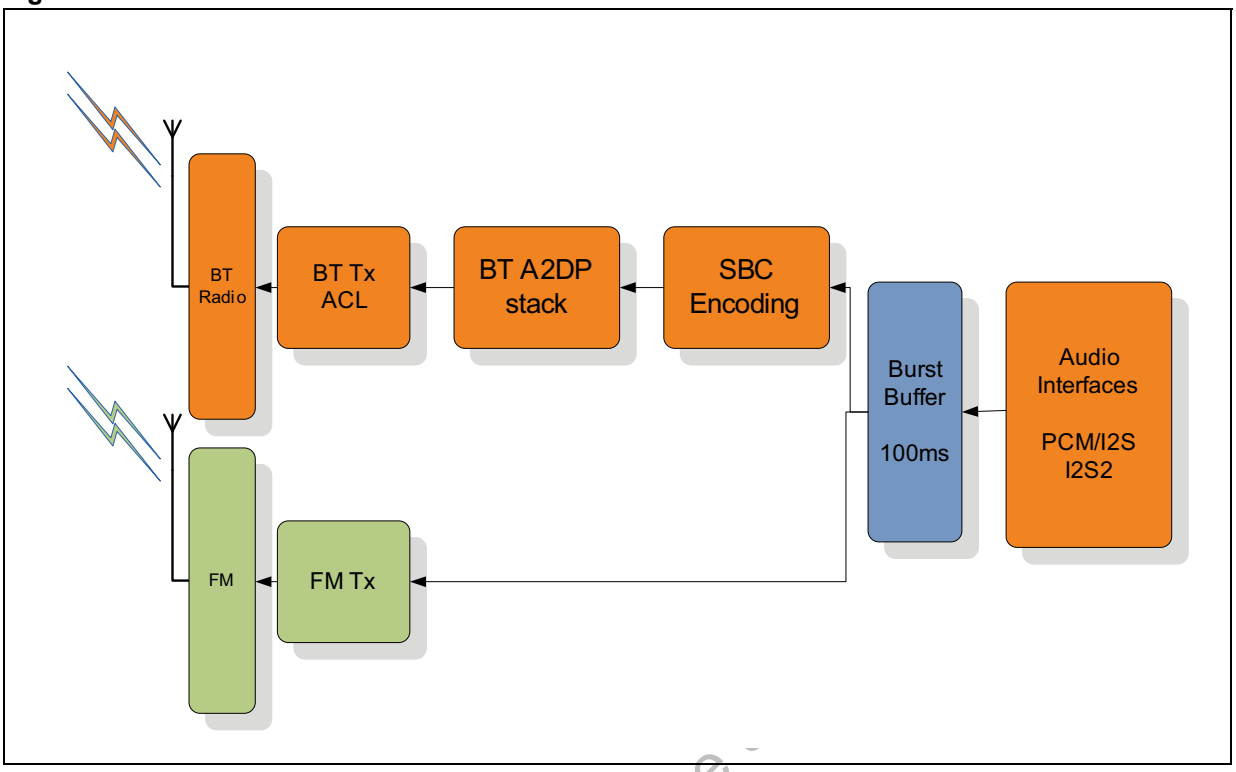
1.10.4 Audio burst mode

The CX2001 offers methods to decrease platform communication during A2DP or FM TX streaming. Because of its large audio buffer, the CX2001 can store audio samples transferred in burst from the host over audio interfaces (PCM/I2S).

Once the audio samples are transferred, the host can enter low power sleep mode and the audio is streamed from the burst buffer over either FM TX or A2DP.

Burst request mechanism can be handled either through an HCI event or by using the unused PCM data_out line as an interrupt line to the host.

Figure 25. Audio burst mode



2 GPS subsystem

The CX2001 provides a complete GPS solution designed for ease of integration into host platforms. The key components are described below.

- Baseband channel block
  - Flexible multichannel architecture readily adaptable for search or tracking
- GPS software
  - Indoor acquisition and tracking
  - Stand-alone GPS operation
  - Instant fix mode
- Host-based navigation software
  - Well-defined API for control and reporting to host applications
  - 'OS wrapper' enabling simple porting to customer-preferred operating system
  - Network-assistance ready (mobile-based, mobile-assisted, CDMA, W-CDMA, GSM, control plane and user plane)
  - Support of different location-based service protocols

2.1 Receiver section

The CX2001 includes a low-power, single-conversion low-IF GPS receiver for the 1575.42 MHz, L1 signal. The device contains a fully-integrated GPS receive path, including LNA, that down-convert the GPS L1 signal of 1575.42 MHz, to an IF signal quantized to 4 bits and delivered to the integrated GPS baseband device.

2.2 Additional GPS-related features

- Channels: dynamic channel and dynamically configurable architecture management
- Positioning modes: autonomous/standalone, mobile-assisted, mobile-based, simultaneous or mixed modes, navigation (Kalman filter)
- Update rate: user selectable - event, position, command/request, periodic (2 per second to once per hour)
- Host software protocol support: NMEA 0183, ST-Ericsson API
- Application microprocessor requirements: no real-time processing requirements, only requirement is C-compiler and floating-point libraries

2.3 GPS baseband

2.3.1 Overview

The GPS baseband provides the baseband signal processing for the GPS receiver (IF down-conversion, correlation and integration). The GPS baseband includes an embedded DSP whose firmware controls the baseband's GPS acquisition and tracking. The DSP firmware is a ROM within the CX2001 that does not require support from any external

device. Higher-level software running on a separate host calculates navigation solutions (the host-based navigation software).

The GPS baseband has the following features:

- Embedded DSP
- Correlation engine
- GPS code generation
- Coherent and incoherent summation block
- Doppler wipe off
- Magnitude calculation
- Compare-and-threshold signal detection
- Timing and control
- Power saving
- Clocking architectures
- Integrated universal asynchronous receiver/transmitter interfaces
- Measurement engine with a search capacity of 35000 correlators
- 14 search and three track channels used to track up to 47 individual satellite signals

2.3.2 Embedded DSP firmware

The embedded DSP firmware performs the following functions:

- Interfaces to GPS baseband hardware
- Searches for satellites either autonomously or commanded using acquisition data from the host
- When a satellite has been acquired, transitions to track the satellite
- Where possible, demodulates the satellite navigation message data
- During satellite tracking, monitors the signals for validity and multipath
- At the required update rate (typically 1 Hz) sends the latest raw satellite measurements to the host-based navigation software

All real-time, critical or high-interrupt rate functions are performed within the embedded DSP firmware.

2.3.3 Interface between CX2001 and host-based navigation software

Communication to the GPS baseband can be via the Bluetooth HCI interface.

The host-based navigation software sends requests for when the next raw satellite measurements are required, and also provides satellite acquisition aiding data and channel/satellite reset commands.

The host-based navigation software also sends the CX2001 mode set commands for Sleep, Coma, or Deep coma. The Sleep mode command also specifies a time-out for the automatic transition from Sleep to Coma mode. A wake-up command is also provided.

The CX2001 responds by sending raw satellite measurements to the host-based navigation software at the requested time, and also provides the parity-checked raw subframes of the satellite navigation messages (when available).

2.3.4 Firmware update mechanism

To be able to update the firmware, a patch mechanism is implemented in the GPS subsystem. The patch is downloaded to RAM. In the application, the download can be done through dedicated HCI commands sent by the host stack software. More details are provided in *[11.]*

2.4 GPS performance

Table 30. GPS performances(1)(2)(3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Antenna input						
$\|S_{11}\|^2$	Input return loss	50 ohm	-4	-6	-	dB
NF	Input Noise Figure	cascaded	2.0	2.5	3.5	dB
LO_{leak}	LO leakage		-	-	-80	dBm
Sensitivity						
	GPS tracking		-165	-163	-161	dBm
	GPS acquisition(4)	(4)	-147	-145	-142	dBm
	aGPS acquisition	fine time accuracy(5)	-	-161	-	dBm
		approximate time accuracy	-157	-155	-153	dBm
GPS TTFF(6)(7)						
	GPS (95 % TTFF)	Cold start (open sky) @ -130 dBm(4) (8)	-	38	-	sec
		Cold start (open sky) @ -135 dBm(4) (8)	-	45	-	sec
		Cold start (open sky) @ -143 dBm(4) (8)	-	110	-	sec
	aGPS (50% TTFF)	-130 dBm(9)	-	2	-	sec
		-148 dBm(9)	-	8	-	sec
		-152 dBm(9)	-	14	-	sec
GPS accuracy(6) (10)						
	Fix position	-130 dBm, no multi-path, PDOP <1.5	-	4	-	m
GPS out-of-band blocking performance(11)(12)						
GSM850	824 – 849 MHz	EDGE	-	-18	-	dBm
E-GSM900	880 – 915 MHz	EDGE	-	-19	-	dBm
WCDMA III	1710 – 1785 MHz	WCDMA	-	-30	-	dBm
WCDMA II	1850 – 1910 MHz	WCDMA	-	-30	-	dBm

Table 30. GPS performances(1)(2)(3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
WLAN 2.4GHz	2412 – 2472 MHz	WLAN	-	-31	-	dBm
WLAN 5GHz	5150 – 5825 MHz	WLAN	-	-5	-	dBm

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated)
2. Minimum and maximum values are worst cases over corner lots, temperature and supply voltages.
3. At the IC pin, no external LNA used
4. Cold start definition, no almanac, no ephemeris, FU = ±2 ppm; TU = inf; PU = inf
5. Hot start definition, almanac retained, ephemeris retained, FU = ±0.18 ppm; TU = ±2 µs; PU = ±3 km
6. Measured with the ST-Ericsson GPS positioning software running on the host
7. 50 percentile numbers
8. User acceleration < 0.5 g; coverage = 50%; type = 2D; accuracy < 50 m; maximum test time = 300 s
9. Hot start definition: Alamanac retained; ephemeris retained; TU = ±2 s; PU = ±3 km; T = 25 °C; freq = 0.05 ppm; user acceleration < 0.5 g; coverage = 50%; type = 2D; accuracy < 50 m
10. RMS numbers
11. GPS engine sensitivity not degraded by more than 3 dB, measured at RF input using modulated interface source (No SAW)
12. These measurements do not use the additional feature of TX blanking which is used to avoid desensitization of the GPS receiver by excessive 2G transmitter noise

Table 31. GPS power consumption(1)(2)

Symbol	Parameter	Condition	Typ.	Unit
	Deep Coma	Host Interface off, 1.8 V (FE LDO not used), VDDIOx = on, LPO_CLK =o n, SYS_CLK = off	76	µA
	Sleep	Host interface in power save, DSP only, RF off, LNA off, accurate GPS time can be maintained	3.4	mA
	Tracking	Weak signal, 8 satellites @ -148 dBm, 1 second update, no power saving.	38.1	mA
	Acquisition	Full acquisition, average current when all SVs at -143 dBm - hot start	60	mA
		Cold start : average current	48	mA
	Tracking	Position report rate = 1 every 10 seconds. 6 SVs at -140 dBm, the rest weaker.	7.6	mA

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V, power supply architecture 1 (*Figure 5*), TCXO current not included, (unless otherwise stated)
2. Other systems (BT and FM) in their lowest power mode.

3 BT and BT low energy subsystem

3.1 BT/BLE functional description

3.1.1 Receiver

The Bluetooth subsystem implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from the RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a DCO signal running at twice the LO frequency. The I and Q mixer output signals are sampled by a state of the art SD A/D converter. The decimation and subsequent channel filtering is performed in the digital section.

The digital section demodulates the GFSK, pi/4-DQPSK or 8-DPSK coded bit stream by evaluating the phase information. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally.

3.1.2 Transmitter

The transmitter uses the serial transmit data from the Bluetooth controller. The transmitter's modulator converts this data into GFSK, pi/4-DQPSK or 8-DPSK modulated digital signals in polar format for respectively 1, 2 and 3 Mbps transmission data rate.

The vector magnitude is used to modulate the output power level.

The vector phase is used for modulating the synthesizer's instantaneous phase. The magnitude and phase components are recombined in the power amplifier.

3.1.3 RF DPLL

The on-chip DCO is part of a DPLL. The tank resonator circuitry for the DCO is completely integrated without the need of external components. Variations in the DCO center frequency are calibrated out automatically.

3.1.4 Bluetooth BR/EDR controller

V1.2 and V2.0 + EDR features

The Bluetooth controller is backward compatible with the Bluetooth specification V1.2 *[5.]* and V2.0 + EDR *[4.]*. Following is a list with the main features of those specifications:

- Adaptive Frequency Hopping (AFH)
- Fast connection: Interlaced scan for page and inquiry scan, answer FHS at first reception, RSSI used to limit range
- Extended SCO (eSCO) links: supports EV3, EV4, EV5, 2EV5 packets
- Channel Quality Driven Data Rate change (CQDDR)
- QoS flush
- Synchronization: BT clocks are available at HCI level for synchronization of parallel applications on different slaves
- LMP SCO handling
- Scatternet support
- 2 Mbps packet types
  - ACL: 2-DH1, 2-DH3, 2-DH5
  - eSCO: 2-EV3, 2-EV5
- 3 Mbps packet types
  - ACL: 3-DH1, 3-DH3, 3-DH5
  - eSCO: 3-EV3, 3-EV5

Bluetooth controller V2.1 + EDR features *[3.]*

- Encryption Pause/Resume (EPR)
- Extended Inquiry Response (EIR)
- Support Link Supervision Time Out changed event (LSTO)
- Secure Simple Pairing (SSP)
- Sniff Sub Rating (SSR)
- Quality of Service (QoS)
  - Support flushable and non-flushable packets in the Packet Boundary Flag (PBF)

Bluetooth controller V3.0 features *[2.]*

- Enhanced power control
- Read encryption key size

TX output power control

The Bluetooth subsystem supports output power control. With the standard TX power control algorithm enabled, the Bluetooth subsystem adapts its output power when a remote BT device supports the RSSI feature; this allows the remote device to measure the link strength and to request the Bluetooth subsystem to decrease/increase its output power. In case the remote device does not support the RSSI feature, the Bluetooth subsystem uses its 'default' output power level.

The maximum output power and power steps can be set via the static settings. The CX2001 supports operation at class 1 output power levels up to 13 dBm, class 2 at 4 dBm and class

3 at 0 dBm. Also a separate, very low, output power for inquiry can be set, to detect only close-by devices.

3.1.5 BLE controller

- Compatible with Bluetooth system specification V4.0 *[1.]* (including Bluetooth low energy)
- Support for all Link Layer state machine state combinations allowed by the BLE specification, see *Table 32*.

Table 32. Supported Link Layer state machine state combinations

Multiple state machine state and roles		Advertising	Scanning	Initiating	Connection	
					Master role	Slave role
Advertising		Prohibited	Supported	Supported(1)	Supported(1)	Supported(1)
Scanning		Supported	Prohibited	Supported	Supported	Supported
Initiating		Supported(1)	Supported	Prohibited	Supported	Prohibited
Connection	Master role	Supported(1)	Supported	Supported	Supported	Prohibited
	Slave role	Supported(1)	Supported	Prohibited	Prohibited	Prohibited

1. Only advertising packets that will not result in the link layer entering connection state in the slave role allowed

- Support for all four BLE GAP profile roles: observer, broadcaster, peripheral and central
- Support for optional link layer encryption
- Support for direct test mode using HCI interface
- Host to controller data flow control:
  - Support for packet based flow control using separate buffers for BLE
  - Size of BLE TX packet buffers: 27 octets
  - Number of BLE TX packet buffers: two buffers per simultaneously allowed BLE connection.
- Controller to host data flow control
  - Support for optional controller to host flow control
  - Size of BLE RX packet buffers: 27 octets
  - Number of BLE RX packet buffers: two buffers per simultaneously allowed BLE connection.
- Maximum throughput: full theoretical maximum data throughput for max-sized (27 octets) BLE packets, i.e. up to 319 kbps unidirectional and 242 kbps bidirectional.
- Maximum simultaneous BLE master connections: 16
- Maximum simultaneous BLE slave connections: one
- BR/EDR + BLE dual-mode support: All single-mode configurations supported for BR/EDR single-mode and LE single-mode can be combined within the obvious

limitation of bandwidth and timing restrictions. (Note that BR/EDR and BLE use the same radio in TDMA mode).

- Proprietary extensions
  - (Optional) fast connection event termination in case of flow control asserted by peer device to reduce unnecessary power consumption
  - (Optional) use of MD bit to request immediate acknowledgement to reduce average latency
  - Detailed diagnostics for BLE connections: number of empty packets, correlation failures, CRC errors, and so on
  - Configurable TX power for the different BLE modes (scan, advertise, master connection, slave connection, test)

3.1.6 Main processor and memory

- ARM-Cortex M3
- On-chip RAM, including provision for patches
- On-chip ROM pre-loaded with
  - BT stack up to HCI
  - A2DP media packet encapsulation
- Patch RAM
  - The Bluetooth subsystem includes a hardware block that allows patching of the ROM code.
  - Additionally, a software patch mechanism allows replacing complete software functions without changing the ROM image.
  - One part of the RAM memory is used for hardware and software patches.

3.1.7 Coprocessor

- Audio processor
- RAM, including provision for patches
- ROM, pre-loaded with
  - SBC encoding/decoding
- Patch RAM
  - A software patch mechanism allows replacing complete software functions without changing the ROM image,
  - One part of the RAM memory is used for software patches.

3.1.8 Download of the SW parameter file

To change the device configuration, a set of customizable parameters have been defined and put together in one file, the SW parameter file. This SW parameter file is downloaded at start-up into the Bluetooth subsystem.

Examples of parameters are: radio configuration, PCM settings and so on.

The same HCI command is used to download the file containing the patches (both those for the software and hardware mechanism).

For a more detailed description of the SW parameter file, refer to *[11.]*.

3.1.9 Pitch Period Error Concealment (PPEC)

PPEC stands for Pitch Period Error Concealment. PPEC is an algorithm and associated hardware used in the CX2001 chip to improve the quality of voice transfer over the Bluetooth air channel. It increases the speech quality in the vicinity of interference, and improves the coexistence with WLAN. The algorithm works at the receiver side and has no implications at all on the implementation of the Bluetooth specification.

PPEC works as follows: whenever a received packet is completely lost, instead of muting the output, some previously received CVSD samples are inserted. These inserted samples are retrieved from a buffer. The PPEC algorithm continuously analyzes the samples that were previously received, and it uses fundamental speech properties to determine which samples from the buffer need to be inserted. As samples are just replaced, the PPEC algorithm does not add any latency to the voice transfer.

3.1.10 Bluetooth - WLAN coexistence in collocated scenario

See *Section 1.8.8*.

3.1.11 HCI transport layer

See *Section 1.9*.

3.1.12 BT voice/audio interface

The Bluetooth subsystem of the CX2001 supports one audio interface that can be used for (e)SCO narrowband speech, for wideband speech, or for A2DP. This interface can be either the PCM/I2S1 or I2S2 as defined in *Section 1.8.5* and *Section 1.8.6*.

The interface is fully configurable by the host via the SW parameter file download and when a SCO connection, wideband speech connection or A2DP connection is started-up (to allow different configuration based on use case).

For Bluetooth voice operation (PCM/I2S1/I2S2 and (e)SCO), the interface always works at 8 kHz. However, it is possible to configure the interface to other frame rates, such as, 16 or 32 kHz, and link it to an eSCO link operating at the same rate. In I2S mode, it is possible to exchange voice on the left or on the right channel only.

For wideband speech, raw audio samples (16 bit at 16 kHz) are transferred PCM/I2S1/I2S2 interface and all necessary processing, such as SBC codec and encapsulation in (e)SCO packets is handled internally in the CX2001.

For A2DP operation, either the PCM/I2S1 or the I2S2 can be used. The I2S sample rate is configurable, for example, 44.1 or 48 kHz. The audio is SBC encoded and A2DP encapsulated in the CX2001, before being transmitted over the BT link.

3.2 BT performances

Table 33. BT transmitter characteristics(1)(2)(3)(4)(5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FSK (1Mbps) transmitter performance						
P_{outmax}	Maximum output power		11	13	15	dBm

Table 33. BT transmitter characteristics(1)(2)(3)(4)(5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_{outmin}	Minimum output power		-	-20	-	dBm
$P_{outmininq}$	Minimum output power in inquiry mode		-	-30	-	dBm
P_{outacc}	Output power accuracy		-2	-	2	dB
F_{range}	Frequency range		2400		2483.5	MHz
$\Delta f1_{avg}$	Modulation characteristics F0 pattern		140	–	175	kHz
$\Delta f2_{max}$	Modulation characteristics 10 pattern		99.9	100	–	%
$\Delta f2_{avg}$ / $\Delta f1_{avg}$	Modulation characteristics ratio		0.85	–	–	-
$F_{C\text{-}Initialfsk}$	Initial carrier frequency tolerance		-75	–	75	kHz
$F_{drift1slot}$	Carrier frequency drift 1 slot packet		-25	–	25	kHz
$F_{drift3slot}$	Carrier frequency drift 3 slots packet		-40	–	40	kHz
$F_{drift5slot}$	Carrier frequency drift 5 slots packet		-40	–	40	kHz
$F_{driftrate}$	Carrier frequency drift rate		-20	–	20	kHz/50µs
BW_{20dB}	20 dB bandwidth		–	–	1.0	MHz
$P_{InB\pm2Mhz}$	Adjacent channel power at ±2 MHz (|M-N| = 2)	Meas. bw = 100 kHz	–	–	-20	dBm
$P_{InB\geq\pm3MHz}$	Adjacent channel power at ≥±3 MHz (|M-N| ≥ 3)	Meas. bw = 100 kHz	–	-	-40	dBm
PSK (2 and 3 Mbps) transmitter performance						
$P_{out2max}$	Maximum output power (2 Mbps)		8	10	12	dBm
$P_{out3max}$	Maximum output power (3 Mbps)		8	10	12	dBm
P_{outrel}	EDR relative transmit power		-1	0	1	dB
P_{outmin}	Minimum output power		-	-20	-	dBm
$F_{C\text{-}\omega i}$	Initial carrier frequency stability over header		-75	–	75	kHz
$F_{C\text{-}\omega i+\omega o}$	EDR maximum excursion from F_C		-75	–	75	kHz
$F_{drift\text{-}\omega o}$	Maximum drift over EDR synchronization sequence and payload		-10	–	10	kHz

Table 33. BT transmitter characteristics(1)(2)(3)(4)(5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$DEVM_{rms2}$	RMS differential error vector magnitude (2 Mbps)		–	5	20	%
$DEVM_{rms3}$	RMS differential error vector magnitude (3 Mbps)		–	5	13	%
$DEVM_{99\%2}$	99% differential error vector magnitude (2 Mbps)		–	12	30	%
$DEVM_{99\%3}$	99% differential error vector magnitude (3 Mbps)		–	14	20	%
$DEVM_{peak2}$	Peak differential error vector magnitude (2 Mbps)		–	12	35	%
$DEVM_{peak3}$	Peak differential error vector magnitude (3 Mbps)		–	14	25	%
$Encode_{error}$	EDR differential phase error		99	–	–	%
$P_{InB\pm1MHz}$	Adjacent channel power at ±1 MHz	Meas. bw = 100 kHz	–	-33	-26	dBc
$P_{InB\pm2MHz}$	Adjacent channel power at ±2 MHz (|M-N| = 2)	Meas. bw = 100 kHz	–	-30	-20	dBm
$P_{InB\geq\pm3MHz}$	Adjacent channel power at ≥±3 MHz (|M-N| ≥ 3)	Meas. bw = 100 kHz	–	-41	-38(6)	dBm
FSK (1 Mbps) and PSK (2 & 3 Mbps) Out-of-Band Emission						
GSM850	869 – 894 MHz			-145	-	dBm/Hz
E-GSM900	925 – 960 MHz			-145	-	dBm/Hz
WCDMA III	1805 – 1880 MHz			-142	-	dBm/Hz
WCDMA II	1930 – 1990 MHz			-141	-	dBm/Hz
WLAN 5GHz	5150 – 5825 MHz			-142	-	dBm/Hz

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated)
2. Minimum and maximum values are worst cases over corner lots, temperature, and supply voltages.
3. According to Bluetooth specification
4. At the IC pins
5. At 10 dBm output power at the IC pins
6. Assuming a 2 dB insertion loss of a typical filter, this become -40 dBm at the antenna interface.

Table 34. BT - receiver characteristics(1)(2)(3)(4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Antenna input						
$\|S_{11}\|^2$	Input return loss	RX enabled		-16	-10	dB
P_{LOleak}	Local oscillator leakage level	Band: 30 MHz – 1 GHz	-	-75	-65	dBm
FSK (1Mbps) receiver performance						
$Sens_f$	Receiver sensitivity (Clean transmitter)	At the IC pin, BER≤0.1%	–	-92	-89	dBm
$Sens_d$	Receiver sensitivity (Dirty transmitter(5))	At the IC pin, BER≤0.1%	–	-91	-88	dBm
$C/I_{co\text{-}channel}$	Co-channel interference		–	–	11	dB
C/I_{1MHz}	Adjacent (±1 MHz) interference		–	–	0	dB
C/I_{2MHz}	Adjacent (±2 MHz) interference		–	–	-30	dB
$C/I_{\geq 3MHz}$	Adjacent (≥±3 MHz) interference		–	–	-40	dB
C/I_{image}	Image (-2 MHz) frequency interference		–	–	-9	dB
$C/I_{image\pm 1 MHz}$	Adjacent (-3 MHz) interference to inband image frequency		–	–	-20	dB
IMD	Intermodulation performance	BER ≤ 0.1% including BPF, n=5 at antenna	-	-39	–	dBm
P_{inmaxf}	Maximum usable receive input level	At the IC, BER ≤0.1% and PER ≤1%, 0 kHz offset	-10	0	–	dBm
$RSSI_{accabs}$	RSSI absolute accuracy	monotonic, from -88 to -32 dBm	-6	–	6	dB
PSK (2 and 3 Mbps) receiver performance						
$Sens_{p2}$	EDR sensitivity 2 Mbps (Clean transmitter)	At the IC, BER ≤ 0.01%	–	-92	-88	dBm
$Sens_{p3}$	EDR sensitivity 3 Mbps (Clean transmitter)	At the IC, BER ≤ 0.01%	–	-86	-82	dBm
$Sens_{d2}$	EDR sensitivity 2 Mbps (Dirty transmitter(6))	At the IC, BER < 0.01%	–	-91	-87	dBm
$Sens_{d3}$	EDR sensitivity 3 Mbps (Dirty transmitter(6))	At the IC, BER < 0.01%	–	-85	-81	dBm
$C/I_{co\text{-}chan\_p2}$	Co-channel interference 2 Mbps		-	-	13	dB

Table 34. BT - receiver characteristics(1)(2)(3)(4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$C/I_{co\text{-}chan\_p3}$	Co-channel interference 3 Mbps		-	-	21	dB
C/I_{1MHz_p2}	Adjacent (±1 MHz) interference 2 Mbps		-	-	0	dB
C/I_{1MHz_p3}	Adjacent (±1 MHz) interference 3 Mbps		-	-	5	dB
C/I_{2MHz_p2}	Adjacent (±2 MHz) interference 2 Mbps		-	-	-30	dB
C/I_{2MHz_p3}	Adjacent (±2 MHz) interference 3 Mbps		-	-	-25	dB
$C/I_{\geq 3MHz\_p2}$	Adjacent (≥±3 MHz) interference 2 Mbps		-	-	-40	dB
$C/I_{\geq 3MHz\_p3}$	Adjacent (≥±3MHz) interference 3 Mbps		-	-	-33	dB
C/I_{image_p2}	Image (-2 MHz) frequency interference 2 Mbps		-	-	-7	dB
C/I_{image_p3}	Image (-2 MHz) frequency interference 3 Mbps		-	-	0	dB
$C/I_{image\pm1\_p2}$	Adjacent (-3 MHz) interference to inband image frequency 2 Mbps		-	-	-20	dB
$C/I_{image\pm1\_p3}$	Adjacent (-3 MHz) interference to inband image frequency 3 Mbps		-	-	-13	dB
P_{inmaxp}	Maximum usable receive input level (for 2 and 3 Mbps)	At the IC, BER≤0.01% and PER ≤1%, 0kHz offset	-10	0	-	dBm
PSK (1 Mbps and 2 Mbps) out-of-band blocking performance(6)(7)						
GSM850	824 – 849 MHz	EDGE(8)	-	9	-	dBm
E-GSM900	880 – 915 MHz	EDGE	-	9	-	dBm
WCDMA III	1710 – 1785 MHz	WCDMA	-	2	-	dBm
WCDMA II	1850 – 1910 MHz	WCDMA	-	3	-	dBm
WLAN 5GHz	5150 – 5825 MHz	WLAN	-	-2	-	dBm

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated)
2. Minimum and maximum values are worst cases over corner lots, temperature, and supply voltages.
3. According to Bluetooth specification
4. At the IC pins
5. Dirty transmitter including carrier frequency drift, as defined in the BT SIG spec.

6. With a -72 dBm wanted signal at the chip pins (BT RF port)
7. BER ≤ 0.1% at 1 Mbps or BER ≤ 0.01% at 2 Mbps and 3 Mbps
8. Except third harmonic of cellular transmitter (For this case typical blocker level of -12 dBm is reached).

Table 35. BLE - TX and RX characteristics(1)(2)(3)(4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
BLE transmitter performance						
P_{outmax}	Maximum output power(5)		11	13	15	dBm
P_{outmin}	Minimum output power		-	-20	-	dBm
$P_{outminadv}$	Minimum output power in advertising mode		-	-30	-	dBm
P_{outacc}	Output power accuracy		-2	-	2	dB
$\Delta f1_{avg}$	Modulation characteristics any pattern		225	–	275	kHz
$F_{C\text{-}Initial}$	Initial carrier frequency tolerance		-100	–	100	kHz
$F_{driftpacket}$	Carrier frequency drift packet		-50	–	50	kHz
$F_{driftrate}$	Carrier frequency drift rate		-20	–	20	kHz/50µs
$P_{InB\pm2Mhz}$	Adjacent channel power at ±2 MHz (|M-N| = 2)	Meas. bw = 100 kHz	–	–	-20	dBm
$P_{InB\geq\pm3MHz}$	Adjacent channel power at ≥±3 MHz (|M-N| ≥ 3)	Meas. bw = 100 kHz	–	-	-30	dBm
BLE receiver performance						
$Sens_f$	Receiver sensitivity (Clean transmitter)	At the IC pin, PER ≤ 30.8%	–	-93	-91	dBm
$Sens_d$	Receiver sensitivity (Dirty transmitter(6))	At the IC pin, PER ≤ 30.8%	–	-92	-90	dBm
$C/I_{co\text{-}channel}$	Co-channel interference		–	–	21	dB
C/I_{1MHz}	Adjacent (±1 MHz) interference		–	–	15	dB
C/I_{2MHz}	Adjacent (±2 MHz) interference		–	–	-17	dB
$C/I_{\geq3MHz}$	Adjacent (≥±3 MHz) interference		–	–	-27	dB
C/I_{image}	Image (-2 MHz) frequency interference		–	–	-9	dB
$C/I_{image\pm1 MHz}$	Adjacent (-3 MHz) interference to inband image frequency		–	–	-15	dB

Table 35. BLE - TX and RX characteristics(1)(2)(3)(4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IMD	Intermodulation performance	BER ≤ 0.1% including BPF, n=5 at antenna	-50	-	–	dBm
P_{inmaxf}	Maximum usable receive input level	At the IC, PER ≤30.8% including BPF, n=5 at antenna	-10	0	–	dBm

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated)
2. Minimum and maximum values are worst cases over corner lots, temperature, and supply voltages.
3. According to Bluetooth specification
4. At the IC pins
5. Depending on the external filter loss, this needs to be programmed to get 10 dBm at antenna pins according to BT-SIG specification.
6. Dirty transmitter including carrier frequency drift, as defined in the BT SIG spec.

Table 36. BT and BLE power consumption(1)(2) (3)

Symbol	Parameter	Condition	Typ.	Unit
BT system mode				
IBTScan	Page and inquiry scan	Page period = 1.28 s Inquiry period = 2.56 s(4)	490	µA
	Sniff in Master mode	Master, Tsniff = 1.28 s, 4 attempts, 0 sniff timeout	140	µA
	Sniff in Slave mode	Slave, Tsniff = 1.28 s, 4 attempts, 0 sniff timeout	170	µA
	Sniff in Master mode	Master, Tsniff = 500 ms, 4 attempts, 0 sniff timeout	230	µA
	Sniff in Slave mode	Slave, Tsniff = 500 ms, 4 attempts, 0 sniff timeout	285	µA
BT voice link				
	HV3 + Sniff in Master mode	HV3, Sniff (Master, 500 ms, 4 attempts, 0 sniff timeout), P=1.28 s; I=2.56 s	12.4	mA
	HV3 + Sniff in Slave mode	HV3, Sniff (Slave, 500 ms, 4 attempts, 0 sniff timeout), P=1.28 s; I=2.56 s	12.5	mA
	2-EV3 + Sniff in Master mode	2-EV3, T_eSCO=12, W_eSCO=2; Sniff (Master, 500 ms, 4 attempts, 0 sniff timeout), P=1.28 s; I=2.56 s	9.2	mA
	2-EV3 + Sniff in Slave mode	2-EV3, T_eSCO=12, W_eSCO=2; Sniff (Slave, 500 ms, 4 attempts, 0 sniff timeout), P=1.28 s; I=2.56 s	9.5	mA

Table 36. BT and BLE power consumption(1)(2) (3) (continued)

Symbol	Parameter	Condition	Typ.	Unit
BT ACL link				
	DH1 TX - DH5 RX in Master mode	@ maximum throughput	29.3	mA
	DH1 TX - 3-DH5 RX in Master mode	@ maximum throughput	29.9	mA
	DH5 TX - Null RX in Master mode	@ maximum throughput	38.1	mA
	3-DH5 TX - Null RX in Master mode	@ maximum throughput	38.9	mA
BT A2DP link				
	A2DP from FM RX	TX 3-DH5 - RX null, 400 kbps, A2DP SBC high quality joint stereo hostoffload from FM RX 48 kHz (incl. FM RX active)	27.7	mA
	A2DP from I2S	TX 3-DH5 - RX null, 400 kbps, A2DP SBC high quality joint stereo hostoffload from I2S 500 kHz burst mode	15.6	mA
	A2DP from HCI	TX 3-DH5 - RX NULL, 400 kbps, A2DP SBC high quality joint stereo from HCI	14.6	mA
BLE				
	Advertising (non-connectable)	Interval: 1.28 s Data: 15 bytes 3 channels	175	µA
	Advertising (discoverable)	Interval: 1.28 s Data: 15 bytes 3 channels	195	µA
	Scanning	interval: 1.28 s Window: 11.25 ms Single frequency per window	380	µA
	Link layer connection	Master Interval: 500 ms Slave Latency : 0 Empty TX/RX packets	250	µA
	Link layer connection	Master Interval: 1 s Slave Latency : 0 Empty TX packets RX payload: 27 bytes	155	µA

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V, power supply architecture 1 (*Figure 5*), VBAT current not included
2. For BT BR/EDR with 4 dBm output power at the IC pins, for BLE with 10 dBm output power at the IC pins, unless otherwise stated
3. GPS and FM in low power mode, unless otherwise stated
4. The BT Low Power modes include also leakage from the GPS and FM systems.

4 FM TX/RX subsystem

4.1 Introduction

The FM subsystem of CX2001 can operate in receive (RX) and transmit (TX) modes. The host controls which mode is selected. The TX and RX subsystems cannot be active simultaneously (full-duplex operation).

The FM receiver contains the FM demodulator, the stereo decoder, and the R(B)DS demodulator and decoder. It is optimized to be used either with a wire antenna (for example, a headset wire) or with a small loop antenna, which can be embedded in the enclosure of the mobile or personal device in which the CX2001 is integrated. The audio output signals can be delivered in analog or digital formats. A direct, on-chip, loop-through to the Bluetooth subsystem is available. Multiple audio output paths can be active at the same time.

The FM transmitter contains an R(B)DS encoder and modulator, a stereo encoder, and an RF modulator. The audio input signals are delivered in digital format. A dual-RF feature enables the transmission of the same information on two separate frequencies, to make the link more robust. The use of the RDS AF feature enables a suitably advanced receiver (for instance, a car radio receiver) to track the better of the two channels. The output amplifier can deliver a voltage of up to 120 dBµV across the terminals of the small loop antenna, which is shared with the FM receiver.

Special care has been taken to ensure optimum cohabitation and coexistence performance with the other radios and systems in CX2001, as well as with the radios of cellular pipes which may be present in a phone containing CX2001.

The FM part of CX2001 complies with the following standards and regulations:

- ITU-R BS 450-3 - Transmission standards for FM sound broadcasting at VHF, 2001
- BS EN 62106 - Specification of the radio data system (RDS) for VHF/FM sound broadcasting in the frequency range from 87.5 MHz to 108 MHz, 2001 (with updates to the 2008 proposed version where applicable)
- EN 55020 - Sound and television broadcast receivers and associated equipment - immunity characteristics - limits and methods of measurement, May 2002
- Relevant clauses (intentional and unintentional transmitters) from FCC part 15
- ETSI 301 357

Firmware update mechanism

A patch mechanism is implemented in the FM subsystem and used to update the firmware. The patch is downloaded to RAM. In the application, the download can be done through dedicated HCI commands sent by the host. More details are provided in *[11.]*.

4.2 FM receiver

4.2.1 RF and audio signal processing

The FM subsystem of CX2001 has two RF inputs, both of which are single-ended. One of these is optimized to be connected to a small loop antenna, which could be internal to the application (for example, a cell phone). This small loop antenna is shared with the FM transmit subsystem. Internally there is a tunable capacitance, to resonate the loop antenna for optimum sensitivity and output level. The tunable capacitance has been designed to guarantee operation over the frequency band from 76 MHz up to 108 MHz for a loop antenna with an inductance of 120 nH +/-10%. An integrated, fully transparent, alignment algorithm ensures that the resonant circuit is optimally tuned.

The other input is single-ended as well and is optimized for a wire antenna with a length of approximately ¼ wavelength (for example, a headset wire), which will normally be external to the application. It has a rather low input impedance of around 16 Ω in series with 14 pF. This enables direct connection to the headphone wire and has low sensitivity for noise that is generated inside the application. For optimum co-existence performance, a series inductor is recommended. This is not needed for those applications where full co-existence with cellular PAs in the same application is not required. When operating from the wire antenna, the FM radio can be tuned from 70 MHz to 108 MHz to cover the European, US, Chinese, and Japanese FM bands, without requiring change in application.

Automatic Gain Control (AGC), both before and after LNAs, maintains LNAs and subsequent analog signal processing circuits within their linear operating range.

A Received Signal Strength Indicator (RSSI) is provided, which can be read by the host. The CX2001 uses an enhanced reception quality indication algorithm for channel detection during search and band scan. Advantage of this algorithm over conventional RSSI-threshold level algorithms is that the number of missed channels, as well as the number of false stops is decreased considerably. This algorithm makes use of three decision criteria for accepting a channel during the search tuning and band-scan operation. The parameters of all these criteria (RSSI, audio SNR, channel frequency offset) are fully adjustable.

The received RF frequency is down-converted to a low Intermediate Frequency (IF) by a quadrature or complex mixer. Quadrature analog signal processing gives (in-band) image suppression without the need for additional filtering. Two first-order analog low-pass filters after the mixer are used for wide band selectivity and as anti-aliasing filters before the Analog to Digital Converters (ADC).

To improve co-existence with other radio systems (Cellular, GPS, and Bluetooth) that are present in the CX2001, the tuning algorithm automatically selects an oscillator frequency that is non-overlapping with other radio system frequencies or their harmonics. Additionally, it selects the optimum LO frequency (low-side or high-side injection) based on the detection of in-band and out-of-band interferers.

ADCs convert signals to the digital domain. They are clocked by a frequency which is an integer subharmonic of the LO frequency. This guarantees that spurs due to the clock frequency and its harmonics always fall well outside the FM channel.

Digital filters remove adjacent channels from the complex low-IF signal. The bandwidth of the digital filters depends on the reception conditions, to optimize the trade-off between adjacent channel suppression and sound quality. In this stage, the low-IF signal is also mixed down to baseband.

The ‘clean’, complex baseband signal is then demodulated by the digital signal processor. The output of the demodulator is a digital representation of the classical MPX signal comprising of the mono signal and if applicable the stereo signal, pilot tone, and R(B)DS signal.

The sound processing applied to the MPX signal incorporates the following functions:

- Soft mute, reducing the noise and audio level under low RF signal conditions.
- Stereo decoding, with the following features:
  - Sliding stereo, giving a smooth transition between mono and stereo.
  - Stereo indication to the host. The transition point is defined at 10 dB channel separation.
  - Extended stereo, controlling the stereo noise by reducing the stereo bandwidth.
- High cut control, reducing audio noise under low SNR conditions
- Volume and balance control
- De-emphasis
- Audio mute

Parameters of the sound processing features are programmable through the control interface.

After sound processing, the audio signals can be output either in a digital or in an analog format. For digital interfacing, two sample rate converters are provided so that independent interfacing to the host processor (external to the CX2001) and direct loop through to the Bluetooth subsystem (internal to the CX2001) are possible. For interfacing to the host, I2S and PCM formats are supported. The direct loop through uses an on-chip parallel interface. In all cases, the digital audio interfacing is controlled centrally in the CX2001.

To obtain analog audio output signals, the digital audio signals are filtered and converted to analog with a stereo DAC. The stereo DAC can directly drive external audio amplifiers using two coupling capacitors. In case of mono reception, both audio outputs get the same signal. Additionally, if required for mono receivers, one DAC can be switched off to save current.

4.2.2 R(B)DS demodulation and decoding

The CX2001 is capable of demodulating and decoding RDS and RBDS signals. This includes error detection and correction. R(B)DS demodulation/decoding is compatible with mono and stereo FM transmitters (pilotless RDS is supported).

The RDS decoder has provisions to avoid false sync messages to the host in case there is no R(B)DS signal present. The R(B)DS decoder will signal its status to the host by generating interrupts and setting status flags. Upon command from the host, the R(B)DS decoder starts counting the number of sync losses and the number of received, correct, correctable, uncorrectable, and rejected blocks.

To reduce the interrupt load on the host software, the CX2001 has an extended RDS data buffer of up to 22 RDS groups of four blocks each. This corresponds to 2 s of RDS data. The data buffer size can be configured to match the host software. Each RDS data buffer block contains the 16-bit RDS block data and 5 bits per block of status information.

Some more advanced RDS-based functionality is available:

- PI-code masking, detecting changes in the received PI-code
- RDS E-block rejection, filtering out E-blocks, as defined in the RBDS standard for a proprietary paging system (MMBS)
- RDS preset tuning with PI-code, tuning only when the received PI-code on the preset channel matches with the host defined PI-code.
- RDS group rejection, filtering out RDS groups with uncorrectable errors in A- and B-blocks.
- RDS block request, notifies when certain RDS block types have been received.
- To ease the support of alternative frequency functionality in the host, extended AF algorithms are present.
- QoS indication, checks the signal strength of the current received signal.
- RSSI interrupt, generates interrupt when signal strength on current frequency is below threshold.
- AF update, inaudible check of the signal strength of alternative frequencies.
- RDS AF switch, automatic inaudible switch to an alternative frequency including checking of RSSI and PI-code.

RDS data is transferred as ‘raw’ data to the host using the control interface, that is, the RDS blocks are transferred as they are received (with possibly error correction applied). Apart from PI code decoding, which is required for local tuning algorithms, no attempt is made to decode RDS blocks into the respective data fields. The parameters of the RDS functions are fully configurable by the host.

4.3 FM transmitter

4.3.1 Audio and RF signal processing

Audio data can be provided using a digital interface (PCM/I2S1 or I2S2).

In the digital signal processing part, the left and right channels are combined to form the M and S components of the MPX stereo multiplex signal, to which a 19 kHz pilot tone and a 57 kHz RDS-modulated subcarrier are added. This MPX signal is modulated onto a complex, digital low-IF carrier. If required, simultaneous modulation of the same information onto two complex low-IF frequencies is possible. The two complex IF frequencies can be up to 800 kHz apart.

Two digital-to-analog converters followed by third-order Butterworth low-pass filter convert the complex digital IF signal(s) into a complex analog signal, which is subsequently up-converted by a complex LO signal and combined to form a single, real RF signal.

This RF signal is fed into the PA. The PA has been optimized to drive a small (embedded) loop antenna, which is the same one as the (embedded) loop antenna in receive mode. The loop antenna must be connected to an RF ground plane on one side.

To minimize current consumption in the PA, the loop antenna is part of a resonant circuit where the capacitor is integrated into the CX2001 and tunable. Tuning the resonant circuit, including making corrections for variable antenna parameters because of, for example hand effect, is done by an integrated, fully transparent, software algorithm.

The PA can deliver up to 120 dBµV, to drive very small antennas and still fully exploit the regulatory freedom (FCC, ETSI). The tunable capacitance has been designed to guarantee operation over the band from 76 MHz up to 108 MHz for a loop antenna with an inductance of 120 nH +/- 10%. The output amplifier is designed for very low spurious outputs, so that co-existence with receivers in cellular, GPS, and ISM bands is guaranteed.

The output level of the PA can be controlled over 35 dB to ensure operation with antennas with different efficiency, without exceeding legislative limits. Level control must be done by the host. Relevant information is stored and pre-loaded in the form of factory settings.

The PA is supplied by its own LDO, which is connected directly to the battery. Under normal circumstances, this LDO delivers 2.5 V to accommodate the 120 dBµV (1.0 V_{RMS}) output swing. When the battery voltage decreases because of discharge, the PA output level is decreased to maximum 117 dBµV and the LDO is switched to a 1.8 V output.

4.3.2 RDS data

RDS data is transferred as RDS groups (four blocks of 16 bit data) from the host using the control interface. The CX2001 takes care of adding error correction data, of encoding, bitshaping, modulating onto the 57 kHz RDS subcarrier and adding to the MPX signal.

4.4 Tuning and control

4.4.1 Tuning system

The tuning system consists of a fully integrated Frequency Locked Loop (FLL). The FLL locks the internal oscillator frequency to the 32.768 kHz LPO clock reference frequency. In parallel to the FLL, a PLL is implemented, which uses the (normally) 26 MHz system clock as reference frequency. This PLL makes the FM part more robust against noise and interference that may be generated on-chip.

The tuning system can compensate for slowly time-dependent variations on the reference frequency of up to 170 ppm in RX mode, and up to 80 ppm in TX mode. To guarantee this, the LPO clock is frequently calibrated against the system clock, which typically has an inaccuracy of 20 ppm or better. In addition, a static offset of up to +/- 32 000 ppm can be compensated for. The value of this offset is communicated using the control interface.

From the internal oscillator frequency, the clocks for the DSP and for the A-to-D and D-to-A converters are derived. This guarantees that clock-related spurs always fall well outside the channel of interest.

There are three pre-programmed regional FM frequency bands:

- North America/EU (87.5 MHz – 108 MHz)
- Japan (76 MHz – 90 MHz)
- China (70 MHz – 108 MHz)

The default band is the North America/EU band. For any selected frequency band, the tuning grid is selectable between 50 kHz, 100 kHz, or 200 kHz. A set maker can also define a dedicated frequency band by defining the lower and upper band edges.

There are three types of tuning and a bandscan function pre-defined:

- Preset tuning, used to set the tuning frequency of the receiver to a certain channel as defined by the host;
- Search tuning, searches for the next available valid channel in increasing (search up) or decreasing (search down) frequency direction;
- Stepped tuning, tunes to a channel that is higher (step-up) or lower (step-down) by the tuning frequency grid;
- The band-scan function scans the selected FM band for the strongest available radio channels and stores the strongest channels, with a maximum of 32, in an internal buffer that can be read by the host.

During tuning, the audio outputs are muted, i.e., the audio amplitude is made equal to zero.

4.4.2 Host interfacing and control

The FM part in the CX2001 is controlled using a command interface. This command interface replaces direct register manipulation and so simplifies host software development. Commands for the FM part are encapsulated in HCI commands on the interface between the host and the CX2001.

Two types of commands exist, function control commands and data acquisition commands. The commands are written to a command buffer and the response is read from a response buffer. Both buffers can hold one full command or response.

The commands consist of a header and up to seven data words, all 16-bit wide. The actual number of data words is indicated in the header. A command has a unique and permanent identifier. The header holds the command identifier. The command set of the CX2001 is backwards compatible with the command sets of ST-Ericsson TEA599X/CF599X family.

The command interface can handle one command at a time. The CX2001 responds within 50 µs upon reception of a command. The host does not have to read the response, but the response header is cleared upon reception of a new command.

The response to a data acquisition command holds either the requested data or an indication that data was not available. Response to a function control command indicates whether the command has been received correctly or not.

The CX2001 detects invalid command identifiers; it gives an error response and ignores the (invalid) command. Other types of errors (number of data words not correct, out-of-range parameters or not applicable command for current mode of operation) are not recognized and can lead to unexpected behavior.

A ‘command complete event’ is returned upon completion of each command. Additional events can be triggered by FM IP interrupts, either in response to command or due to an asynchronous event.

4.5 FM performances

Table 37. FM transmitter characteristics (1)(2)(3)(4)(5)(6)(7)(8)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RF performances						
P_{Txout}	Maximum output voltage (single transmit)	$V_{DD\_FM\_PA}$ = 2.5 V	–	120(9)	–	dBµV
		$V_{DD\_FM\_PA}$ = 1.8 V	–	117	–	dBµV
	Maximum output voltage (dual transmit)	$V_{DD\_FM\_PA}$ = 2.5 V	–	114	–	dBµV
		$V_{DD\_FM\_PA}$ = 1.8 V	–	111	–	dBµV
$P_{Txoutrange}$	Output level control range		88	-	123	dBµV
$P_{Txoutstepsize}$	Output level step size		-	1	-	dB
$P_{Txoutacc}$	Output level accuracy		-2	-	+2	dB
F_{range}	Frequency range		76	-	108	MHz
F_{TxAcc}	Frequency accuracy		–	-	10	kHz
DF_{dual}	Maximum difference between 2 channels of FM dual TX		–	0.8	–	MHz
BW	Output occupied bandwith	Δf <= 75kHz, 99% of power, f_{mod} = 1 kHz	–	–	165	kHz
	Input impedance resistive part		–	1.6	–	kΩ
	Input impedance capacitive part	Programmable	5.5	–	51	pF
$Tx_{spectrum}$	Transmitted spectrum	0 kHz from carrier	–	–	0	dBc
		+/-50 kHz from carrier	–	–	0	dBc
		+/-75 kHz from carrier	–	–	0	dBc
		+/-120 kHz from carrier	–	–	-12.2	dBc
MPX performances						
VAF	Audio input level	Stereo, Δf_{audio} = 67.5 kHz, f_{audio} = 400 Hz	-	-6	-	dBFS
A_{DEV}	Audio frequency deviation programmable range	Programmable, stereo, 50% of full scale digital input	66.5	67.5	68.5	kHz
A_{DEVacc}	Audio frequency deviation accuracy		-0.2	–	+0.2	dB
P_{DEV}	Pilot tone frequency deviation	Programmable	0	6.75	10	kHz
RDS_{DEV}	RDS signal frequency deviation programmable range	Programmable	0	2.0	10	kHz

Table 37. FM transmitter characteristics (1)(2)(3)(4)(5)(6)(7)(8) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$total_{DEV}$	Total deviation	default audio, pilot, RDS, 50% of full scale digital input	–	–	75	kHz
$T_{preem50us}$	Pre-emphasis time constant 50 µs		45	50	55	µs
$T_{preem75us}$	Pre-emphasis time constant 75 µs		70	75	80	µs
Audio performances						
SNR_{audio}	Audio SNR (after perfect demodulation, A-weighting filter)	Mono (5) (7)	-	62	-	dB
		Stereo (5) (8)	-	58	-	dB
THD_{audio}	Audio THD (after perfect demodulation, A-weighting filter)	Mono (7), f_{audio} = 75 kHz	-	0.05	0.1	%
		Stereo (8), f_{audio} = 67.5 kHz	-	0.06	0.1	%
CH_{audio}	Audio stereo channel separation (after perfect demodulation, A-weighting filter)	Stereo (8) L only or R only	40	45	-	dB
BAL_{audio}	Audio stereo channel balance (after perfect demodulation, A-weighting filter)	Stereo (8)	-0.1	-	+0.1	dB
$Tx_{spurious}$	Audio spurious content (after perfect demodulation, IEC and A-weighting filter)	Stereo (8)	-	-	-60	dBc
$ripple_{audio}$	In band audio ripple (after perfect demodulation, de-emphasis)(10)		-0.5	-	+0.5	dB
FM_{CU_Low}	FM audio lower cut off frequency		-	-	20	Hz
FM_{CU_Up}	FM audio upper cut off frequency		15	-	-	kHz
FM TX Out-of-Band Emission (9)(11)						
GSM850	869 – 894 MHz	BW = 200 kHz	-	12	-	dBµV
E-GSM900	925 – 960 MHz	BW = 200 kHz	-	12	-	dBµV
WCDMA III	1805 – 1880 MHz	BW = 3.84 MHz	-	15	-	dBµV
WCDMA II	1930 – 1990 MHz	BW = 3.84 MHz	-	15	-	dBµV
WLAN 2.4GHz	2412 – 2471 MHz	BW = 20 MHz	-	15	-	dBµV

Table 37. FM transmitter characteristics (1)(2)(3)(4)(5)(6)(7)(8) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
WLAN 5GHz	5150 – 5825 MHz	BW = 20 MHz	-	15	-	dBµV
GPS	1570 - 1580 MHz	BW = 2 MHz		6		dBµV

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated)
2. Minimum and maximum values are worst cases over corner lots, temperature, and supply voltages.
3. At IC pins.
4. With a load at the IC FM TX RF pins of 120 nH +/- 10%, Q >= 30, with external notch filter.
5. In PLL mode (i.e. with SYS_CLK), 26 MHz.
6. Over 76 - 108 MHz, 120 dBµV.
7. Mono, Δf_{audio} = 22.5 kHz, f_{mod} = 1 kHz, pre-emphasis = 50 µs, unless otherwise stated.
8. Stereo, Δf_{audio} = 22.5 kHz, Δf_{pilot} = 6.75 kHz, f_{mod} = 1 kHz, L=R, pre-emphasis = 50 µs, unless otherwise stated.
9. 123 dBµV can be met if requirement on spurious emission is relaxed.
10. Audio range from 100 Hz to 14 kHz.
11. Across transmitting antenna, assuming a tuned FM loop antenna (120 nH, Q >= 30) see *Note 4*.

Table 38. FM receiver characteristics(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RF input, wired antenna (FM_WANT)(9)						
FM range	FM frequency range		70	-	108	MHz
FM grid	FM tuning grid		50	100	200	kHz
$V_{WANTsensf}$	Sensitivity when using wired antenna input	26 dB audio SNR	-	1.1	3.5	μV_{EMF}
$V_{FMWANTintsnr}$	Intermediate SNR when using wired antenna input	at 10 μV_{EMF}	-	48	-	dB
$V_{RDSsens}$	RDS sensitivity	95% BQR, error correction on, Δf_{RDS} = 2 kHz, stereo (6)	-	7.0	-	μV_{EMF}
$IP3_{in}$	In band 3rd-order intercept point	Δf_1= 200 kHz, Δf_2= 400 kHz	97	100	-	$dB\mu V_{EMF}$
$IP3_{in}$	In band 3rd-order intercept point	Δf_1= 4 MHz, Δf_2= 8 MHz	97	100	-	$dB\mu V_{EMF}$
LO	LO breakthrough		-	-	-55	dBm
	Input impedance resistive part		-	16	-	Ω
	Input impedance capacitive part		-	14	-	pF
RF input, embedded antenna (FM_ANT)(10)						
FM range	FM frequency range		76	-	108	MHz
FM grid	FM tuning grid		50	100	200	kHz

Table 38. FM receiver characteristics(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{embsensf}$	Sensitivity when using embedded antenna input	26 audio dB SNR	-	0.2	-	μV_{EMF}
$V_{embintsnr}$	Intermediate SNR when using embedded antenna input	2.5 μV_{EMF}	-	50	-	dB
$V_{RDSsens}$	RDS sensitivity	95% BQR, error correction on, Δf_{RDS} = 2 kHz, stereo (6)	-	1.6	3.5	μV_{EMF}
$IP3_{in}$	In band 3rd-order intercept point	Δf_1= 200 kHz, Δf_2= 400 kHz	75	80	-	$dB\mu V_{EMF}$
$IP3_{in}$	In band 3rd-order intercept point	Δf_1= 4 MHz, Δf_2= 8 MHz	82	87	-	$dB\mu V_{EMF}$
LO	LO breakthrough		-	-	75	dBµV
	Input impedance resistive part		-	1.6	-	kΩ
	Input impedance capacitive part	Programmable	5.5	-	51	pF
RSSI						
$RSSI_{accabs}$	RSSI absolute accuracy		-6	-	6	dB
Signal rejections						
A_{ch}	Adjacent channel selectivity	Mono(5), Δf = 200 kHz, EN55020	45	50	-	dB
		Stereo(6), Δf = 200 kHz, EN55020	45	50	-	dB
		Mono(5), Δf = 300 kHz, EN55020	40	45	-	dB
		Stereo(6), Δf = 300 kHz, EN55020	35	42	-	dB
IA_{ch}	Image channel rejection	Mono(5), Δf = 400 kHz, (2 x IF), EN55020	45	50	-	dB
		Stereo(6), Δf = 400 kHz, (2 x IF), EN55020	40	45	-	dB
FA_{ch}	Far Away channel rejection	|Δf| >= 400 kHz, not including image frequency, EN55020	45	50	-	dB
AM	AM suppression	m = 0.3 for AM, mono(5) $V_{RFwired}$ = 14 μV_{EMF}, $V_{RFembedded}$ = 2.5 μV_{EMF}	40	-	-	dB
		m = 0.3 for AM, stereo(6) $V_{RFwired}$ = 1mV_{EMF}	50	-	-	dB

Table 38. FM receiver characteristics(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Analog audio outputs						
V_{AUDOL}, V_{AUDOR}	AUDOL, AUDOR output voltage	Mono(5) and stereo(6) (7)	60	70	90	mV_{rms}
DV_{AF} = V_{AUDOL}/ V_{AUDOR}	L-AF, R-AF output voltage ratio	Stereo(6), (7), Δf_{audio} = 67.5 kHz	-1	-	1	dB
$a_{mute(R)}$, $a_{mute(L)}$	AF or hard mute attenuation (not power off)	w.r.t. Δf_{audio} = 22.5 kHz, fmod = 1 kHz	70	80	-	dB
Z_{AUDOL}, Z_{AUDOR}	AUDOL, AUDOR output impedance		-	200	-	Ω
$Za_{mute(R)}$, $Za_{mute(L)}$	AUDOL, AUDOR output impedance during hard mute (not power off)		500	-	-	kΩ
Digital audio outputs						
VAF	audio output level	Stereo, Δf_{audio} = 22.5 kHz	-	-15.7	-	dBFS
DV_{AF} = V_{AUDOL}/V_{AUDOR}	L-AF, R-AF output voltage ratio	Stereo(6)(7), Δf_{audio} = 67.5 kHz	-1	-	1	dB
Audio signal processing						
(S+N)/N	Signal-to-Noise Ratio analog outputs	Mono(5)	57	60	-	dB
		Stereo(6)	53	56	-	dB
(S+N)/N	Signal-to-Noise Ratio digital outputs	Mono(5)	59	64	-	dB
		Stereo(6)	54	58	-	dB
THD	Total Harmonic Distortion	Mono(5), Δf_{audio} = 75 kHz, f_{audio} = 1 kHz	-	0.1	0.3	%
		Mono(5), Δf_{audio} =100 kHz, f_{audio} = 1 kHz	-	0.2	0.5	%
		Stereo(6), Δf_{audio} = 67.5 kHz	-	0.1	0.3	%
		Mono(3),(5) Δfaudio = 75 kHz, faudio = 400 Hz	-	0.1	0.3	%
		Mono(3),(5) Δfaudio = 75 kHz, faudio = 3 kHz	-	0.1	0.3	%
$Rx_{spurious}$	In-band audio spurious suppression (relative to 1 kHz carrier)	Mono(5)	60	-	-	dBc
		Stereo(6)	60	-	-	dBc
A_{sep}	Stereo channel separation	Stereo(6), Δf_{audio} = 67.5 kHz, only L or only R	45	55	-	dB

Table 38. FM receiver characteristics(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_{sep}	Pilot suppression	Stereo(6), Δf_{audio} = 67.5 kHz, only L or only R, de-emphasis 75 µs	55	60	-	dB
$Ripple_{audio}$	In band audio ripple(11)		-1	-	1	dB
FM_{CU_Low}	FM audio lower cut off frequency		-	-	20	Hz
FM_{CU_Up}	FM audio upper cut off frequency		15	-	-	kHz
$T_{deem50us}$	de-emphasis time constant 50 µs		45	50	55	µs
$T_{deem75us}$	de-emphasis time constant 75 µs		70	75	80	µs
FM RX out-of-band blocking performance(12)						
GSM850	824 – 849 MHz	EDGE	-	116	-	dBuV
E-GSM900	880 – 915 MHz	EDGE	-	116	-	dBuV
WCDMA III	1710 – 1785 MHz	WCDMA	-	110	-	dBuV
WCDMA II	1850 – 1910 MHz	WCDMA	-	110	-	dBuV
WLAN 2.4 GHz	2412 – 2472 MHz	WLAN	-	103	-	dBuV
WLAN 5 GHz	5150 – 5825 MHz	WLAN	-	103	-	dBuV

1. Typical is defined at Tamb = 25 °C, VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V (unless otherwise stated).
2. Minimum and maximum values are worst cases over corner lots, temperature, and supply voltages.
3. In PLL mode (i.e. with SYS_CLK), 26 MHz.
4. For wire antenna over 70 - 108 MHz, for embedded antenna over 76 - 108 MHz.
5. Mono, Δf_{audio} = 22.5 kHz, f_{mod} = 1 kHz, de-emphasis = 50 µs, unless otherwise stated.
6. Stereo, Δf_{audio} = 22.5 kHz, Δf_{pilot} = 6.75 kHz, f_{mod} = 1 kHz, L=R, de-emphasis = 50 µs, no RDS, unless otherwise stated.
7. V_{RFin} = 1 mV_{EMF}.
8. With IEC filter and A-weighting filter.
9. For wire antenna (FM_WANT) measured with the circuit: shown in *Figure 26*.
10. For embedded antenna (FM_ANT) measured with following circuit shown in *Figure 27*.
11. Audio range from 100 Hz to 14 kHz.
12. FM RX performance not degraded by more than 1 dB under the blocker power level listed at the FM wired antenna input (including a 150 nH matching inductor).

Figure 26. Measurement of the wired antenna (FM_WANT)

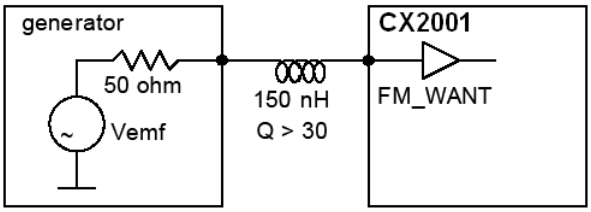


Figure 27. Measurement of embedded antenna (FM_ANT)

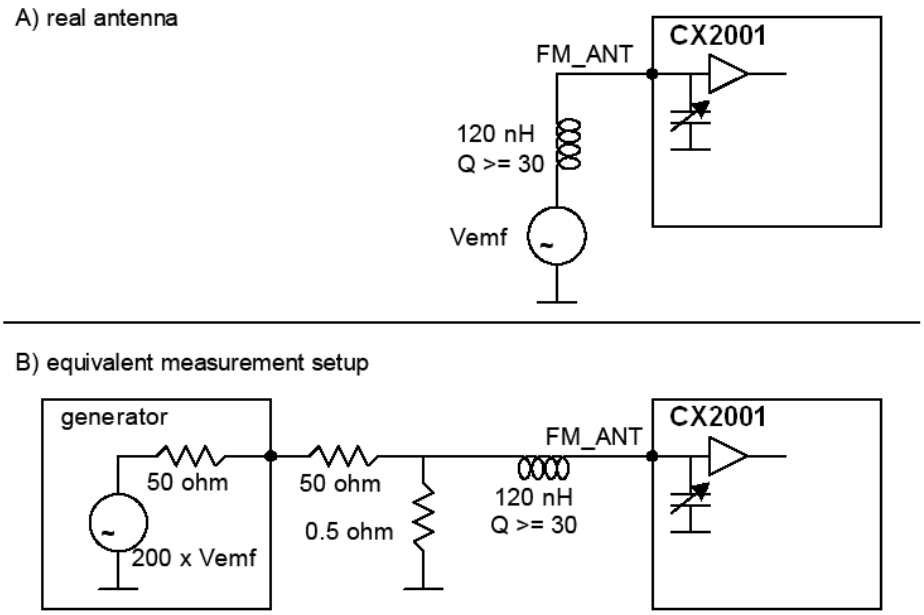


Table 39. FM power consumption(1)

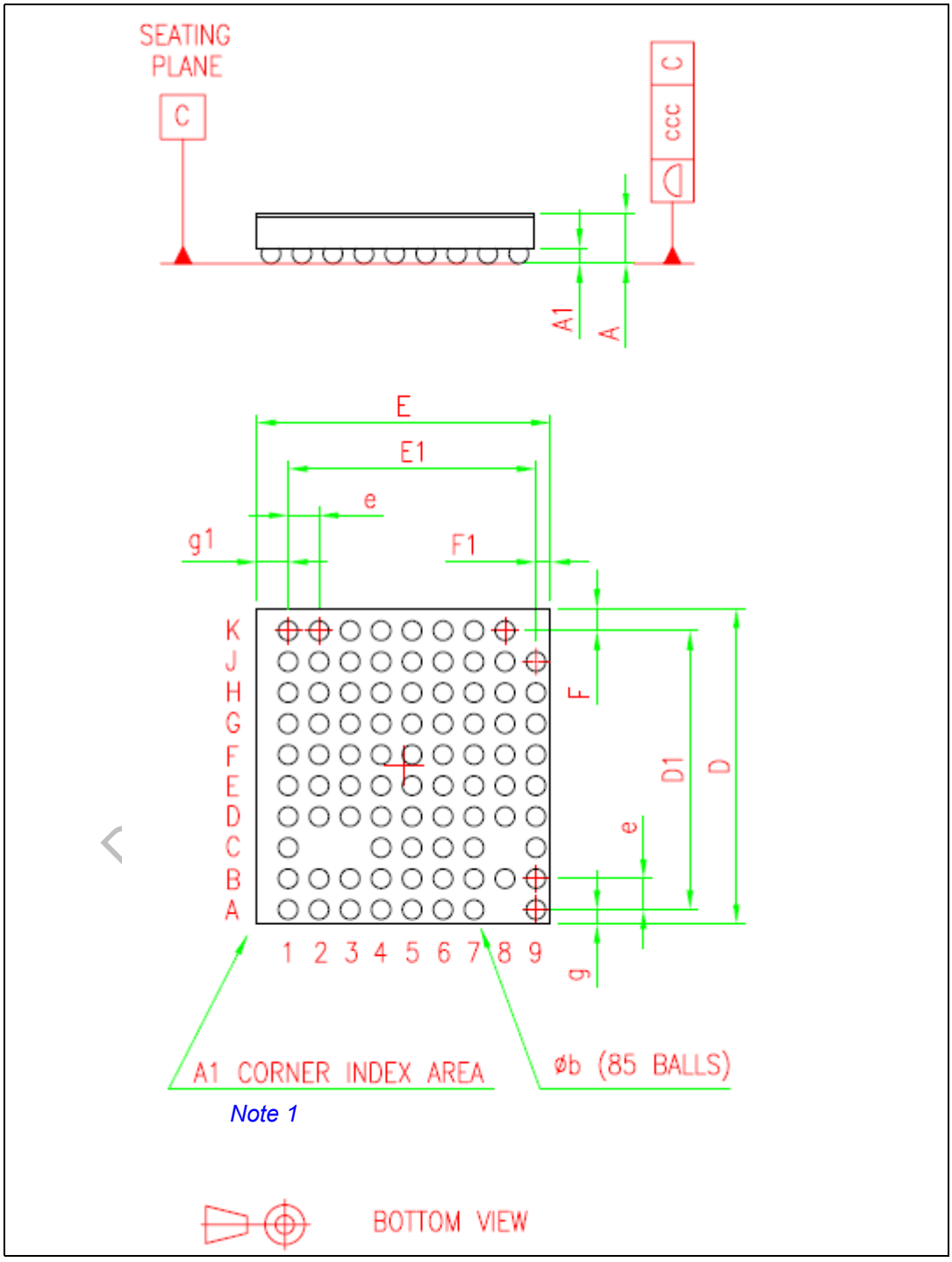
Symbol	Parameter	Condition	Typ.	Unit
I_{FMRX}	Receiver supply current consumption	(2)	12.6	mA
I_{FMTX}	Core supplies (1.8 V)	(3)	11.1	mA
	VDD_FM_PA domain (2.5 V)	(3)	3.8	mA

1. VDDIOx, VDD_DIG, VDD_GPS, VDD_BT_RF, VDD_BT_PA, VDDA_FM = 1.8 V, VDD_FM_PA = 2.5 V; temperature = 25 °C, power supply architecture 1 (*Figure 5*), VBAT current not included, unless otherwise specified.
2. Strong signal, digital audio output, PLL operation (i.e. SYS_CLK), stereo, including RDS.
3. 120 dBµV, PLL operation (i.e. SYS_CLK).

5 Package mechanical data

5.1 Package dimensions

Figure 28. WLCSP 3.80 mm x 4.07 mm x 0.6 mm, depopulated 0.4 mm pitch and 0.25 mm ball



1. The terminal A1 corner must be identified on the top surface by using a laser marking dot

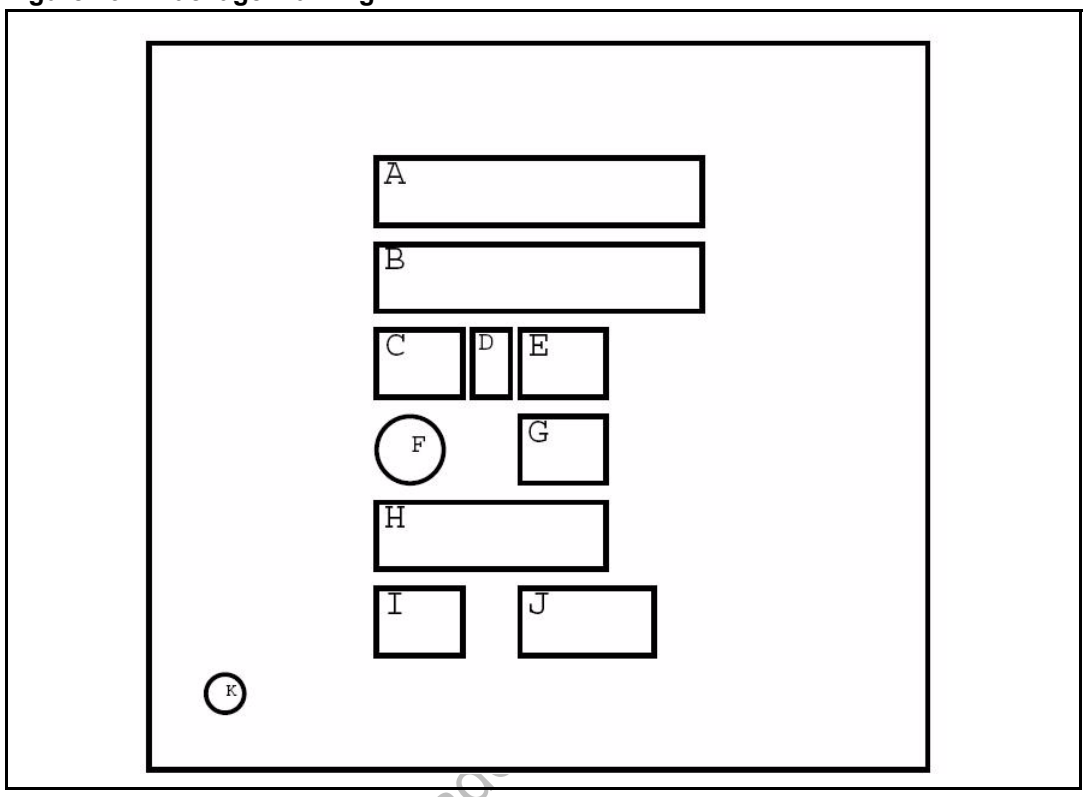
Table 40. WLCSP(1) package dimensions

Reference	Min.	Typ.	Max.	Unit
A			0.65	mm
A1		0.20		mm
b(2)		0.27		mm
D(3)	4.034	4.074	4.114	mm
D1		3.60		mm
E(4)	3.756	3.796	3.836	mm
E1		3.20		mm
e		0.40		mm
F(5)		0.29		mm
F1(5)		0.19		mm
g(5)		0.19		mm
g1(5)		0.41		
ccc			0.05	mm

1. WLCSP stands for Wafer Level Chip Scale Package
2. The typical ball parameter before mounting is 0.25 mm
3. D = D1 + F + g
4. E = E1 + F1 + g1
5. The matrix ball array is not centered

5.2 Package marking

Figure 29. Package marking

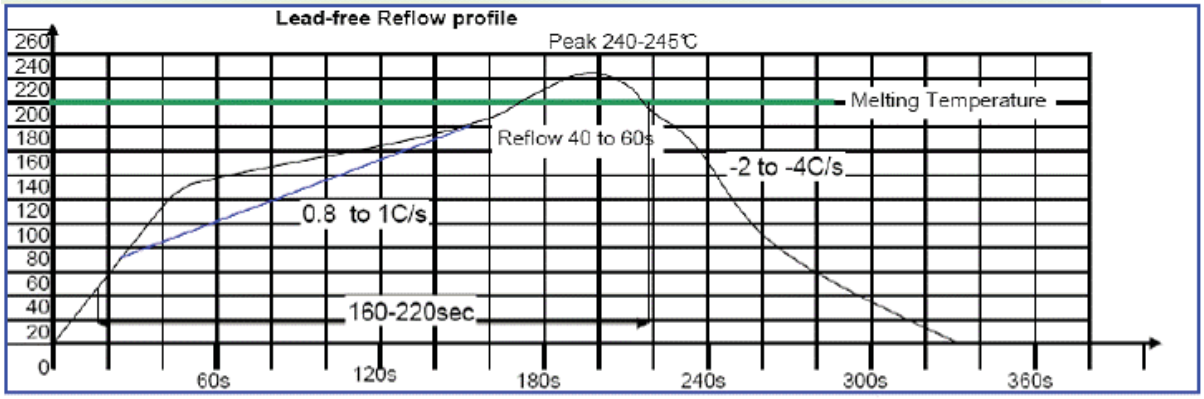


Where :

A	Marking area
B	Diff lot
C	Assy plant (PP)
D	Assy year (Y)
E	Assy week (WW)
F	Second_lvl_intct
G	Marking area
H	Marking area
I	Diffusion traceability plant (WX)
J	Country of origin
K	DOT

5.3 Recommended reflow profile

Figure 30. Recommended reflow profile



Profile	Ramp to Strike	
Temp. gradient in preheat	(T= 70-180°C):	0.9 +/-0.1°C/s
Temp. gradient	(T=200-225°C):	1.1 – 3.0°C/s
Peak temp. in reflow	240 +/- 5°C	
Time above 220°C	50 +/- 10sec	
Temp. gradient in cooling	-2 to -4 °C/s (-6 °C/s max.)	
Time from 50 to 220°C	160 to 220sec.	

5.4 Moisture sensitivity level

CX2001 is a MSL1 device according to JESD 22-A-113 convention. Moisture sensitivity levels are ranked from level 1 (most resistive to moisture) to level 5 (least resistive to moisture).

6 Handling information

Inputs and outputs are protected against Electro-Static Discharge (ESD) during handling and mounting. A Human-Body Model (HBM), and a Charged Device Model (CDM) are used for ESD susceptibility testing. All pins are able to withstand the following threshold voltages:

Table 41. ESD threshold voltages(1)

Parameter	Method	Value	Class
ESD threshold voltage	HBM (JESD22-A114-B)	1000 (V)	1B
	CDM (JESD22-C101-A)	500 (V)	2

1. The above specification include the RF pins.

7 Glossary

BR	Bluetooth Basic Rate (1 Mbit/s)
BT	Bluetooth
CDM	Charged Device Model
Coexistence	Coexistence scenarii refer to the interferences between two systems via antenna coupling or any other form of coupling mechanism external to the product.
Cohabitation	Scenarios refer to the interferences between two systems via coupling mechanisms internal to the product
DEVM	Differential Error Vector Magnitude
EA	Enumeration Address
EDR	Bluetooth Enhanced Data Rate (2 and 3 Mbit/s)
EIR	Extended Inquiry Response
EPR	Encryption Pause/Resume
ESD	Electro-Static Discharge
FM	Frequency Modulation
FU	Frequency Uncertainty
GPS	Global Positioning System
HBM	Human Body Model
I2S-bus	Inter Integrated circuit Sound bus
IF	Intermediate Frequency
LEB	Low Energy Bluetooth (previously called Ultra Low Power)
LSB	Less Significant Bit
LSTO	support Link Supervision Time Out Changed event
LSW	Less Significant Word
ME	Measurement Engine
MM	Machine Model
MSB	Most Significant Bit
MSW	Most Significant Word
NRZI	Non-Return-to-Zero Inverted
PA	Power Amplifier
PBF	support flushable and non-flushable packets in the Packet Boundary Flag
PE	Processor Engine
PU	Position Uncertainty

QoS	Quality of Service
RX	Receiver
SSP	Secure Simple Pairing
SSR	Sniff Sub Rating
TDM	Time Division Multiplexed
TX	Transmitter

8 References

1. Specification of the Bluetooth System V4.0, December 2009, Bluetooth SIG
2. Specification of the Bluetooth System V3.0, April 2009, Bluetooth SIG
3. Specification of the Bluetooth System V2.1 + EDR, July 2007, Bluetooth SIG
4. Specification of the Bluetooth System V2.0 + EDR, November 2004, Bluetooth SIG
5. Specification of the Bluetooth System V1.2, November 2003, Bluetooth SIG
6. Specification of the Bluetooth System - Host Controller Interface [Transport Layer] Volume 04 Revision 1.2 or later, part A: UART v1.1, January 2006, Bluetooth SIG
7. Radio Frequency Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR, document number RF.TS/2.0.E.3, March 2005, Bluetooth SIG
8. IEEE 802.15.2, IEEE Recommended Practice for Telecommunications and Information exchange between systems – Local and metropolitan area networks Specific Requirements - Part 15.2: Coexistence of Wireless Personal Area Networks with Other Wireless Devices Operating in Unlicensed Frequency Band, August 2003, IEEE
9. The I2S-bus specification, June 1996, Philips Semiconductors
10. CX2001 hardware manual, description of how to integrate the CX2001 in a host platform from Hardware point of view
11. CX2001 software manual, description of how to integrate the CX2001 in a host platform from Software point of view
12. JEDEC J-STD-020B Classification procedure for moisture sensitive components
13. JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
14. JESD22-C101-A Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

9 Ordering information

Table 42. Ordering information

Order code(1)	Description	Package(2)
CX200101UKTM	Product include GPS, Bluetooth, and FM	Package CSP without BSC

1. Refer to *Section 5.2: Package marking*
2. Back-Side Coating. It is a tape of 40 micron thickness, used for protecting and reinforcing the chip surface.

10 Revision history

Table 43. Document revision history

Data	Revision	Changes
14-Dec-2012	1	Objective specification

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