ROCKCHIPS
PRODUCT DATASHEET
RKNanoC

Revision 1.7

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Revision History

Date	Revision	Description
2012-09-30	0.0	Initial spec for RKnanoC
2012-02-01	0.1	Adjustment for spec
2012-02-16	1.0	First release datasheet
2012-3-2	1.1	Change pin assignment
2012-3-16	1.3	Change some hardware information
2012-4-7	1.4	Modify electrical specification & Change some hardware information
2012-6-7	1.5	Add LQFP80 package information
2012-8-23	1.6	fix pin description and add TBGA81 information, updated
2013-4-3	1.7	fix pin description

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1. Overview

RKnanoC is a low-cost, low-power, high-efficiency digital multimedia chip which is based on ARM low power processor architecture with hardware accelerator. It is designed for portable audio product applications such as MP3 player etc.

RKnanoC can support decode for various types of audio standards such as MP3/WMA /OGG/FLAG/AAC etc. Because of build-in audio hardware accelerator, RKnanoC can achieve audio decode at a very low system frequency, this can save chip power consumption. By providing a complete set of peripheral interface, RKnanoC can support very flexible applications, including NAND Flash, LCDC, USB OTG, SD/MMC, I2C, I2S, SPI, UART, PWM etc.

2. Features

- **System Operation**
  - ARM processor
  - AHB-lite bus connection
  - Selectable booting method
    - Boot from NAND FLASH
    - Boot from eMMC flash
    - Boot from SPI NOR flash
- **Memory Organization**
  - Internal 224KB SRAM for IRAM and DRAM
  - Embedded 64KB ROM for decoder and system code
- **Processor**
  - ARM Cortex-M3 low power core
    - A Thumb instruction set subset
    - Banked Stack Pointer (SP) only
    - Hardware divide instructions, SDIV and UDIV (Thumb 32-bit instructions)
    - Handler and Thread modes
    - Thumb and Debug states
    - Interruptible-continued LDM/STM, PUSH/POP for low interrupt latency
    - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Nested Vectored Interrupt Controller (NVIC)
    - 26 external interrupts.
    - 8-level priority of interrupt
- **Clock & Power Management**
  - One on-chip PLL, system main clock can be PLL clock or OSC input clock
  - Support different main clock and internal AHB Bus clock ratio:
    1:1, 1:2, 1:3, 1:4, up to 1:8 modes
  - Support different AHB Bus clock and ARM system tick clock ratio:
    1:2, 1:3, 1:4, up to 1:8 modes
  - Support different AHB Bus clock and ARM APB Bus clock ratio:
    1:1, 1:2, 1:3 and 1:4 mode
  - 100MHz Max frequency for ARM Core
  - Clock gating for ARM Cortex-M3 sleep mode and other peripherals

- Support ARM clock bypass/divider 2/divider 4 path for 24MHz arm clock

- **Hardware Accelerator for MP3 decode**
  - MP3 imdct36 calculation module
  - MP3 subband synthesize module

- **Memory Interface**
  - External-Memory controller
    - Support 4 chip selects for NAND flash
    - Support 24/40/60bits ECC error correction
    - Support 8bits data-width to external NAND
  - SD/MMC controller
    - SD/MMC SPI mode/1bit mode/4bit mode
    - Support Multi Media Card Specification Version 4.41
    - Support SD Memory Card Specification Version 3.0
    - Support Secure Digital I/O(SDIO Version3.0)
    - Cards Clock Rate up to PCLK, Re-scaling the SD/MMC clock (PCLK) with the 8-bits pre-scale register in SCU block

- **VIDEO interface**
  - LCD controller
    - Compatible with MCU LCD Panel
    - Up to 8 LCD data output bus

- **DMA Controller**
  - One DMA Controller in chip
    - Support 3 DMA channels, 7 external requests
    - Support incremental and fixed addressing mode
    - Support hardware and software trigger DMA transfer mode
    - Support error interrupt, transport-complete interrupt
    - When transport data is not align with source burst, the last data will be transported in single burst mode
    - Support configurable channel priority

- **USB interface**
  - USB 2.0 OTG controller and PHY
  - Operates in High-Speed and Full-Speed mode
  - Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
  - Support 6 endpoints , one control endpoint, two IN/OUT endpoints, one IN endpoint
  - Support 4 channels at Host mode, support bulk transfer

- **Low speed Peripheral interface**
  - I2C controller
    - Supports master and slave modes of I2C bus
    - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
    - Supports 7 bits and 10 bits addressing modes

- I2S
  - Support mono/stereo audio file
  - Support audio resolution: 8, 16 bits
  - Support audio sample rate from 8KHz to 48 KHz
  - Support I2S, Left-Justified and Right-Justified digital serial data format
- PWM
  - 3 Channels Built-in 16 bit timer
  - 0 ~ 100 % duty ratio PWM signal generation
  - Re-scaling the counting clock (PCLK) with the 8-bits pre-scale register in SCU block
- SPI master
  - Serial-master operation – Enables serial communication with serial-slave peripheral devices.
  - DMA Controller Interface – Enables interface to a DMA controller using a handshaking interface for transfer requests.
  - Support interrupt interface to interrupt controller, and independently masking of interrupts.
  - One hardware slave-select lines.
  - Dynamic control of the serial bit rate of the data transfer.
- GPIO
  - Support 28 individually programmable input/output pins
  - 28 GPIOs with external interrupt capability
- Timer
  - Built-in One 24-bits timer module
  - Support for two operation modes : free-running and user-defined count
- Uart
  - AMBA APB interface – Allows for easy integration into a Synthesizable Components for AMBA 2 implementation.
  - DMA Controller Interface – Enables interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
  - Support interrupt interface to interrupt controller.

- **Analog IP interface**
  - AUDIO-DAC
    - 24bit Audio DAC with Headphone Amplifier
    - Ultra Low Quiescent Current
    - Pop Noise free
    - High Efficiency Class G Headphone Amplifier
    - Asynchronous adopting different sampling rate
  - MIC amplifier
    - 20DB low noise boost amplifier
    - Low noise programmed amplifier for MIC input
  - ADC Converter
    - 4-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
  - DCDC
    - 1.2V Default Output Voltage setting

- Current mode control with Internal Compensation
- 100mA Output Current
- Forced PWM operation
- Adjustable output voltage.
- 3MHz operating frequency.
- Integrated COUT discharge Switch.

- LDO
  - 3.3V Default Output Voltage
  - Stable with 0.8uF low ESR ceramic capacitor
  - 100mA Output Current limit
  - Adjustable output voltage.
  - Integrated COUT discharge Switch

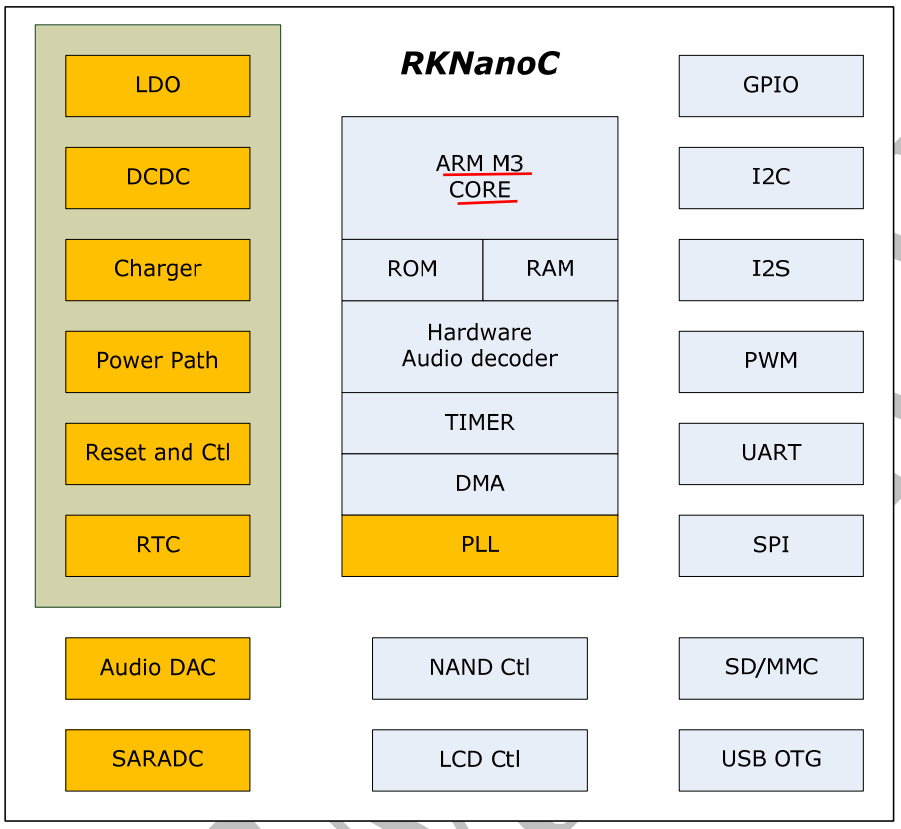
- RTC
  - Working at 32.768KHz oscillator clock
  - 16 bits compensation.

- Power Manager Unit
  - On/Off Logic for power up/down control
  - Power on reset
  - Power on sequence control
  - Power path, switch power supply between battery and USB/AC adaptor input
  - Max 200mA charger, Charges Single Cell Li-Ion Batteries Directly from USB prot

- Package
  - NanoC LQFP80
  - NanoC-L LQFP64
  - NanoC-G TFBGA81

3. Block Diagram

The following figure shows block diagram of RKnanoC.



4. Package Type

The following Table shows package of RKnanoC.

Table 41 RKnanoC LQFP64 Pin Description

RKnano			
PIN No	**Names**	**Direction**	**PIN Description**
LEFT			
1	PMU_AVDD12	P	1.2V Power from DCDC for DAC and HP
2	PMU_INL	A	Line-in left channel
3	PMU_INR	A	Line-in right channel
4	PMU_AGND	G	Analog ground for DAC and HP
5	PMU_HPR	A	Headphone right output
6	PMU_AOM	G	Headphone virtual ground output
7	PMU_AOMS	G	Headphone virtual ground sense input
8	PMU_HPL	A	Headphone left output
9	PMU_AVDD33	P	Power Supply for HP
10	PMU_DCDC_FB	A	DC-DC feedback
11	PMU_PGND	G	Analog ground for DC-DC
12	PMU_DCDC_SW	A	DC-DC Switched Output
13	PMU_DCDC_VIN	A	Power Path output and DCDC input
14	PMU_ADP_VIN	P	Adapter Power Supply
15	PMU_BAT	P	Battery Supply
16	PMU_PLAYON	A	Function button press signal
BOTTOM			
17	LADC_AIN0	A	SARADC AIN channel 0
18	LADC_AIN1	A	SARADC AIN channel 1
19	LADC_AIN2	A	SARADC AIN channel 2
20	LADC_VSSA	G	SARADC analog ground
21	LADC_VMID	A	Connected With a External Capacitor
22	LADC_VDDA	P	SARADC analog power
23	USB_VSS33	G	Power supply 3.3v
24	USB_DP	A	USB D+ signal
25	USB_TXRTUNE	A	USB tx resistor tune
26	USB_DM	A	USB D- signal
27	USB_VSS33_1	G	Ground for USBPHY
28	USB_VDD33_1	P	Power for USBPHY
29	PLL_VSS	G	PLL ground
30	PLL_VDD	P	PLL power 1.2v
31	PD3/pwm2	IO/PD	GPIO0D[3]/pwm2 output
32	OSC24M_OUT	O	24M Oscillator Output
RIGHT			
33	OSC24M_IN	I	24M Oscillator Input
34	PD2/PWM 1	IO/PD	GPIO0D[2]/pwm1 output
35	PC3/SDMMC_D0	IO/PU	GPIO0C[3]/SDMMC data[0]
36	PC2/SDMMC_CLK	IO/PD	GPIO0C[2]/SDMMC clock output

37	PC1/SDMMC_CMD	IO/PU	GPIO0C[1]/SDMMC command output
38	VCCIO	P	IO Power 3.3V
39	VSS	G	Core Ground
40	VDD	P	Core Power 1.2v
41	PA1/FLASH_CSN1	IO/PU	GPIO0A[1]/FLASH chip select 1
42	PA6/FLASH_CLE/SPI_CSN0/SDMMC_CMD	IO/PU	GPIO0A[6]/FLASH CLE/SPI CS0/SDMMC command signal
43	PA5/FLASH_WR/SPI_CLK	IO/PU	GPIO0A[5]/FLASH WR/SPI CLK signal
44	PA4/FLASH_RDN/SPI_TXD/SDMMC_RSTN	IO/PU	GPIO0A[4]/FLASH RDN/SPI TX/SDMMC Reset signal
45	PA3/FLASH_RDY/SPI_TXD/SDMMC_CLK	IO/PU	GPIO0A[3]/FLASH RDY/SPI RX/SDMMC CLK
46	PA2/FLASH_CLE/LCD_RS	IO/PD	GPIO0A[2]/FLASH ALE/LCD RS
47	PA0/FLASH_CSN0/SDMMC_PWR_EN	IO/PU	GPIO0A[0]/FLASH chip select 0/SDMMC power enable
48	PB6/UART_RXD	IO/PU	GPIO0B[6]/ UART RX data
TOP			
49	PB5/UART_TXD	IO/PU	GPIO0B[5]/UART TX data
50	FLASH_DATA[7]	IO/PU	FLASH /SDMMC/LCD data bit7
51	FLASH_DATA[6]	IO/PU	FLASH /SDMMC/LCD data bit6
52	FLASH_DATA[5]	IO/PU	FLASH/SDMMC/LCD data bit5
53	FLASH_DATA[4]	IO/PU	FLASH/SDMMC/LCD data bit4
54	FLASH_DATA[3]	IO/PU	FLASH/SDMMC/LCD data bit3
55	VCCIO	P	IO Power 3.3v
56	VSS	G	Core Ground
57	VDD	P	Core Power 1.2v
58	FLASH_DATA[2]	IO/PU	FLASH/SDMMC/LCD data bit2
59	FLASH_DATA[1]	IO/PU	FLASH/SDMMC/LCD data bit1
60	FLASH_DATA[0]	IO/PU	FLASH/SDMMC/LCD data bit0
61	PB0/LCD_WR	IO/PU	GPIO0B[0]/LCD_WR output
62	PA7/LCD_CSN	IO/PU	GPIO0A[7]/LCD_CSN output
63	PD0/ I2C SDA/FLASH_CSN3	IO/PU	GPIO0D[0]/I2C SDA/FLASH chip select 3
64	PC7/I2C_SCL/FLASH_CSN2	IO/PU	GPIO0C[7]/I2C_SCL/FLASH chip select 2

Note:

P : Power

G : Ground

I : Input Only

O : Output Only

IO : INPUT & OUTPUT

PU : Pull-Up

PD : Pull-Down

Table 42 RKnanoC-L LQFP80 Pin Description

PIN No	Names	Direction	PIN Description
LEFT			
1	PMU_AVDD12	P	1.2V Power from DCDC for DAC and HP
2	PMU_INL	A	Line-in left channel
3	PMU_INR	A	Line-in right channel
4	PMU_AGND	G	Analog ground for DAC and HP

5	PMU_HPR	A	Headphone right output
6	PMU_AOM	G	Headphone virtual ground output
7	PMU_AOMS	G	Headphone virtual ground sense input
8	PMU_HPL	A	Headphone left output
9	PMU_AVDD33	P	Power Supply for HP
10	PMU_DCDC_FB	A	DC-DC feedback
11	PMU_PGND	G	Analog ground for DC-DC
12	PMU_DCDC_SW	A	DC-DC Switched Output
13	PMU_DCDC_VIN	A	Power Path output and DCDC input
14	PMU_ADP_VIN	P	Adapter Power Supply
15	PMU_BAT	P	Battery Supply
16	PMU_OSC_SEL	I	Select PMU OSC source (32K or RC)
17	PMU_PLAYON	A	Function button press signal
18	OSC32K_IN	I	32.768K Oscillator Input
19	OSC32K_OUT	O	32.768K Oscillator Output
20	LADC_AIN0	A	SARADC AIN channel 0
BOTTOM			
21	LADC_AIN1	A	SARADC AIN channel 1
22	LADC_AIN2	A	SARADC AIN channel 2
23	LADC_VSSA	G	SARADC analog ground
24	LADC_VMID	A	Connected With a External Capacitor
25	LADC_VREF	A	SARADC reference voltage input
26	LADC_VDDA	P	SARADC analog power
27	USB_VSS33	G	Power supply 3.3v
28	USB_DP	A	USB D+ signal
29	USB_TXRTUNE	A	USB tx resistor tune
30	USB_DM	A	USB D- signal
31	USB_VSS33_1	G	Ground for USBPHY
32	USB_VDD33_1	P	Power for USBPHY
33	USB_VSS33	G	PLL ground
34	PLL_AVDD	P	PLL power 1.2v
35	JTAG_TCK	I/PU	JTAG TCK
36	JTAG_TRSTN	I/PD	JTAG TRSTN
37	JTAG_TDI	I/PU	JTAG TDI
38	JTAG_TMS	I/PU	JTAG TMS
39	JTAG_TDO	O	JTAG TDO
40	PD3/pwm2	IO/PD	GPIO0D[3]/pwm2 output
RIGHT			
41	OSC24M_OUT	O	24M Oscillator Output
42	OSC24M_IN	I	24M Oscillator Input
43	PD2/PWM 1	IO/PD	GPIO0D[2]/pwm1 output
44	PC6/SDMMC_D3	IO/PU	GPIO0_C[6]/SD0_D[3]/SDI
45	PC5/SDMMC_D2	IO/PU	GPIO0_C[5]/SD0_D[2]/SDO
46	PC4/SDMMC_D1	IO/PU	GPIO0_C[4]/SD0_D[1]/BCK
47	PC3/SDMMC_D0	IO/PU	GPIO0C[3]/SDMMC data[0]

48	PC2/SDMMC_CLK	IO/PD	GPIO0C[2]/SDMMC clock output
49	PC1/SDMMC_CMD	IO/PU	GPIO0C[1]/SDMMC command output
50	VCCIO	P	IO Power 3.3V
51	VSS	G	Core Ground
52	VDD	P	Core Power 1.2v
53	PA1/FLASH_CSN1	IO/PU	GPIO0A[1]/FLASH chip select 1
54	PA6/FLASH_CLE/SPI_CSN0/SDMMC_CMD	IO/PU	GPIO0A[6]/FLASH CLE/SPI CS0/SDMMC command signal
55	PA5/FLASH_WR/SPI_CLK	IO/PU	GPIO0A[5]/FLASH WR/SPI CLK signal
56	PA4/FLASH_RDN/SPI_TXD/SDMMC_RSTN	IO/PU	GPIO0A[4]/FLASH RDN/SPI TX/SDMMC Reset signal
57	PA3/FLASH_RDY/SPI_TXD/SDMMC_CLK	IO/PU	GPIO0A[3]/FLASH RDY/SPI RX/SDMMC CLK
58	PA2/FLASH_CLE/LCD_RS	IO/PD	GPIO0A[2]/FLASH ALE/LCD RS
59	PA0/FLASH_CSN0/SDMMC_PWR_EN	IO/PU	GPIO0A[0]/FLASH chip select 0/SDMMC power enable
60	PC0/UART_RTS	IO/PU	GPIO0C[0]/ UART RTS
TOP			
61	PB7/UART_CTS	IO/PU	GPIO0B[7]/ UART CTS
62	PB6/UART_RXD	IO/PD	GPIO0B[6]/ UART RX data
63	PB5/UART_TXD	IO/PD	GPIO0B[5]/UART TX data
64	PB4/SPI1_RXD	IO/PD	GPIO0_B[4]/SPI1_RXD
65	PB3/SPI1_TXD	IO/PU	GPIO0_B[3]/SPI1_TXD
66	PB2/SPI1_CLK	IO/PU	GPIO0_B[2]/SPI1_CLK
67	PB1/SPI1_CS1	IO/PU	GPIO0_B[1]/SPI1_CS1
68	FLASH_DATA[7]	IO/PU	FLASH /SDMMC/LCD data bit7
69	FLASH_DATA[6]	IO/PU	FLASH /SDMMC/LCD data bit6
70	FLASH_DATA[5]	IO/PU	FLASH/SDMMC/LCD data bit5
71	FLASH_DATA[4]	P	FLASH/SDMMC/LCD data bit4
72	FLASH_DATA[3]	G	FLASH/SDMMC/LCD data bit3
73	VCCIO	P	IO Power 3.3v
74	VDD	IO/PU	Core Power 1.2v
75	FLASH_DATA[2]	IO/PU	FLASH/SDMMC/LCD data bit2
76	FLASH_DATA[1]	IO/PU	FLASH/SDMMC/LCD data bit1
77	FLASH_DATA[0]	IO/PU	FLASH/SDMMC/LCD data bit0
78	PB0/LCD_WR	IO/PU	GPIO0B[0]/LCD_WR output
79	PD0/ I2C SDA/FLASH_CSN3	IO/PU	GPIO0D[0]/I2C SDA/FLASH chip select 3
80	PC7/I2C_SCL/FLASH_CSN2	IO/PU	GPIO0C[7]/I2C_SCL/FLASH chip select 2

Note：

P : Power

G : Ground

I : Input Only

O : Output Only

IO : INPUT & OUTPUT

PU : Pull-Up

PD : Pull-Down

Table 43 RKnanoC-G TFBGA81 Pin Description

	1	2	3	4	5	6	7	8	9	10	11	
A	PA7/LCD_CSN	FLASH_D0/LCD_D0	FLASH_D2/LCD_D2	VCCIO1	FLASH_D4/LCD_D4	FLASH_D6/LCD_D6	PB1/SPI_CSN1	PB3/SPI_TXD	PB5/TXD	PB7	PD7	A
B	AVDD12	PC7/FLASH_CSN2/I2C_SCL	PB0/LCD_WRN	VDD1	FLASH_D3/LCD_D3	FLASH_D5/LCD_D5	PB2/SPI_CLK	PB6/RXD	PC0	PD6	PD5	B
C	AIL	PD0/FLASH_CSN3/I2C_SDA	NP	NP	NP	NP	NP	NP	NP	PD4	PA0/FLASH_CSN0	C
D	AVSS	AIR	NP	NP	VSS1	NP	FLASH_D7/LCD_D7	NP	NP	PA2/FLASH_ALE/LCD_RS	PA3/FLASH_RDY/SPI_RXD	D
E	AOM	AOR	NP	FLASH_D1/LCD_D1	NP	NP	NP	PB4/SPI_RXD	NP	PA4/FLASH_RDN/SPI_TXD	PA5/FLASH_WRN/SPI_CLK	E
F	AVDD33	AOMS	NP	NP	NP	OSC_SEL	NP	NP	NP	PA6/FLASH_CLE/SPI_CSN0	VDD2	F
G	DCDC_SW	DCDC_FB	NP	AOL	NP	NP	NP	PC1/SD_CMD	NP	PA1/FLASH_CSN1	PC2/SD_CLK/I2S_CLK	G
H	VSYS	DCDC_PGND	NP	NP	PLAYON	NP	PC3/SD_D0/I2S_LRCK	NP	NP	VSS2	PC4/SD_D1/I2S_SCLK	H
J	ADP_IN	MIC_IN/ADC_AIN0	NP	NP	NP	NP	NP	NP	NP	VCCIO2	PC6/SD_D3/I2S_SDI	J
K	BAT	ADC_AIN1	REXT100K	VSS3	TXRTUNE	JTAG_TRSTN	PD3/PWM2/JTAG_TDI	JTAG_TMS	JTAG_TDO	PC5/SD_D2/I2S_SDO	PD1/PWM0	K
L	32K_IN	32K_OUT	ADC_AIN2	OTG_DP	OTG_DM	VBUS	OTG_ID	JTAG_TCK	XOUT24M	XIN24M	PD2/PWM1	L
	1	2	3	4	5	6	7	8	9	10	11	

5. Pin Mux Description

This pin mux list is for digital die pad.The IOs not bonded out are not included in LQFP64 package pinlist. And the IO_GPIO0_X[Y] also marked as PXY,like IO_GPIO0_A[0] equals to PA0.

Table 51 RKnano Pin Mux

Pad name	func2	func3	func4	Pull up / down	Pad Dir
IO_GPIO0_A[0]	flash_csn0	dummy	sdmmc_pwr_en	up	I/O
IO_GPIO0_A[1]	flash_csn1	dummy	dummy	up	I/O
IO_GPIO0_A[2]	flash_ale	lcd_rs	dummy	down	I/O
IO_GPIO0_A[3]	flash_rdy	spi_rxd_p0	sdmmc_cclk_p1	up	I/O
IO_GPIO0_A[4]	flash_rdn	spi_txd_p0	sdmmc_rstn_p1	up	I/O
IO_GPIO0_A[5]	flash_wrn	spi_clk_p0	dummy	up	I/O
IO_GPIO0_A[6]	flash_cle	spi_csn0	sdmmc_cmd_p1	up	I/O
IO_GPIO0_A[7]	lcd_csn	dummy	dummy	up	I/O
IO_GPIO0_B[0]	lcd_wrn			up	I/O
IO_GPIO0_B[1]	spi_csn1			up	I/O
IO_GPIO0_B[2]	spi_clk_p1			down	I/O
IO_GPIO0_B[3]	spi_txd_p1			down	I/O
IO_GPIO0_B[4]	spi_rxd_p1			down	I/O
IO_GPIO0_B[5]	uart_txd			up	I/O
IO_GPIO0_B[6]	uart_rxd			up	I/O
IO_GPIO0_B[7]	uart_cts			up	I/O
IO_GPIO0_C[0]	uart_rts	uart_sir_i		up	I/O
IO_GPIO0_C[1]	sdmmc_cmd_p0			up	I/O
IO_GPIO0_C[2]	sdmmc_clk_p0	i2s_clk		down	I/O
IO_GPIO0_C[3]	sdmmc_data0_p0	i2s_lrck		up	I/O
IO_GPIO0_C[4]	sdmmc_data1_p0	i2s_sclk		up	I/O
IO_GPIO0_C[5]	sdmmc_data2_p0	i2s_sdo		up	I/O
IO_GPIO0_C[6]	sdmmc_data3_p0	i2s_sdi		up	I/O
IO_GPIO0_C[7]	i2c_scl	flash_csn2		up	I/O
IO_GPIO0_D[0]	i2c_sda	flash_csn3		up	I/O
IO_GPIO0_D[1]	pwm0			down	I/O
IO_GPIO0_D[2]	pwm1			down	I/O
IO_GPIO0_D[3]	pwm2	clk_obs		down	I/O
IO_GPIO0_D[4]				up	I/O
IO_GPIO0_D[5]				up	I/O
IO_GPIO0_D[6]				down	I/O
IO_GPIO0_D[7]				down	I/O
IO_FLASH_DATA[0]	sdmmc_data0_p1	lcd_data0		up	I/O
IO_FLASH_DATA[1]	sdmmc_data1_p1	lcd_data1		up	I/O
IO_FLASH_DATA[2]	sdmmc_data2_p1	lcd_data2		up	I/O
IO_FLASH_DATA[3]	sdmmc_data3_p1	lcd_data3		up	I/O
IO_FLASH_DATA[4]	sdmmc_data4_p1	lcd_data4		up	I/O
IO_FLASH_DATA[5]	sdmmc_data5_p1	lcd_data5		up	I/O
IO_FLASH_DATA[6]	sdmmc_data6_p1	lcd_data6		up	I/O

IO_FLASH_DATA[7]	sdmmc_data7_p1	lcd_data7		up	I/O
IO_JTAG_TCK				up	I/O
IO_JTAG_TRSTN				down	I/O
IO_JTAG_TDI				up	I/O
IO_JTAG_TMS				up	I/O
IO_JTAG_TDO				down	O
IO_TEST				down	I

6. Electrical Specification

6.1 Absolute Maximum Ratings

Table 61 Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	VDD	1.32	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB)	VCCIO	3.6	V
DC supply voltage for Analog part of SAR-ADC	LADC_VDDA	3.6	V
DC supply voltage for Analog part of PLL	PLL_AVDD	1.32	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_VDD33	3.63	V
Analog Input voltage for SAR-ADC		3.6	V
Analog Input voltage for DP/DM of USB OTG/Host2.0		3.6	V
Storage Temperature		125	℃

6.2 Recommend Operation Conditions

Table 62 Operation Ranges

Parameter	Symbol	Min	Type	Max	Units
Core Supply Voltage	VDD	1.0	1.2	1.32	V
Digital I/O Supply Voltage	V_{IN}	2.8	3.3	3.6	V
Analog Supply Voltage	PMU_DCDC_VIN	2.3		5.5	V
	PMU_AVDD33	2.7		3.6	V
	PMU_ADP_VIN	4.25	5	5.5	V
	USB_VDD33_1	3.069	3.3	3.6	V
	PLL_VDD		1.2		V
	LADC_VDDA	2.7	3.3	3.6	V
	PMU_AVDD12		1.2		V
Storage Temperature	$T_{STORAGE}$	-40		125	ºC
Ambient Operation Temperature Range	T_{ope}	-10		70	ºC
ESD Damage Immunity	V_{ESD}				V
Human Body Model(HBM)		-	-	TBD	
Machine Model(MM)		-	-	TBD	
Charge Device Model(CDM)		-	-	TBD	

6.3 DC Characteristics

Table 63 DC Characteristics

Parameters		Symbol	Min	Type	Max	Units
Digital GPIO	Input Low Voltage	V_{il}	-0.3	0	0.8	V
	Input High Voltage	V_{ih}	0.7*VCCIO			V
	Output Low Voltage	V_{ol}		0	0.4	V
	Output High Voltage	V_{oh}	2.4	3.3	N/A	V

	Pull-up Resistor	R_{pu}	63	77	106	Kohms
	Pull-down Resistor	R_{pd}	60	81	143	Kohms

6.4 Interfaces Frequency

Table 64 Interfaces Frequency

Parameter	Symbol	Min	Type	Max	Units
JTAG TCK Frequency	f_{JTAG}	-	10	-	MHz
SPI clkout Frequency	f_{SPI}	-	-	49	MHz
SDMMC cclk Frequency	f_{SDMMC}	-	-	48	MHz

6.5 Analog Performance Characteristics

Table 65 Audio Playback Path Performance Characteristics

Parameter	Description	Min	Type	Max	Units
Dynamic Range	20Hz to 20kHz, -60dBFS input, A-Weighted(rms)		90		dB
SNR	20Hz to 20kHz,A-Weighted, relative to full scale		90		dB
THD+N	At -1dBFS, 1kHz		60		dB
Inter channel Isolation	AOM output, Sense connect out earphone Jack		70		dB
PSRR	100mVpp@AVDD,217kHz		80		dB
Quiescent Current	1.2V		2		mA
Pout	16oHm,@1%THD		10		mW
	16ohm @0.1mw hp		0.2		mW
Digital Volume Control	Step		0.375		dB
	Range		95		dB
Analog volume Control	Step		1		dB
	form -12dB to +3dB				dB

Note: all spec are testing at 10mW output, 16Ohms loading, 2.8V/1.2V duel power supply

Table 66 Line-in Amplifier Performance Characteristics

Parameter	Description	Min	Type	Max	Units
Dynamic Range	20Hz to 20kHz, -60dBFS input, A-Weighted(RMS)		90		dB
SNR	20Hz to 20kHz,A-Weighted, relative to full scale		90		dB
THD+N	At -1dBFS, 1kHz		70		dB
PSRR	100mVpp@AVDD,217kHz		75		dB
Volume Control Gain	Variable from -6dB to +14dB in 4 steps	-6		14	dB
Mute Attenuation			85		dB

Table 67 PMU Performance Characteristics

Parameter	Conditions	Min.	Type	Max.	Un
Input Voltage	Temp=-40 to +125	4.25	5	5.4	V
BUCK					
Output Accuracy	Vout=1.2v	-2		2	%
Line Regulation	△Vout/△Vin	-0.3		0.3	%/V
Load Regulation	△Vout/△Iout		0.0015		%/mA
Quiescent Current	Iload=0mA		80	100	uA
Shutdown Current	EN=GND		10		uA
Oscillator Frequency			3		MHz
Startup Time			400		us
Thermal Shutdown	Temp rising		125		℃
	Temp falling hys		10		℃
Output Voltage	Step=0.05V,default=1.2V	0.8		1.4	V
Adjust step			50		mV
Rated output current			100		mA
Conversion efficiency	PFM mode, output 1V, Iload= 6mA	80			%
	PFM mode, output 1V Iload = 20mA	85			%
	PWM mode, output 1.2V Iload = 100mA	80			%
LDO					
Quiescent Current	Iout=0uA		70		uA
	Iout=10mA		80		uA
	Iout=100mA		120		uA
Shutdown Current	EN=GND		0.1		uA
Output Accuracy	Vout=3.3v	-2		2	%
Line Regulation	△Vout/△Vin	-0.08		0.08	%/V
Load Regulation	△Vout/△Iout		0.005		%/mA
Dropout Voltage	Iout=10mA		40		mV
	Iout=80mA		300		mV
Startup Time			500		Us
Thermal Shutdown	Temp rising		125		℃
	Temp falling hys		10		℃
PSRR	1K,Vout=3.3v		70		dB
Output Voltage	Step=0.1V,default=3.0V	2.7		3.4	V
Adjust step			100		mV
Rated output current			100		mA
Charger					
Quiescent Current	Charge Mode		60		uA
	Standby Mode		20		uA
	Shutdown Mode		10		uA
Regulated Output Voltage	Ibat=20mA	4.15	4.2	4.25	V

BAT Pin Current	Charge Mode		200		mA
	Standby Mode, Vbat=4.2v		-5		uA
	Shutdown Mode		+/-2		uA
Trickle Charge Current			20		mA
Trickle Charge Threshold Voltage			2.9		V
Trickle Charge Hysteresis Voltage			100		mV
Recharge Threshold Voltage			4.05		V
Charge Termination Current Threshold			20		mA
Junction Temperature in Constant Temperature Mode			120		℃
Soft-Start Time			100		uS
Power FET Resistor			0.7		ohm
Power Path					
SwichRon Resistance	USB side		400		mohm
	Vbat side		200		mohm
Path Selection Threshold(USB-Vbat)	Select USB side		150		mV
	Select Vbat side hys		0		mV

7. Hardware Information

7.1 Oscillator Connection

RKnano will use two oscillators for input of on-chip PLLs , for USB PHY,which should be 24MHz， and for RTC should be 32.768KHz.

The design for oscillator pad has been optimized for stability and minimum jitter, and characterized to allow a variation of 10pF to 18pF on both XI and XO pins for crystal stability. In following Fig., the variation range for C value is 10pF to 18pF.

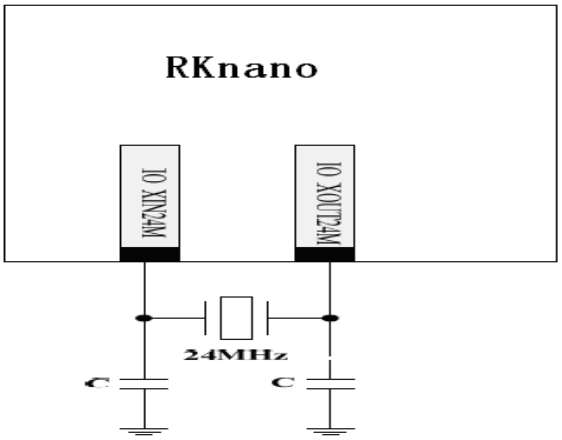


Fig. 71 external oscillator connection diagram

7.2 USB PHY Connection

USB2.0 OTG PHY is used in RKnano for USB OTG. The following figure shows external connection for USB PHY interface.

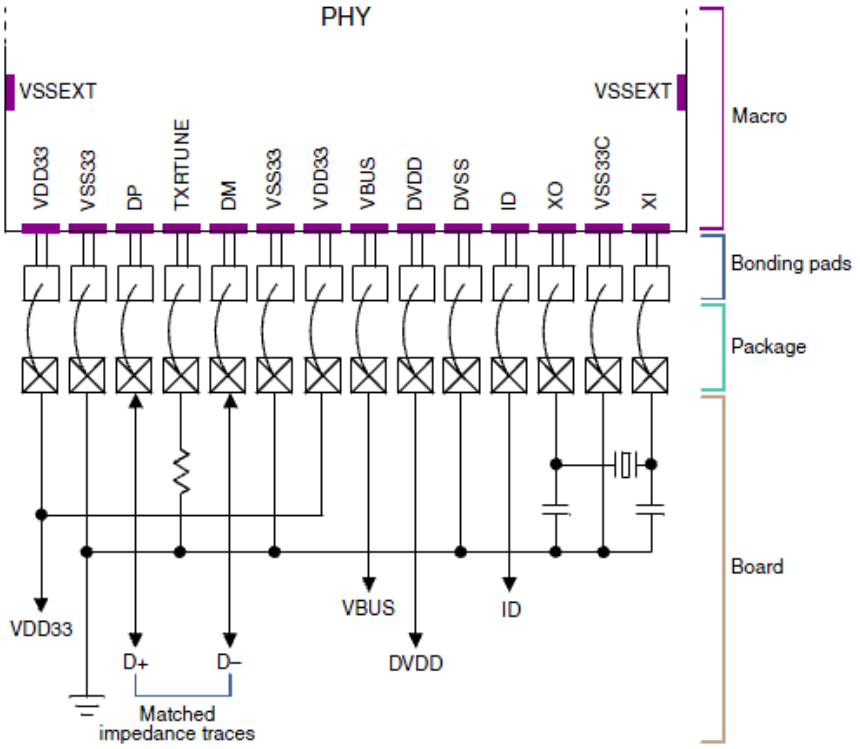


Fig. 72 RKnano USB PHY connection diagram

In the above diagram, some parameters and its viariant will be shown in the following table.

Design Implementation	Value
Macro size	1,037 µm x 759 µm (0.79 mm^2) This area does not include bondpads.
External resistor (REXT)	44.2 Ω (± 1%)
Analog power supply	3.3 V (+ 10%, – 7%) at the macro pins with respect to VSS33 and VSS33C
Digital power supply	1.2 V (+ 10%, – 7%) at the macro pins with respect to DVSS
Junction temperature	–40° C through +125° C

7.3 Power on & off Sequence

NORMAL POWER ON/OFF SEQUENCE

- When detect a press on PLAYON in off state, start the power on sequence.
- When receive the 'I_pd' signal from CPU, start the power down sequence.
- When the battery supply is too low (under 3.0V), force start the power down sequence, even no 'I_pd' signal.

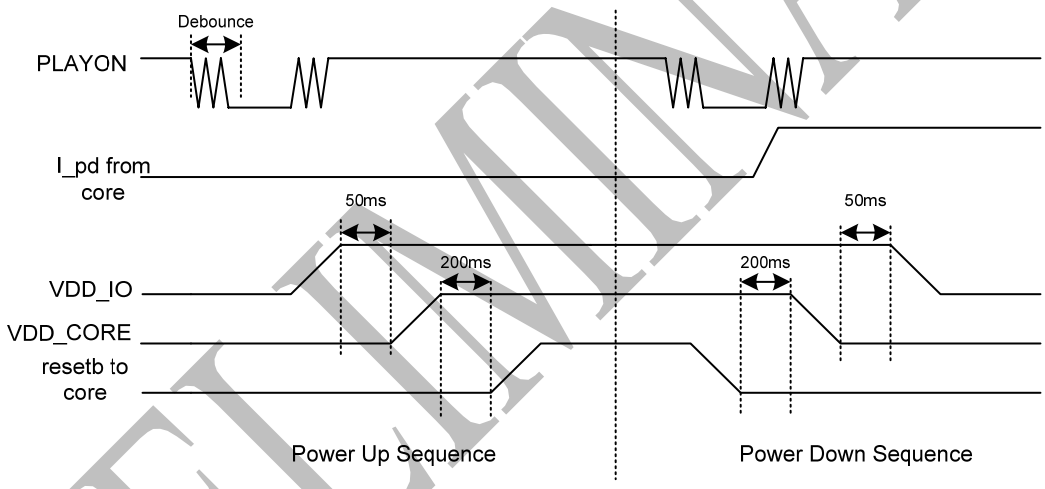


Fig. 73 Normal Power On/Off Sequence

ADAPTER PLUG IN POWER ON

- When an adapter plugging in detected in off state, start the power on sequence. Have no relationship with the 'PLAYON' signal.

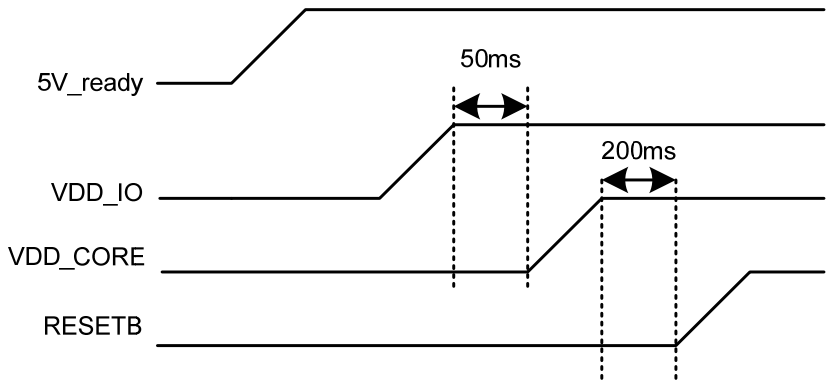


Fig. 74 Adapter Plug-In Power On Sequence

PROTECTED POWER OFF

- When an abnormal issue happens, we'll give out abnormal signals (oc, ot, ovp, uvp) and wait CPU to start a power off sequence.

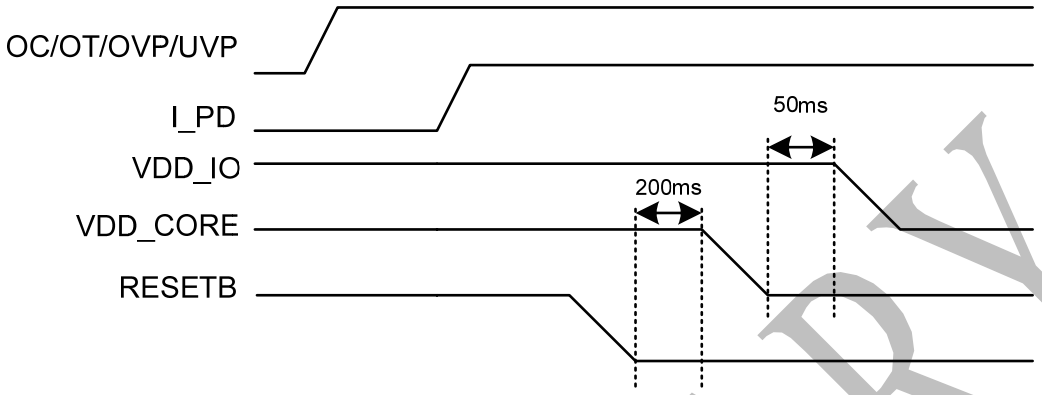


Fig. 75 Protected Power-off Sequence

LONG PRESS 'PLAYON' POWEROFF

- When a long press happened on 'PLAYON', the power down sequence will be triggered at the 8 seconds of the pressing.

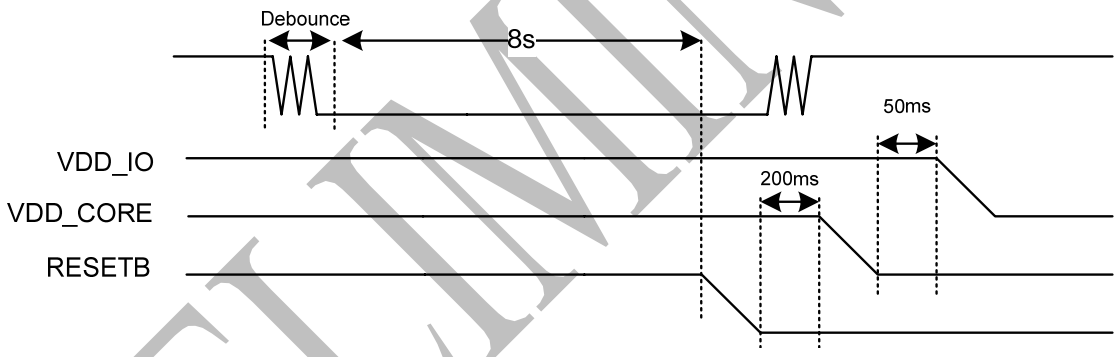
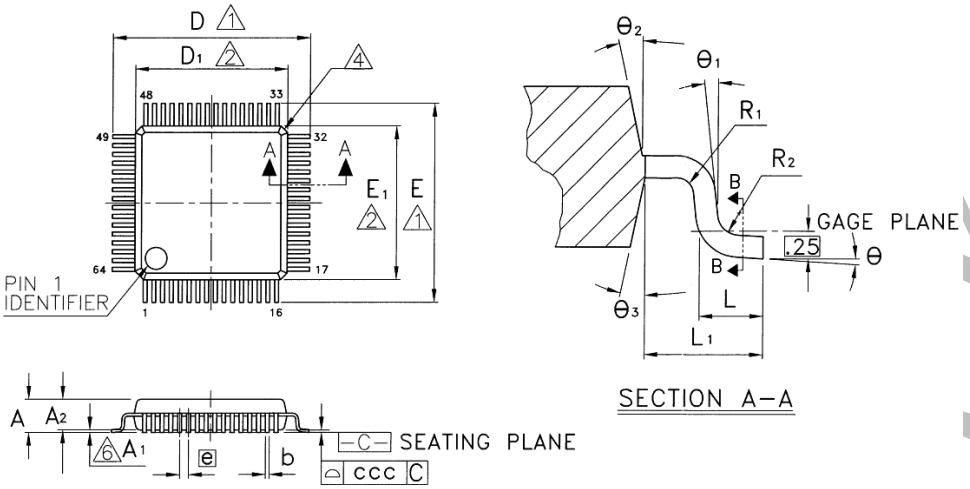


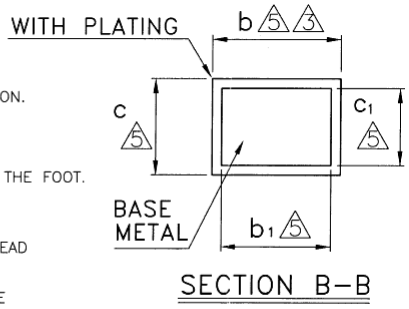
Fig. 76 Long-Press "PLAYON" Power-Off Sequence

8 Package Description

8.1 LQFP64 Package



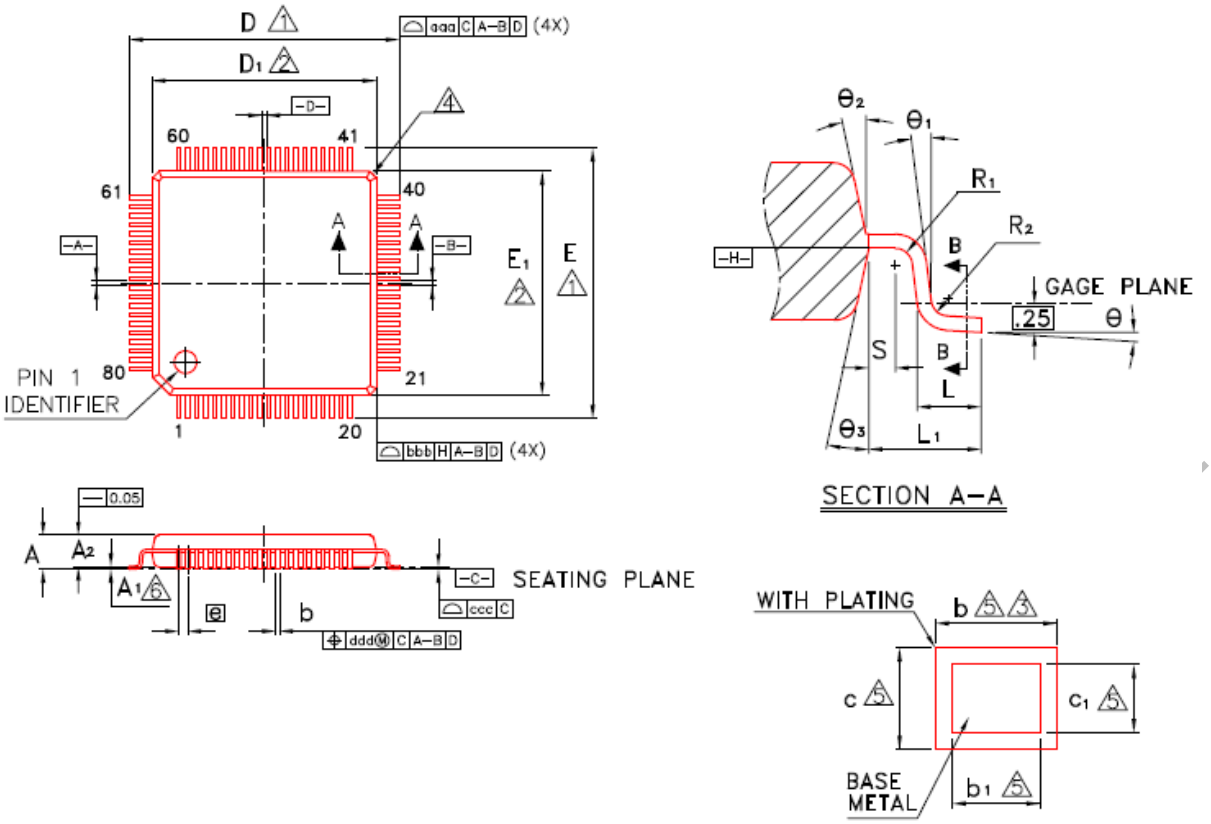
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		



NOTE :

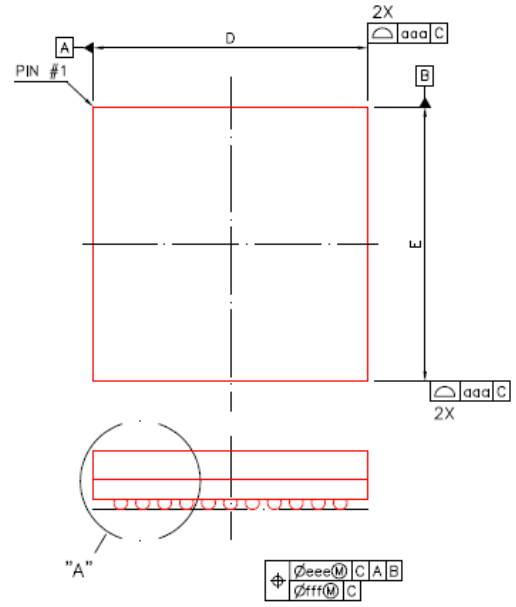
1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026

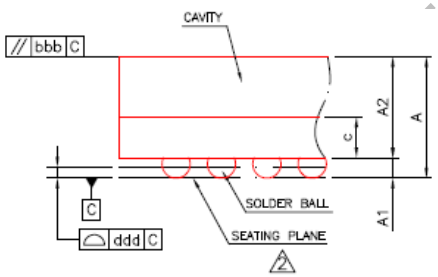
8.2 LQFP80 Package



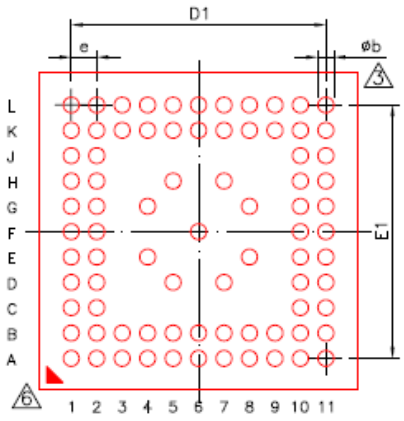
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

8.3 TFBGA81 Package





DETAIL : "A"



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.17	---	---	0.046
A1	0.13	0.18	0.23	0.005	0.007	0.009
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
D1	---	4.00	---	---	0.157	---
E1	---	4.00	---	---	0.157	---
e	---	0.40	---	---	0.016	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	11/11			11/11		