SONY

Diagonal 7.81 mm (Type 1/2.3) CMOS Image Sensor with Square Pixel for Color Cameras

IMX377CQT

Description

The IMX377CQT is a diagonal 7.81 mm (Type 1/2.3) CMOS image sensor with a color square pixel array and approximately 12.35 M effective pixels. 12-bit digital output makes it possible to output the signals of approximately 12.35 M effective pixels with high definition for shooting still pictures.
It also operates with three power supply voltages : analog 2.8 V, digital 1.2 V, and 1.8 V for I/O interface and achieves low power consumption.
Furthermore, it realizes 12-bit digital output for shooting high-speed and high-definition moving pictures by horizontal and vertical addition and subsampling. Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable integration time.
In addition, this product is designed for use in consumer use digital still camera and consumer use camcorder. When using this for another application, Sony does not guarantee the quality and reliability of the product.
Therefore, don't use this for applications other than consumer use digital still camera and consumer use camcorder.
In addition, individual specification change cannot be supported because this is a standard product.
Consult your Sony sales representative if you have any questions.

Features

- CMOS active pixel type pixels
- Input clock frequency 6 to 27 MHz
- MIPI Specifications (CSI-2 high-speed serial interface)
- All-pixel scan mode
  Horizontal/vertical 2/2-line binning mode
  Horizontal/vertical 3/3-line binning mode
  Vertical 1/3 subsampling horizontal 3 binning mode
  Vertical 1/3 subsampling horizontal 2/4 subsampling mode
  Vertical 2/9 subsampling binning horizontal 3 binning mode
  Vertical 2/9 subsampling binning horizontal 3 binning mode low power consumption
  Vertical 2/17 subsampling binning horizontal 3 binning mode
- High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- Vertical and horizontal arbitrary cropping function
- Variable-speed shutter function (minimum unit: 1 horizontal period)
- Low power consumption
- H driver, V driver and I^2C communication circuit on chip
- CDS/PGA on chip. Gain +27 dB (step pitch 0.1 dB)
- 10-bit/12-bit A/D conversion on chip
- R, G, B primary color mosaic filters on chip
- All-pixel simultaneous reset supported
- 98-pin high-precision ceramic package

Exmor R

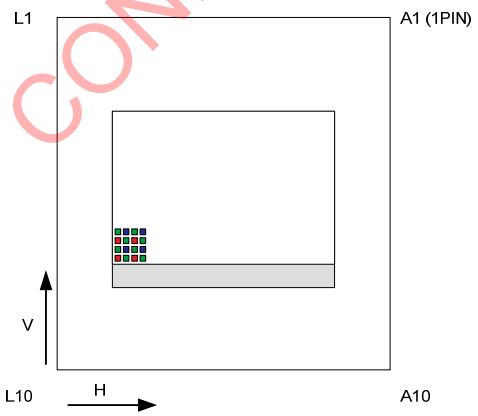
E15414A57

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 7.81 mm (Type 1/2.3)
- ◆Total number of pixels
  4152 (H) × 3062 (V) approx. 12.71 M pixels
- ◆Number of effective pixels
  - Type 1/2.3 approx. 12.35 M pixels use : 4056 (H) × 3046 (V) approx. 12.35 M pixels
  - Type 1/2.5 approx. 9.03 M pixels use : 4152 (H) × 2174 (V) approx. 9.03 M pixels
- ◆Number of active pixels
  - Type 1/2.3 approx. 12.35 M pixels use : 4024 (H) × 3036 (V) approx. 12.22 M pixels diagonal 7.81 mm
  - Type 1/2.5 approx. 9.03 M pixels use : 4120 (H) × 2168 (V) approx. 8.93 M pixels diagonal 7.22 mm
- ◆Number of recommended recording pixels
  - Type 1/2.3 approx. 12.35 M pixels use : 4000 (H) × 3000 (V) 12.00 M pixels aspect ratio 4:3
  - Type 1/2.5 approx. 9.03 M pixels use : 4096 (H) × 2160 (V) approx. 8.85 M pixels aspect ratio approx. 17:9
- ◆Chip size
  10.200 mm (H) × 8.000 mm (V) (include scribe area)
- ◆Unit cell size
  1.55 µm (H) × 1.55 µm (V)
- ◆Optical black
  Horizontal (H) direction : Front 0 pixels, rear 0 pixel
  Vertical (V) direction : Front 16 pixels, rear 0 pixel
- ◆Substrate material
  Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Optical Black Array and Readout Scan Direction

Absolute Maximum Ratings

◆ Supply voltage (Analog)	V_{ADD} *1	–0.3 to +3.3	V
◆ Supply voltage (Digital 1)	V_{DDD1} *2	–0.5 to +2.0	V
◆ Supply voltage (Digital 2)	V_{DDD2} *3	–0.5 to +3.3	V
◆ Input voltage (Digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
◆ Output voltage (Digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
◆ Guaranteed operating temperature	T_{OPR}	–10 to +75	˚C
◆ Storage guarantee temperature	T_{STG}	–30 to +80	˚C
◆ Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

◆ Supply voltage (Analog)	V_{ADD} *1	2.8 ± 0.1	V
◆ Supply voltage (Digital 1)	V_{DDD1} *2	1.2 ± 0.1	V
◆ Supply voltage (Digital 2)	V_{DDD2} *3	1.8 ± 0.1	V
◆ Input voltage (Digital)	V_I	–0.1 to V_{DDD2} + 0.1	V
◆ Output voltage (Digital)	V_O	–0.1 to V_{DDD2} + 0.1	V

*1 V_{ADD}: V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP (2.8 V power supply)
*2 V_{DDD1}: V_{DD}LCN1 to 2, V_{DD}LSC1 to 2, V_{DD}LPL1 to 3, V_{DD}LIF1 to 2 (1.2 V power supply)
*3 V_{DDD2}: V_{DD}MIO (1.8 V power supply)

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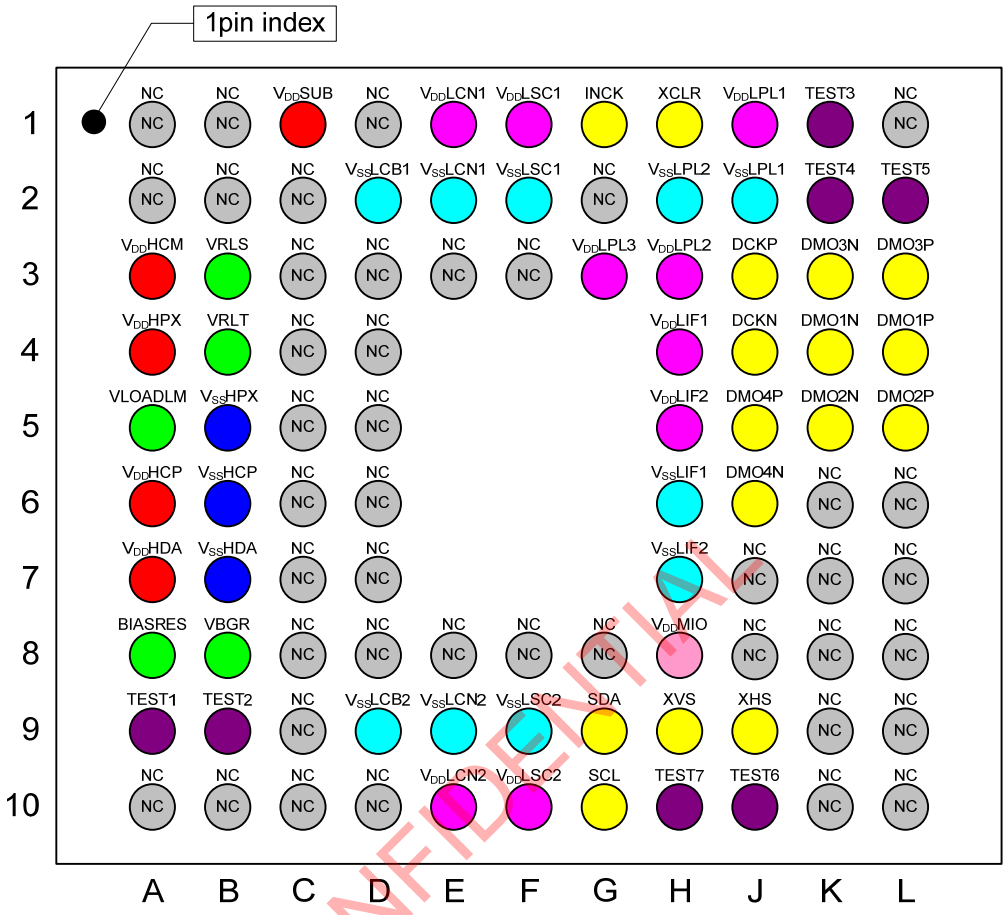
General-0.0.8

Contents

Pin Configuration

(Bottom View)



Pin Configuration

Pin Description

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
A3	V_{DD}HCM	Power	A	Analog power supply (2.8 V)	—	
A4	V_{DD}HPX	Power	A	Analog power supply (2.8 V)	—	
A5	VLOADLM	O	A	Capacitor connection		Leave open. (No connection)
A6	V_{DD}HCP	Power	A	Analog power supply (2.8 V)	—	
A7	V_{DD}HDA	Power	A	Analog power supply (2.8 V)	—	
A8	BIASRES	O	A	Resistor connection		Leave open. (No connection)
A9	TEST1	I	D	Test		Leave open. (No connection)
B3	VRLS	O	A	Capacitor connection	Pull-down	
B4	VRLT	O	A	Capacitor connection	Pull-down	
B5	V_{SS}HPX	GND	A	Analog GND (2.8 V)	—	
B6	V_{SS}HCP	GND	A	Analog GND (2.8 V)	—	
B7	V_{SS}HDA	GND	A	Analog GND (2.8 V)	—	
B8	VBGR	O	A	Capacitor connection		Leave open. (No connection)
B9	TEST2	I	D	Test		Leave open. (No connection)
C1	V_{DD}SUB	Power	A	Analog power supply (2.8 V)	—	
D2	V_{SS}LCB1	GND	D	Digital GND (1.2 V)	—	
D9	V_{SS}LCB2	GND	D	Digital GND (1.2 V)	—	
E1	V_{DD}LCN1	Power	D	Digital power supply (1.2 V)	—	
E2	V_{SS}LCN1	GND	D	Digital GND (1.2 V)	—	
E9	V_{SS}LCN2	GND	D	Digital GND (1.2 V)	—	
E10	V_{DD}LCN2	Power	D	Digital power supply (1.2 V)	—	
F1	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
F2	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
F9	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
F10	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
G1	INCK	I	D	Input clock	—	
G3	V_{DD}LPL3	Power	D	Digital power supply (1.2 V)	—	
G9	SDA	I	D	I^2C communication data input	—	
G10	SCL	I	D	I^2C communication clock input	—	
H1	XCLR	I	D	Reset pulse input	—	
H2	V_{SS}LPL2	GND	D	Digital GND (1.2 V)	—	
H3	V_{DD}LPL2	Power	D	Digital power supply (1.2 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
H4	V_{DD}LIF1	Power	D	Digital MIPI power supply (1.2 V)	—	
H5	V_{DD}LIF2	Power	D	Digital MIPI power supply (1.2 V)	—	
H6	V_{SS}LIF1	GND	D	Digital MIPI GND (1.2 V)	—	
H7	V_{SS}LIF2	GND	D	Digital MIPI GND (1.2 V)	—	
H8	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
H9	XVS	O	D	Vertical sync signal output	—	If unused XVS, leave open. (No connection)
H10	TEST7	O	D	Test		Leave open. (No connection)
J1	V_{DD}LPL1	Power	D	Digital power supply (1.2 V)	—	
J2	V_{SS}LPL1	GND	D	Digital GND (1.2 V)	—	
J3	DCKP	O	D	Digital MIPI output	Low Level	Clock Lane connection.
J4	DCKN	O	D	Digital MIPI output	Low Level	Clock Lane connection.
J5	DMO4P	O	D	Digital MIPI output	Low Level	Data Lane 4 connection.
J6	DMO4N	O	D	Digital MIPI output	Low Level	Data Lane 4 connection.
J9	XHS	O	D	Horizontal sync signal output	—	If unused XHS, leave open. (No connection)
J10	TEST6	I	D	Test		Connect with either of V_{DD}MIO.
K1	TEST3	O	D	Test		Leave open. (No connection)
K2	TEST4	O	A	Test		Leave open. (No connection)
K3	DMO3N	O	D	Digital MIPI output	Low Level	Data Lane 3 connection.
K4	DMO1N	O	D	Digital MIPI output	Low Level	Data Lane 1 connection.
K5	DMO2N	O	D	Digital MIPI output	Low Level	Data Lane 2 connection.
L2	TEST5	O	A	Test		Leave open. (No connection)
L3	DMO3P	O	D	Digital MIPI output	Low Level	Data Lane 3 connection.
L4	DMO1P	O	D	Digital MIPI output	Low Level	Data Lane 1 connection.
L5	DMO2P	O	D	Digital MIPI output	Low Level	Data Lane 2 connection.

Electrical Characteristics

Electrical characteristics of the IMX377CQT are shown below.

1. DC Characteristics

Current Consumption and Gain Variable Range

(V_{ADD} = 2.9 V, V_{DDD1} = 1.3 V, V_{DDD2} = 1.9 V, Tj = 60 ˚C, Reference Gain (0 dB), approximately 12.35 M pixels readout (MODE0), 34.97 frame/s)

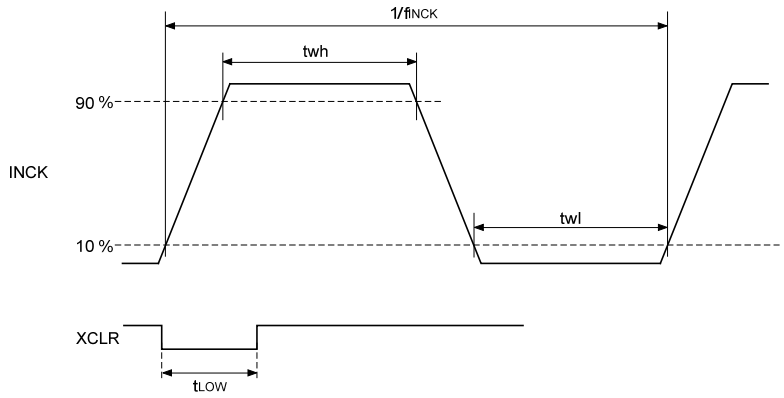
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	91	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	256	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	1	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	150	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	40	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	50	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP	V_{ADD}	2.70	2.80	2.90	V
	Digital 1	V_{DD}LCN1 to 2, V_{DD}LSC1 to 2, V_{DD}LPL1 to 3, V_{DD}LIF1 to 2	V_{DDD1}	1.10	1.20	1.30	V
	Digital 2	V_{DD}MIO	V_{DDD2}	1.70	1.80	1.90	V
Digital input voltage		SDA, SCL	V_{IH1}	0.7 × V_{DDD2}	—	1.9	V
			V_{IL1}	–0.3	—	0.3 × V_{DDD2}	V
		XCLR, INCK	V_{IH2}	0.65 × V_{DDD2}	—	V_{DDD2} + 0.3	V
			V_{IL2}	–0.3	—	0.35 × V_{DDD2}	V

2. AC Characteristics

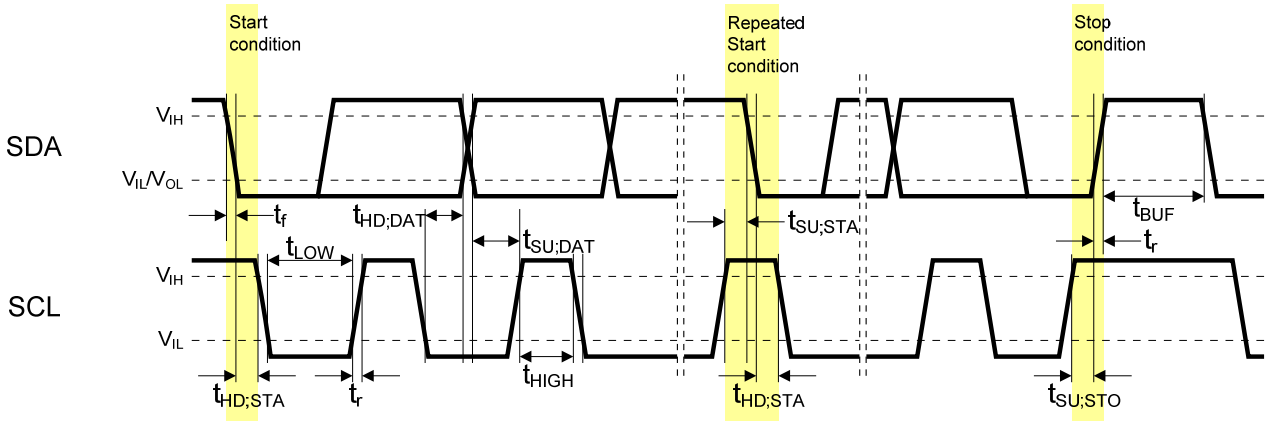
INCK, XCLR



INCK, XCLR AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	6	—	27	MHz
INCK Low level pulse width	twl	5	—	—	ns
INCK High level pulse width	twh	5	—	—	ns
Clock duty	—	40	50	60	%
XCLR Low level pulse width	t_{LOW}	100	—	—	ns

I²C Communication



I²C Communication Characteristics

I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × V_{DDD2}	V	
High level input voltage	V_{IH}	0.7 × V_{DDD2}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × V_{DDD2}	V	V_{DDD2} < 2 V,Sink 3 mA
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × V_{DDD2} to 0.3 × V_{DDD2}
Input current	Ii	-10	—	10	μA	0.1 × V_{DDD2} to 0.9 × V_{DDD2}
Input capacitance of SCL / SDA	Ci	—	—	10	pF	

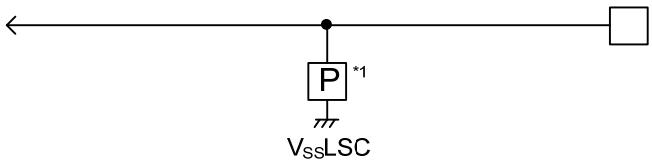
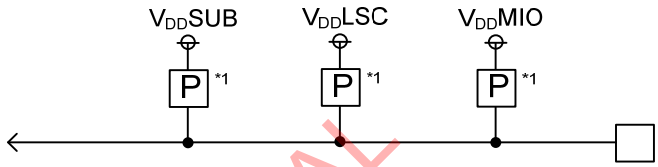
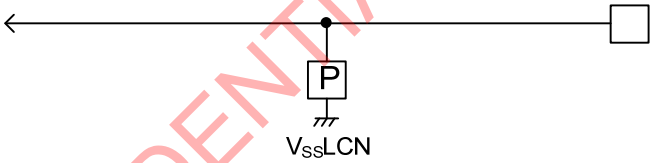
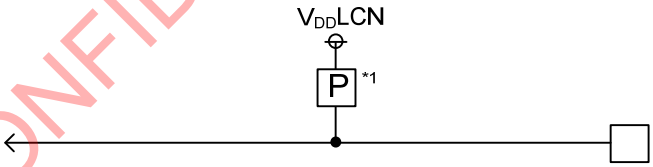
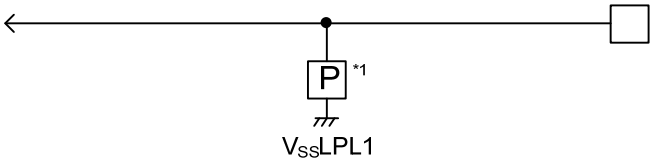
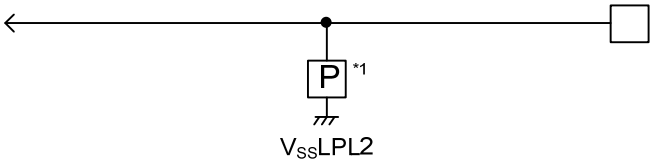
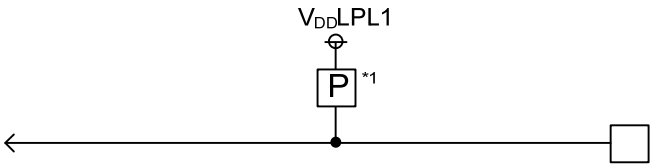
I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs

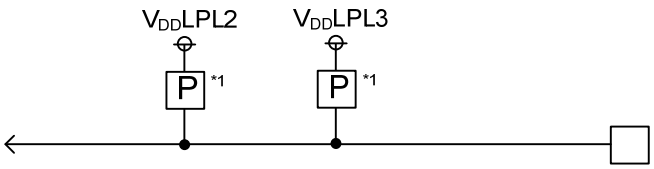
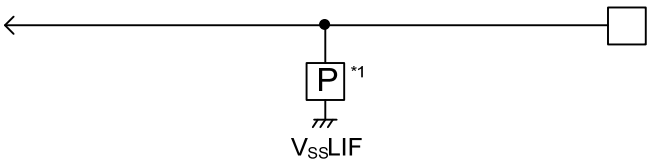
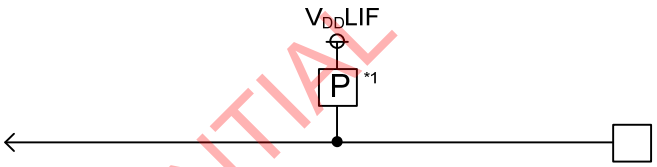
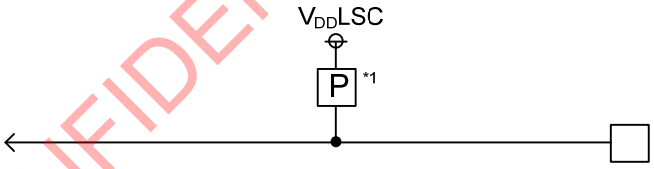
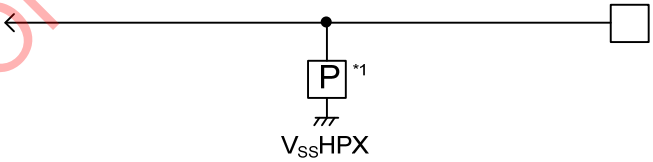
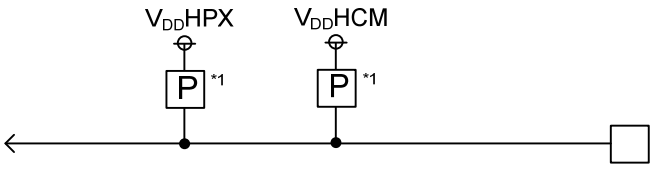
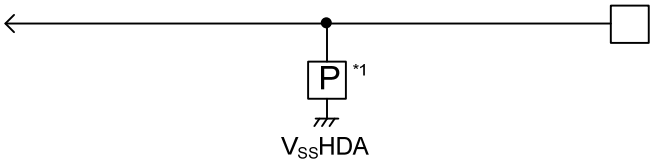
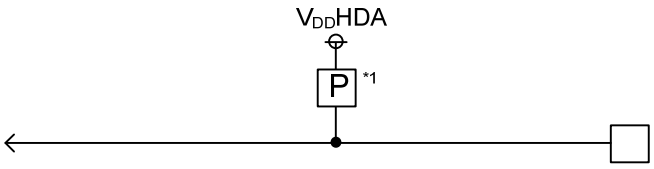
DCKP / DCKN,DMO

Detailed explanation of CSI-2 interface is in following two documents, "MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.1" and "MIPI Alliance Specification for D-PHY Version 1.1".
Four data output Lanes are applied from MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.1.

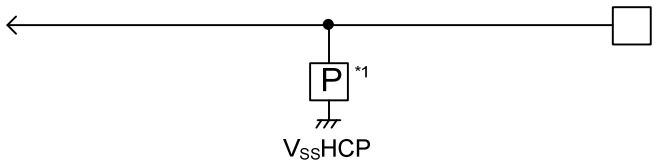
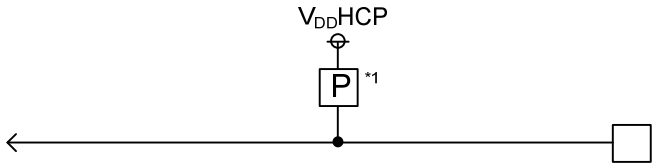
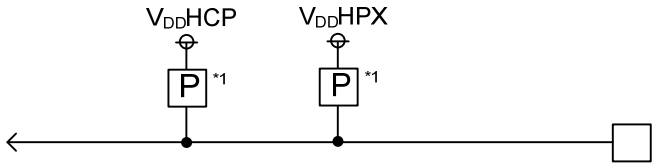
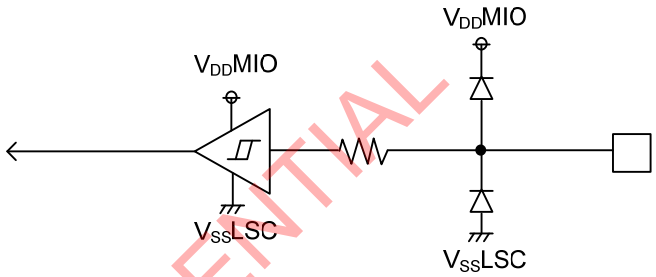
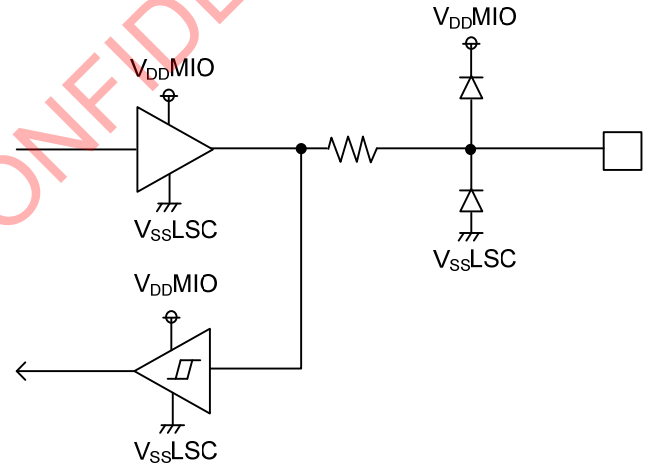
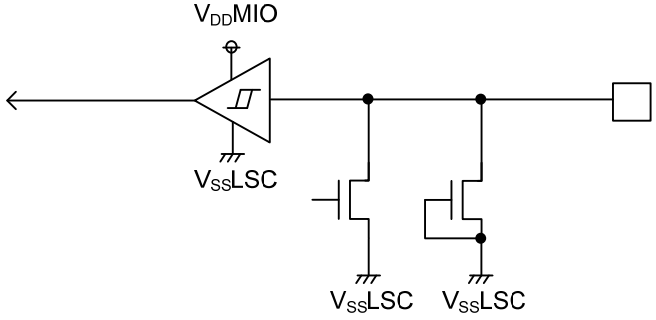
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
V_{DD}LSC1 to 2 V_{DD}MIO V_{DD}SUB	V_{DD}LSC1 to 2 are internally connected. 
V_{SS}LSC1 to 2	V_{SS}LSC1 to 2 are internally connected. 
V_{DD}LCN1 to 2	
V_{SS}LCN1 to 2	
V_{DD}LPL1	
V_{DD}LPL2 to 3	
V_{SS}LPL1	

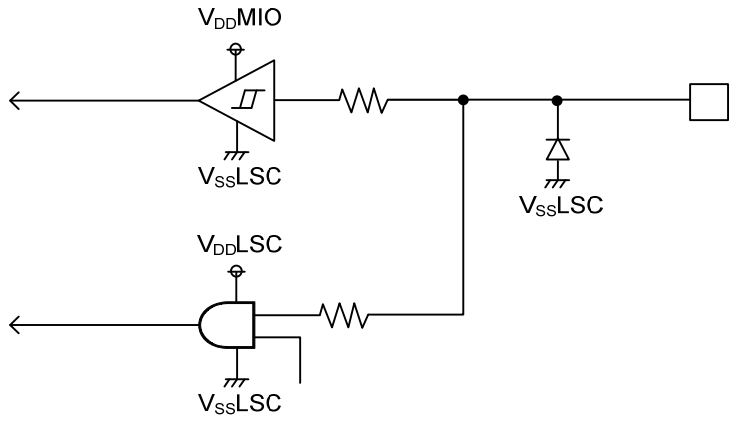
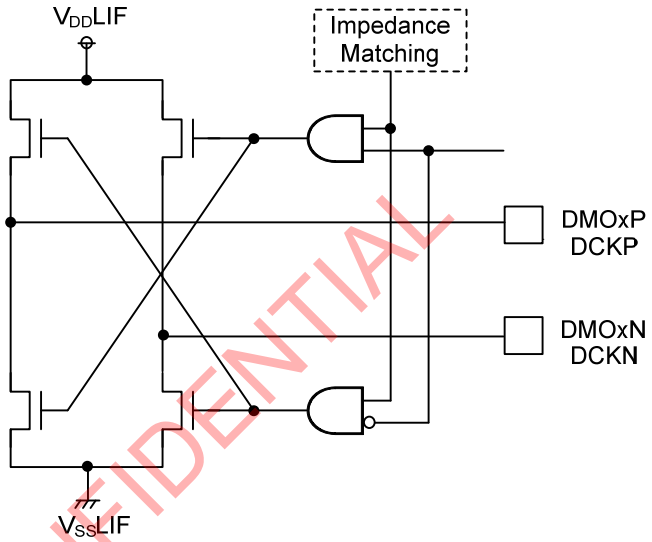
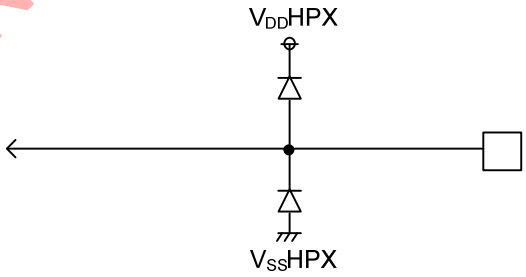
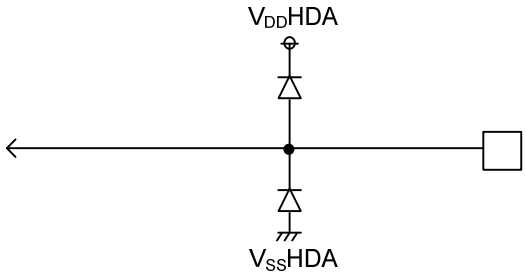
☐External pins

Symbol	Equivalent circuit
V_{SS}LPL2	
V_{DD}LIF1 to 2	V_{DD}LIF1 to 2 are internally connected. 
V_{SS}LIF1 to 2	V_{SS}LIF1 to 2 are internally connected. 
V_{SS}LCB1 to 2	
V_{DD}HPX V_{DD}HCM	
V_{SS}HPX	
V_{DD}HDA	
V_{SS}HDA	

☐External pins

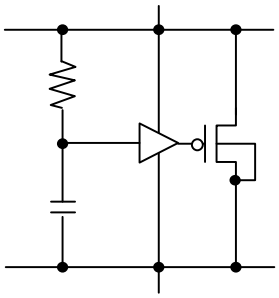
Symbol	Equivalent circuit
V_{DD}HCP	
V_{SS}HCP	
VRLT VRLS	
INCK	
XVS XHS	
SDA SCL	

☐External pins

Symbol	Equivalent circuit
XCLR	
DMOxP (x = 1 to 4) DMOxN (x = 1 to 4) DCKP DCKN	
VLOADLM	
BIASRES VBGR	

☐External pins

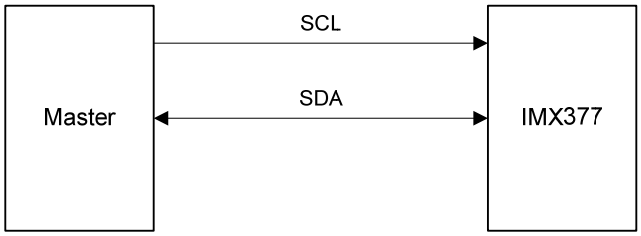
Description of special symbol

Symbol	Equivalent circuit
P *1	

Setting Registers Using I²C Communication

Description of Setting Registers

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R / W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

Pin Connection of Serial Communication Operation Specifications

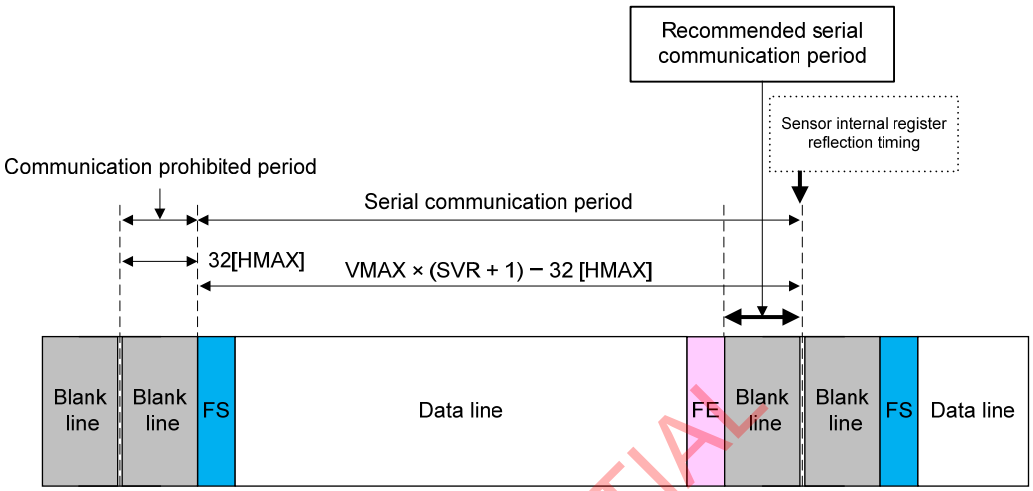
The pin connection of serial communication method conforms to the Camera Control Instance (CCI). CCI is an I²C fast-mode compatible interface, and the data transfer protocol is I²C standard.
This pin connection of serial communication circuit can be used to access the control-registers and status-registers of IMX377CQT.

I²C pin description

Symbol	Pin No.	Remarks
SCL	G10	Serial clock input
SDA	G9	Serial data communication

Register Communication Timing

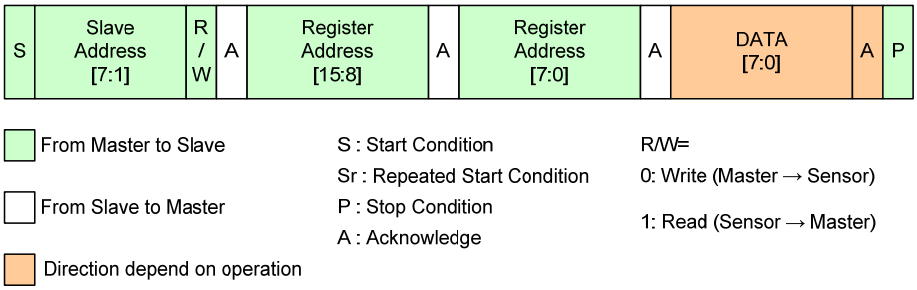
In I^2C communication system, register setting can be performed during the period when communication is from the following figure “VMAX × (SVR + 1) − 32[HMAX]”.
Perform I^2C communication within “FS of next frame − 32[HMAX]” period (recommended serial communication period) after FE period end to prevent noise. However, for non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), then register communication can be performed other than during the recommended serial communication period of those frames.



Register Communication Timing

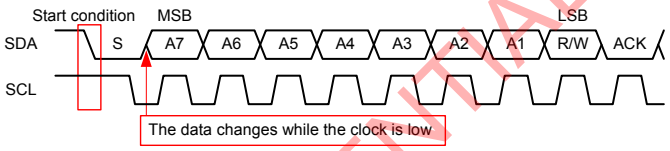
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

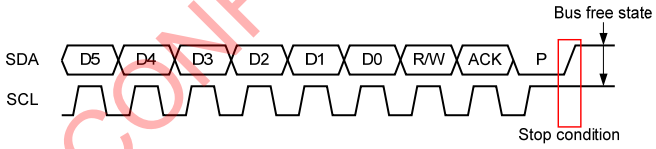


I²C Communication Protocol

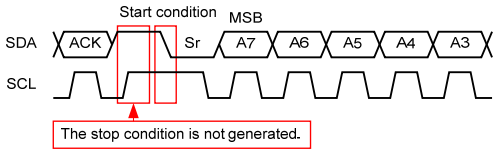
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) is transferred. Data is transferred at the clock cycle of SCL. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

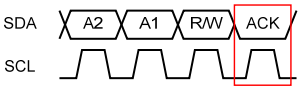


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge and release (does not drive) SDA.



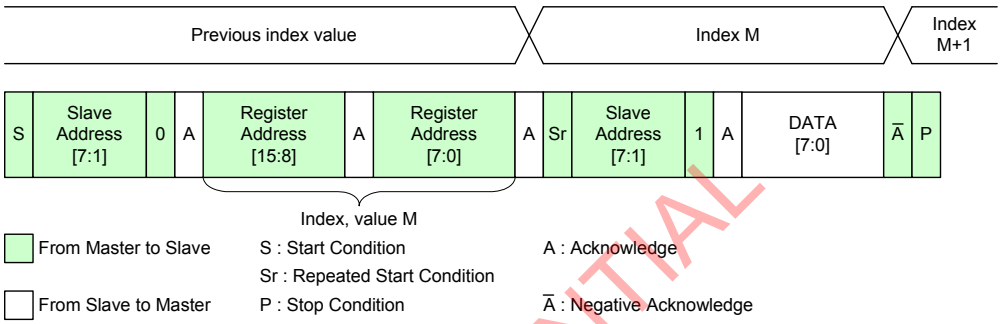
Acknowledge

Register Write and Read

This sensor supports to four read operations and two write operations.
In addition, INCK signal must be driven during the I^2C serial communication period.

Single Read from Random Location

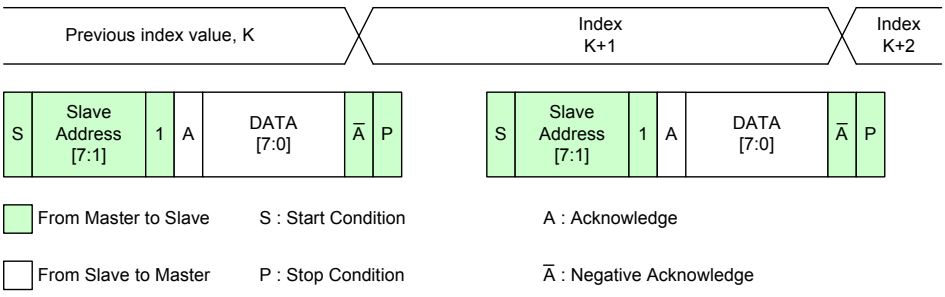
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data,it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

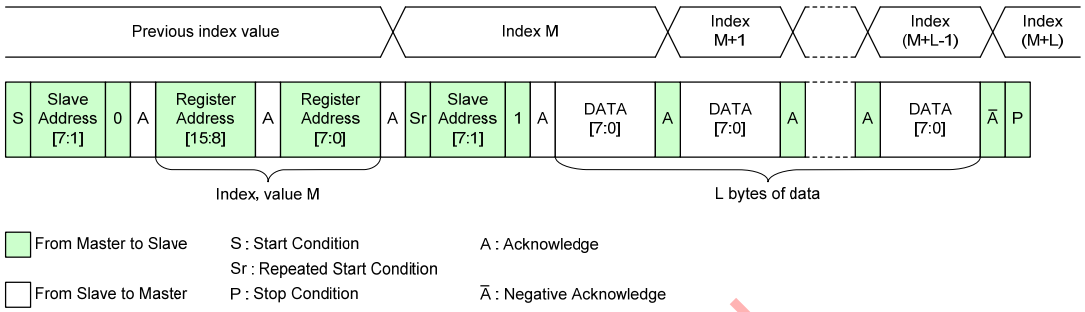
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

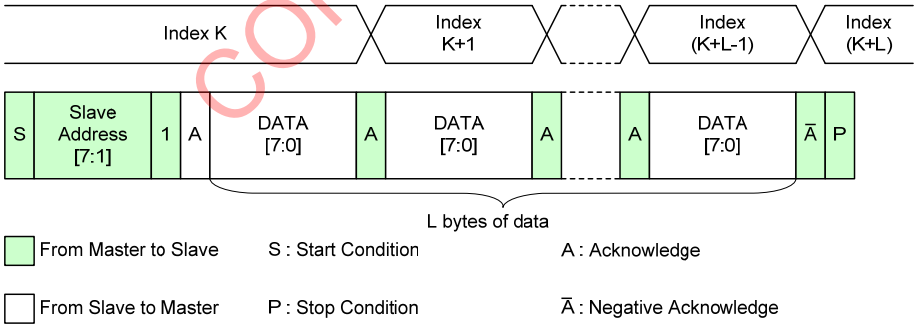
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

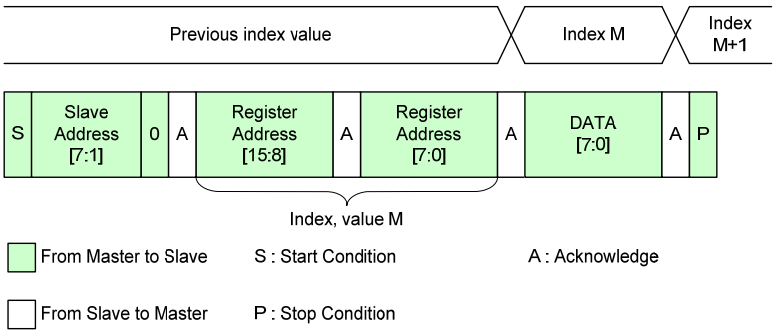
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

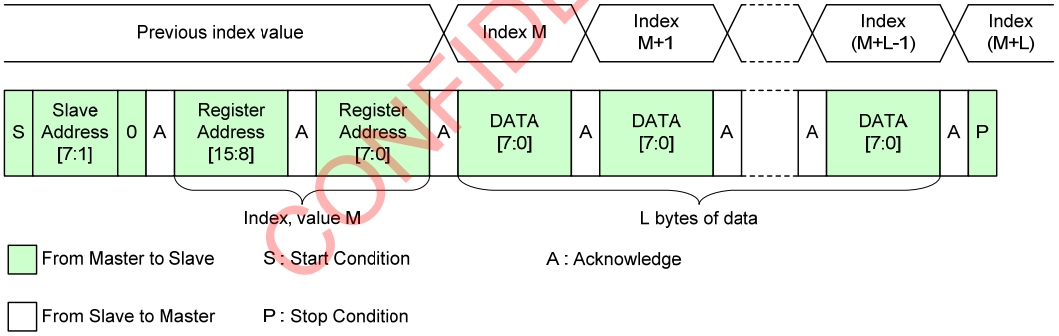
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

The register map is given below.

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3000h	[0]	1h	Immediately	STANDBY	0h : Normal operation 1h : Overall standby	Setting range: 0h to 1h
	[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communication block	Setting range: 0h to 1h
	[2]	0h	Immediately	PLSTMG01	Drive pulse timing setting 01	Set to 1h
	[3]	0h	Immediately	STBMIPI	0h: Normal operation 1h: CSI-2 standby	Setting range: 0h to 1h
	[4]	1h	Immediately	STBDV	0h: Normal operation 1h: Frequency demultiplier standby	Setting range: 0h to 1h
	[7:5]	0h			—	Set the default value.
3001h	[3:0]	0h			—	Set the default value.
	[4]	0h	1st frame after communication ends*1	CLPSQRST	When changing form 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
	[7:5]	0h			—	Set the default value.
3003h	[7:0]	40h	*1	PLSTMG02	Drive pulse timing setting 02	Set to 20h
3004h	[7:0]	45h	*1	MDSEL1		Set the value according to each readout mode register setting.
3005h	[7:0]	35h	*1	MDSEL2		Set the value according to each readout mode register setting.
3006h	[7:0]	00h	*1	MDSEL3		Set the value according to each readout mode register setting.
3007h	[7:0]	00h	*1	MDSEL4		Set the value according to each readout mode register setting.
3008h	[0]	0h	*1	SMD	0h: Rolling shutter 1h: Global reset shutter	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
3009h	[7:0]	000h	*1	PGC	Analog gain setting	Setting range: 000h to 7A5h
300Ah	[2:0]					
	[7:3]	00h			—	Set the default value.
300Bh	[7:0]	0007h	2nd frame after communication ends*2	SHR	Specifies the integration start horizontal period	Setting range is shown in ”Description of Registers”
300Ch	[7:0]					
300Dh	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0000h to FFFFh
300Eh	[7:0]					
3011h	[1:0]	0h	*1	DGAIN	Digital gain setting 0h: 0 dB gain setting value 1h: +6 dB gain setting value 2h: +12 dB gain setting value 3h: +18 dB gain setting value	Setting range: 0h to 3h
	[7:2]	00h			—	Set the default value.
3018h	[1:0]	3h	Immediately	SYNCDRV	Internal setting register	Refer to the ”Standby Cancel Sequence”
	[7:2]	28h			—	Set the default value.
301Ah	[0]	0h	*1	MDVREV	0h : Vertical direction normal readout 1h : Vertical direction inversion readout	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
302Dh	[0]	0h	Immediately	REGHOLD	Register setting hold function	Setting range is shown in ”Description of Registers”
	[7:1]	00h			—	Set the default value.

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3039h	[7:0]	0000h	*1	HTRIMMING_ END	Horizontal cropping end position + 1	Setting range is shown in ”Description of Registers”
303Ah	[4:0]					
	[7:5]	0h			—	Set the default value.
303Eh	[7:0]	0000h	*1	HTRIMMING_ START	Horizontal cropping start position	Setting range is shown in ”Description of Registers”
303Fh	[4:0]					
	[7:5]	0h			—	Set the default value.
3040h	[0]	0h	*1	HTRIMMING_ EN	Horizontal arbitrary cropping enable	Setting range is shown in ”Description of Registers”
	[7:1]	00h			—	Set the default value.
3045h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 0h to FFh 10-bit readout mode: 1 digit/1h 12-bit readout mode: 4 digit/1h
304Eh	[7:0]	00h	*1	PLSTMG31	Drive pulse timing setting 31	Set to 02h
3057h	[7:0]	47h	Immediately	PLSTMG22	Drive pulse timing setting 22	Set to 4Ah
3058h	[7:0]	0E8h	Immediately	PLSTMG23	Drive pulse timing setting 23	Set to 0F6h
3059h	[1:0]					
	[7:2]	00h			—	Set the default value.
3068h	[7:0]	00h	*1	MDSEL7		Set the value according to each readout mode register setting.
306Bh	[7:0]	07h	Immediately	PLSTMG24	Drive pulse timing setting 24	Set to 04h
307Eh	[7:0]	0000h	*1	MDSEL5		Set the value according to each readout mode register setting.
307Fh	[7:0]					
3080h	[7:0]	0000h	Immediately	MDPLS01		Set the value according to each readout mode register setting.
3081h	[7:0]					
3082h	[7:0]	0000h	Immediately	MDPLS02		Set the value according to each readout mode register setting.
3083h	[7:0]					
3084h	[7:0]	0000h	Immediately	MDPLS03		Set the value according to each readout mode register setting.
3085h	[7:0]					
3086h	[7:0]	0000h	Immediately	MDPLS04		Set the value according to each readout mode register setting.
3087h	[7:0]					
3095h	[7:0]	0000h	Immediately	MDPLS05		Set the value according to each readout mode register setting.
3096h	[7:0]					
3097h	[7:0]	0000h	Immediately	MDPLS06		Set the value according to each readout mode register setting.
3098h	[7:0]					
3099h	[7:0]	0000h	Immediately	MDPLS07		Set the value according to each readout mode register setting.
309Ah	[7:0]					
309Bh	[7:0]	0000h	Immediately	MDPLS08		Set the value according to each readout mode register setting.
309Ch	[7:0]					
30BCh	[7:0]	0000h	Immediately	MDPLS40		Set the value according to each readout mode register setting.
30BDh	[7:0]					
30BEh	[7:0]	0000h	Immediately	MDPLS41		Set the value according to each readout mode register setting.
30BFh	[7:0]					
30C0h	[7:0]	0000h	Immediately	MDPLS42		Set the value according to each readout mode register setting.
30C1h	[7:0]					
30C2h	[7:0]	0000h	Immediately	MDPLS43		Set the value according to each readout mode register setting.
30C3h	[7:0]					
30C4h	[7:0]	0000h	Immediately	MDPLS44		Set the value according to each readout mode register setting.
30C5h	[7:0]					
30C6h	[7:0]	0000h	Immediately	MDPLS45		Set the value according to each readout mode register setting.
30C7h	[7:0]					
30C8h	[7:0]	0000h	Immediately	MDPLS46		Set the value according to each readout mode register setting.
30C9h	[7:0]					
30CAh	[7:0]	0000h	Immediately	MDPLS47		Set the value according to each readout mode register setting.
30CBh	[7:0]					
30CCh	[7:0]	00h	Immediately	MDPLS48		Set the value according to each readout mode register setting.
30D0h	[7:0]	1008h	*1	MDPLS52		Set the value according to each readout mode register setting.
30D1h	[7:0]					

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
30D5h	[0]	0h	*1	VWIDCUTEN	Vertical arbitrary cropping enable	Setting range is shown in ”Description of Registers”
	[7:1]	00h			—	Set the default value.
30D6h	[7:0]	000h	*1	VWIDCUT	Width of vertical arbitrary cropping	Setting range is shown in ”Description of Registers”
30D7h	[2:0]					
	[7:3]	00h			—	Set the default value.
30D8h	[7:0]	000h	*1	VWINPOS	Start position of vertical arbitrary cropping (two's complement)	Setting range is shown in ”Description of Registers”
30D9h	[3:0]					
	[7:4]	0h			—	Set the default value.
30DAh	[7:0]	00h	*1	MDREG01		Set the value according to each readout mode register setting.
30EEh	[7:0]	01h	*1	MDREG02		Set the value according to each readout mode register setting.
30F4h	[0]	1h	Immediately	XMSTA	Master mode operation 0h: Master mode start 1h: Master mode stop	Refer to the ”Standby Cancel Sequence”
	[7:1]	00h			—	Set the default value.
30F5h	[7:0]	0172h	*1	HMAX	Horizontal drive period length	Setting range is shown in ”Description of Registers”
30F6h	[7:0]					
30F7h	[7:0]	00CB2h	*1	VMAX	Vertical drive period length	Setting range is shown in ”Description of Registers”
30F8h	[7:0]					
30F9h	[3:0]					
	[7:4]	0h			—	Set the default value.
310Bh	[0]	1h	Immediately	STBPL_IF	PLL standby control register for IF	Refer to the ”Standby Cancel Sequence”
	[3:1]	0h			—	Set the default value.
	[4]	1h	Immediately	STBPL_AD	PLL standby control register for AD	Refer to the ”Standby Cancel Sequence”
	[7:5]	0h			—	Set the default value.
3120h	[7:0]	0010h	Immediately	PLRD1	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3121h	[7:0]					
3122h	[7:0]	00h	Immediately	PLRD3	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3123h	[7:0]	01h	Immediately	PLRD10	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3124h	[7:0]	01h	Immediately	PLRD11	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3125h	[7:0]	00h	Immediately	PLRD12	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3127h	[7:0]	07h	Immediately	PLRD13	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3129h	[7:0]	0Dh	Immediately	PLRD2	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
312Ah	[7:0]	00h	Immediately	PLRD4	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
312Dh	[7:0]	03h	Immediately	PLRD14	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
312Fh	[7:0]	03FEh	*1	MDSEL9		Set the value according to each readout mode register setting.
3130h	[4:0]					
	[7:5]	0h			—	Set the default value.
3131h	[7:0]	03FAh	*1	MDSEL10		Set the value according to each readout mode register setting.
3132h	[4:0]					
	[7:5]	0h			—	Set the default value.
3145h	[1:0]	1h	Immediately	PLSTMG04	Drive pulse timing setting 04	Set to 0h
	[7:2]	00h			—	Set the default value.
3202h	[7:0]	066h	Immediately	PLSTMG25	Drive pulse timing setting 25	Set to 063h
3203h	[0]					
	[7:1]	00h			—	Set the default value.
3236h	[7:0]	067h	Immediately	PLSTMG26	Drive pulse timing setting 26	Set to 064h
3237h	[0]					
	[7:1]	00h			—	Set the default value.

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3304h	[7:0]	005h	Immediately	PLSTMG32	Drive pulse timing setting 32	Set to 00Bh
3305h	[3:0]					
	[7:4]	0h			—	Set the default value.
3306h	[7:0]	005h	Immediately	PLSTMG33	Drive pulse timing setting 33	Set to 00Bh
3307h	[3:0]					
	[7:4]	0h			—	Set the default value.
337Fh	[7:0]	067h	Immediately	PLSTMG27	Drive pulse timing setting 27	Set to 064h
3380h	[0]					
	[7:1]	00h			—	Set the default value.
338Dh	[7:0]	067h	Immediately	PLSTMG28	Drive pulse timing setting 28	Set to 064h
338Eh	[0]					
	[7:1]	00h			—	Set the default value.
3399h	[7:0]	00h	Immediately	LMRSVRG	Internal setting register	Refer to the ”Standby Cancel Sequence”
3510h	[7:0]	054h	Immediately	PLSTMG05	Drive pulse timing setting 05	Set to 072h
3511h	[0]					
	[7:1]	00h			—	Set the default value.
3528h	[7:0]	0Eh	Immediately	PLSTMG06	Drive pulse timing setting 06	Set to 0Fh
3529h	[7:0]	0Eh	Immediately	PLSTMG07	Drive pulse timing setting 07	Set to 0Fh
352Ah	[7:0]	0Eh	Immediately	PLSTMG08	Drive pulse timing setting 08	Set to 0Fh
352Bh	[7:0]	0Eh	Immediately	PLSTMG09	Drive pulse timing setting 09	Set to 0Fh
3538h	[7:0]	0Eh	Immediately	PLSTMG10	Drive pulse timing setting 10	Set to 0Fh
3539h	[7:0]	0Eh	Immediately	PLSTMG11	Drive pulse timing setting 11	Set to 13h
353Ch	[7:0]	04h	Immediately	PLSTMG13	Drive pulse timing setting 13	Set to 01h
3553h	[7:0]	1Fh	Immediately	PLSTMG34	Drive pulse timing setting 34	Set to 00h
3554h	[7:0]	1Fh	Immediately	PLSTMG35	Drive pulse timing setting 35	Set to 00h
3555h	[7:0]	1Fh	Immediately	PLSTMG36	Drive pulse timing setting 36	Set to 00h
3556h	[7:0]	1Fh	Immediately	PLSTMG37	Drive pulse timing setting 37	Set to 00h
3557h	[7:0]	1Eh	Immediately	PLSTMG38	Drive pulse timing setting 38	Set to 00h
3558h	[7:0]	1Dh	Immediately	PLSTMG39	Drive pulse timing setting 39	Set to 00h
3559h	[7:0]	1Dh	Immediately	PLSTMG40	Drive pulse timing setting 40	Set to 00h
355Ah	[7:0]	1Ah	Immediately	PLSTMG41	Drive pulse timing setting 41	Set to 00h
357Dh	[7:0]	0Ch	Immediately	PLSTMG14	Drive pulse timing setting 14	Set to 07h
357Fh	[7:0]	08h	Immediately	PLSTMG16	Drive pulse timing setting 16	Set to 07h
3580h	[7:0]	05h	Immediately	PLSTMG17	Drive pulse timing setting 17	Set to 04h
3583h	[2:0]	1h	Immediately	PLSTMG19	Drive pulse timing setting 19	Set to 0h
	[3]	0h			—	Set the default value.
	[6:4]	5h	Immediately	PLSTMG20	Drive pulse timing setting 20	Set to 6h
	[7]	0h			—	Set the default value.
3587h	[0]	0h	*1	PLSTMG21	Drive pulse timing setting 21	Set to 1h
	[7:1]	00h			—	Set the default value.
3590h	[7:0]	005h	Immediately	PLSTMG42	Drive pulse timing setting 42	Set to 00Bh
3591h	[3:0]					
	[7:4]	0h			—	Set the default value.
35BAh	[7:0]	0Eh	Immediately	PLSTMG43	Drive pulse timing setting 43	Set to 0Fh
366Ah	[7:0]	10h	Immediately	PLSTMG44	Drive pulse timing setting 44	Set to 0Ch
366Bh	[7:0]	0Eh	Immediately	PLSTMG45	Drive pulse timing setting 45	Set to 0Bh
366Ch	[7:0]	0Ch	Immediately	PLSTMG46	Drive pulse timing setting 46	Set to 07h
366Dh	[7:0]	0Ah	Immediately	PLSTMG47	Drive pulse timing setting 47	Set to 00h
366Eh	[7:0]	08h	Immediately	PLSTMG48	Drive pulse timing setting 48	Set to 00h
366Fh	[7:0]	06h	Immediately	PLSTMG49	Drive pulse timing setting 49	Set to 00h
3670h	[7:0]	04h	Immediately	PLSTMG50	Drive pulse timing setting 50	Set to 00h
3671h	[7:0]	02h	Immediately	PLSTMG51	Drive pulse timing setting 51	Set to 00h
3672h	[7:0]	146h	Immediately	PLSTMG52	Drive pulse timing setting 52	Set to 000h
3673h	[2:0]					
	[7:3]	00h			—	Set the default value.
3674h	[7:0]	258h	Immediately	PLSTMG53	Drive pulse timing setting 53	Set to 0DFh
3675h	[2:0]					
	[7:3]	00h			—	Set the default value.
3676h	[7:0]	400h	Immediately	PLSTMG54	Drive pulse timing setting 54	Set to 1A7h
3677h	[2:0]					
	[7:3]	00h			—	Set the default value.
3687h	[7:0]	01h	Immediately	PLSTMG55	Drive pulse timing setting 55	Set to 00h
375Ch	[7:0]	05h	Immediately	PLSTMG56	Drive pulse timing setting 56	Set to 02h

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3799h	[0]	0h	Immediately	EBDDATAEN	0h: Dummy data (00h) is output 1h: Embedded data is output	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
380Ah	[7:0]	09h	Immediately	PLSTMG29	Drive pulse timing setting 29	Set to 0Ah
382Bh	[7:0]	1Eh	Immediately	PLSTMG30	Drive pulse timing setting 30	Set to 16h
3A41h	[7:0]	04h	Immediately	MDSEL11		Set the value according to each readout mode register setting.
3A56h	[0]	1h	Immediately	MIPIEBD_TAGEN	Internal setting register	Refer to the ”Standby Cancel Sequence”
	[7:1]	00h			—	Set the default value.

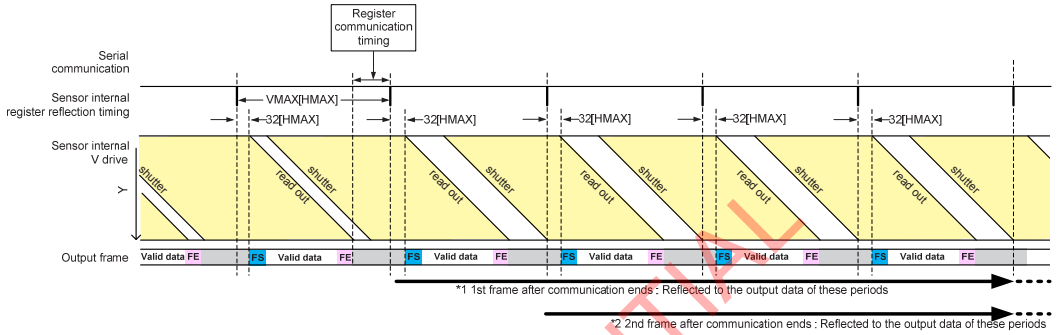
Note)
- The “Default value” column indicates the initial value set in each register in the status before register communication is performed after start-up or after the reset signal XCLR is set to Low to reset the sensor.
- Operation is not guaranteed when using register settings other than noted in these specifications. Do not access addresses not noted in the table above, and do not set register values other than those noted in “2. Description of Register” on pages 31 to 39.
- When changing the mode, the address set designated in “3. Register Settings for Each Readout Drive Mode” on pages 40 to 43 must be written.
- For the detailed reflection timing, see “1. Register Value Reflection Timing to Output Data” on page 30.

1. Register Value Reflection Timing to Output Data

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1 1st frame after communication ends	The communication contents are reflected to the output data from 1st frame after communication ends.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from 2nd frame after communication ends.
Immediately	The communication contents are reflected immediately.

For which reflection timing of each register, see “Register Map” on pages 25 to 29.



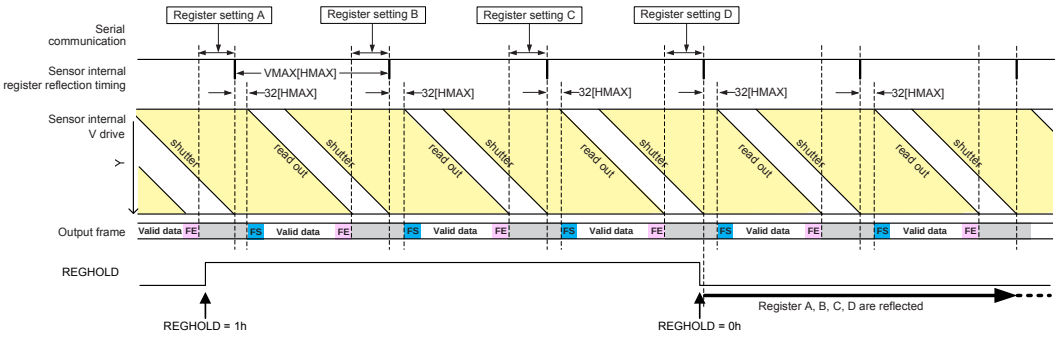
Register Value Reflection Timing to Output Data

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD (address 302Dh, bit [0]) for the registers of which reflection timing is frame unit (*1 and *2). Registers are set when REGHOLD = 1h, and REGHOLD is set to “0h” during communication period just before the frame the registers are reflected from.
Register hold function is invalid for the registers of which reflection timing is immediately. Therefore these registers are reflected immediately when even though REGHOLD = 1h.

REGHOLD Setting

Register value	Function
0h	Normal communication Reflecting register setting when register settings are held
1h	Register setting hold



Example of REGHOLD operation

2. Description of Register

Total Standby Control

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY (address 3000h, bit [0]) to “1h”.
(Standby mode is established immediately after reset.)
The serial communication block operates even in standby mode, so standby mode can be canceled by setting “0h” in the STANDBY register.

STANDBY Setting

Register value	Function
0h	Normal operation
1h	Overall standby

Input Frequency Setting

The input clock frequency can be set arbitrarily by setting input clock setting register PLRD1 (address 3120h, bit [7:0] and address 3121h, bit [7:0]) , PLRD2 (address 3129h, bit [7:0]) , PLRD3 (address 3122h, bit [7:0]) , PLRD4 (address 312Ah, bit [7:0]) , PLRD10 (address 3123h, bit [7:0]) , PLRD11 (address 3124h, bit [7:0]) , PLRD12 (address 3125h, bit [7:0]) , PLRD13 (address 3127h, bit [7:0]) and PLRD14 (address 312Dh, bit [7:0]).
Set this registers according to the recommended sequence during power-on or when canceling standby mode.

PLRD1 to PLRD4 and PLRD10 to PLRD14 Setting

Input clock frequency [MHz][*1]	Register value								
	PLRD1	PLRD2	PLRD3	PLRD4	PLRD10	PLRD11	PLRD12	PLRD13	PLRD14
6	00F0h	90h	00h	00h	00h	00h	01h	02h	02h
12	00F0h	90h	01h	01h					
18	00A0h	60h	01h	01h					
24	00F0h	90h	02h	02h					

[*1] Consult your Sony sales representative concerning other input frequency settings.

Clamp Reset

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST (address 3001h, bit [4]).
Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the reset process, so there is no need to write “0h”.

CLPSQRST Setting

Register value	Function
Changed from 0h to 1h	Resets the internal clamp circuit operation status

Electronic Shutter Timing

The exposure start timing can be designated by setting the electronic shutter timing register SHR (address 300Bh, bit [7:0] and address 300Ch, bit [7:0]). Designate the lower 8 bits in address 300Bh, and the upper 8 bits in address 300Ch, for a total of 16 bits.
Note that this setting value unit is 1[HMAX][*1] period regardless of the readout drive mode.
In addition, 1 frame period can be extended at VMAX period unit according to the SVR register SVR (address 300Dh, bit [7:0] and address 300Eh, bit [7:0]). (1 frame cycle is (SVR value + 1) times as long as VMAX period.)

[*1] Setting value of register HMAX × 72 MHz clock

Shutter Setting

Register	Register Value		Function
SHR	8 to {(SVR value + 1) × VMAX value – 4}	Readout mode No.0, 1 All-pixel scan mode (12 bits) All-pixel scan mode (10 bits)	Specifies the integration start horizontal period
	12 to {(SVR value + 1) × VMAX value – 4}	Readout mode No.1A All-pixel scan mode (10 bits) low power consumption drive	
	7 to {(SVR value + 1) × VMAX value – 4}	Readout mode No.2, 2A Horizontal/vertical 2/2-line binning mode (horizontal and vertical weighted binning) Vertical 2 binning horizontal 2/4 subsampling (vertical weighted 2 binning)	
	8 to {(SVR value + 1) × VMAX value – 1}	Readout mode No.3 Horizontal/vertical 3/3-line binning mode	
	4 to {(SVR value + 1) × VMAX value – 6}	Readout mode No.4, 5 Vertical 1/3 subsampling horizontal 3 binning mode Vertical 1/3 subsampling horizontal 2/4 subsampling mode	
	4 to {(SVR value + 1) × VMAX value − 1}	Readout mode No.6 Vertical 2/9 subsampling binning horizontal 3 binning mode	
	4 to {(SVR value + 1) × VMAX value/4 − 1}	Readout mode No.7 Vertical 2/9 subsampling binning horizontal 3 binning mode (low power consumption drive)	
	4 to {(SVR value + 1) × VMAX value − 5}	Readout mode No.8 Vertical 2/17 subsampling binning horizontal 3 binning mode	
	0 to {(SVR value + 1) × VMAX value − 1}	Global reset shutter mode (SMD = 1) (12 bits)	
	0 to {(SVR value + 1) × VMAX value − 2}	Global reset shutter mode (SMD = 1) (10 bits)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

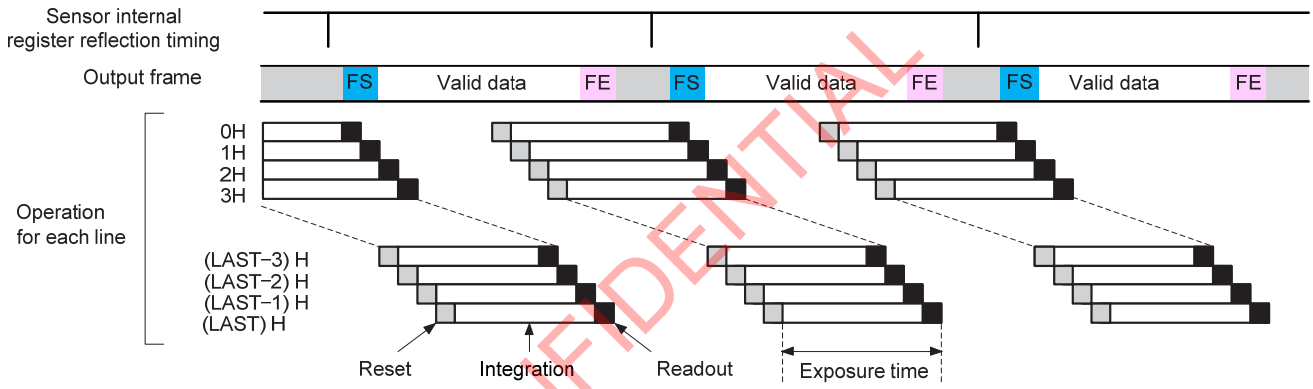
Note) 1. See ”1. Integration Time in Each Readout Drive Mode” on page 81 for the integration time calculation formula.
2. The SVR register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 3008h, bit [0]).

Electronic Shutter Drive Mode

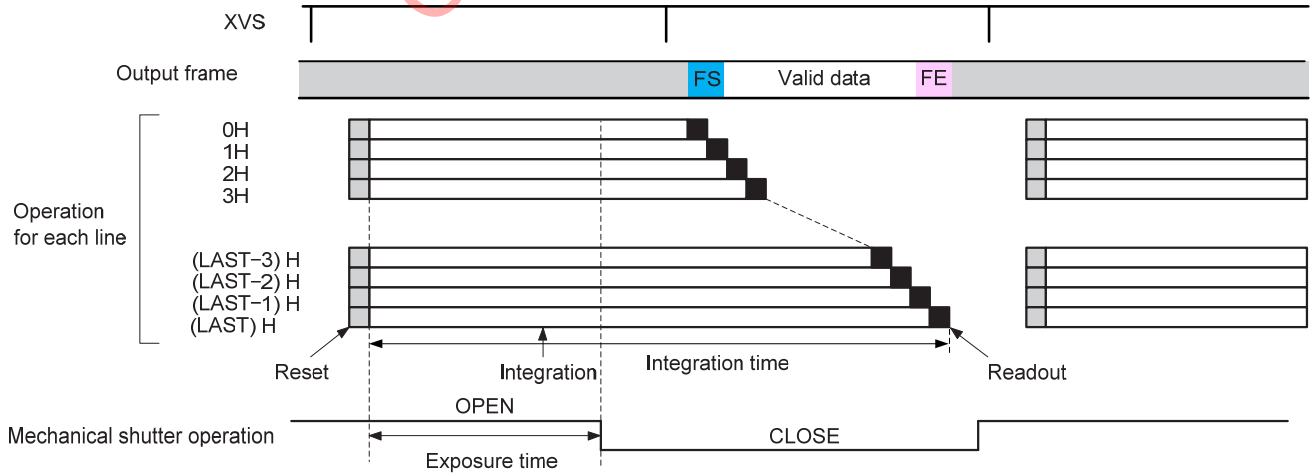
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD (address 3008h, bit [0]). Rolling shutter operation performs pixel reset and integration sequentially in line units. Global reset shutter operation resets all pixels at once and then starts integration after that.
("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.)
The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.
Using XVS output sync signal from sensor as trigger signal is recommended in the case of synchronizing global reset shutter timing of sensor and mechanical shutter timing outside of sensor is needed for fine adjustment of integration time.
Consult your Sony sales representative concerning to use XVS output signal.

SMD Setting

Register value	Function
0h	Rolling shutter (normal shutter mode)
1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

Analog Gain

The analog gain value can be set by setting the analog gain register PGC (address 3009h, bit [7:0] and address 300Ah, bit [2:0]). Set the lower 8 bits and the upper 3 bits, for total of 11 bits.

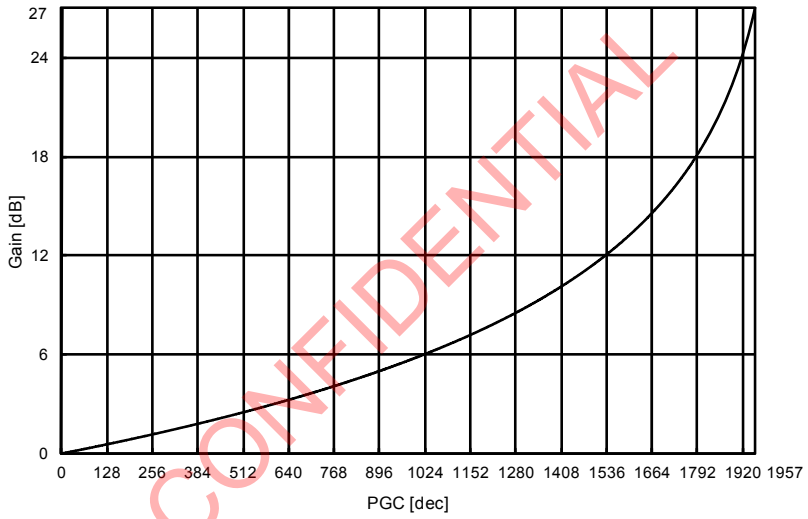
PGC Setting

Register	Function
0h to 7A5h (0d to 1957d)	Analog gain setting

In addition, the figure below shows the relationship between the register setting value and the gain value. When the register setting value is “0h (0d)”, the gain value is 0 dB (minimum settable value), and when “7A5h (1957d)”, the gain value is approximately 27 dB (maximum settable value).

Relation Formula

Gain [dB] = –20log{(2048 – PGC [10:0]) /2048}



Relationship between Register Setting Value and Set Gain Value

Digital Gain

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN (address 3011h, bit [1:0]).

DGAIN Setting

Register value	Function
0h	Digital gain setting value = 0 dB
1h	Digital gain setting value = +6 dB
2h	Digital gain setting value = +12 dB
3h	Digital gain setting value = +18 dB

Vertical Direction Readout Inversion

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV (address 301Ah, bit [0]).

MDVREV Setting

Register value	Function
0h	Vertical direction normal readout
1h	Vertical direction inversion readout

Digital Black Level Offset

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL (address 3045h, bit [7:0]).
Note that the offset unit changes according to the readout drive mode.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits.

BLKLEVEL Setting

Register value	Function
00h to FFh	Digital black level offset setting

Horizontal Drive Period Length and Vertical Drive Period Length

Horizontal drive period length (Unit: Number of 72 MHz clock) and vertical drive period length (Unit: Number of horizontal drive period) can be set by horizontal drive period length setting register HMAX (address 30F5h, bit [7:0] and address 30F6h, bit [7:0]) and vertical drive period length setting register VMAX (address 30F7h, bit [7:0], address 30F8h, bit[7:0] and address 30F9h, bit [3:0]).
Calculating formula of vertical drive period (1 frame) is shown below.

$$\text{Vertical drive period length [s]} = \text{VMAX value} \times (\text{SVR value} + 1) \times \text{HMAX value} / (72 \times 10^6)$$

For example, in the case of VMAX = 3080d, HMAX = 390d, SVR = 0h, vertical drive period length [s] is as below.
$3080 \times (0 + 1) \times 390 / (72 \times 10^6) \approx 0.0167$ [s] (59.94 [frame/s]).
See “ (1) Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page 54, 66 and “ (2) NTSC/PAL Compatible Drive” on page 55, 67 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Vertical Arbitrary Cropping

Arbitrary cropping in vertical direction can be enabled by setting vertical arbitrary cropping enable register VWIDCUTEN, and arbitrary cropping in vertical direction can be performed by designating cropping position of vertical direction to setting cropping width of vertical direction register VWINPOS and VWIDCUT. See “3-3. Vertical Arbitrary Cropping Function” on page 77 for details.

Horizontal Arbitrary Cropping

Arbitrary cropping in horizontal direction can be enabled by setting horizontal arbitrary cropping enable register HTRIMMING_EN, and arbitrary cropping in horizontal direction can be performed by designating cropping position of horizontal direction to setting cropping position of horizontal direction register HTRIMMING_START and HTRIMMING_END. See “3-4. Horizontal Arbitrary Cropping Function” on page 79 for details.

Readout Drive Mode

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL, MDPLS, MDREG, vertical arbitrary cropping registers, horizontal arbitrary cropping registers, HMAX and VMAX. When changing the mode, make the setting according to “3. Register Settings for Each Readout Drive Mode” on pages 40 to 43.

CSI-2 Standby Control

CSI-2 can be standby by CSI-2 standby register STBMIPI (address 3000h, bit [3]).

STBMIPI Setting

Register value	Function
0h	Normal operation
1h	CSI-2 standby

Embedded Data Output Setting

Sensor internal operation information (readout mode, shutter, gain and so on) can be output as Embedded data using the register EBDDATAEN (address 3799h, bit [0]). These data are output in 2 lines (1 line data × 2) just before user clamp area. See Readout Pixel Image Diagram of each mode for detailed output timing. And see pages 50 to 51 “Embedded Data Line” for details of Embedded data.

EBDDATAEN Setting

Register value	Function
0h	Dummy data (00h) is output *
1h	Embedded data is output

* EBDDATAEN register can only change the output data of Embedded data output period.
Embedded data output period is not disabled by EBDDATAEN register.

Digital Circuit Standby Control

When power-on, set the digital circuit standby control register STBLOGIC (address 3000h, bit [1]) according to the standby cancel sequency. This register is valid only when STANDBY = 0h.

STBLOGIC Setting

Register value	Function
0h	Normal operation
1h	Digital circuit standby other than serial communications block

Frequency Demultiplier Standby Control

When power-on, set the frequency demultiplier standby control register STBDV (address 3000h, bit [4]) according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBDV Setting

Register value	Function
0h	Normal operation
1h	Frequency demultiplier standby

PLL Standby Control

When power-on, set the PLL standby control registers STBPL_IF (address 310Bh, bit [0]) and STBPL_AD (address 310Bh, bit [4]) according to the standby cancel sequence. These registers are valid only when STANDBY = 0h.

STBPL_IF and STBPL_AD Setting

Register value	Function
0h	Normal operation
1h	Standby

Master Mode Operation Control

When power-on, set the master mode operation control register XMSTA (address 30F4h, bit [0]) according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

XMSTA Setting

Register value	Function
0h	Master mode start
1h	Master mode stop

Readout Drive Pulse Timing

When power-on, set the readout drive pulse timing registers PLSTMG (the following table) according to the standby cancel sequence.

PLSTMG Setting

Address	Bit assignment	Default value	Register name	Register value
3000h	[2]	0h	PLSTMG01	Set to 1h
3003h	[7:0]	40h	PLSTMG02	Set to 20h
304Eh	[7:0]	00h	PLSTMG31	Set to 02h
3057h	[7:0]	47h	PLSTMG22	Set to 4Ah
3058h	[7:0]	0E8h	PLSTMG23	Set to 0F6h
3059h	[1:0]			
	[7:2]	00h		Set to Default value
306Bh	[7:0]	07h	PLSTMG24	Set to 04h
3145h	[1:0]	1h	PLSTMG04	Set to 0h
	[7:2]	00h		Set to Default value
3202h	[7:0]	066h	PLSTMG25	Set to 063h
3203h	[0]			
	[7:1]	00h		Set to Default value
3236h	[7:0]	067h	PLSTMG26	Set to 064h
3237h	[0]			
	[7:1]	00h		Set to Default value
3304h	[7:0]	005h	PLSTMG32	Set to 00Bh
3305h	[3:0]			
	[7:4]	0h		Set to Default value
3306h	[7:0]	005h	PLSTMG33	Set to 00Bh
3307h	[3:0]			
	[7:4]	0h		Set to Default value
337Fh	[7:0]	067h	PLSTMG27	Set to 064h
3380h	[0]			
	[7:1]	00h		Set to Default value
338Dh	[7:0]	067h	PLSTMG28	Set to 064h
338Eh	[0]			
	[7:1]	00h		Set to Default value
3510h	[7:0]	054h	PLSTMG05	Set to 072h
3511h	[0]			
	[7:1]	00h		Set to Default value
3528h	[7:0]	0Eh	PLSTMG06	Set to 0Fh
3529h	[7:0]	0Eh	PLSTMG07	Set to 0Fh
352Ah	[7:0]	0Eh	PLSTMG08	Set to 0Fh
352Bh	[7:0]	0Eh	PLSTMG09	Set to 0Fh
3538h	[7:0]	0Eh	PLSTMG10	Set to 0Fh
3539h	[7:0]	0Eh	PLSTMG11	Set to 13h
353Ch	[7:0]	04h	PLSTMG13	Set to 01h
3553h	[7:0]	1Fh	PLSTMG34	Set to 00h
3554h	[7:0]	1Fh	PLSTMG35	Set to 00h
3555h	[7:0]	1Fh	PLSTMG36	Set to 00h
3556h	[7:0]	1Fh	PLSTMG37	Set to 00h
3557h	[7:0]	1Eh	PLSTMG38	Set to 00h
3558h	[7:0]	1Dh	PLSTMG39	Set to 00h
3559h	[7:0]	1Dh	PLSTMG40	Set to 00h
355Ah	[7:0]	1Ah	PLSTMG41	Set to 00h
357Dh	[7:0]	0Ch	PLSTMG14	Set to 07h
357Fh	[7:0]	08h	PLSTMG16	Set to 07h
3580h	[7:0]	05h	PLSTMG17	Set to 04h
3583h	[2:0]	1h	PLSTMG19	Set to 0h
	[3]	0h		Set to Default value
	[6:4]	5h	PLSTMG20	Set to 6h
	[7]	0h		Set to Default value
3587h	[0]	0h	PLSTMG21	Set to 1h
	[7:1]	00h		Set to Default value

Address	Bit assignment	Default value	Register name	Register value
3590h	[7:0]	005h	PLSTMG42	Set to 00Bh
3591h	[3:0]			
	[7:4]	0h		Set to Default value
35BAh	[7:0]	0Eh	PLSTMG43	Set to 0Fh
366Ah	[7:0]	10h	PLSTMG44	Set to 0Ch
366Bh	[7:0]	0Eh	PLSTMG45	Set to 0Bh
366Ch	[7:0]	0Ch	PLSTMG46	Set to 07h
366Dh	[7:0]	0Ah	PLSTMG47	Set to 00h
366Eh	[7:0]	08h	PLSTMG48	Set to 00h
366Fh	[7:0]	06h	PLSTMG49	Set to 00h
3670h	[7:0]	04h	PLSTMG50	Set to 00h
3671h	[7:0]	02h	PLSTMG51	Set to 00h
3672h	[7:0]	146h	PLSTMG52	Set to 000h
3673h	[2:0]			
	[7:3]	00h		Set to Default value
3674h	[7:0]	258h	PLSTMG53	Set to 0DFh
3675h	[2:0]			
	[7:3]	00h		Set to Default value
3676h	[7:0]	400h	PLSTMG54	Set to 1A7h
3677h	[2:0]			
	[7:3]	00h		Set to Default value
3687h	[7:0]	01h	PLSTMG55	Set to 00h
375Ch	[7:0]	05h	PLSTMG56	Set to 02h
380Ah	[7:0]	09h	PLSTMG29	Set to 0Ah
382Bh	[7:0]	1Eh	PLSTMG30	Set to 16h

3. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below.

3-1. When Using Type 1/2.3 Approx. 12.35 M Pixels (4:3)

Description of Register Setting for Each Readout Drive Mode

Address	Bit Assign-ment	Register Name	Readout mode No. *1									
			0	1	1A	2	3	4	5	6	7	8
3004h	[7:0]	MDSEL1	00h	00h	06h	A2h	45h	08h	09h	2Ah	0Bh	2Ch
3005h	[7:0]	MDSEL2	07h	01h	01h	25h	35h	35h	41h	35h	35h	35h
3006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h	00h	00h	38h	00h
3007h	[7:0]	MDSEL4	A0h	A0h	A2h	A0h	A0h	A0h	A0h	A0h	A9h	A0h
300Dh	[7:0]	SVR	According to exposure time								Multiple of 8 −1	According to exposure time
300Eh	[7:0]											
301Ah	[0]	MDVREV	0h: vertical direction normal /1h: inverted									
	[7:1]		00h									
3039h	[7:0]	HTRIMMING_END	0000h	0000h	1008h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
303Ah	[4:0]											
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
303Eh	[7:0]	HTRIMMING_START	0000h	0000h	0030h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
303Fh	[4:0]											
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
3040h	[0]	HTRIMMING_EN	0h	0h	1h	0h	0h	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
3068h	[7:0]	MDSEL7	00h	00h	01h	00h	00h	00h	00h	00h	01h	00h
307Eh	[7:0]	MDSEL5	0000h	0000h	0041h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
307Fh	[7:0]											
3080h	[7:0]	MDPLS01	0000h	0000h	000Fh normal/ 0040h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3081h	[7:0]											
3082h	[7:0]	MDPLS02	0000h	0000h	0034h normal/ 0030h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3083h	[7:0]											
3084h	[7:0]	MDPLS03	0000h	0000h	00C7h normal/ 1894h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3085h	[7:0]											
3086h	[7:0]	MDPLS04	0000h	0000h	17CAh normal/ 17CCh inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3087h	[7:0]											
3095h	[7:0]	MDPLS05	0000h	0000h	191Ch	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3096h	[7:0]											
3097h	[7:0]	MDPLS06	0000h	0000h	0001h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3098h	[7:0]											
3099h	[7:0]	MDPLS07	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
309Ah	[7:0]											
309Bh	[7:0]	MDPLS08	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
309Ch	[7:0]											
30BCh	[7:0]	MDPLS40	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30BDh	[7:0]											
30BEh	[7:0]	MDPLS41	0000h	0000h	0007h normal/ 0005h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30BFh	[7:0]											

Address	Bit Assign-ment	Register Name	Readout mode No. *1									
			0	1	1A	2	3	4	5	6	7	8
30C0h	[7:0]	MDPLS42	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C1h	[7:0]											
30C2h	[7:0]	MDPLS43	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C3h	[7:0]											
30C4h	[7:0]	MDPLS44	0000h	0000h	004Ah normal/ 0042h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C5h	[7:0]											
30C6h	[7:0]	MDPLS45	0000h	0000h	003Eh normal/ 0040h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C7h	[7:0]											
30C8h	[7:0]	MDPLS46	0000h	0000h	1898h normal/ 1896h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C9h	[7:0]											
30CAh	[7:0]	MDPLS47	0000h	0000h	002Fh normal/ 0030h inverted	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30CBh	[7:0]											
30CCh	[7:0]	MDPLS48	00h	00h	02h	00h	00h	00h	00h	00h	00h	00h
30D0h	[7:0]	MDPLS52	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30D1h	[7:0]											
30D5h	[0]	VWIDCUTEN	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
30D6h	[7:0]	VWIDCUT	000h	000h	000h	000h	000h	000h	000h	000h	000h	000h
30D7h	[2:0]											
	[7:3]		00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
30D8h	[7:0]	VWINPOS	000h	000h	000h	000h	000h	000h	000h	000h	000h	000h
30D9h	[3:0]											
	[7:4]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
30DAh	[7:0]	MDREG01	00h	00h	01h	02h	04h	05h	05h	07h	08h	09h
30EEh	[7:0]	MDREG02	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h
30F5h	[7:0]	HMAX	Setting horizontal drive period length (72 MHz clock unit)*2									
30F6h	[7:0]											
30F7h	[7:0]	VMAX	Setting vertical drive period length (horizontal drive period length unit)*2									
30F8h	[7:0]											
30F9h	[3:0]											
	[7:4]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
312Fh	[7:0]	MDSEL9	0BF6h	0BF6h	0BF6h	05F4h	03FEh	03FCh	0302h	0158h	0158h	00BAh
3130h	[4:0]											
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
3131h	[7:0]	MDSEL10	0BE6h	0BE6h	0BE6h	05F0h	03FAh	03F8h	02FEh	0154h	0154h	00B6h
3132h	[4:0]											
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
3A41h	[7:0]	MDSEL11	10h	10h	10h	04h	04h	04h	04h	04h	04h	04h

*1 See “1. Readout Drive Modes” on page 44 for details of readout mode No.

*2 See “ (1) Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page 54 and “ (2) NTSC/PAL Compatible Drive” on pages 55 to 56 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

3-2. When Using Type 1/2.5 Approx. 9.03 M Pixels (Approx. 17:9)

Description of Register Setting for Each Readout Drive Mode

Address	Bit Assign-ment	Register Name	Readout mode No. *1								
			0	1	1A	2	2A	3	4	6	8
3004h	[7:0]	MDSEL1	10h	19h	06h	B1h	B1h	53h	14h	35h	36h
3005h	[7:0]	MDSEL2	07h	01h	01h	25h	45h	35h	35h	35h	35h
3006h	[7:0]	MDSEL3	01h	04h	04h	01h	01h	01h	01h	01h	01h
3007h	[7:0]	MDSEL4	A0h	A0h	A2h	A0h	A0h	A0h	A0h	A0h	A0h
300Dh	[7:0]	SVR	According to exposure time								
300Eh	[7:0]										
301Ah	[0]	MDVREV	0h: vertical direction normal /1h: inverted								
	[7:1]		00h								
3039h	[7:0]	HTRIMMING_END	0000h	0000h	0F48h	0000h	0000h	0000h	0000h	0000h	0000h
303Ah	[4:0]										
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h
303Eh	[7:0]	HTRIMMING_START	0000h	0000h	0030h	0000h	0000h	0000h	0000h	0000h	0000h
303Fh	[4:0]										
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h
3040h	[0]	HTRIMMING_EN	0h	0h	1h	0h	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h	00h	00h	00h	00h
3068h	[7:0]	MDSEL7	00h	00h	01h	00h	00h	00h	00h	00h	00h
307Eh	[7:0]	MDSEL5	0000h	0800h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
307Fh	[7:0]										
3080h	[7:0]	MDPLS01	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3081h	[7:0]										
3082h	[7:0]	MDPLS02	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3083h	[7:0]										
3084h	[7:0]	MDPLS03	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3085h	[7:0]										
3086h	[7:0]	MDPLS04	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3087h	[7:0]										
3095h	[7:0]	MDPLS05	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3096h	[7:0]										
3097h	[7:0]	MDPLS06	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
3098h	[7:0]										
3099h	[7:0]	MDPLS07	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
309Ah	[7:0]										
309Bh	[7:0]	MDPLS08	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
309Ch	[7:0]										
30BCh	[7:0]	MDPLS40	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30BDh	[7:0]										
30BEh	[7:0]	MDPLS41	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30BFh	[7:0]										
30C0h	[7:0]	MDPLS42	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C1h	[7:0]										
30C2h	[7:0]	MDPLS43	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C3h	[7:0]										
30C4h	[7:0]	MDPLS44	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C5h	[7:0]										
30C6h	[7:0]	MDPLS45	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C7h	[7:0]										
30C8h	[7:0]	MDPLS46	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30C9h	[7:0]										
30CAh	[7:0]	MDPLS47	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30CBh	[7:0]										
30CCh	[7:0]	MDPLS48	00h	00h	00h	00h	00h	00h	00h	00h	00h
30D0h	[7:0]	MDPLS52	0000h	0F48h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
30D1h	[7:0]										

Address	Bit Assign-ment	Register Name	Readout mode No. *1								
			0	1	1A	2	2A	3	4	6	8
30D5h	[0]	VWIDCUTEN	0h	0h	0h	0h	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h	00h	00h	00h	00h
30D6h	[7:0]	VWIDCUT	000h	000h	000h	000h	000h	000h	000h	000h	000h
30D7h	[2:0]										
	[7:3]		00h	00h	00h	00h	00h	00h	00h	00h	00h
30D8h	[7:0]	VWINPOS	000h	000h	000h	000h	000h	000h	000h	000h	000h
30D9h	[3:0]										
	[7:4]		0h	0h	0h	0h	0h	0h	0h	0h	0h
30DAh	[7:0]	MDREG01	00h	00h	01h	02h	02h	04h	05h	07h	09h
30EEh	[7:0]	MDREG02	01h	01h	01h	01h	01h	01h	01h	01h	01h
30F5h	[7:0]	HMAX	Setting horizontal drive period length (72 MHz clock unit)*2								
30F6h	[7:0]										
30F7h	[7:0]	VMAX	Setting vertical drive period length (horizontal drive period length unit)*2								
30F8h	[7:0]										
30F9h	[3:0]										
	[7:4]		0h	0h	0h	0h	0h	0h	0h	0h	0h
312Fh	[7:0]	MDSEL9	0886h	0886h	0886h	044Ah	044Ah	02E2h	02E2h	00FAh	0086h
3130h	[4:0]										
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h
3131h	[7:0]	MDSEL10	087Eh	087Eh	087Eh	0446h	0446h	02DEh	02DEh	00F6h	0082h
3132h	[4:0]										
	[7:5]		0h	0h	0h	0h	0h	0h	0h	0h	0h
3A41h	[7:0]	MDSEL11	08h	08h	08h	04h	04h	04h	04h	04h	04h

*1 See “1. Readout Drive Modes” on page 45 for details of readout mode No.

*2 See “ (1) Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page 66 and “ (2) NTSC/PAL Compatible Drive” on pages 67 to 68 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Readout Drive Modes

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.
All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).

1-1. When Using Type 1/2.3 Approx. 12.35 M Pixels (4:3)

Description of Readout Drive Modes

Readout Mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12 bits)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (10 bits)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1A	All-pixel scan mode (10 bits) low power consumption drive	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning on page 47.)
3	Horizontal/vertical 3/3-line binning	Horizontal and vertical direction 3-line binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning on page 47.)
4	Vertical 1/3 subsampling horizontal 3 binning	1 of every 3 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 47.)
5	Vertical 1/3 subsampling horizontal 2/4 subsampling 16:9 cropping	1 of every 3 lines in the vertical direction at the all-pixel scan area (16:9 cropping) are subsampled. Then, 2 of every 4 lines in the horizontal direction are output. (See the image of binning on page 47.)
6	Vertical 2/9 subsampling binning horizontal 3 binning	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 48.)
7	Vertical 2/9 subsampling binning horizontal 3 binning low power consumption drive	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 48.)
8	Vertical 2/17 subsampling binning horizontal 3 binning	2 of every 17 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 48.)

See the following pages for the detailed specifications of each mode noted in the table above.

1-2. When Using Type 1/2.5 Approx. 9.03 M Pixels (Approx. 17:9)

Description of Readout Drive Modes

Readout Mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12 bits)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (10 bits)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1A	All-pixel scan mode (10 bits) low power consumption drive	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning on page 47.)
2A	Vertical 2 binning horizontal 2/4 subsampling (vertical weighted 2 binning)	Add 2 lines with weighting in the vertical direction at the all-pixel scan area and 2 of every 4 lines in the horizontal direction are output. (See the image of binning on page 47).
3	Horizontal/vertical 3/3-line binning	Horizontal and vertical direction 3-line binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning on page 47.)
4	Vertical 1/3 subsampling horizontal 3 binning	1 of every 3 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 47.)
6	Vertical 2/9 subsampling binning horizontal 3 binning	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 48.)
8	Vertical 2/17 subsampling binning horizontal 3 binning	2 of every 17 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning on page 48.)

See the following pages for the detailed specifications of each mode noted in the table above

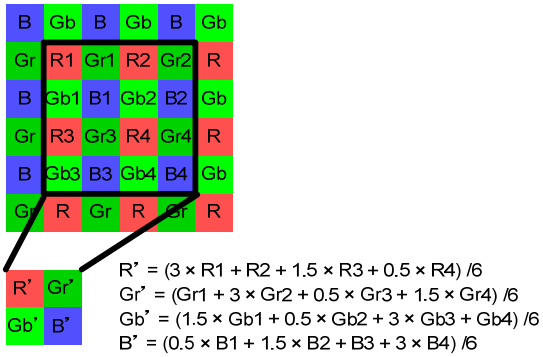
1-3. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.
Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits. So the weight of 1 digit is 4 times greater than during 12-bit output.

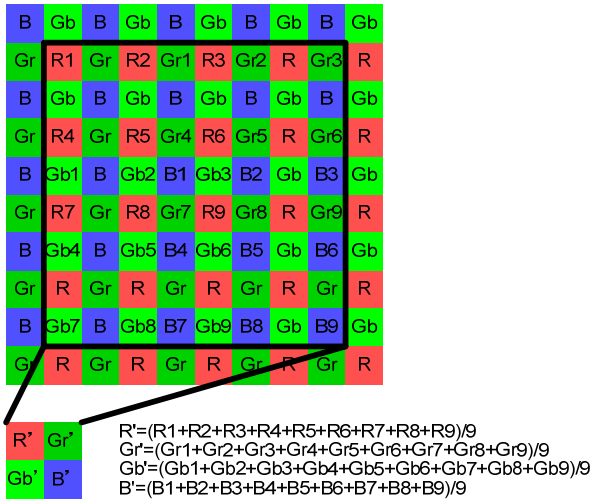
Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Horizontal pixel processing	Vertical pixel processing	Total Number of binning pixels	Internal arithmetic processing	Number of output bits
0	12 bits	—	—	—	—	10 bit + 2 bit *1
1	10 bits	—	—	—	—	10 bit
1A	10 bits	—	—	—	—	10 bit
2	10 bits	2 binning	2 binning	4 pixels	3/6, 1.5/6, 1/6, 0.5/6 (weighted binning *3)	10 bit + 2 bit *2
2A	10 bits	2/4 subsampling	2 binning	2 pixels	3/4, 1/4 (weighted 2 binning *3)	10 bit + 2 bit *2
3	10 bits	3 binning	3 binning	9 pixels	1/9	10 bit + 2 bit *2
4	10 bits	3 binning	1/3 subsampling	3 pixels	1/3	10 bit + 2 bit *2
5	10 bits	2/4 subsampling	1/3 subsampling	—	—	10 bit
6	10 bits	3 binning	2/9 subsampling binning	6 pixels	1/6	10 bit + 2 bit *2
7	10 bits	3 binning	2/9 subsampling binning	6 pixels	1/6	10 bit + 2 bit *2
8	10 bits	3 binning	2/17 subsampling binning	6 pixels	1/6	10 bit + 2 bit *2

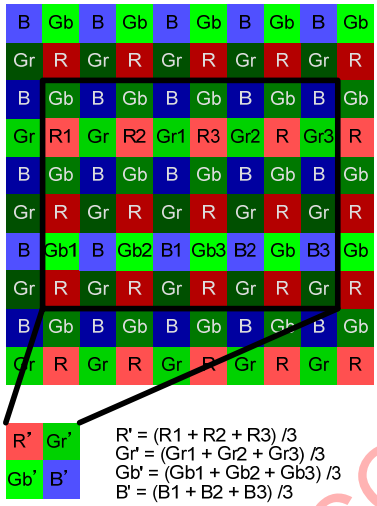
*1 A/D conversion is performed with a resolution 4 times that of 10-bit A/D conversion, and the results are output in 12 bits regarded as a 10-bit integer item and a 2-bit decimal item.
*2 Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.
*3 See page 47 “Binning Image” for details of weighted binning.



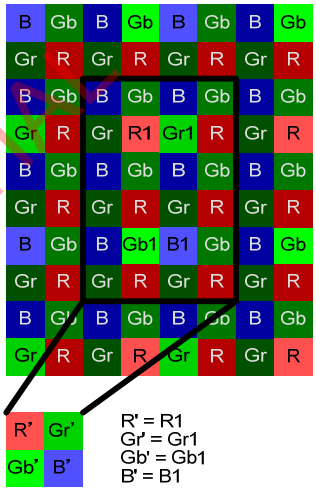
Horizontal/Vertical 2/2-line Binning
(Horizontal and vertical weighted binning)
Binning Image



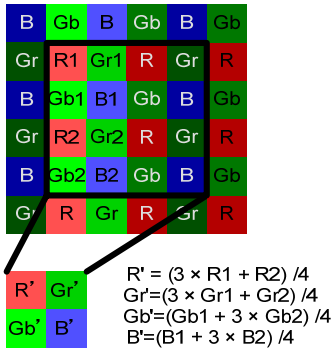
Horizontal/Vertical 3/3-line Binning
Binning Image



Vertical 1/3 Subsampling
Horizontal 3 Binning Binning Image

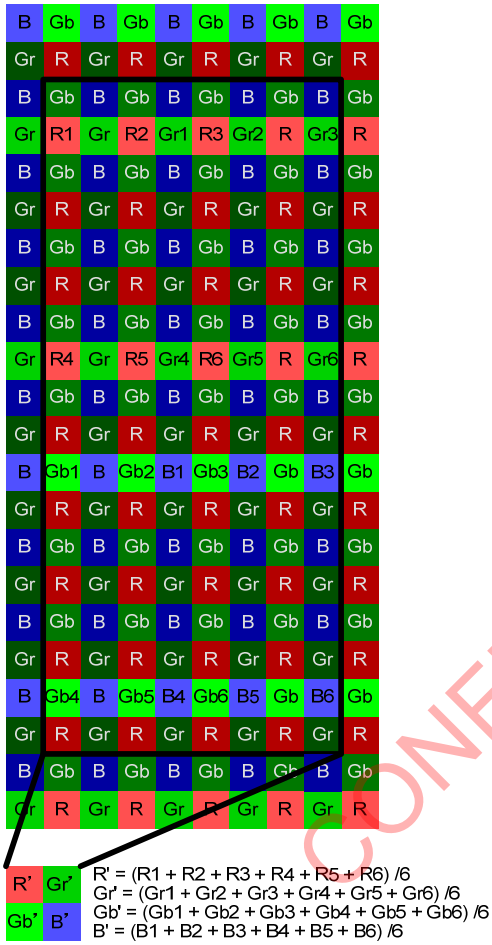


Vertical 1/3 Subsampling
Horizontal 2/4 SubsamplingBinning Image

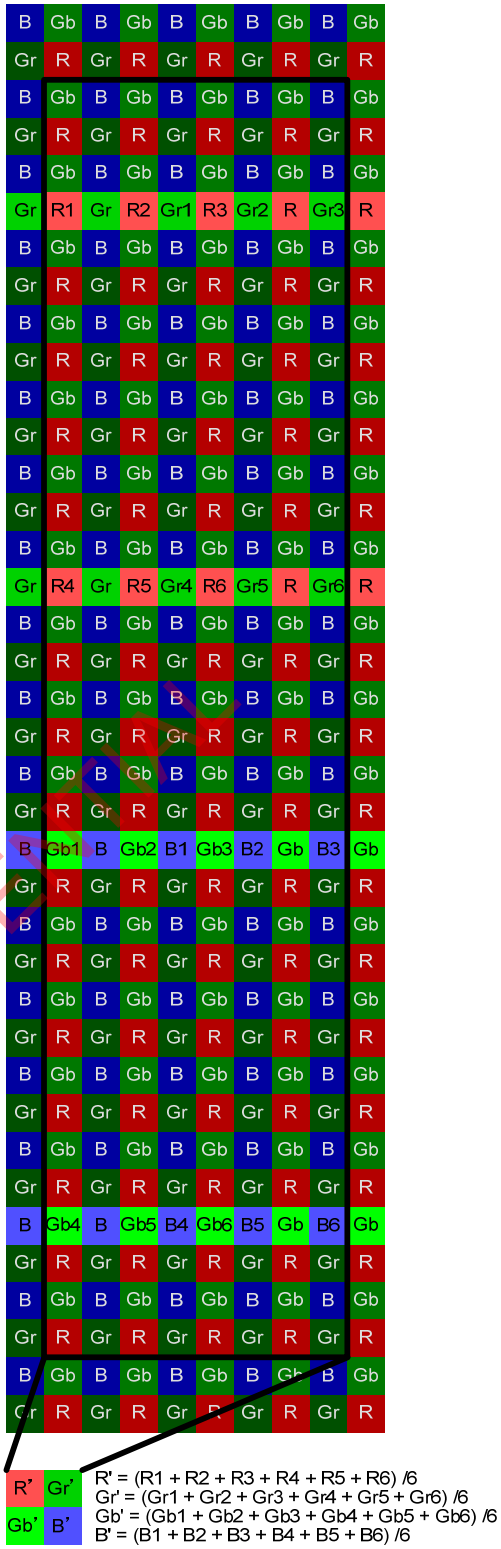


Vertical 2 Binning
Horizontal 2/4 Subsampling
(Vertical Weighted 2 Binning) Binning Image

Note) White letters in the diagram indicate pixels which are not read out.



Vertical 2/9 Subsampling Binning
Horizontal 3 Binning Binning Image



Vertical 2/17 Subsampling Binning
Horizontal 3 Binning Binning Image

Note) White letters in the diagram indicate pixels which are not read out.

2. Image Data Output Format (CSI-2)

Frame Format

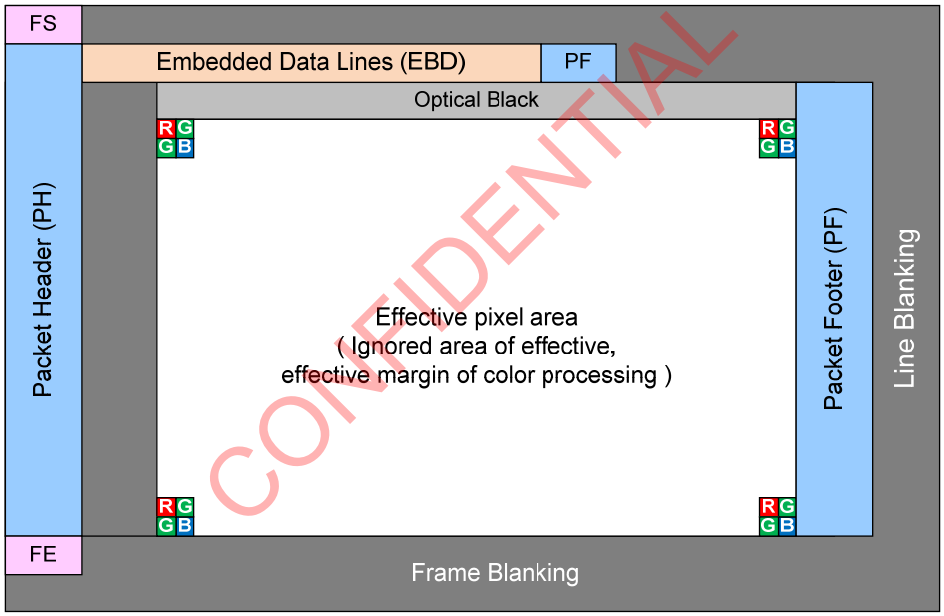
Each line of each image frame is output like the General Frame Format to CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Description
00h	Frame Start Code	FS
01h	Frame End Code	FE
10h	NULL	Invalid data
12h	Embedded Data	Embedded data
2Bh	RAW10	When output data bit length is 10-bits
2Ch	RAW12	When output data bit length is 12-bits
37h	Optical Black Data	Vertical Optical Black line data

Frame Structure

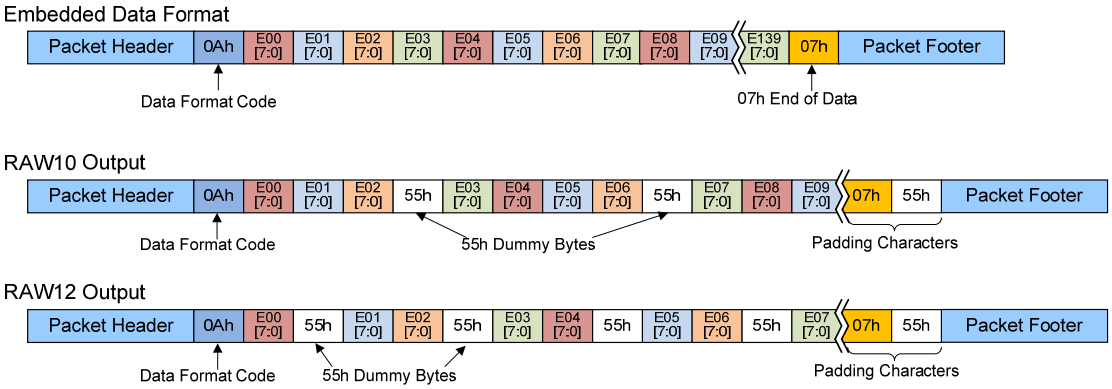
The figure below shows the image frame structure.



Frame Structure (CSI-2)

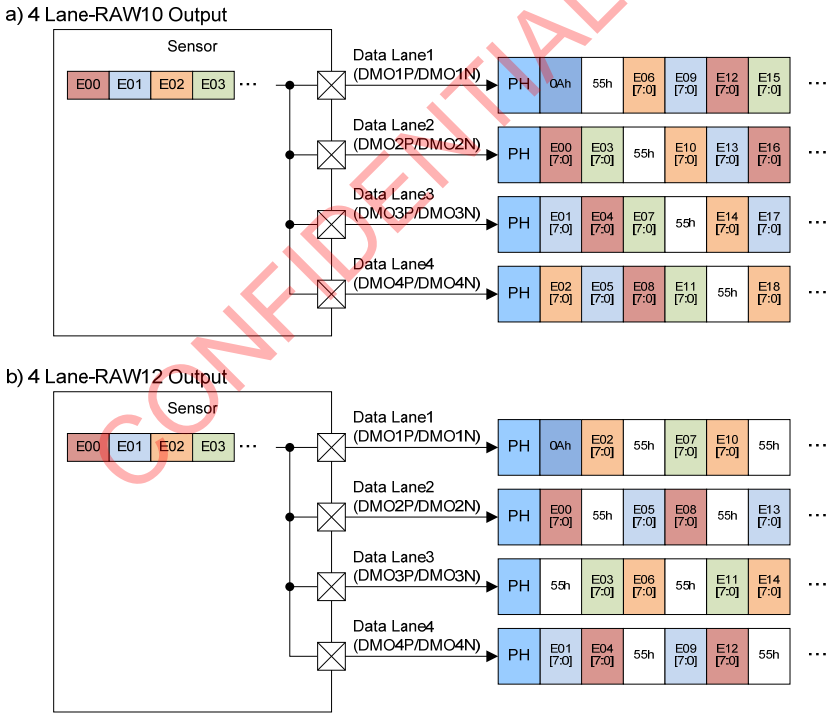
Embedded Data Line

The Embedded data line is output in a line following the sync code FS.
In RAW10 mode, 55h dummy bytes are inserted after outputting 4 bytes of data each.
In RAW12 mode, 55h dummy bytes are inserted after outputting 2 bytes of data each.



Output Format of Embedded Data

The each format of 4 Lane are shown below.



Output Format of Embedded 4 Lane (CSI-2)

Note) By setting EBDDATAEN = 0h output data of this period changes to dummy data (00h).
It is not supported removing this embedded data line period itself.

Specific output examples are shown below.

Output timing	bit	Transfer data	Description
E00 to E05	[7:0]	—	(Ignored)
E06	[0]	SMD	
	[7:1]	—	(Ignored)
E07	[7:0]	PGC	
E08	[2:0]		
	[7:3]	—	(Ignored)
E09	[7:0]	SHR	
E10	[7:0]		
E11	[7:0]	SVR	
E12	[7:0]		
E13 to E14	[7:0]	—	(Ignored)
E15	[2:0]	DGAIN	
	[3]	MDVREV	
	[7:4]	—	(Ignored)
E16	[7:0]	BLKLEVEL	
E17 to E24	[7:0]	—	(Ignored)
E25	[0]	HTRIMMING_EN	
	[7:1]	—	(Ignored)
E26	[7:0]	HTRIMMING_START	
E27	[4:0]		
	[7:5]	—	(Ignored)
E28	[7:0]	HTRIMMING_END	
E29	[4:0]		
	[7:5]	—	(Ignored)
E30	[0]	VWIDCUTEN	
	[7:1]	—	(Ignored)
E31	[7:0]	VWINPOS	
E32	[3:0]		
	[7:4]	—	(Ignored)
E33	[7:0]	VWIDCUT	
E34	[2:0]		
	[7:3]	—	(Ignored)
E35 to E139	[7:0]	—	(Ignored)

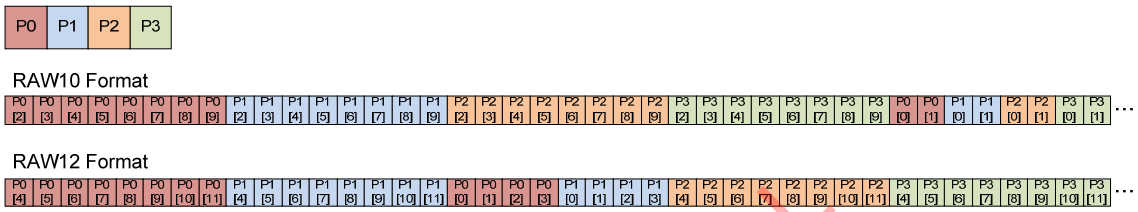
CSI-2 serial Output Setting

The output formats of this sensor support the following modes.

CSI-2 serial data output 4 Lane, RAW10 and RAW12

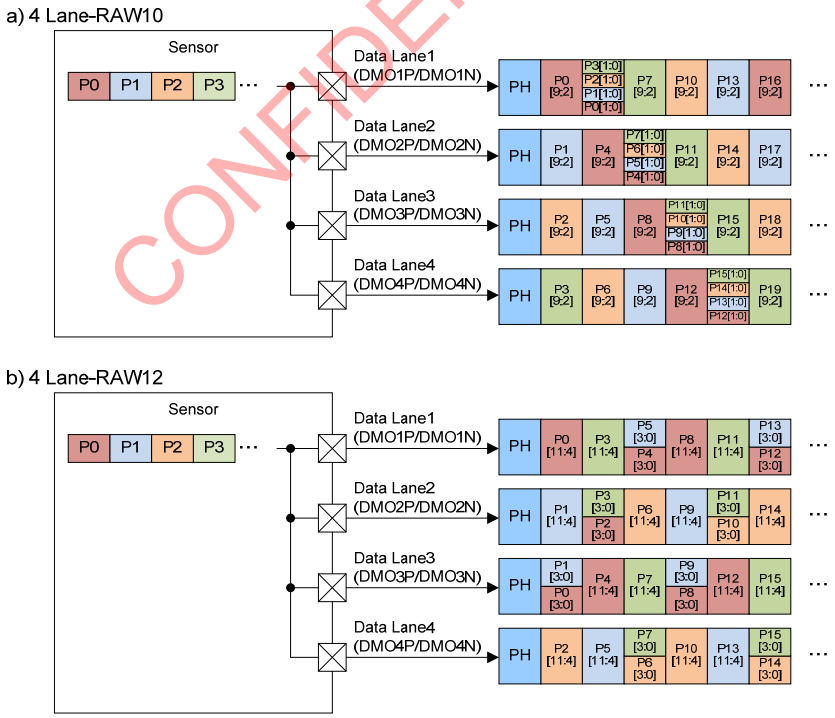
The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal and the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DCKP/DCKN of the CSI-2 pins.
In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The bit rate maximum value is 1.440G bps/Lane.

The formats of RAW10 and RAW12 are shown below.



The example of formats of RAW10 and RAW12

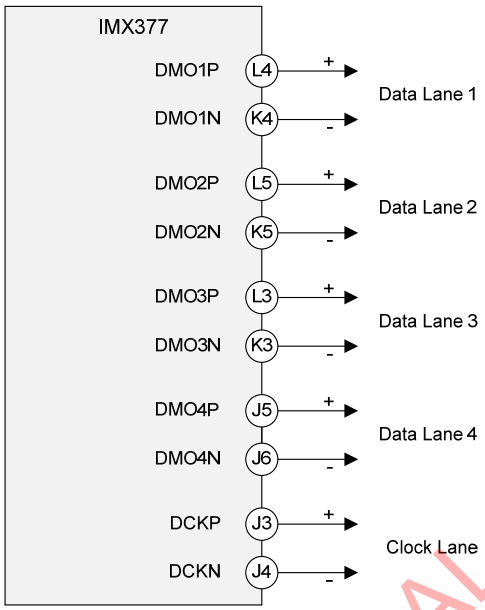
The each format of 4 Lane are shown below.



Output Format of 4 Lane (CSI-2)

MIPI Transmitter

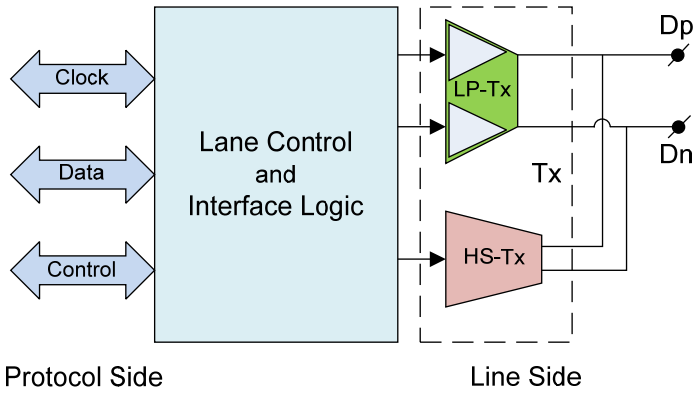
Output pins (DMO1P to DMO4P, DMO1N to DMO4N, DCKP, DCKN) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1
・MIPI Alliance Specification for D-PHY Version 1.1

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver.
The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1.440 Gbps/Lane.



Universal Lane Module Functions

3. Detailed Specification of Each Mode

3-1. When Using Type 1/2.3 Approx. 12.35 M Pixels (4:3)

(1) Horizontal/Vertical Operation Period in Each Readout Drive Mode

Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX minimum value
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	48	14	12	4000	12	18	655
1	48	14	12	4000	12	18	551
1A	48	14	12	4000	12	18	276
2	24	8	6	2000	6	8	260
3	16	6	4	1332	4	6	260
4	16	6	4	1332	4	6	260
5	24	8	6	2000	6	8	295
6	16	6	4	1332	4	6	260
7	16	6	4	1332	4	6	260
8	16	6	4	1332	4	6	260

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX minimum value
	Front OPB	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	16	5 [*1] 6 [*2]	18	3000	18	4	3100
1	16	5 [*1] 6 [*2]	18	3000	18	4	3100
1A	16	5 [*1] 6 [*2]	18	3000	18	4	6200
2	4	4	6	1500	6	4	3080
3	4	4 [*1] 3 [*2]	6	998	6	4	3104
4	4	2 [*1] 1 [*2]	6	1000	6	2	1058
5	4	2 [*1] 1 [*2]	6	750	6	2	808
6	4	2	2	332	2	2	726
7	4	2	2	332	2	2	700
8	4	2	2	174	2	2	390

[*1] When vertical direction normal readout.
[*2] When vertical direction inverted readout.

(2) NTSC/PAL Compatible Drive

This sensor can be used with a frame frequency that supports NTSC or PAL by using the recommended horizontal operating period (H period) and recommended vertical operating period (V period) for each readout drive mode shown in the table below.

Recommended H Period and V Periods (NTSC/PAL Compatible)

Readout mode No.	NTSC compatible drive			PAL compatible drive		
	Number of HMAX[*1]	Number of VMAX[*2]	Frame frequency [frame/s]	Number of HMAX[*1]	Number of VMAX[*2]	Frame frequency [frame/s]
0	660	3120	34.97	750	3200	30.00
1	572	3150	39.96	625	3600	32.00
1A	280	8580	29.97	288	10000	25.00
2	390	3080	59.94	375	3840	50.00
3	273	4400	59.94	288	5000	50.00
4	273	1100	239.76	288	1250	200.00
5	325	924	239.76	320	1125	200.00
6	264	910	299.70	300	800	300.00
7	429	700	29.97[*3]	300	1200	25.00[*3]
8	273	400	659.34	300	400	600.00

[*1] The value set as HMAX (address 30F5h, bit [7:0] and address 30F6h, bit [7:0]).
[*2] The value set as VMAX (address 30F7h, bit [7:0], address 30F8h, bit [7:0] and address 30F9h, bit [3:0]).
[*3] When performing a low power consumption drive, (multiple of 8) - 1 is set to SVR (address 300Dh, bit[7:0] and address 300Eh, bit [7:0]).

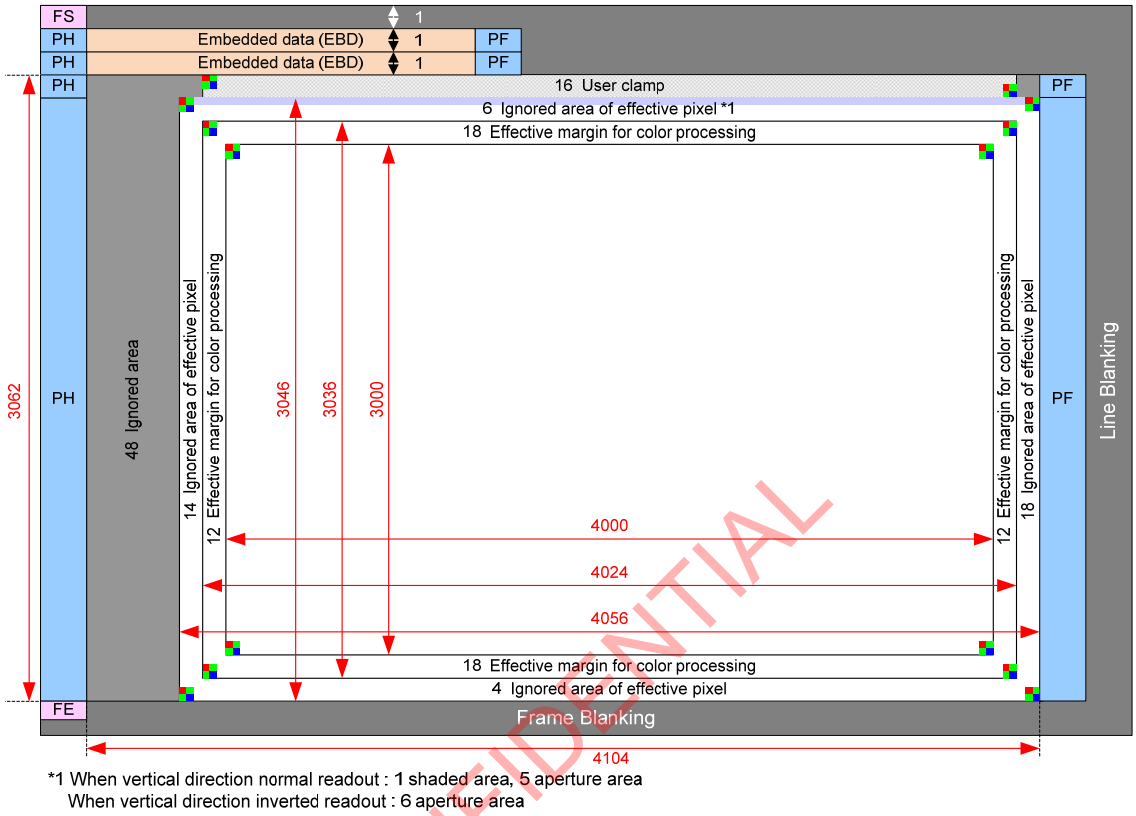
Imaging Conditions in Each Readout Drive Mode (NTSC/PAL Compatible Drive)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/ RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	4	12	RAW12	4000	3000	12.00 M Pixels
1	4	10	RAW10	4000	3000	12.00 M Pixels
1A	4	10	RAW10	4000	3000	12.00 M Pixels
2	4	10	RAW12	2000	1500	3.00 M Pixels
3	4	10	RAW12	1332	998	Approximately 1.33 M Pixels
4	4	10	RAW12	1332	1000	Approximately 1.33 M Pixels
5	4	10	RAW10	2000	750	1.50 M Pixels
6	4	10	RAW12	1332	332	Approximately 0.44 M Pixels
7	4	10	RAW12	1332	332	Approximately 0.44 M Pixels
8	4	10	RAW12	1332	174	Approximately 0.23 M Pixels

(3) Image Data Output Format

The output format in each readout drive mode is as follows.

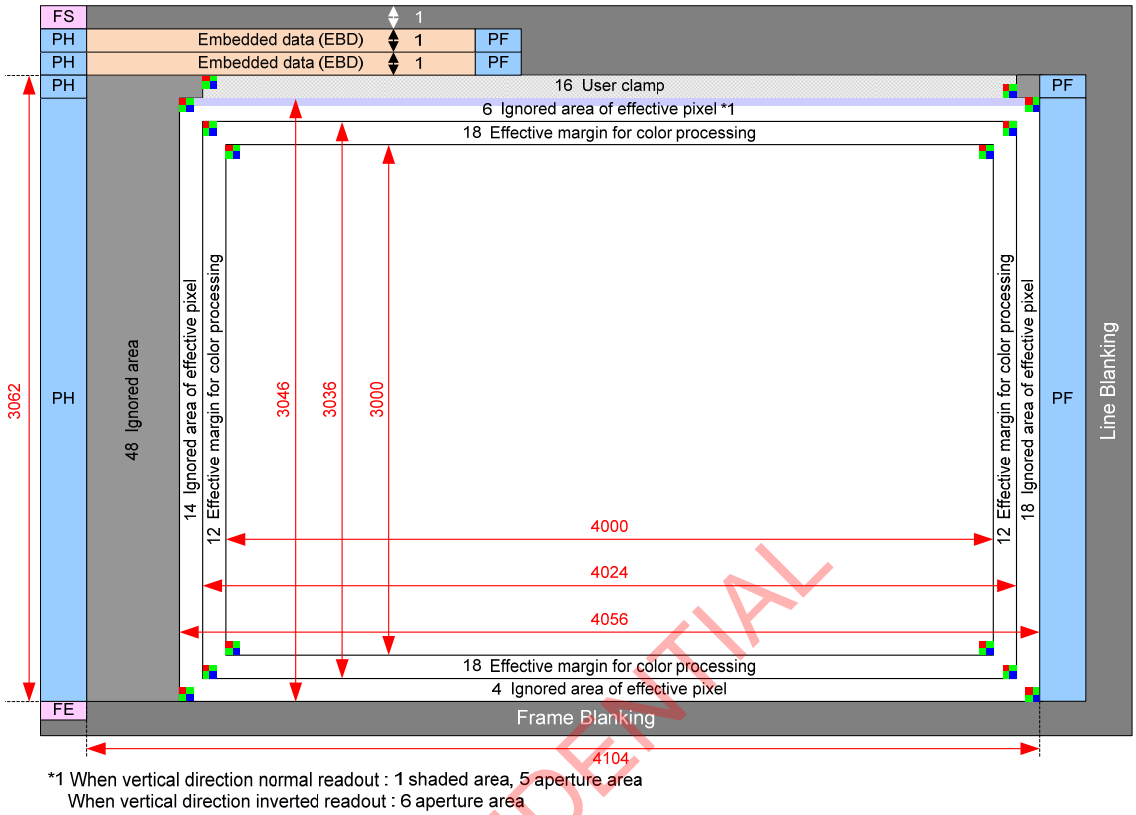
MODE0: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)



*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4000 × 3000)

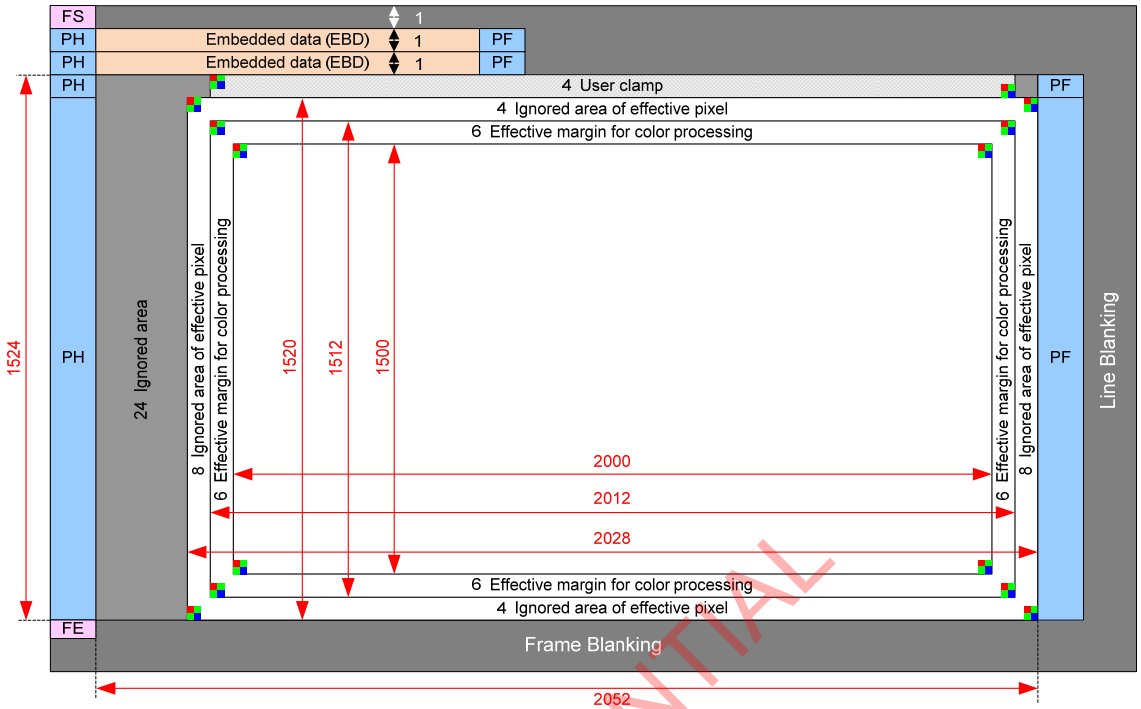
MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)
MODE1A: All-pixel scan mode low power consumption drive (10-bit A/D conversion, 10-bit length output)



*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

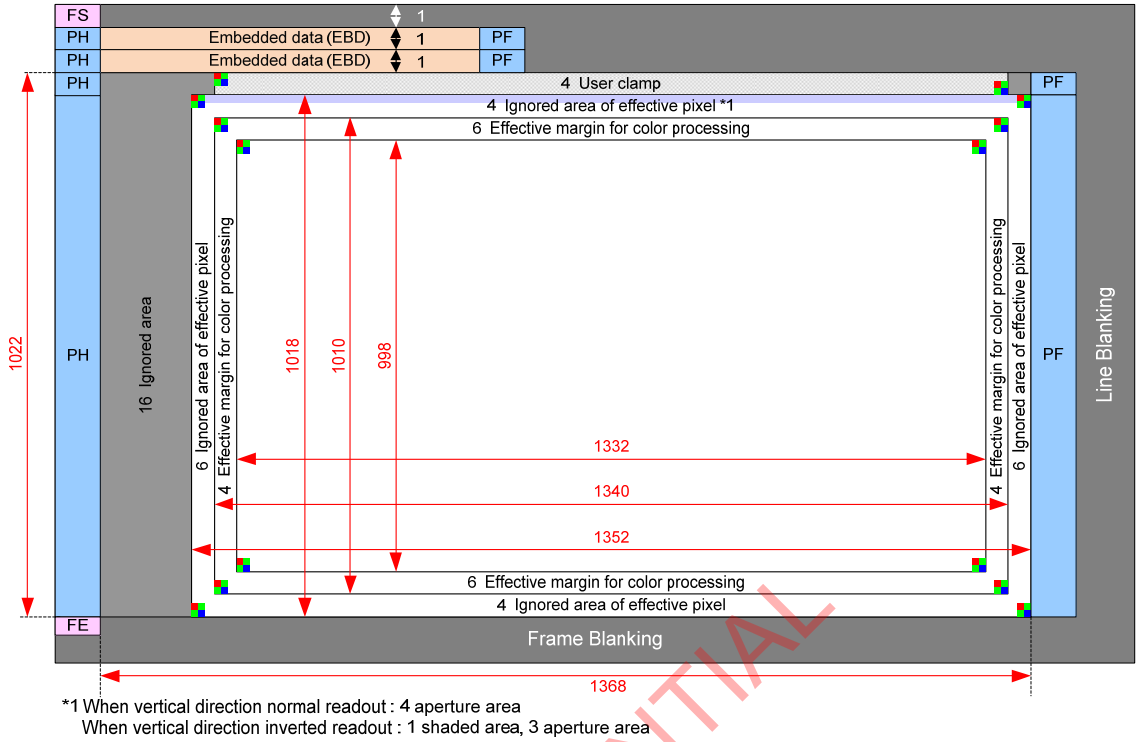
Readout Pixel Image Diagram (4000 × 3000)

MODE2: Horizontal/vertical 2/2-line binning mode
(horizontal and vertical weighted binning)
(10-bit A/D conversion, 12-bit length output)



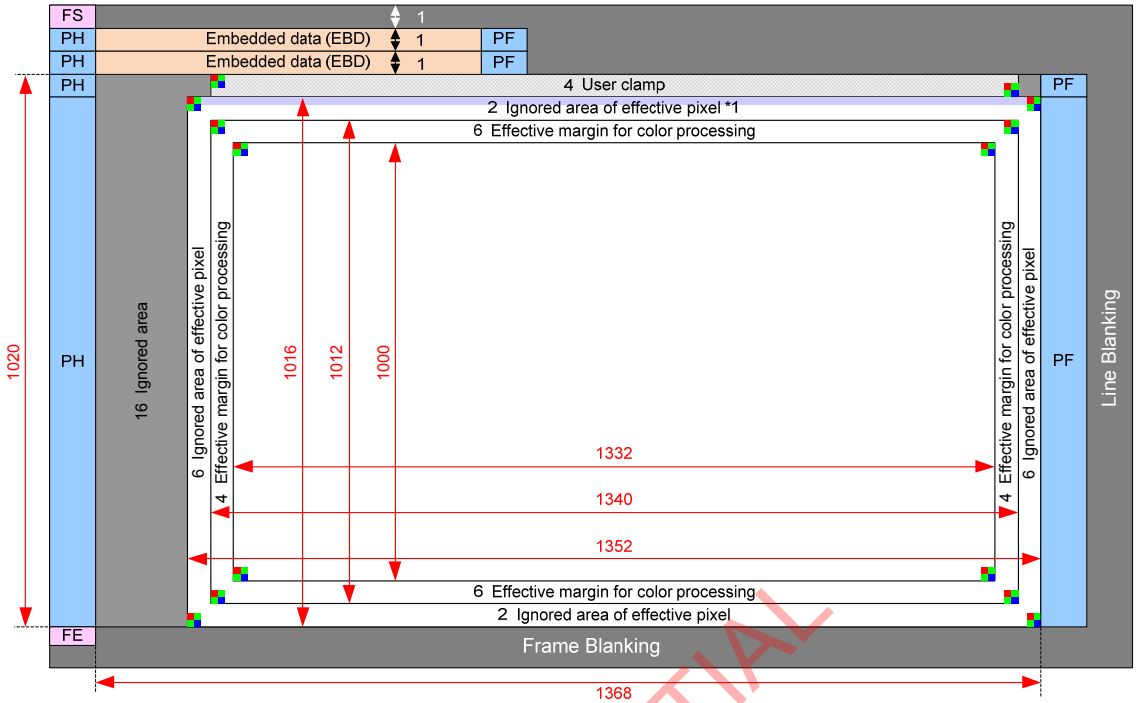
Readout Pixel Image Diagram (2000 × 1500)

MODE3: Horizontal/vertical 3/3-line binning mode (10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1332 × 998)

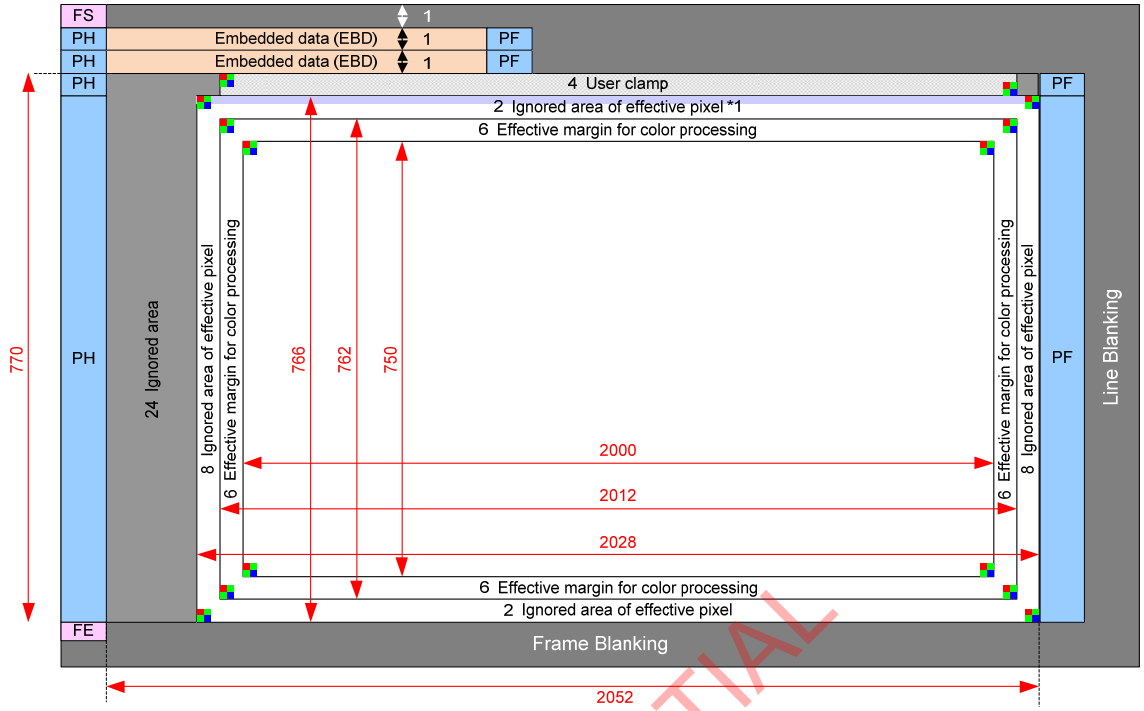
MODE4: Vertical 1/3 subsampling horizontal 3 binning mode (10-bit A/D conversion, 12-bit length output)



*1 When vertical direction normal readout : 2 aperture area
When vertical direction inverted readout : 1 shaded area, 1 aperture area

Readout Pixel Image Diagram (1332 × 1000)

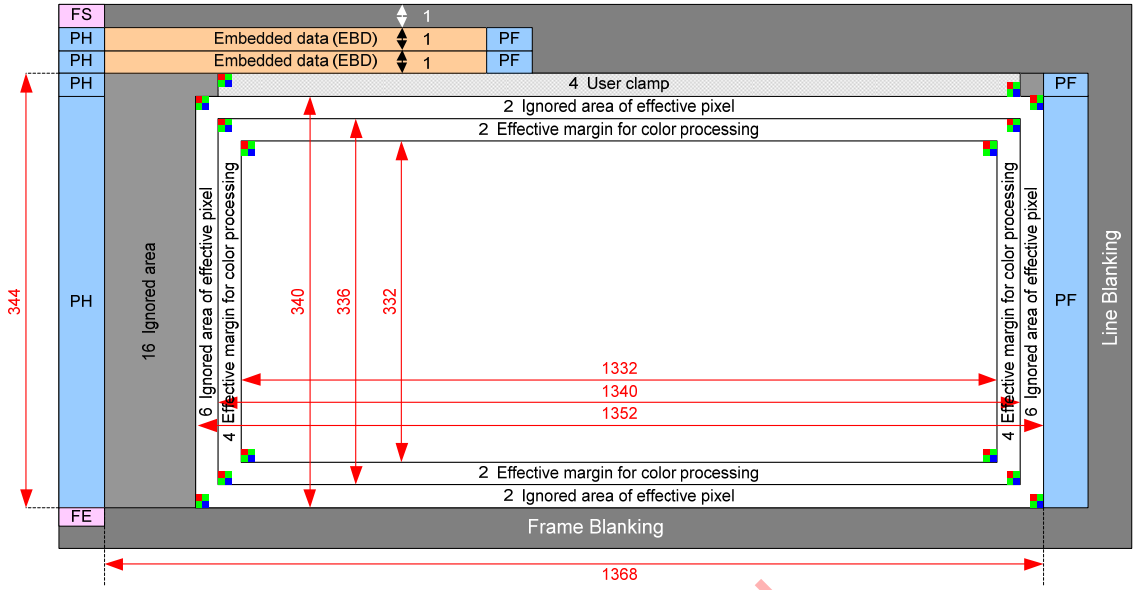
MODE5: Vertical 1/3 subsampling horizontal 2/4 subsampling mode 16:9 cropping (10-bit A/D conversion, 10-bit length output)



*1 When vertical direction normal readout : 2 aperture area
When vertical direction inverted readout : 1 shaded area, 1 aperture area

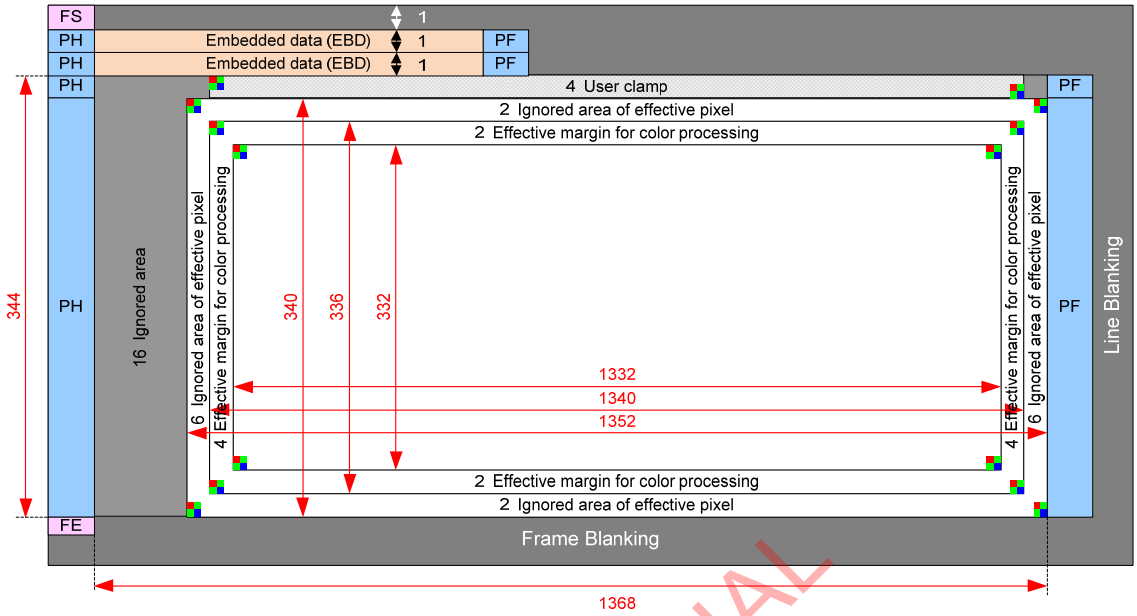
Readout Pixel Image Diagram (2000 × 750)

MODE6: Vertical 2/9 subsampling binning horizontal 3 binning mode (10-bit A/D conversion, 12-bit length output)



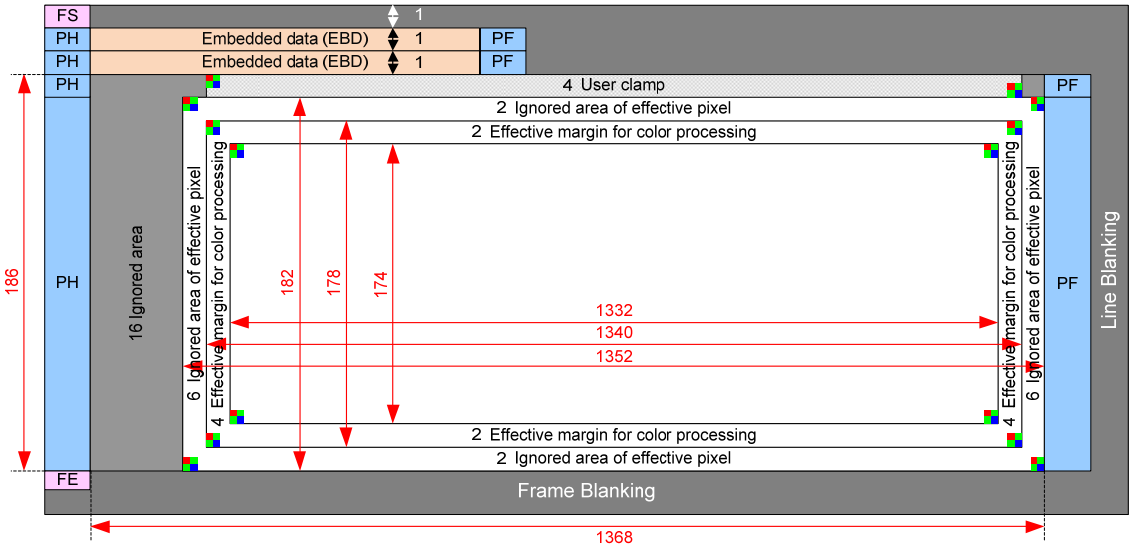
Readout Pixel Image Diagram (1332 × 332)

MODE7: Vertical 2/9 subsampling binning horizontal 3 binning mode
Low power consumption drive
(10-bit A/D conversion, 12-bit output length)



Readout Pixel Image Diagram (1332 × 332)

MODE8: Vertical 2/17 subsampling binning horizontal 3 binning mode (10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1332 × 174)

3-2. When Using Type 1/2.5 Approx. 9.03 M Pixels (Approx. 17:9)

(1) Horizontal/Vertical Operation Period in Each Readout Drive Mode

Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX minimum value
	Front ignore area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	48	14	12	4096	12	18	669
1	48	0	12	3840	12	0	527
1A	48	0	12	3840	12	0	264
2	24	8	6	2048	6	8	260
2A	24	8	6	2048	6	8	260
3	16	6	4	1364	4	6	260
4	16	6	4	1364	4	6	260
6	16	6	4	1364	4	6	260
8	16	6	4	1364	4	6	260

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX minimum value
	Front OPB	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	8	5 *1 6 *2	4	2160	4	0	2220
1	8	5 *1 6 *2	4	2160	4	0	2220
1A	8	5 *1 6 *2	4	2160	4	0	4440
2	4	6	4	1080	4	0	2234
2A	4	6	4	1080	4	0	2234
3	4	6 *1 5 *2	4	720	4	0	2252
4	4	6 *1 5 *2	4	720	4	0	776
6	4	2	2	240	2	0	538
8	4	2	2	124	2	0	306

*1 When vertical direction normal readout.
*2 When vertical direction inverted readout.

(2) NTSC/PAL Compatible Drive

This sensor can be used with a frame frequency that supports NTSC or PAL by using the recommended horizontal operating period (H period) and recommended vertical operating period (V period) for each readout drive mode shown in the table below.

Recommended H Period and V Periods (NTSC/PAL Compatible)

Readout mode No.	NTSC compatible drive			PAL compatible drive		
	Number of HMAX[*1]	Number of VMAX[*2]	Frame frequency [frame/s]	Number of HMAX[*1]	Number of VMAX[*2]	Frame frequency [frame/s]
0	672	3575	29.97	720	4000	25.00
1	528	2275	59.94	576	2500	50.00
1A	264	4550	59.94	288	5000	50.00
2	264	2275	119.88	288	2500	100.00
2A	264	2275	119.88	288	2500	100.00
3	264	2275	119.88	288	2500	100.00
4	264	910	299.70	300	800	300.00
6	264	650	419.58	288	625	400.00
8	264	325	839.16	300	320	750.00

[*1] The value set as HMAX (address 30F5h, bit [7:0] and address 30F6h, bit [7:0]).
[*2] The value set as VMAX (address 30F7h, bit [7:0], address 30F8h, bit [7:0] and address 30F9h, bit [3:0]).

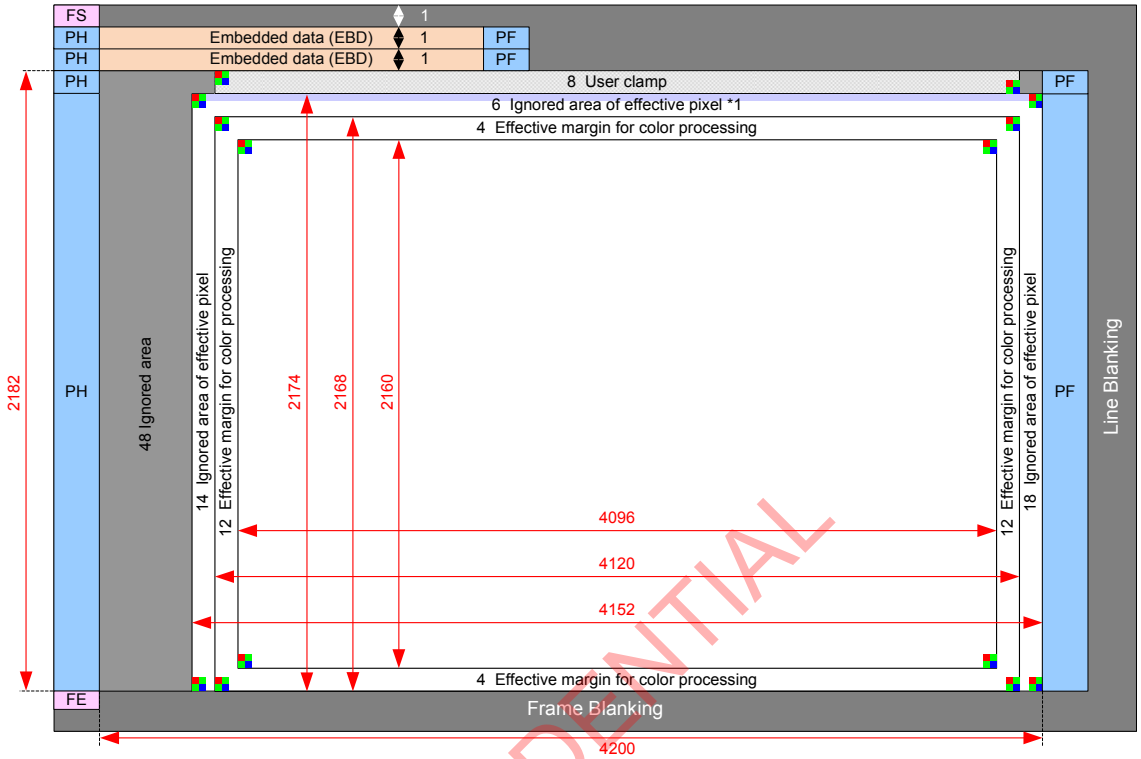
Imaging Conditions in Each Readout Drive Mode (NTSC/PAL Compatible Drive)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/ RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	4	12	RAW12	4096	2160	Approximately 8.85 M Pixels
1	4	10	RAW10	3840	2160	Approximately 8.29 M Pixels
1A	4	10	RAW10	3840	2160	Approximately 8.29 M Pixels
2	4	10	RAW12	2048	1080	Approximately 2.21 M Pixels
2A	4	10	RAW12	2048	1080	Approximately 2.21 M Pixels
3	4	10	RAW12	1364	720	Approximately 0.98 M Pixels
4	4	10	RAW12	1364	720	Approximately 0.98 M Pixels
6	4	10	RAW12	1364	240	Approximately 0.33 M Pixels
8	4	10	RAW12	1364	124	Approximately 0.17 M Pixels

(3) Image Data Output Format

The output format in each readout drive mode is as follows.

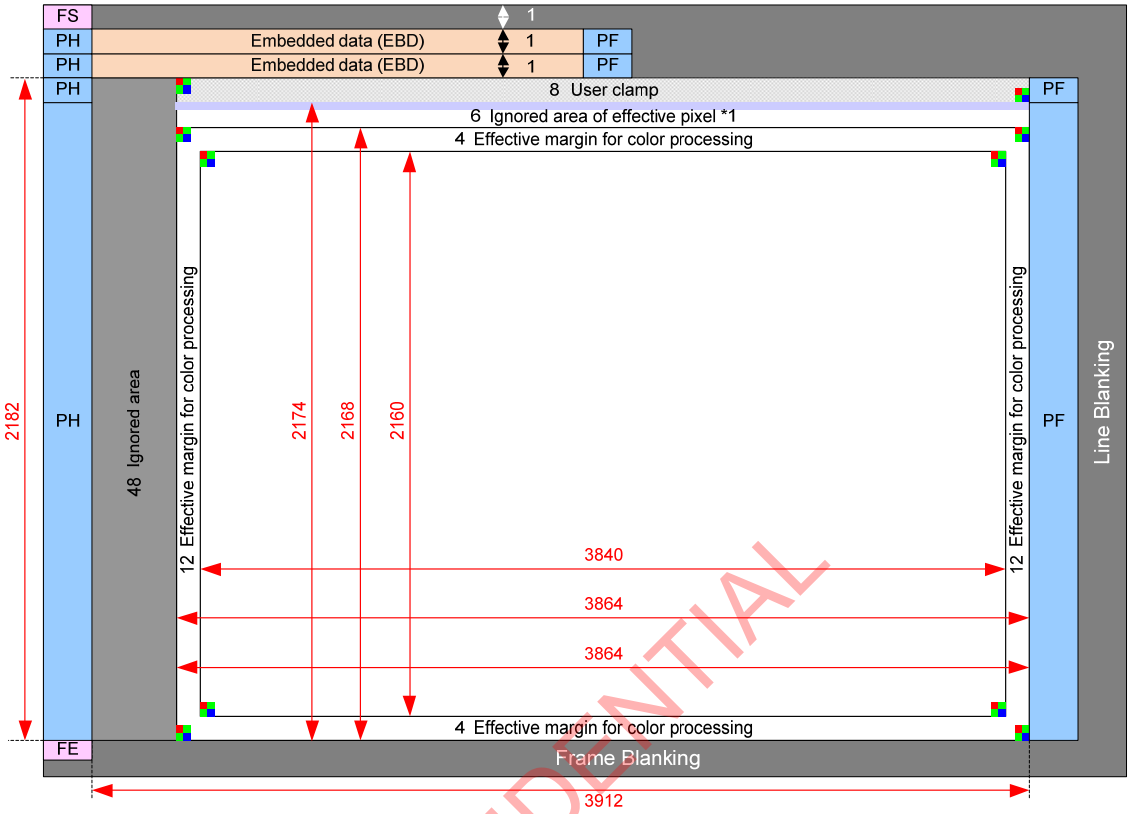
MODE0: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)



*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4096 × 2160)

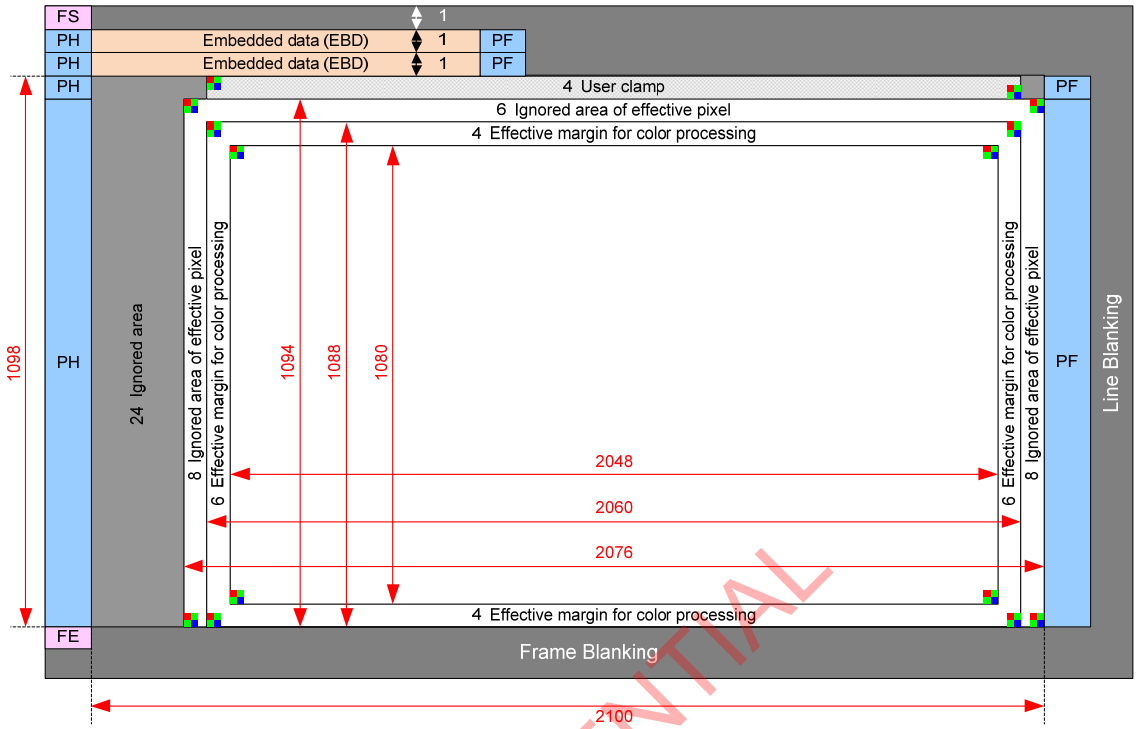
MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)
MODE1A: All-pixel scan mode low power consumption drive (10-bit A/D conversion, 10-bit length output)



*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

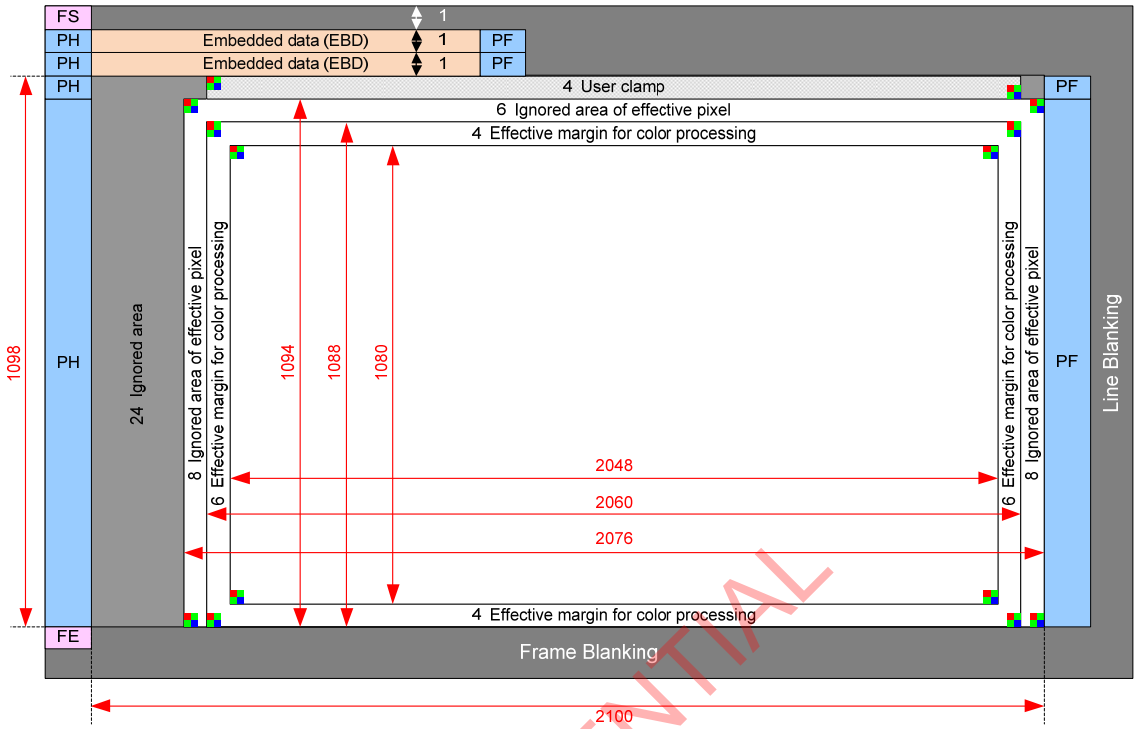
Readout Pixel Image Diagram (3840 × 2160)

MODE2: Horizontal/vertical 2/2-line binning mode
(horizontal and vertical weighted binning)
(10-bit A/D conversion, 12-bit length output)



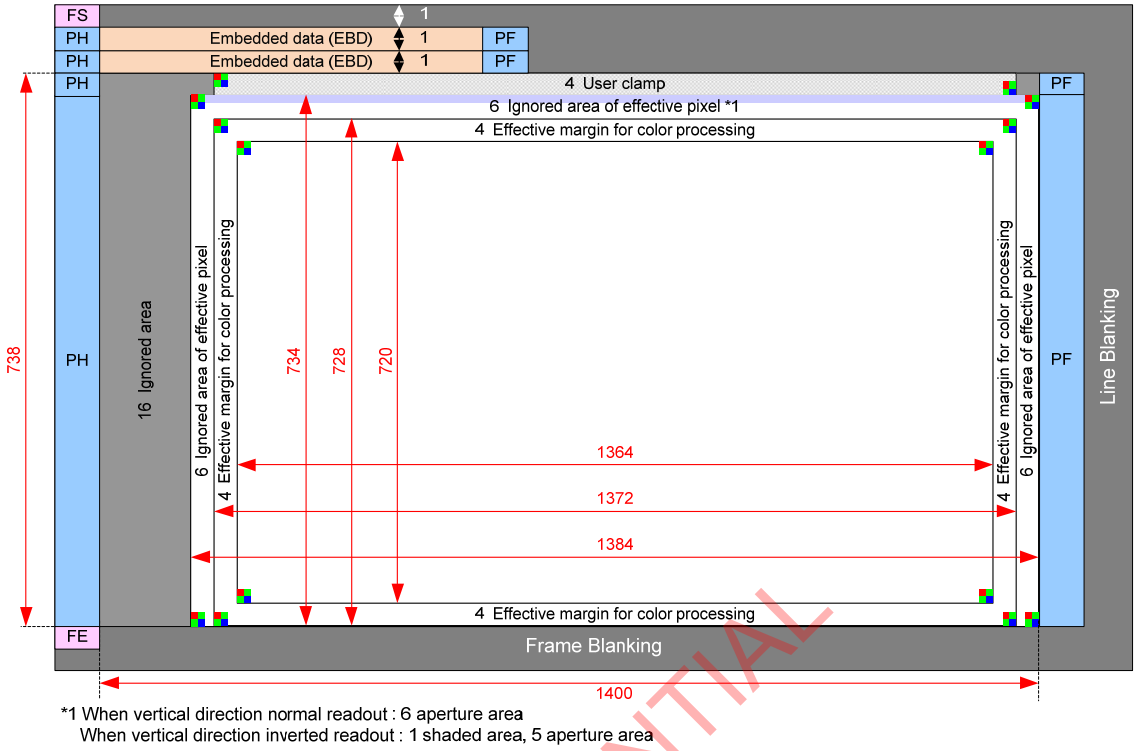
Readout Pixel Image Diagram (2048 × 1080)

MODE2A: Vertical 2 binning horizontal 2/4 subsampling mode
(vertical weighted 2 binning)
(10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (2048 × 1080)

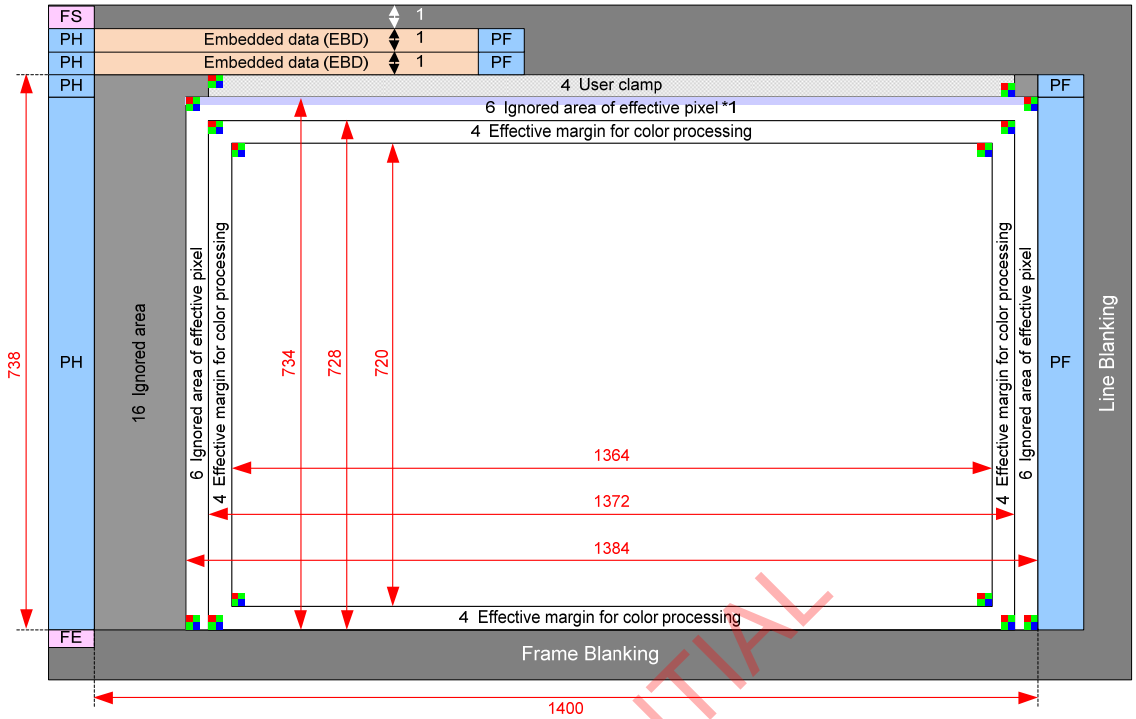
MODE3: Horizontal/vertical 3/3-line binning mode (10-bit A/D conversion, 12-bit length output)



*1 When vertical direction normal readout : 6 aperture area
When vertical direction inverted readout : 1 shaded area, 5 aperture area

Readout Pixel Image Diagram (1364 × 720)

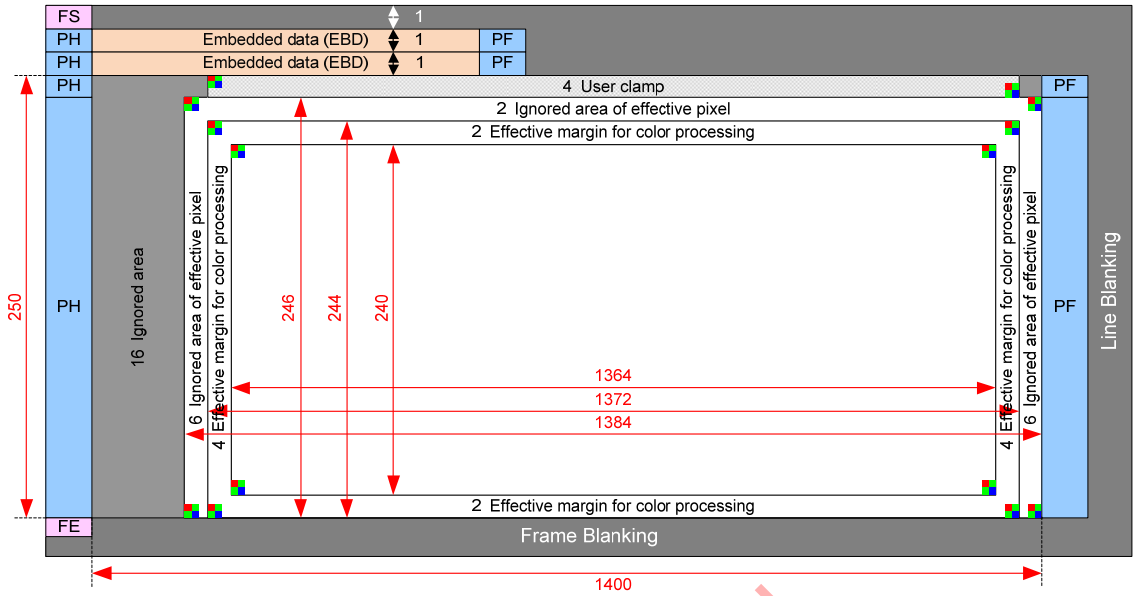
MODE4: Vertical 1/3 subsampling horizontal 3 binning mode (10-bit A/D conversion, 12-bit output length)



*1 When vertical direction normal readout : 6 aperture area
When vertical direction inverted readout : 1 shaded area, 5 aperture area

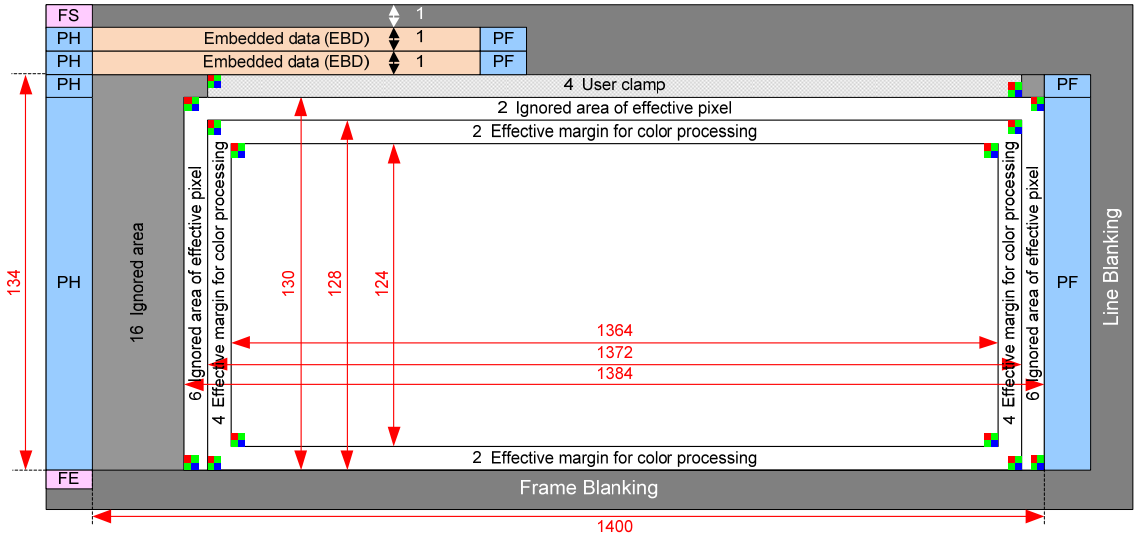
Readout Pixel Image Diagram (1364 × 720)

MODE6: Vertical 2/9 subsampling binning horizontal 3 binning mode (10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1364 × 240)

MODE8: Vertical 2/17 subsampling binning horizontal 3 binning mode (10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1364 × 124)

3-3. Vertical Arbitrary Cropping Function

Vertical cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings

Enable vertical cropping with setting vertical arbitrary cropping enable register VWIDCUTEN (address 30D5h, bit [0]) to 1h, and specify cropping width by the vertical cropping width register VWIDCUT (address 30D6h, bit [7:0] and address 30D7h, bit [2:0]), and cropping position by the vertical cropping start position register VWINPOS (address 30D8h, bit [7:0] and address 30D9h, bit [3:0]).
And set the number of total output lines (including VOB) after cropping to the register MDSEL9 (address 312Fh, bit [7:0] and address 3130h, bit [4:0]), and the number of effective pixel lines (not including VOB) after cropping to the register MDSEL10 (address 3131h, bit [7:0] and address 3132h, bit [4:0]).
Set VWINPOS negative value (two's complement) when the direction of vertical readout is inverted (address 301Ah, bit[0], MDVREV = 1h)
V_{eff} indicates the number of effective lines output before cropping (VWIDCUTEN = 0h) in following description.

VWIDCUTEN Setting

Register value	Function
0h	Vertical arbitrary cropping is disabled
1h	Vertical arbitrary cropping is enabled

VWIDCUT Setting

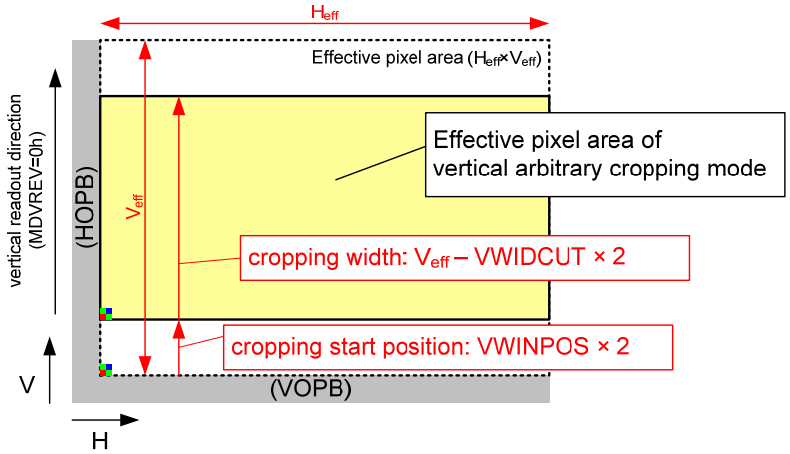
Register value	Function
0 to 2047	Specify vertical cropping width Veff - VWIDCUT × 2 [line]

VWINPOS Setting

Register	Function
VWINPOS	Vertical cropping start position (two's complement)

When vertical readout direction is normal (MDVREV = 0h), relation between register setting values of VWINPOS / VWIDCUT and cropping region on physical pixel array is shown below.
Register setting values must satisfy following relations. (Setting ranges are within those values which satisfy following.)

$VWINPOS \times 2 \geq 0$ (Starting position of readout must be 0 or more)
$V_{eff} - VWIDCUT \times 2 \geq V_{eff} / 2$ (Number of readout lines must be 1/2 or more before cropping)
$(VWINPOS \times 2) + V_{eff} - VWIDCUT \times 2 \leq V_{eff}$ (End position of readout must be within the area before cropping)

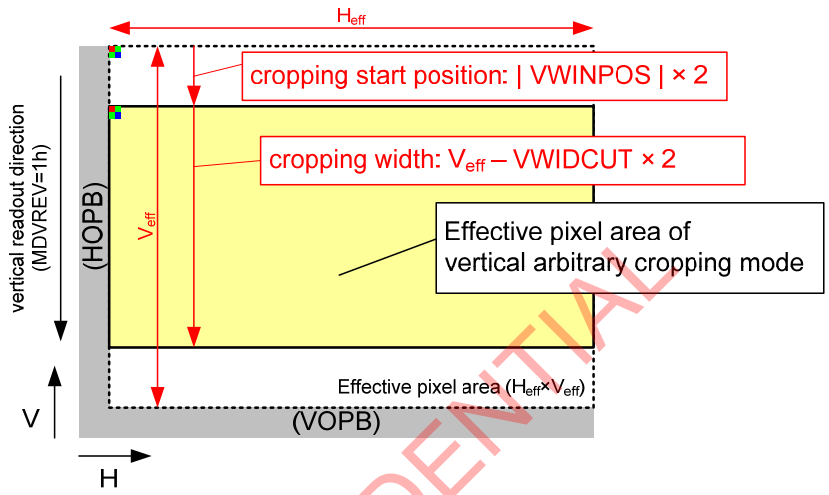


Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array
(Vertical Readout Direction Normal)

For example, when the top 400 lines and bottom 400 lines (totally 800 lines) of all-pixel scan area is skipped and start cropping readout from the 401st line, setting values are as follows:
VWIDCUT 190h (400d) / VWINPOS 0C8h (200d) / MDSEL9 8D6h (2262d) / MDSEL10 8C6h (2246d)

When vertical readout direction is inverted (MDVREV = 1h), relation between register setting value of VWINPOS / VWIDCUT and cropping region is shown below. Register setting values must satisfy following relations also.
Note that VWINPOS must be negative.

$| VWINPOS | \times 2 \geq 0$ (Starting position of readout must be 0 or more)
$V_{eff} - VWIDCUT \times 2 \geq V_{eff} / 2$ (Number of readout lines must be 1/2 or more before cropping)
$(| VWINPOS | \times 2) + V_{eff} - VWIDCUT \times 2 \leq V_{eff}$ (End position of readout must be within the area before cropping)



Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array
(Vertical Readout Direction Inverted)

For example, when the top 400 lines and bottom 400 lines (total 800 lines) of all-pixel scan area (when vertical readout direction inverted) is skipped and start cropping readout from the 401st line, setting values are as follows:
VWIDCUT 190h (400d) / VWINPOS F38h (-200d) / MDSEL9 8D6h (2262d) / MDSEL10 8C6h (2246d)

(2) Vertical Minimum Period When Using Vertical Arbitrary Cropping Function

When using vertical arbitrary cropping function, VMAX minimum value gets smaller according to cropping width. The table below shows VMAX minimum value after cropping when VMAX minimum value before cropping is represented as V_{MAX0}.

VMAX Minimum Value When Using Vertical Arbitrary Cropping Function

Readout mode No.	VMAX minimum value
0, 1, 4, 5	$V_{MAX0} - VWIDCUT \times 2$
1A, 2, 2A, 6, 7, 8	$V_{MAX0} - VWIDCUT \times 4$
3	$V_{MAX0} - VWIDCUT \times 6$

3-4. Horizontal Arbitrary Cropping Function

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings

Set horizontal cropping enable register HTRIMMING_EN (address 3040h, bit [0]) to 1h to enable horizontal arbitrary cropping function, and horizontal cropping area are determined by horizontal cropping position register HTRIMMING_START (address 303Eh, bit [7:0] and address 303Fh, bit [4:0]) and HTRIMMING_END (address 3039h, bit [7:0] and address 303Ah, bit [4:0])

HTRIMMING_EN Setting

Register value	Function	Remarks
0	Horizontal arbitrary cropping OFF	Send with register setting for each readout drive mode.
1	Horizontal arbitrary cropping ON	

Horizontal Arbitrary Cropping Position Setting

Register	Function	Remarks
HTRIMMING_START	horizontal cropping start position[*1] + 48	Unit: pixel Send with register setting for each readout drive mode.
HTRIMMING_END	horizontal cropping end position[*1] + 48 + 1	

[*1] In the readout mode with horizontal binning or subsampling, set the value of HTRIMMING_START and HTRIMMING_END according to the position before processing horizontal binning or subsampling.

HTRIMMING_START and HTRIMMING_END must satisfy following 3 restrictions.

HTRIMMING_START = 48 + N × step
HTRIMMING_END = HNUM – M × step
HTRIMMING_END – HTRIMMING_START ≥ 240
(M and N are integers equal or more than 0)

Refer to the following tables in the value of step and HNUM.

step value

Readout mode Horizontal pixel processing	no binning 2/4 subsampling	2 binning	3 binning
step	12	8	12

HNUM value

Readout mode	Type 1/2.3 approx. 12.35 M pixels	Type 1/2.5 approx. 9.03 M pixels	
	No.0 to 8	No.0, 2, 2A, 3 to 8	No.1, 1A
HNUM	4104	4200	3912

(2) Horizontal Minimum Period When Using Horizontal Arbitrary Cropping Function

When using horizontal arbitrary cropping function, HMAX minimum value is as follows:

HMAX Minimum Value When Using Horizontal Arbitrary Cropping Function

Readout mode No.	HMAX minimum value
0	max (507, [HTRIMMING_END - HTRIMMING_START] × 3/20 + 46.2)
1	max (260, [HTRIMMING_END - HTRIMMING_START] × 1/8 + 44.0)
1A	max (260, [HTRIMMING_END - HTRIMMING_START] × 1/16 + 22.0)
2	260
2A	260
3	260
4	260
5	max (260, [HTRIMMING_END - HTRIMMING_START] × 1/8 + 41.0)
6	260
7	260
8	260

* max (A, B) means the larger value of A and B.
* Fractions should be rounded up.

Integration Time in Each Readout Drive Mode and Mode Changes

1. Integration Time in Each Readout Drive Mode

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR and SVR. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

◆ **Integration time of normal readout drive mode**

Integration Time [s] = [{VMAX value × (SVR value + 1) – SHR value}
× HMAX value + Number of clocks per internal offset period] / (72 x 10^6)

* See the following tables for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page 32 of the SHR register setting range.

◆ **Integration time of low power consumption drive mode (Mode No.7)**

Integration Time [s] = [{VMAX value × (SVR value + 1) – SHR value × 4}
× HMAX value + Number of clocks per internal offset period] / (72 x 10^6)

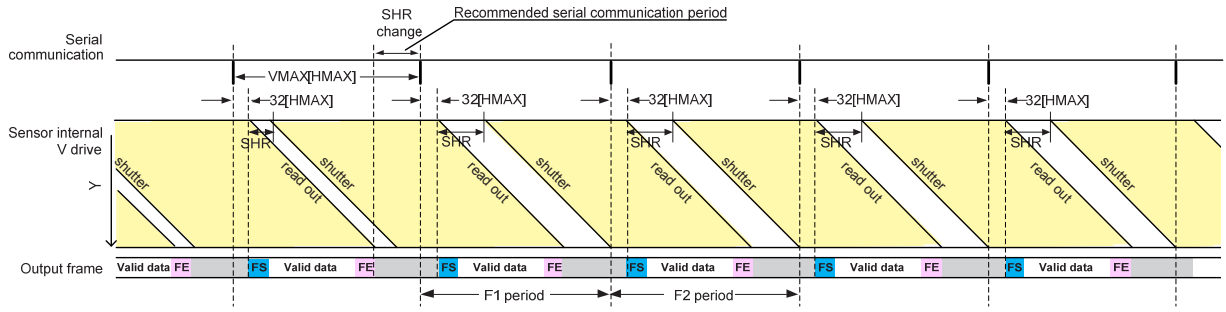
* See the following tables for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page 32 of the SHR register setting range.

Number of clocks per internal offset period

Readout mode No.	0	1	1A	2	2A	3	4	5	6	7	8
Number of clocks per internal offset period	174	117	117	117	117	117	117	117	117	117	117

The figure below shows operation when SHR is being changed and REGHOLD is 0h. The F1 and F2 periods in the figure below are two continuous frames. The SHR value which is set in the recommended serial communication period[*1] just before F1 period is updated internally at the end of the communication period and then output data which reflect the new setting is output in the F2 period. Note that the SHR setting and output are offset by a frame.

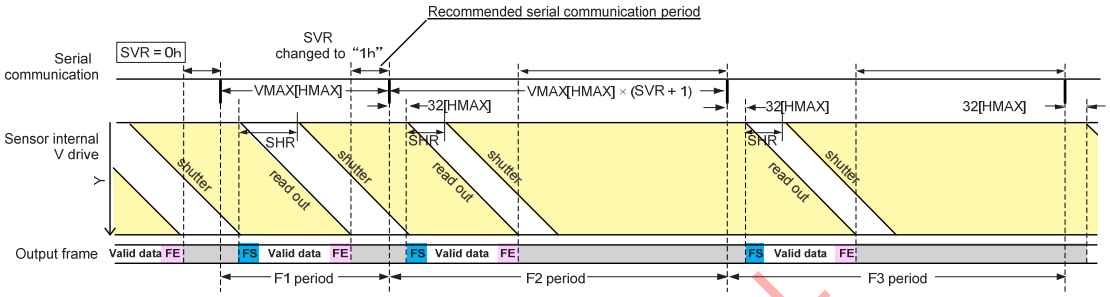
[*1] Refer to "Register Communication Timing" on page 20.



SHR Change Sequence

The internal vertical drive period which is set by the VMAX register can be subsampled by the SVR register. Its period is (SVR value + 1) times as long as VMAX period. Therefore the frame rate is multiplied by 1/(SVR value + 1).
The figure below shows the operation when the SVR register is being changed from “0h” to “1h” and REGHOLD is 0h. The SVR value, which is set in the recommended serial communication period[*1] just before F2 period, is updated internally at the end of the communication period and then applied from the shutter operation in the F2 period. The output data which reflect the changing of SVR is output in the F3 period.
The image data of the F1 period before the SVR value is changed is output as valid data in the F2 period.

[*1] Refer to "Register Communication Timing" on page 20.



SVR Change Sequence

2. Operation when Changing the Readout Drive Mode

When changing input INCK or CSI-2 output frequency (register SYS_MODE), follow the below procedure.

1st step : Enter the sensor standby mode
2nd step : Change the frequency during standby mode.
3rd step : Follow the standby cancel sequence to resume the normal operation.

When changing input INCK frequency, don't input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low. Then set the state of XCLR to High, following the item of "Power on sequence" in the section of "Power on / off sequence" in page 84. Execute “Standby Cancel Sequence” again because the register settings become default state after system reset.

The following mode change cases are treated as a mode transition on this sensor and one frame of invalid data is generated.

1. Changing the readout mode setting
2. Changing the vertical direction readout setting
3. Changing the vertical arbitrary cropping setting

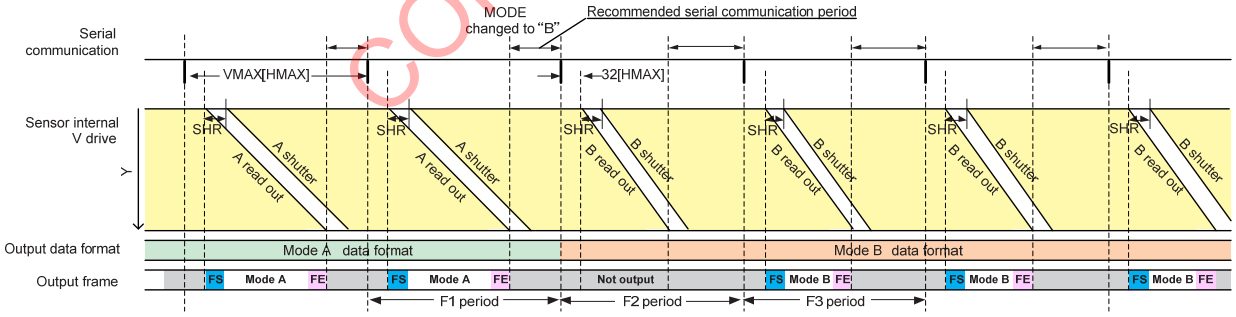
* Changing the horizontal arbitrary cropping setting is not treated as mode transition and no invalid data is generated.

The figure below shows the mode transition sequence, Mode A to Mode B, in case that the mode transition is performed in three continuous frames, F1 to F3, and REGHOLD is 0h.

(1) Set the register setting for Mode B in the recommended serial communication period[*1] just before F2 period. F2 period data is not output.
(2) Valid data which reflect the new setting is output from the next frame (F3 period).

[*1] Refer to "Register Communication Timing" on page 20.

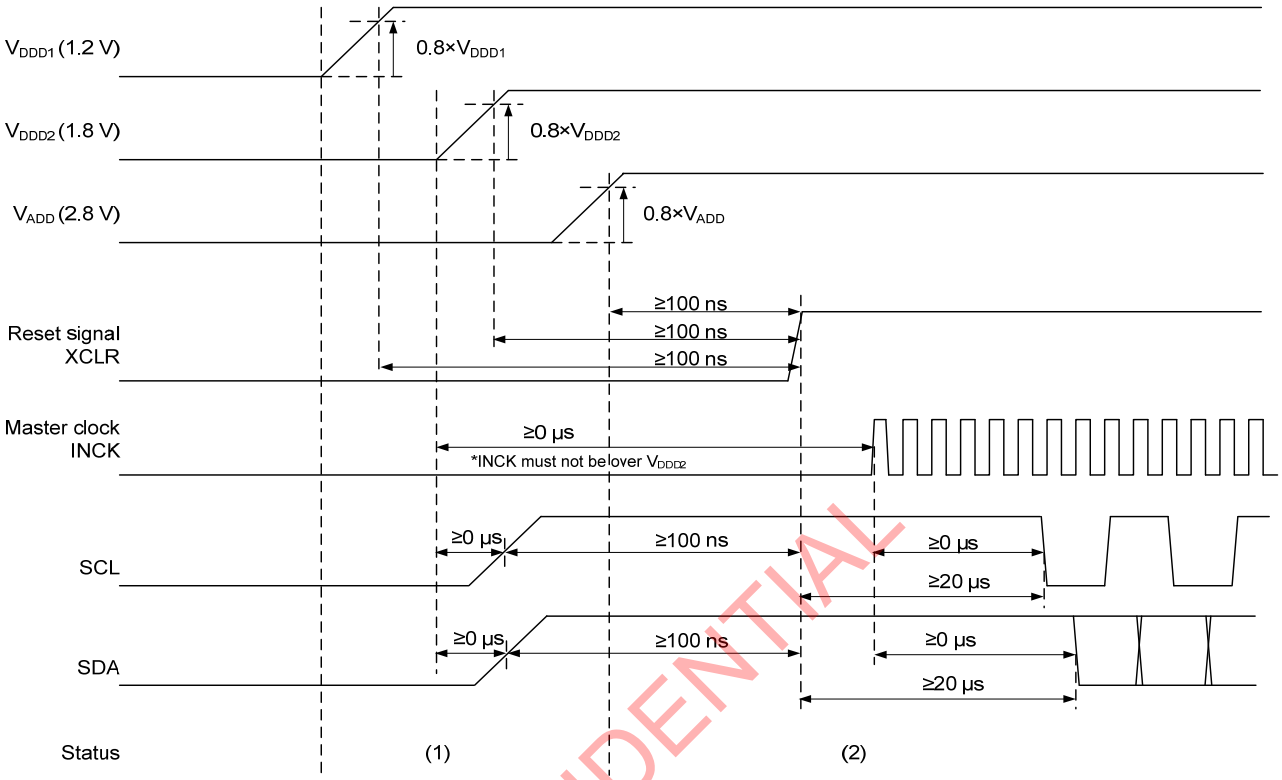
In addition, note that when the output data length differs between Mode A and Mode B, the new data format is output from the start of F2 period in which the setting is changed to Mode B.



Mode Transition

Power-on/off Sequence

1. Power-on Sequence

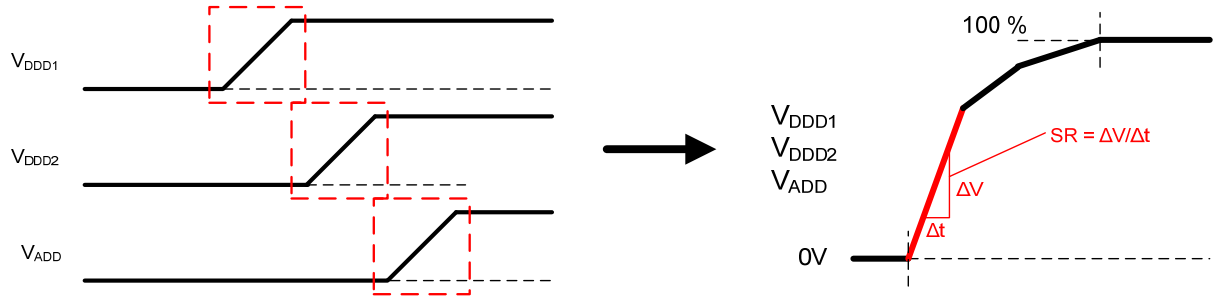


Power-on Sequence

Period name	Remarks
(1) Power stabilization period	All input signals are set to Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1} and V_{DDD2}.
(2) Register communication period for standby cancel	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1} and V_{DDD2}. Then set XCLR to “H” and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence

Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.

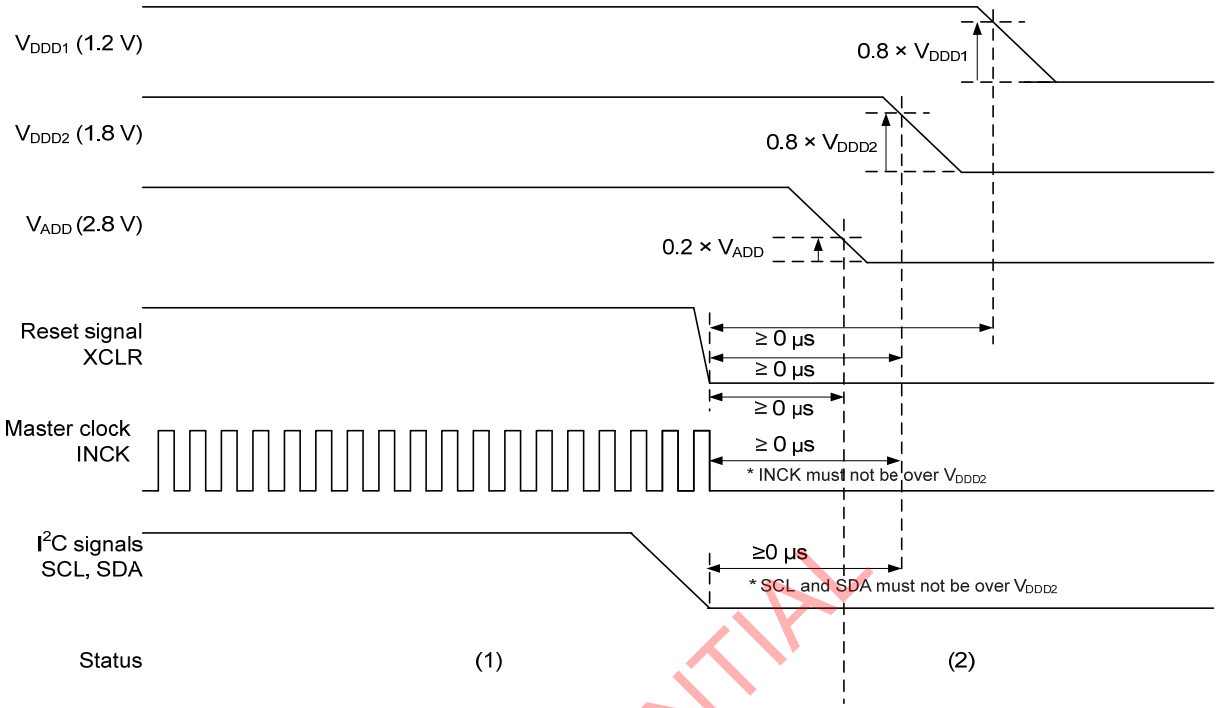


Slew rate of power supply

Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/μs	
		V_{DDD2} (1.8 V)	—	25	mV/μs	
		V_{ADD} (2.8 V)	—	25	mV/μs	

3. Power-off Sequence

Make sure that all input signals are set to LOW level in the area of (2).



Power-off Sequence

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DDD2}. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, and V_{DDD2}.

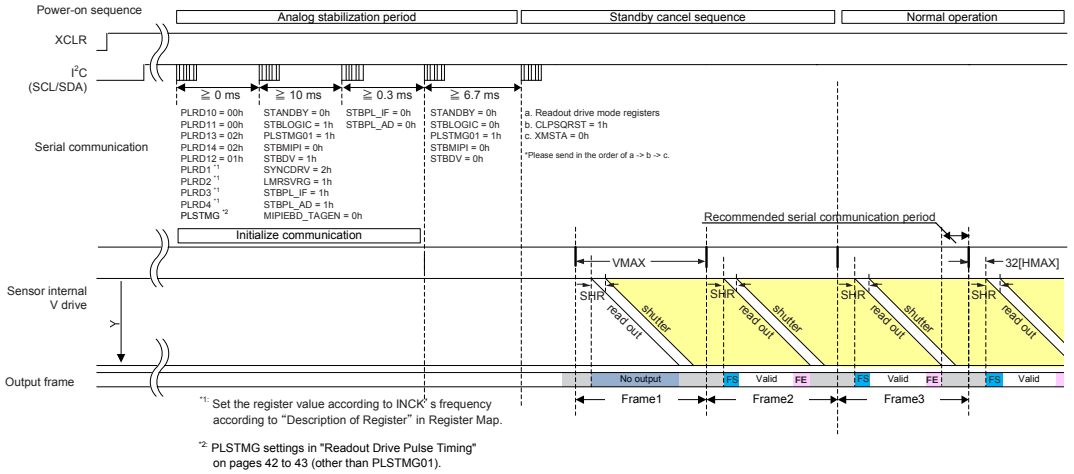
Standby Cancel Sequence

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancels sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, make the following register setting.
   - Set address 3123h, bit [7:0] to “00h” (PLRD10 register = 00h).
   - Set address 3124h, bit [7:0] to “00h” (PLRD11 register = 00h).
   - Set address 3127h, bit [7:0] to “02h” (PLRD13 register = 02h).
   - Set address 312Dh, bit [7:0] to “02h” (PLRD14 register = 02h).
   - Set address 3125h, bit [7:0] to “01h” (PLRD12 register = 01h).

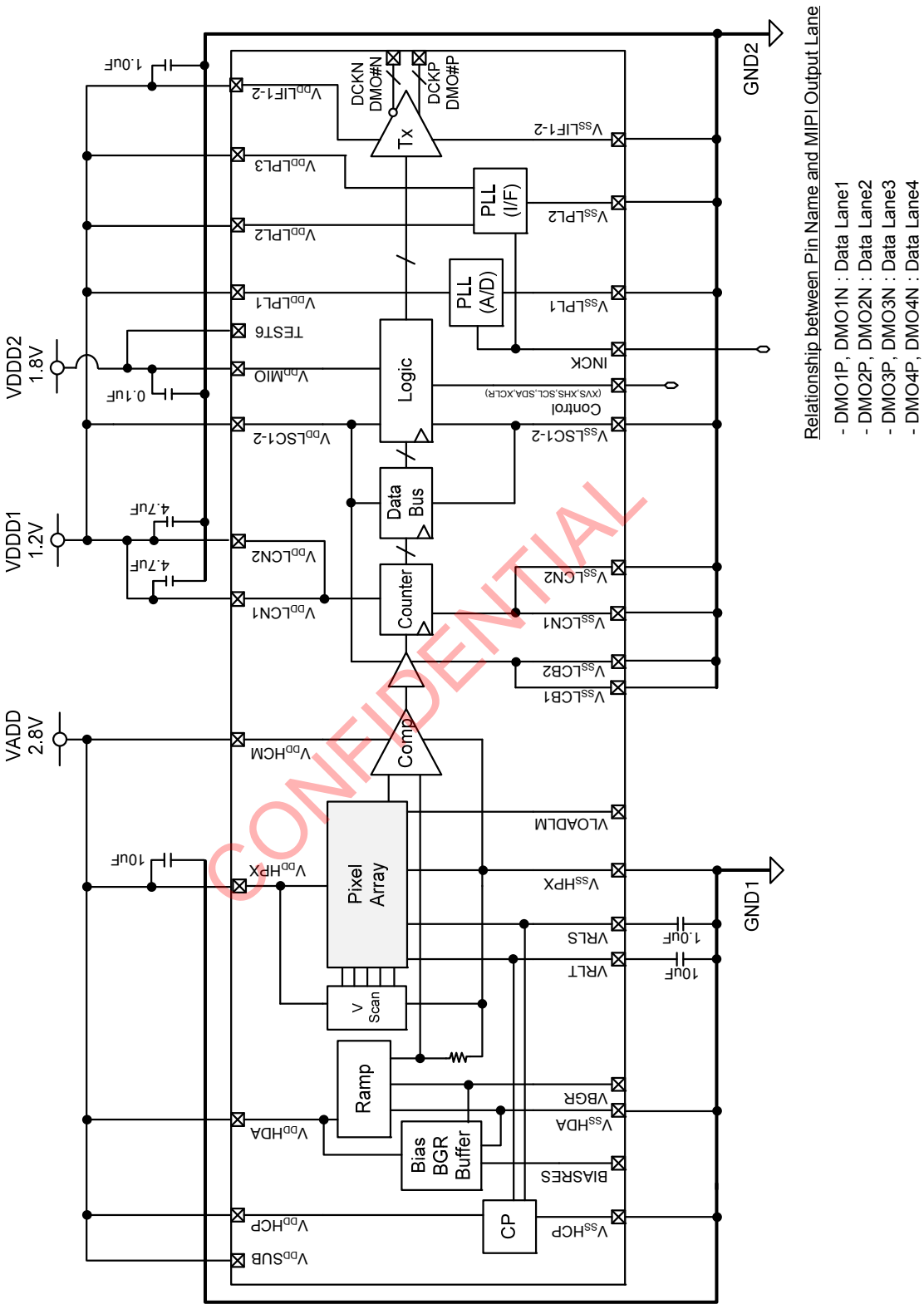
   Set the following registers to the appropriate value according to INCK's frequency.
   Refer to “Description of Register” of “Register Map” on page 31.
   - Address 3120h, bit [7:0], Address 3121h, bit [7:0] (PLRD1 register).
   - Address 3129h, bit [7:0] (PLRD2 register).
   - Address 3122h, bit [7:0] (PLRD3 register).
   - Address 312Ah, bit [7:0] (PLRD4 register)

   Initialize communication
   Set all registers of PLSTMG settings in "Readout Drive Pulse Timing" on pages 38 to 39 (other than PLSTMG01). Register communication can be performed even when STANDBY register is 1h and there is no restriction on the communication order.
2. After the 1st stabilization period, make the following register setting.
   - Set address 3000h, bit [4:0] to “16h” (STANDBY register = 0h, STBLOGIC register = 1h, PLSTMG01 register = 1h, STBMIPI register = 0h as default, STBDV register = 1h).
   - Set address 3018h, bit [1:0] to “2h” (SYNCDRV register = 2h).
   - Set address 3399h, bit [7:0] to “01h” (LMRSVRG register = 01h).
   - Set address 310Bh, bit [7:0] to “11h” (STBPL_IF register = 1h, STBPL_AD register = 1h).
   - Set address 3A56h, bit [0] to “0h” (MIPIEBD_TAGEN register = 0h).
3. After the 2nd stabilization period of 10 ms or more, make the following register setting.
   - Set address 310Bh, bit [7:0] to “00h” (STBPL_IF register = 0h, STBPL_AD register = 0h).
4. After the 3rd stabilization period of 0.3 ms or more, make the following register setting.
   - Set address 3000h, to “04h” (STANDBY register = 0h, STBLOGIC register = 0h, PLSTMG01 register = 1h, STBMIPI register = 0h, STBDV register = 0h).
5. After the 4th stabilization period of 6.7 ms or more, make the following register setting in the order of a -> b -> c.
   -a. Readout drive mode registers
   Set the mode registers of the "Register Setting for Each Readout Drive Mode" on pages 40 to 43. Furthermore, set the required shutter and gain registers.
   -b. Set address 3001h, bit [4] to “1h” (CLPSQRST register = 1h)
   -c. Set address 30F4h, bit [0] to “0h” (XMSTA register = 0h).



Standby Cancel Sequence

Peripheral Circuit Diagram



Peripheral circuit diagram

Note) Locate a bypass capacitor for each pin. Note that even when pins have the same voltage, connecting the power supply wiring before these capacitors produces a common impedance and may result in unexpected trouble.

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

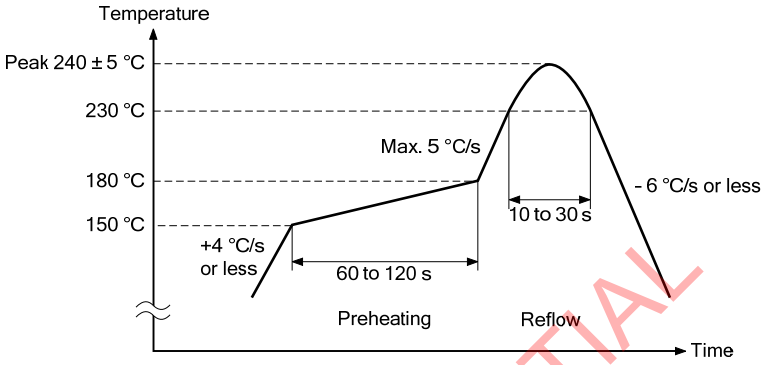
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (– 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



Reflow profile

(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

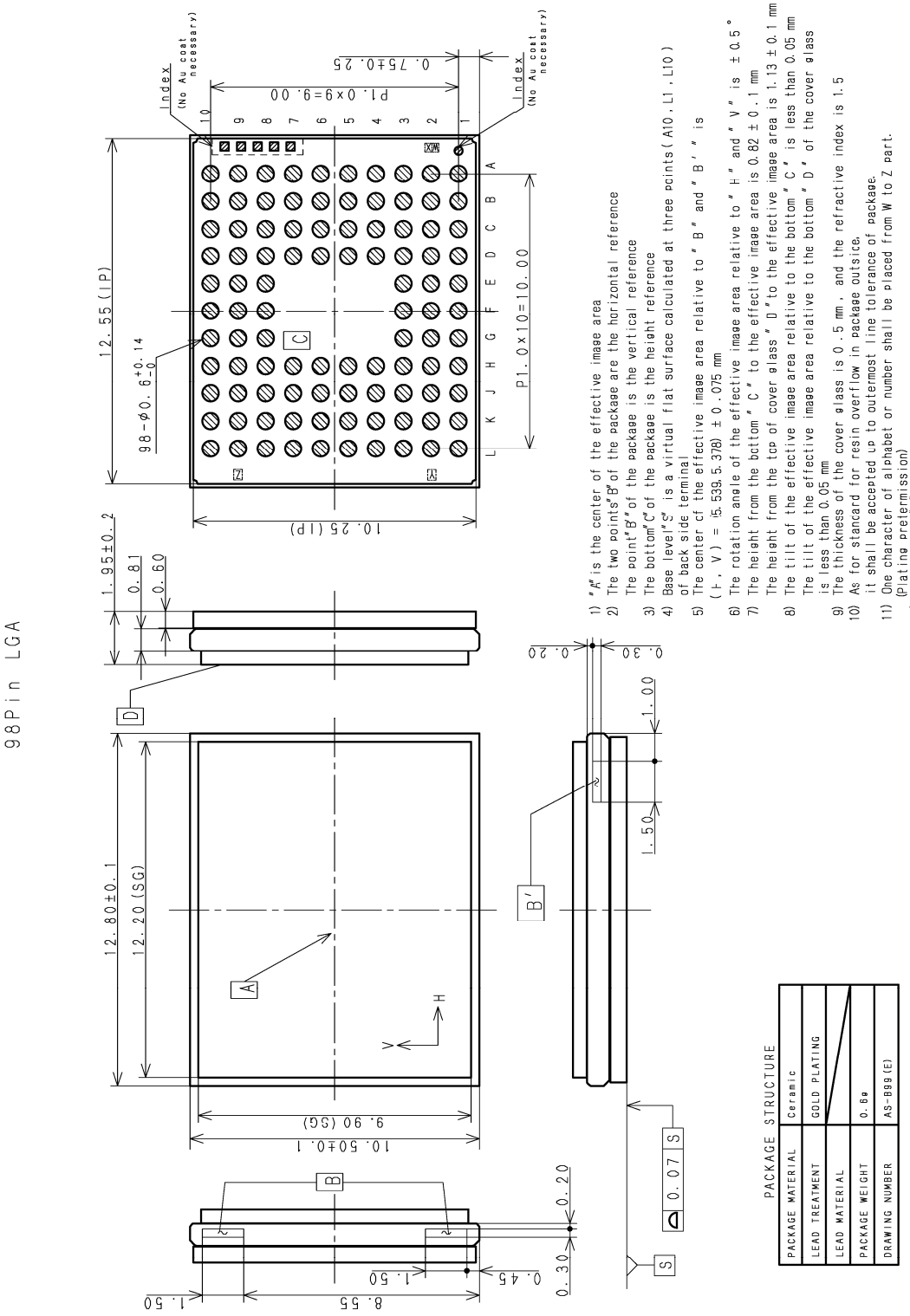
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.6

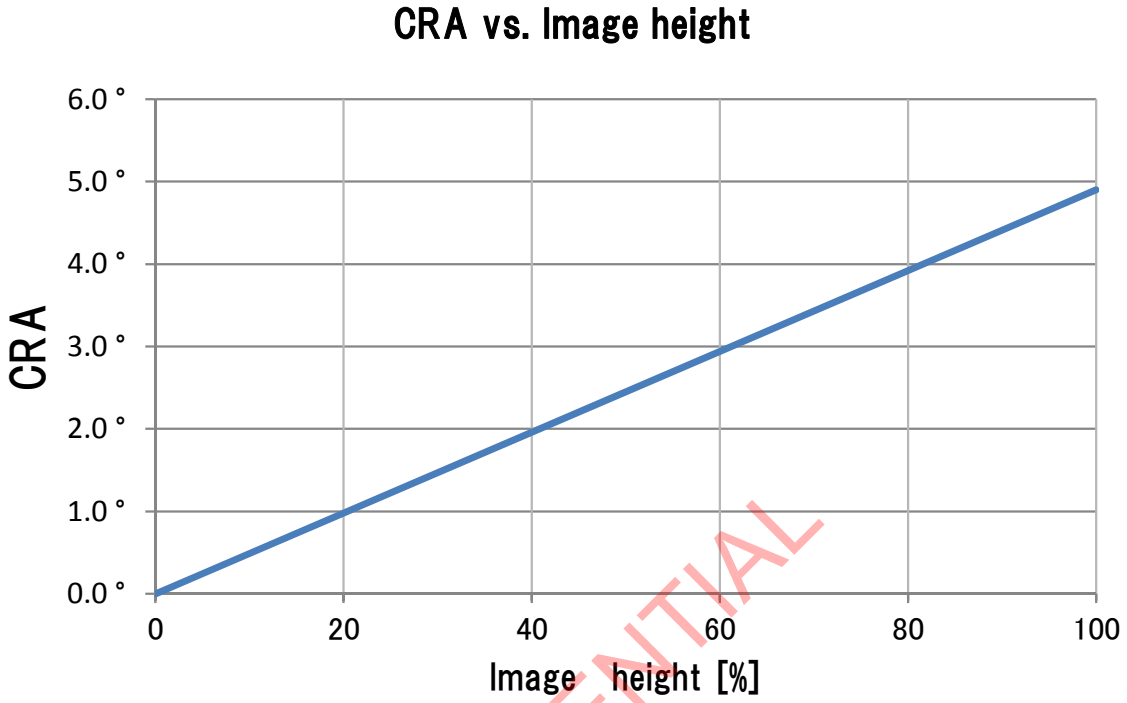
Package Outline

(Unit: mm)



Package Outline

Relation between Image Height and target CRA



Relation between image height and target CRA

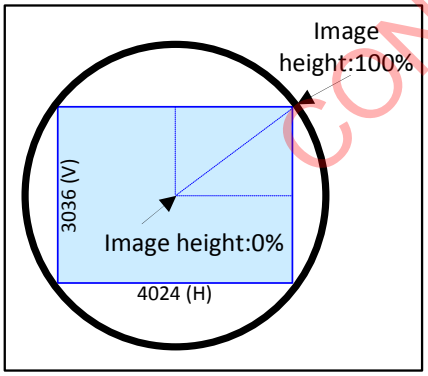
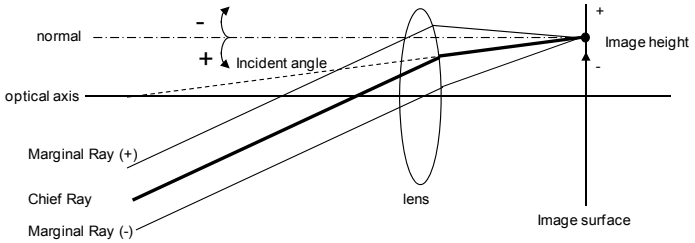


Image height



Incident ray angle

List of Trademark Logos and Definition Statements

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.