Rockchip RK3126 Datasheet

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Revision History

Date	Revision	Description
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Chapter 1 Introduction

RK3126 is a high performance Quad-core application processor for tablet. It is a high-integration and cost efficient SOC.

Quad-core Cortex-A7 is integrates with separately Neon and FPU coprocessor, also shared 256KB L2 Cache. Mali400 MP2 GPU is embedded to support smoothly high-resolution (1080p) display and mainstream game.

Lots of high-performance interface to get very flexible solution, 16bits DDR3 provides high memory bandwidths for high-performance.

1.1 Features

1.1.1 Microprocessor

- Quad-core ARM Cortex-A7MP Core processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Separately Integrated Neon and FPU per CPU
- 32KB/32KB L1 I-Cache/D-Cache per CPU
- Unified 256KB L2 Cache

1.1.2 Memory Organization

- Internal on-chip memory
  - 16KB BootRom
  - 8KB internal SRAM
- External off-chip memory①
  - DDR3-1066/DDR3L-1066, 16bits data width, totally 1GB(max) address space
  - Async/Toggle/SyncNand Flash(include LBA Nand), 8bits data width,4 banks, 60bits ECC

1.1.3 Internal Memory

- Internal BootRom
  - Size : 16KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - 8bits Toggle Nand Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 8KB

1.1.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L)

- Compatible with JEDEC standard DDR3/DDR3L SDRAM
- Data rates up to 1066Mbps(533MHz) for DDR3/DDR3L
- Supports totally 1GB (max) address space.
- 7 host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
- Programmable timing parameters to support DDR3/DDR3L SDRAM from various vendor
- Advanced command reordering and scheduling to maximize bus utilization
- Low power modes, such as power-down and self-refresh for DDR3/DDR3L SDRAM; Compensation for board delays and variable latencies through programmable pipelines
- Programmable output and ODT impedance with dynamic PVT compensation

- Nand Flash Interface
  - Support 8bits async/toggle/sync nand flash, up to 4 banks
  - Support LBA nand flash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For Sync Toggle nand flash, support DLL bypass and 1/4 or 1/8 clock adjust
  - For async/togglenandflash, support configurable interface timing, maximum data rate is 16bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.5 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD2.0, MMC ver 4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.5 System Component

- CRU (clock & reset unit)

- Support clock gating control for individual components inside RK3126
- One oscillator with 24MHz clock input and 4 embedded PLLs
- Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 2 separate voltage domains
  - 3 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 6 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with four 64-bits AXI masters, one 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with three 128-bits AXI master, four 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master with point-to-point AXI-lite architecture and 32-bits APB slave
    - VCODEC interconnect also with two 64-bits AXI master and two 32-bits AHB slave, they are point-to-point AXI-lite architecture

- Flexible different OS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 74 SPI interrupt sources input from different components inside RK3126
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ)separatelyfor each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - One embedded DMA controller PERI_DMAC for peripheral system
  - PERI_DMAC features:
    - 8 channels totally
    - 16 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

1.1.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264,VC-1, RV, VP6/VP8, Sorenson Spark, MVC
  - MMU Embedded
  - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 4.2 : 1080p@60fps
  - MPEG-4 up to ASP level 5 : 1080p@60fps
  - MPEG-2 up to MP : 1080p@60fps
  - MPEG-1 up to MP : 1080p@60fps
  - H.263 : 576p@60fps
  - Sorenson Spark : 1080p@60fps
  - VC-1 up to AP level 3 : 1080p@30fps
  - RV8/RV9/RV10 : 1080p@60fps
  - VP6/VP8 : 1080p@60fps

- MVC : 1080p@60fps
- For H.264, image cropping not supported
- For MPEG-4,GMC(global motion compensation)not supported
- For VC-1, upscaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.1, MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 1920x1080 @ 25FPS[③]

1.1.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[④] is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[④] up to 90million pixels per second
  - Embedded memory management unit(MMU)

1.1.8 Image Enhancement (IEP module)

- Image format support
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - ARGB/XRGB/RGB565/YUV swap
  - UV SP/P
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - RGB dither up/down
  - YUV up/down sampling
  - Max source image resolution: 8192x8192
  - Max scaled image resolution: 4096x4096
- YUV enhancement
  - Hue, Saturation, Brightness, Contrast adjustment
- RGB enhancement & denoise
  - Contrast enhancement
  - Color enhancement
  - Gamma adjustment
- High quality scale
  - Averaging filter down-scaling
  - Bi-cubic up-scaling
  - Arbitrary non-integer horizontal & vertical scaling ratio range from 1/16 to 16
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configured high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Interface
  - Configured direct path to LCDC if source width no more than 1920
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

1.1.9 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 32KB size
- 2D Graphics Engine(RGA module) :
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask

- 8K x 8K raster 2D coordinate system
- Arbitrary degrees rotation with anti-aliasing on every 2D primitive
- Programmable bicubic filter to support image scaling
- Blending, scaling and rotation are supported in one pass for stretch blit
- Source formats :
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar
  - YUV422 planar, YUV422 semi-planar
  - BPP8, BPP4, BPP2, BPP1
- Destination formats :
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
  - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.1.10 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support image crop with arbitrary windows
- Display Interface
  - Support LCD or TFT interfaces up to 1920x1080
  - Parallel RGB LCD Interface :
    RGB888 (24bits), RGB666 (18bits), RGB565 (15bits)
  - Serial RGB LCD Interface: 2x12-bit, 3x8-bit(RGB delta support), 3x8-bit + dummy
  - MCU LCD interface: i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
  - 4 display layers :
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - maximum resolution is 1920x1080,support virtual display
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending(pre-multiplied alpha support)
      - Support transparency color key
      - De-flicker support for interlace output
      - Direct path support
      - YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
      - RGB2YCbCr(BT601/BT709)
    - One video layer (win1)
      - RGB888, ARGB888, RGB565
      - Support virtual display
      - 256 level alpha blending (pre-multiplied alpha support)
      - Support transparency color key

        - Direct path support
        - RGB2YCbCr(BT601/BT709)
    - Hardware cursor(win3)
        - 8BPP (ARGB888 LUT)
        - Support two size: 32x32 and 64x64
        - 256 level alpha blending
        - Support hwc over panel at right and below side
- Win0 and Win1 layer overlay exchangeable
- 3 x 256 x 8 bits display LUTs
- Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
- Blank and blank display
- Scaler
    - Output for LVDS/RGB (max up to 1280x800)

1.1.11 LVDS

- 135MHz clock support
- 28:4 data sub channel compression at data rates up to 945 Mbps per channel
- Support VGA,SVGA,XGA and single pixel SXGA
- PLL requires no external components
- Comply with the Standard TIA/EIA-644-A LVDS standard
- Support alternative LVDS output or LVTTL output

1.1.12 MIPI DPHY

- Embedded 1 MIPI DPHY for TX
- Support 4 data lane
- Support 1080p @ 60fps output

1.1.13 Audio Interface

- I2S/PCM
    - Audio resolution from 16bits to 32bits
    - Sample rate up to 192KHz
    - Provides master and slave work mode, software configurable
    - Support 3 I2S formats (normal , left-justified , right-justified)
    - Support 4 PCM formats(early , late1 , late2 , late3)
    - I2S and PCM cannot be used at the same time
- Audio Codec
    - Digital interpolation and decimation filter integrated
    - Line-in, Microphone in and Speaker out Interface
    - On-Chip Analog Post Filter and digital filters
    - Single–ended or differential Input and Output
    - Sampling Rate of 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz
    - Support 16ohm to 32ohm Head Phone and Speaker Phone Output
    - Mono, Stereo channel supported
    - Optional Fractional PLL available that support 6Mhz to 20Mhz clock input to any clock output that meets 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz and 128 time oversampling ratio.

1.1.14 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- UART Controller
  - 2 on-chip uart controller inside RK3126
  - DMA-based or interrupt-based operation
  - UART1/UART2 Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode

- I2C controller
  - 3 on-chip I2C controller in RK3126
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Embedded 1 USB Host 2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels

- Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.1.15 Others

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL is less than ±1 LSB , INL is less than ±2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface, power dissipation is less than 900uW

- eFuse
  - Two high-density electrical Fuse is integrated: 512bits (64x8)
  - Support standby mode
  - Programming condition : VP must be 2.5V(±10%)
  - Program time is 2us.
  - Read condition: VP must be 0V or Floating.
  - Provide inactive mode, VP must be 0V or Floating in this mode.

- Operation Temperature Range
  - -40°C to +85°C

- Operation Voltage Range
  - IO supply : 3.3V (±10%)

- Package Type
  - LQFP176 (body: 20mm x 20mm)

- Power
  - TBA

Notes : ①: DDR3 are not used simultaneously as well as async and sync ddrnand flash

②: In RK3126, Video decoder and encoder are not used simultaneously because of shared internal buffer

③: Actual maximum frame rate will depend on the clock frequency and system bus performance

④: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK3126.

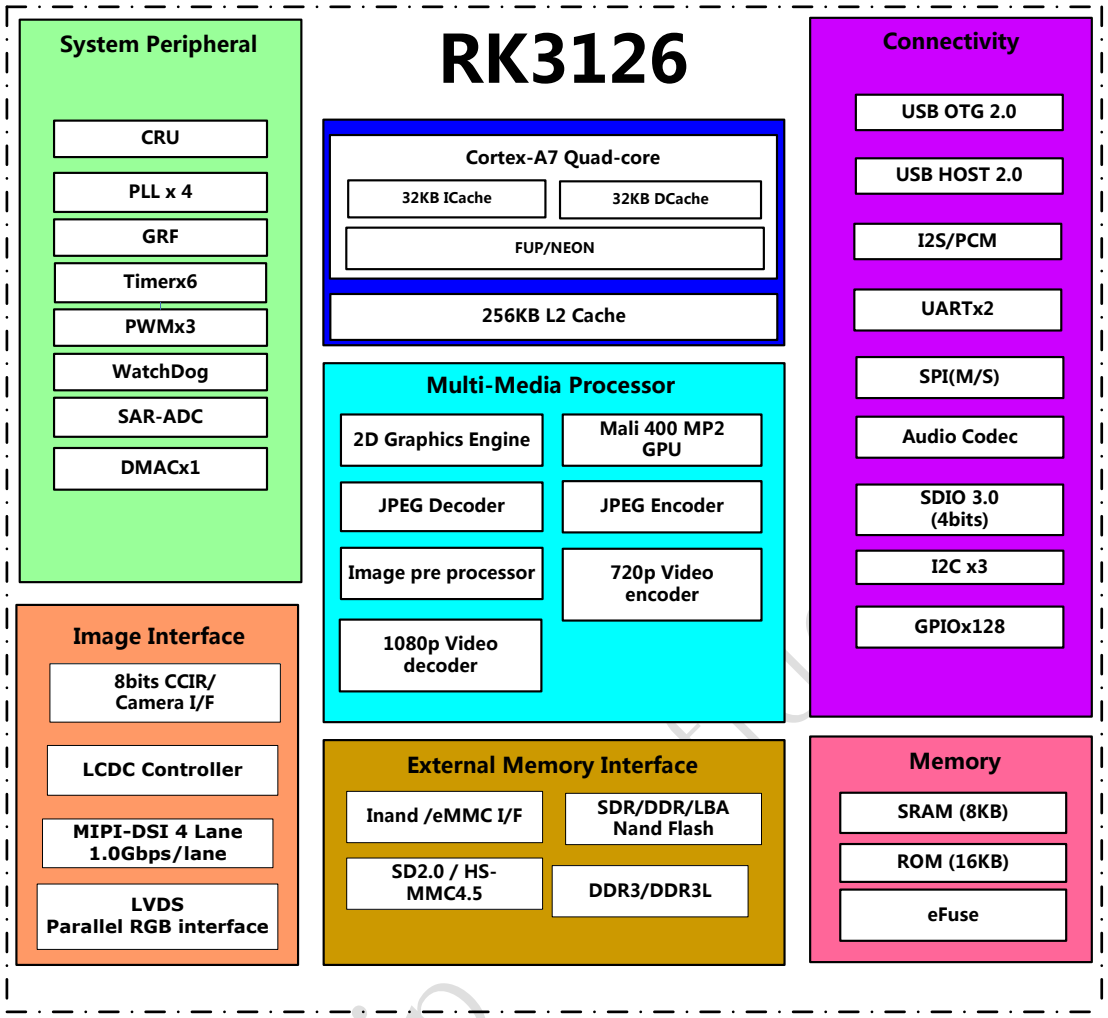


Fig.1-1 RK3126 Block Diagram

1.3 Pin Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 1-1, include analog power/ground, another is all the function signals descriptions in Table 1-2, also include analog power/ground.

1.3.1 RK3126 power/ground IO descriptions

Table 1-1 RK3126 Power/Ground IO informations

Pin Name	Pin No.	Min(V)	Typ(V)	Max(V)	Descriptions
GND	ePAD		0		Internal Core Ground and Digital IO Ground
AVDD	86,88,89,90,91	0.99	1.1	1.21	Internal CPU Power

Pin Name	Pin No.	Min(V)	Typ(V)	Max(V)	Descriptions
CVDD	13,29,69,108,126,161	0.99	1.1	1.21	Core digital Power Supply
VCCIO	35,87,100,115	2.97	3.3	3.63	IO Power Supply
DDR_VDD	10,18,142,150,169	1.425	1.5	1.575	DDR Power Supply
DDR_VSS	139				DDR Power Ground
XVSS	27		0		PLL Power Ground
C/DPLL_DVDD11	22	0.99	1.1	1.21	CODEC/DDR PLL Digital Power
A/GPLL_DVDD11	24	0.99	1.1	1.21	ARM/GENERAL PLL Digital Power
PLL_VCC33	23	2.97	3.3	3.63	PLL Analog Supply
SAR_AVDD33	66	2.97	3.3	3.63	SAR-ADC Analog Power Supply
USB_DVDD11	60	0.99	1.1	1.21	USB Digital Power Supply
USB_AVDD33	59	2.97	3.3	3.63	USB Analog Power Supply
CODEC_AVDD	137	2.97	3.3	3.63	Audio Codec Analog Power Supply
CODEC_AVSS	134,138		0		Audio Codec Ground
LVDS_VCC	44,46	2.97	3.3	3.63	LCD/LVDS Analog Supply

1.3.2 RK3126 function IO descriptions

Table 1-2 RK3126 IO descriptions

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
1	DDR_A0			O	N/A	N/A	O
2	DDR_A2			O	N/A	N/A	O
3	DDR_A5			O	N/A	N/A	O
4	DDR_A9			O	N/A	N/A	O
5	DDR_A13			O	N/A	N/A	O
6	DDR_A7			O	N/A	N/A	O
7	DDR_ODT1			O	N/A	N/A	O
8	DDR_DQ10			I/O	N/A	N/A	I
9	DDR_DQ8			I/O	N/A	N/A	I
11	DDR_DQS1			I/O	N/A	N/A	I
12	DDR_DQS1_N			I/O	N/A	N/A	I
14	DDR_DQ14			I/O	N/A	N/A	I
15	DDR_DQ12			I/O	N/A	N/A	I
16	DDR_DQ15			I/O	N/A	N/A	I
17	DDR_DQ13			I/O	N/A	N/A	I
19	DDR_DQ9			I/O	N/A	N/A	I
20	DDR_DM1			I/O	N/A	N/A	I
21	DDR_DQ11			I/O	N/A	N/A	I
25	XOUT24M			O	N/A	N/A	O
26	XIN24M			I	N/A	N/A	I
28	GPIO2_C5/LCDC_D19/EBC_SDSHR/I2C2_SCL		lcdc_d19	I/O	8	down	I
30	GPIO2_C4/LCDC_D18/EBC_GDRL/I2C2_SDA		lcdc_d18	I/O	8	down	I
31	GPIO2_C3/LCDC_D17/EBC_GDPWR0		lcdc_d17	I/O	8	down	I
32	GPIO2_C2/LCDC_D16/EBC_GDSP		lcdc_d16	I/O	8	down	I
33	GPIO2_C1/LCDC_D15/EBC_GDOE		lcdc_d15	I/O	8	down	I
34	GPIO2_C0/LCDC_D14/EBC_VCOM		lcdc_d14	I/O	8	down	I

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
36	GPIO2_B7/LCDC_D13/EBC_SDCE5		lcdc_d13	I/O	8	down	I
37	GPIO2_B6/LCDC_D12/EBC_SDCE4		lcdc_d12	I/O	8	down	I
38	GPIO2_B5/LCDC_D11/EBC_SDCE3		lcdc_d11	I/O	8	down	I
39	GPIO2_B4/LCDC_D10/EBC_SDCE2		lcdc_d10	I/O	8	down	I
40	GPIO2_B3/LCD_DEN/EBC_GDCLK		lcdc_den	I/O	8	down	I
41	GPIO2_B2/LCD_VSYNC/EBC_SDOE		lcdc_vsync	I/O	8	down	I
42	GPIO2_B1/LCDC_HSYNC/EBC_SDLE		lcdc_hsync	I/O	8	down	I
43	GPIO2_B0/LCDC_CLK/EBC_SDCLK		lcdc_dclk	I/O	12	down	I
45	LVDS_EXTR			A	N/A	N/A	N/A
47	LCDC_D9/LVDS_CLKN/EBC_SDCE1/MIPI_CLKN		lvds_clkn	A	N/A	N/A	N/A
48	LCDC_D8/LVDS_CLKP/EBC_SDCE0/MIPI_CLKP		lvds_clkp	A	N/A	N/A	N/A
49	LCDC_D7/LVDS_TX3N/EBC_SDDO7/MIPI_D3N		lvds_n3	A	N/A	N/A	N/A
50	LCDC_D6/LVDS_TX3P/EBC_SDDO6/MIPI_D3P		lvds_p3	A	N/A	N/A	N/A
51	LCDC_D5/LVDS_TX2N/EBC_SDDO5/MIPI_D2N		lvds_n2	A	N/A	N/A	N/A
52	LCDC_D4/LVDS_TX2P/EBC_SDDO4/MIPI_D2P		lvds_p2	A	N/A	N/A	N/A
53	LCDC_D3/LVDS_TX1N/EBC_SDDO3/MIPI_D1N		lvds_n1	A	N/A	N/A	N/A
54	LCDC_D2/LVDS_TX1P/EBC_SDDO2/MIPI_D1P		lvds_p1	A	N/A	N/A	N/A
55	LCDC_D1/LVDS_TX0N/EBC_SDDO1/MIPI_D0N		lvds_n0	A	N/A	N/A	N/A
56	LCDC_D0/LVDS_TX0P/EBC_SDDO0/MIPI_D0P		lvds_p0	A	N/A	N/A	N/A
57	HOST_DP			A	N/A	N/A	N/A
58	HOST_DM			A	N/A	N/A	N/A
61	USB_EXTR			A	N/A	N/A	N/A
62	OTG_VBUS			A	N/A	N/A	N/A
63	OTG_ID			A	N/A	N/A	N/A
64	OTG_DM			A	N/A	N/A	N/A
65	OTG_DP			A	N/A	N/A	N/A
67	ADCIN0			A	N/A	N/A	N/A
68	ADCIN3/EFUSE			A	N/A	N/A	N/A
70	CIF_D0/TS_D0			I	N/A	down	I

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
71	CIF_D1/TS_D1			I	N/A	down	I
72	CIF_D2/TS_D2			I	N/A	down	I
73	CIF_D3/TS_D3			I	N/A	down	I
74	CIF_D4/TS_D4			I	N/A	down	I
75	CIF_D5/TS_D5			I	N/A	down	I
76	CIF_D6/TS_D6			I	N/A	down	I
77	CIF_D7/TS_D7			I	N/A	down	I
78	CIF_VSYNC/TS_SYNC			I	N/A	down	I
79	CIF_HREF/TS_FAIL			I	N/A	down	I
80	CIF_CLKI/TS_VALID			I	N/A	down	I
81	CIF_CLKO/TS_CLKO			I/O	4	down	I
82	GPIO3_C1/DRIVE_VBUS/PMIC_SLEEP		drive_vbus	I/O	4	down	I
83	GPIO3_B3/CIF_PDN		Cif_pdn	I/O	4	up	I
84	GPIO0_D2/PWM0		pwm_0	I/O	4	down	I
85	GPIO0_D3/PWM1		pwm_1	I/O	4	down	I
92	GPIO1_C6/FLASH_CS2/EMMC_CMD		emmc_cmd	I/O	4	up	I
93	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0		emmc_d0	I/O	8	up	I
94	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1		emmc_d1	I/O	8	up	I
95	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2		emmc_d2	I/O	8	up	I
96	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3		emmc_d3	I/O	8	up	I
97	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD		emmc_d4	I/O	8	up	I
98	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD		emmc_d5	I/O	8	up	I
99	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0		emmc_d6	I/O	8	up	I
100	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1		emmc_d7	I/O	8	up	I
102	GPIO2_A0/FLASH_ALE/SPI_CLK			I/O	8	down	I
103	GPIO2_A1/FLASH_CLE			I/O	8	down	I
104	GPIO2_A2/FLASH_WRN/SFC_CSN0			I/O	8	up	I
105	GPIO2_A3/FLASH_RDN/SFC_CSN1			I/O	8	up	I
106	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK			I/O	8	up	I

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
107	GPIO2_A6/FLASH_CS0			I/O	8	up	I
109	GPIO2_A7/FLASH_DQS/EMMC_CLKO		emmc_clkout	I/O	8	up	I
110	NPOR			I	N/A	down	I
111	GPIO1_C5/SDMMC0_D3/JTAG_TMS		Jtag_tms1	I/O	4	up	I
112	GPIO1_C4/SDMMC0_D2/JTAG_TCK		Jtag_tck1	I/O	4	up	I
113	GPIO1_C3/SDMMC0_D1/UART2_RX			I/O	4	up	I
114	GPIO1_C2/SDMMC0_D0/UART2_TX			I/O	4	up	I
116	GPIO1_C0/SDMMC0_CLKO		mmc0_clkout	I/O	4	down	I
117	GPIO1_B3/UART1_RTSN/SPI_CSN0		spi_csn0	I/O	4	up	I
118	GPIO1_B2/UART1_RX/SPI_RXD		spi_rxd	I/O	4	up	I
119	GPIO1_B1/UART1_TX/SPI_TXD		spi_txd	I/O	4	up	I
120	GPIO1_B0/UART1_CTSN/SPI_CLK		spi_clk	I/O	4	up	I
121	GPIO1_A5/I2S_SDI/SDMMC1_D3		i2s_sdi	I/O	4	down	I
122	GPIO1_A4/I2S_SDO/SDMMC1_D2		i2s_sdo	I/O	4	down	I
123	GPIO1_A2/I2S_LRCK_RX/SDMMC1_D1		i2s_lrckrx	I/O	4	up	I
124	GPIO1_A1/I2S_SCLK/SDMMC1_D0		i2s_sclk	I/O	4	down	I
125	GPIO1_A0/I2S_MCLK/SDMMC1_CLKO/XIN_32K		i2s_mclk	I/O	4	down	I
127	GPIO1_B7/SDMMC0_CMD		mmc0_cmd	I/O	4	up	I
128	GPIO0_A3/I2C1_SDA/SDMMC1_CMD		i2c1_tpsda	I/O	4	up	I
129	GPIO0_A2/I2C1_SCL		i2c1_tpscl	I/O	4	up	I
130	GPIO0_A1/I2C0_SDA		i2c0_pmusda	I/O	4	up	I
131	GPIO0_A0/I2C0_SCL		i2c0_pmuscl	I/O	4	up	I
132	CODEC_VCM			A	N/A	N/A	N/A
133	CODEC_MIC			A	N/A	N/A	N/A
135	CODEC_AOL			A	N/A	N/A	N/A
137	CODEC_AOR			A	N/A	N/A	N/A
140	DDR_DQ2			I/O	N/A	N/A	I
141	DDR_DQ0			I/O	N/A	N/A	I
143	DDR_DQS0			I/O	N/A	N/A	I

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
144	DDR_DQS0_N			I/O	N/A	N/A	I
145	DDR_DQ6			I/O	N/A	N/A	I
146	DDR_DQ4			I/O	N/A	N/A	I
147	DDR_DQ7			I/O	N/A	N/A	I
148	DDR_DQ5			I/O	N/A	N/A	I
150	DDR_DQ1			I/O	N/A	N/A	I
151	DDR_DM0			I/O	N/A	N/A	I
152	DDR_DQ3			I/O	N/A	N/A	I
153	DDR_A8			O	N/A	N/A	O
154	DDR_A6			O	N/A	N/A	O
155	DDR_A14			O	N/A	N/A	O
156	DDR_A15			O	N/A	N/A	O
157	DDR_A11			O	N/A	N/A	O
158	DDR_A1			O	N/A	N/A	O
159	DDR_A4			O	N/A	N/A	O
160	DDR_A12			O	N/A	N/A	O
162	DDR_BA1			O	N/A	N/A	O
163	DDR_BA0			O	N/A	N/A	O
164	DDR_A10			O	N/A	N/A	O
165	DDR_CKE			O	N/A	N/A	O
166	DDR_ODT0			O	N/A	N/A	O
167	DDR_CLK_N			O	N/A	N/A	O
168	DDR_CLK			O	N/A	N/A	O
170	DDR_RASN			O	N/A	N/A	O
171	DDR_CASN			O	N/A	N/A	O
172	DDR_CSN1			O	N/A	N/A	O
173	DDR_CSN0			O	N/A	N/A	O
174	DDR_WEN			G	N/A	N/A	O
175	DDR_BA2			O	N/A	N/A	O

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	Reset State③
176	DDR_A3			O	N/A	N/A	O

Notes :
① ：Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground, DP = Digital Power , DG = Digital Ground, A = Analog
②:Output Drive Unit is mA , only Digital IO have drive value
③:Reset state : I = input without any pull resistor ,O = output without any pull resistor ,
④:It is die location. For examples, "Left side" means that all the related IOs are always in left side of die
⑤:Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring

1.3.3 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 1-3 RK3126 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	TCK	I	JTAG interface clock input/SWD interface clock input
	TMS	I/O	JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_pwr_en	O	emmc card power-enable control signal
	emmc_rstn_out	O	emmc card reset signal

Interface	Pin Name	Direction	Description
DMC	CLK	O	Active-high clock signal to the memory device.
	CLK_N	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSN*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASN	O	Active-low row address strobe to the memory device.
	CASN	O	Active-low column address strobe to the memory device.
	WEN	O	Active-low write enable strobe to the memory device.
	BA*i* (*i*=0,1,2)	O	Bank address signal to the memory device.
	A*i* (*i*=0~15)	O	Address signal to the memory device.
	DQ*i* (*i*=0~15)	I/O	Bidirectional data line to the memory device.
	DQS0 DQS1	I/O	Active-high bidirectional data strobes to the memory device.
	DQS0_N DQS1_N	I/O	Active-low bidirectional data strobes to the memory device.
	DM*i* (*i*=0,1)	O	Active-low data mask signal to the memory device.
	ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select.

Interface	Pin Name	Direction	Description
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal
	flash_data*i* (*i*=0~7)	I/O	8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn*i* (*i*=0,2)	O	Flash chip enable signal for chip i, i=0,2

Interface	Pin Name	Direction	Description
SPI Controller	spi_clk	I/O	spi serial clock
	spi_csn*i* *(i =0,1)*	I/O	spi chip select signal,low active
	spi_txd	O	spi serial data output
	spi_rxd	I	spi serial data input

Interface	Pin Name	Direction	Description
LCDC	lcdc_dclk	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	lcdc_vsync	O	LCDC RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc_hsync	O	LCDC RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc_den	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	lcdc_data *i* (*i*=0~19)	I/O	LCDC data output/input

Interface	Pin Name	Direction	Description
Camera IF	cif_clkin	I	Camera interface input pixel clock
	cif_clkout	O	Camera interface output work clock
	cif_vsync	I	Camera interface vertical sync signal
	cif_href	I	Camera interface horizontial sync signal
	cif_data*i* (*i*=0~7)	I	Camera interface 8-bit input pixel data

Interface	Pin Name	Direction	Description
PWM	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock

Interface	Pin Name	Direction	Description
UART	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output

Interface	Pin Name	Direction	Description
USB OTG2.0 /HOST 2.0	OTG_DP	I/O	USB OTG 2.0 Data signal DP
	OTG_DM	I/O	USB OTG 2.0 Data signal DM
	OTG_VBUS	N/A	USB OTG 2.0 5V power supply pin
	OTG_ID	I	USB OTG 2.0 ID indicator
	HOST_DP	I/O	USB HOST 2.0 Data signal DP
	HOST_DM	I/O	USB HOST 2.0 Data signal DM
	USB_EXTR	N/A	133 Ohm Reference external resistance

Interface	Pin Name	Direction	Description
Audio Codec	MIC	I	Microphone input
	VCM	I	Decoupling for voltage reference
	AOL	O	Left channel DAC driver amplifier output
	AOR	O	Right channel DAC driver amplifier output

Interface	Pin Name	Direction	Description
LVDS	lvds/mipi_extr	I	Connected to external 12Komh through bonding pad
	lvds_txp_n	O	Transmit serial data out(Positive), n=1~4
	lvds_txn_n	O	Transmit serial data out(Negative), n=1~4
	lvds_clkp	O	Output clock
	lvds_clkn	O	Output clock(Negative)

Interface	Pin Name	Direction	Description
MIPI	lvds/mipi_extr	I	Connected to external 12Komh through bonding pad
	mipiD*iP* (*i*=0~3)	O	Transmit serial data out(Positive), i=0~3
	mipiD*iN* (*i*=0~3)	O	Transmit serial data out(Negative), i=0~3
	mipi_clkp	O	Output clock(Positive)
	mipi_clkn	O	Output clock(Negative)

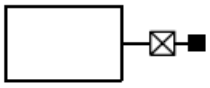
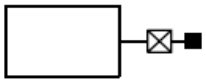
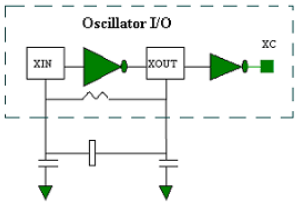
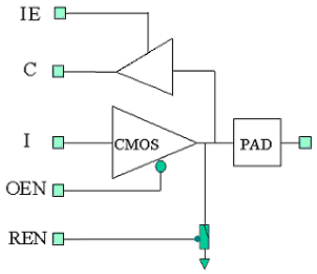
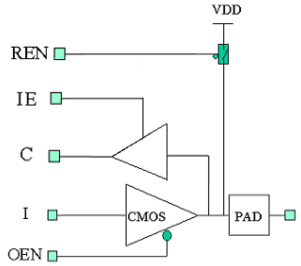
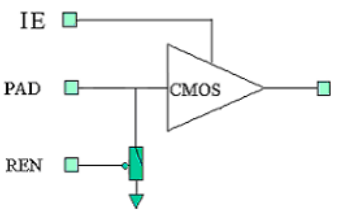
Interface	Pin Name	Direction	Description
SAR-ADC	Saradc_ain *i* *(i =0,2)*	N/A	SAR-ADC input signal for 3 channel

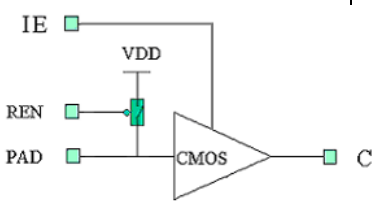
Interface	Pin Name	Direction	Description
eFuse	efuse_vp	N/A	eFuse program and sense power

1.3.4 RK3126 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 1-4 RK3126 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VP
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with internal register	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRNC)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRNC)
F		ontrollable input pad ith controllable ulldown	Part of digital GPIO (PICDRNC)

Type	Diagram	Description	Pin Name
G		ontrollable input pad ith controllable pullup	Part of digital GPIO (PICURNC)

1.4 Package information

The package for RK3126 is LQFP176
body: 20mm x 20mm ; pin pitch : 0.4mm

1.4.1 LQFP176 Dimension

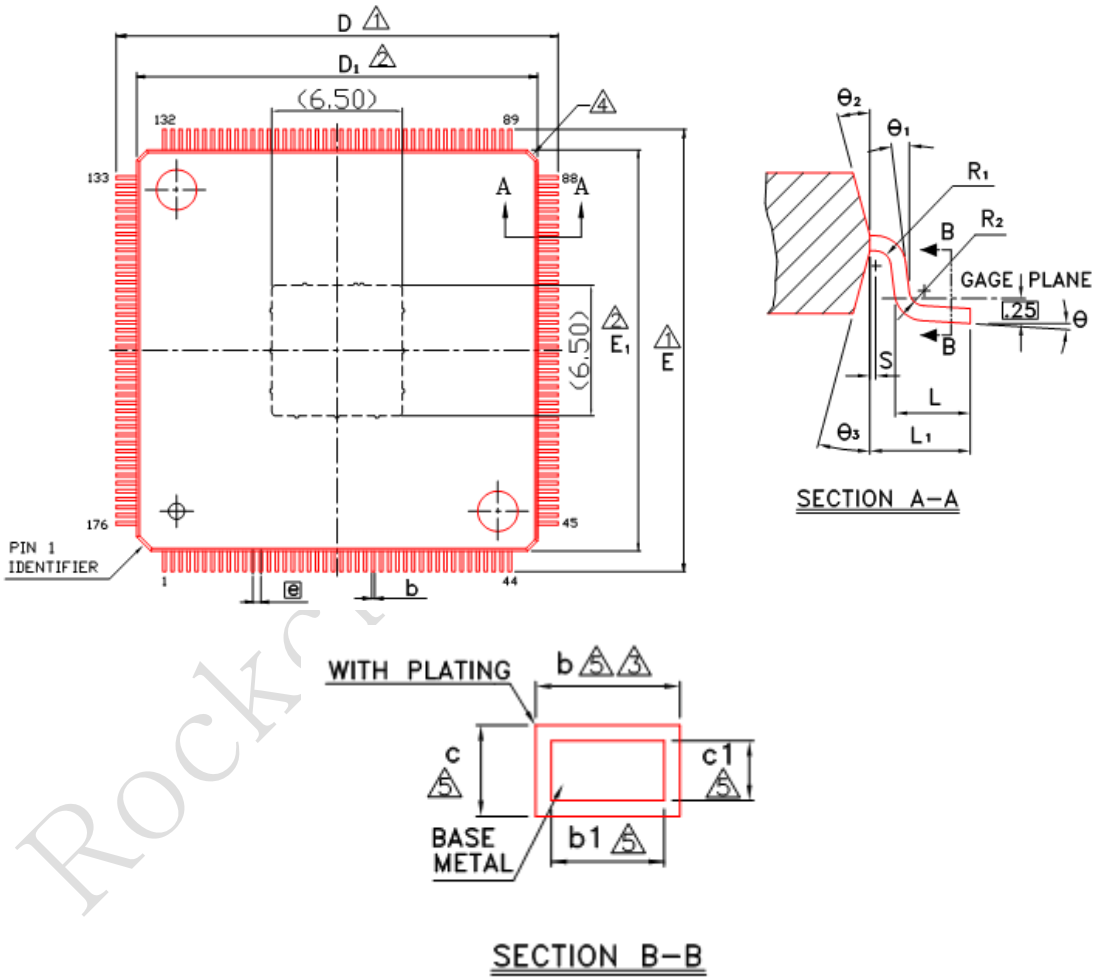


Fig.1-2 RK3126 LQFP176 Package Top View

Fig.1-3 RK3126 LQFP176 Package Side View

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Fig.1-4 RK3126 LQFP176 Package Dimension

1.4.2 Ball Map

Pin Number	Pin Name	176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144	143	142	141	140	139	138	137	136	135	134	133		
		DDR_VDD	DDR_A3	DDR_BA2	DDR_WEN	DDR_CSN0	DDR_CSN1	DDR_CASN	DDR_RASN	DDR_VDD	DDR_CLK	DDR_CLK_N	DDR_ODT0	DDR_CKE	DDR_A10	DDR_BA0	DDR_BA1	CVDD	DDR_A12	DDR_A4	DDR_A1	DDR_A11	DDR_A15	DDR_A14	DDR_A6	DDR_A8	DDR_DQ3	DDR_DM0	DDR_DQ1	DDR_VDD	DDR_DQ5	DDR_DQ7	DDR_DQ4	DDR_DQ6	CVDD	DDR_DQS0_N	DDR_DQS0	DDR_VDD	DDR_DQ0	DDR_DQ2	CODEC_AOR	CODEC_AVDD	CODEC_AOL	CODEC_MICR	CODEC_VCM		
1	DDR_A0																																												CVDD	132
2	DDR_A2																																												I2C0_SCL/GPIO0_A0	131
3	DDR_A5																																												I2C0_SDA/GPIO0_A1	130
4	DDR_A9																																												I2C1_SCL/GPIO0_A2	129
5	DDR_A13																																												I2C1_SDA/GPIO0_A3	128
6	DDR_A7																																												SDMMC0_CMD/GPIO1_B7	127
7	DDR_ODT1																																												VCCIO	126
8	DDR_DQ10																																												I2S_MCLK/GPIO1_A0	125
9	DDR_DQ8																																												I2S_SCLK/GPIO1_A1	124
10	DDR_VDD																																												I2S_LRCK_RX/GPS_CLK/GPIO1_A2	123
11	DDR_DQS1																																												I2S_SDO/GPS_MAG/GPIO1_A4	122
12	DDR_DQS1_N																																												I2S_SDI/GPS_SIGN/GPIO1_A5	121
13	CVDD																																												SPI_CLK/UART1_CTSN/GPIO1_B0	120
14	DDR_DQ14																																												SPI_TXD/UART1_TX/GPIO1_B1	119
15	DDR_DQ12																																												SPI_RXD/UART1_RX/GPIO1_B2	118
16	DDR_DQ15																																												SPI_CSN0/UART1_RTSN/GPIO1_B3	117
17	DDR_DQ13																																												SDMMC0_CLKO/GPIO1_C0	116
18	DDR_VDD																																												VCCIO	115
19	DDR_DQ9																																												SDMMC0_DET/GPIO1_C1	114
20	DDR_DM1																																												SDMMC0_D0/GPIO1_C2	113
21	DDR_DQ11																																												SDMMC0_D1/GPIO1_C3	112
22	C/DPLL_DVDD12																																												SDMMC0_D2/GPIO1_C4	111

VSS VSS VSS VSS

VSS VSS VSS VSS

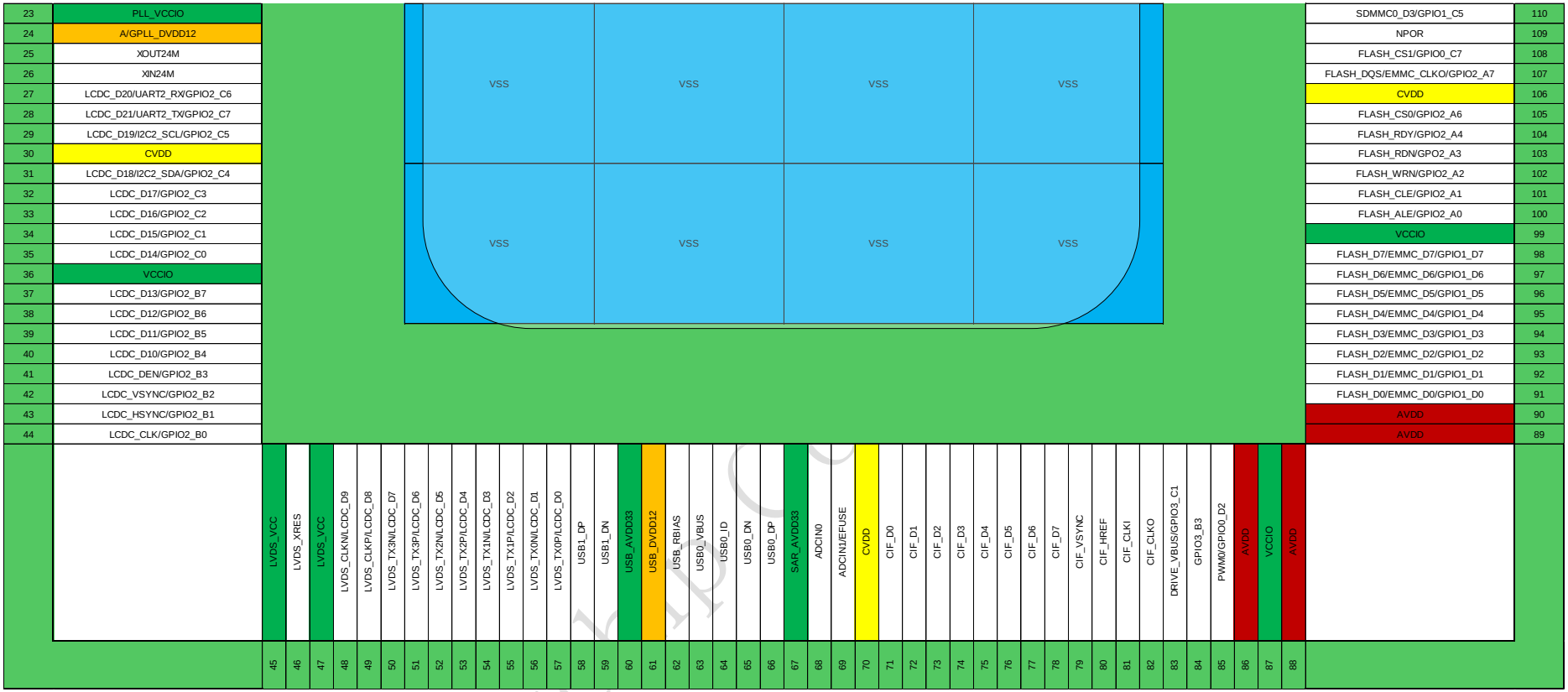


Fig.1-5 RK3126 LQFP176 Ball Map

1.5 Electrical Specification

1.5.1 Absolute Maximum Ratings

Table 1-5 RK3126 absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD,CVDD, USB_DVDD11,LVDS_DVDD11	TBD	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	VCCIO	3.63	V
DC supply voltage for DDR IO	VCC_DDR	1.95	V
DC supply voltage for Analog part of SAR-ADC and PLL	SAR_AVDD33,PLL_VCCIO	3.63	V
DC supply voltage for Analog part of PLL	A/GPLL_DVDD11,C/DPLL_DVDD 11	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of Acodec	CODEC_AVDD	3.63	V
DC supply voltage for Analog part of LVDS	LVDS_VCC	3.63	V
Analog Input voltage for SAR-ADC		2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5.25	V
Digital input voltage for input buffer of GPIO		3.63	V
Digital output voltage for output buffer of GPIO		3.63	V
Storage Temperature		150	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

1.5.2 Recommended Operating Conditions

Table 1-6 RK3126 recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital Core Power	AVDD	0.9	TBD	TBD	V
Internal digital logic Power	CVDD,USB_DVDD11,LVDS_DVDD11	0.9	1.1	1.21	V
Digital GPIO Power	VCCIO	2.97	3.3	3.63	V
DDR IO (DDR3 mode) Power	VCC_DDR	1.425	1.5	1.575	V
DDR IO (LVDDR3 mode) Power	VCC_DDR	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	A/GPLL_DVDD12,C/DPLL_DVDD12	0.99	1.1	1.21	V
SAR-ADC Analog Power	SAR_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0	EXTR	122	135	147	Ohm

Parameters	Symbol	Min	Typ	Max	Units
external resistor					
Acodec Analog Power	CODEC_AVDD	2.97	3.3	3.63	V
EFUSE programming voltage		2.25	2.5	2.75	V
PLL input clock frequency			24		MHz
Operating Temperature		-40	25	85	°C

1.5.3 DC Characteristics

Table 1-7 RK3126 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol		0	0.4	V
	Output High Voltage	Voh	2.4	3.3		V
	Threshold Point	Vt	1.21	1.42	1.64	V
	Schmitt trig Low to High threshold point	Vt+	1.36	1.6	1.86	V
	Schmitt trig High to Low threshold point	Vt-	0.93	1.09	1.3	V
	Pullup Resistor	Rpu	33	41	62	Kohm
	Pulldown Resistor	Rpd	33	42	68	Kohm
DDR IO (Data)	DC Input High Voltage	Vih(DC)	VREF + 0.1		VDDQ+ 0.4	V
	AC Input High Voltage	Vih(AC)	VREF + 0.15		VDDQ+ 0.4	V
	DC Input Low Voltage	Vil(DC)	-0.4		VREF - 0.1	V
	AC Input Low Voltage	Vil(AC)	-0.4		VREF + 0.15	V
	Differential input logic high	Vihdiff	+0.2		VDDQ + 0.4	V

Parameters		Symbol	Min	Typ	Max	Units
	Differential input logic low	Vildiff	-0.4		-0.2	V
	Output High Voltage	Voh	0.9 * VDDQ	VDDQ		V
	Output Low Voltage	Vol		0	0.1 * VDDQ	V
DDR IO (Address and command)	Output High Voltage	Voh	0.9 * VDDQ		VDDQ+0.4	V
	Output Low Voltage	Vol	-0.4	0	0.1 * VDDQ	V
DDR IO (Clock)	DC output voltage	Von	-0.4		VDDQ+0.4	V
	DC output Differential voltage	Vod(DC)	0.4 * VDDQ		VDDQ+0.6	V
	AC output Differential voltage	Vod(AC)	0.6 * VDDQ		VDDQ+0.6	V
	AC differential crossing voltage	Vox	0.4 * VDDQ		0.6 * VDDQ	V
SAR-ADC	Input Range	2-channel single-ended input	0.01* SAR_AVDD33		0.99* SAR_AVDD33	V
	Input Voltage High (Logic “1”)	Vih	0.7* SAR_AVDD33	SAR_AVDD33		V
	Input Voltage Low (Logic “0”)	Vil		0	0.3* SAR_AVDD33	V
	Output Voltage High (Logic “1”)	Voh	0.7* SAR_AVDD33			V
	Output Voltage Low (Logic “0”)	Vol			0.3* SAR_AVDD33	V
USB	Input Voltage High	Vih		1.1		V

Parameters		Symbol	Min	Typ	Max	Units
	Input Voltage Low	Vil		0		V
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V

1.5.4 Recommended Operating Frequency

Table 1-8 Recommended operating frequency for PLL and oscillator domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.1V , 25 °C	XIN24M		24		MHz
	1.21V , -40 °C			24		
	0.99V , 125 °C			24		
DDR PLL	1.1V , 25 °C	ddr_pll_clk			1390	MHz
	1.21V , -40 °C				1690	
	0.99V , 125 °C				800	
ARM PLL	1.1V , 25 °C	arm_pll_clk			1530	MHz
	1.21V , -40 °C				1960	
	0.99V , 125 °C				800	
CODEC PLL	1.1V , 25 °C	cocec_pll_clk			1030	MHz
	1.21V , -40 °C				1380	
	0.99V , 125 °C				600	
GENERAL PLL	1.1V , 25 °C	general_pll_clk			1010	MHz
	1.21V , -40 °C				1350	
	0.99V , 125 °C				600	

Table 1-9 Recommended operating frequency for CPU core

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
Cortex-A7	1.1V , 25 °C	CORE_SRC_CLK			1180	MHz
	1.21V , -40 °C				1470	
	0.99V , 125 °C				775	
	1.1V , 25 °C	aclk_core_pre			678	MHz
	1.21V , -40 °C				890	
	0.99V , 125 °C				410	
	1.1V , 25 °C	clk_core_peri			330	MHz
	1.21V , -40 °C				420	
	0.99V , 125 °C				200	

Table 1-10 Recommended operating frequency for PD_CPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
CPU AXI interconnect	1.1V , 25 °C	CPU_ACLK			520	MHz
	1.21V , -40 °C				710	
	0.99V , 125 °C				300	
	1.1V , 25 °C	CPU_HCLK			190	MHz
	1.21V , -40 °C				350	
	0.99V , 125 °C				150	
	1.1V , 25 °C	CPU_PCLK			170	MHz
	1.21V , -40 °C				250	
	0.99V , 125 °C				75	
DMC	1.1V , 25 °C	DDR_PHY1X_CLK			760	MHz
	1.21V , -40 °C				1000	
	0.99V , 125 °C				400	

Table 1-11 Recommended operating frequency for PD_PERI domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
PERI AXI interconnect	1.1V , 25 °C	PERI_ACLK			498	MHz
	1.21V , -40 °C				700	
	0.99V , 125 °C				300	
	1.1V , 25 °C	PERI_HCLK			259	MHz
	1.21V , -40 °C				330	
	0.99V , 125 °C				150	
	1.1V , 25 °C	PERI_PCLK			140	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				75	
NAND	1.1V , 25 °C	FLASH_HCLK			250	MHz
	1.21V , -40 °C				340	
	0.99V , 125 °C				150	
USB OTG	1.1V , 25 °C	UTMI_CLK_0/ UTMI_CLK_1			30	MHz
	1.21V , -40 °C				30	
	0.99V , 125 °C				30	
UART1	1.1V , 25 °C	UART1_CLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
SDMMC/SDIO	1.1V , 25 °C	MMC0_CLK/ SDIO_CLK			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	
EMMC	1.1V , 25 °C	EMMC_CLK			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	
I2S	1.1V , 25 °C	I2S_CLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
SPI0	1.1V , 25 °C	SPI0_CLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
SAR-ADC	1.1V , 25 °C	SARADC_CLK			12	MHz
	1.21V , -40 °C				12	
	0.99V , 125 °C				12	
Timer0/1	1.1V , 25 °C	TIMER0_CLK/ TIMER1_CLK			24	MHz
	1.21V , -40 °C				24	
	0.99V , 125 °C				24	
	1.1V , 25 °C	TIMER0_PCLK/ TIMER1_PCLK			140	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				75	

Table 1-12 Recommended operating frequency for PD_VIO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
Display AXI interconnection	1.1V , 25 °C	DISP_ACLK			530	MHz
	1.21V , -40 °C				720	
	0.99V , 125 °C				300	
	1.1V , 25 °C	DISP_HCLK			370	MHz
	1.21V , -40 °C				500	
	0.99V , 125 °C				200	
LCDC	1.1V , 25 °C	LCDC_DCLK			179	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				160	
	1.1V , 25 °C	LCDC1_DCLK			230	MHz
	1.21V , -40 °C				290	
	0.99V , 125 °C				160	
CIF	1.1V , 25 °C	IO_CIF_CLKIN			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	

Table 1-13 Recommended operating frequency PD_GPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
GPU	1.1V , 25 °C	GPU_ACLK			510	MHz
	1.21V , -40 °C				691	
	0.99V , 125 °C				300	

Table 1-14 Recommended operating frequency for PD_VIDEO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
VIDEO	1.1V , 25 °C	VEPU_ACLK			520	MHz
	1.21V , -40 °C				690	
	0.99V , 125 °C				300	
	1.1V , 25 °C	hclk_vepu			320	MHz
	1.21V , -40 °C				400	
	0.99V , 125 °C				150	
	1.1V , 25 °C	VDPU_ACLK			520	MHz
	1.21V , -40 °C				690	
	0.99V , 125 °C				300	
	1.1V , 25 °C	hclk_vdpu			320	MHz
	1.21V , -40 °C				490	

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
	0.99V , 125 ℃				150	

1.5.5 Electrical Characteristics for General IO

Table 1-15 RK3126 Electrical Characteristics for Digital General IO

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input leakage current	Il	Vin = 3.3V or 0V	-10		10	uA
Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-10		10	uA

1.5.6 Electrical Characteristics for PLL

Table 1-16 RK3126 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Fractional accuracy				24		bits
Input clock frequency	Fin	Normal mode	1		800	MHz
		Fractional mode	10		800	MHz
Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.1V	12		2400	MHz
VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.1V	600		2400	MHz
Lock time②	Tlt	FREF=24M,REFDIV=1 @ 3.3V/1.1V,		41.7	66.7	us
AVDD Current consumption ③		Fvco = 1GHz, @3.3V, 27℃		1	1.2	mA
DVDD Power consumption (normal mode)		@3.3V/1.1V, 27℃		1.3	1.56	uA/MHz
AVDD Power Down Leakage		@3.3V/1.1V, 27℃		10		nA
DVDD Power Down Leakage		@3.3V/1.1V, 27℃		10		uA
Output Duty Cycle		Even divides @ FOUT=1GHz(falling edge error is ±20ps)	48	50	52	%
		Odd divides @ FOUT=1GHz(falling edge error is ±30ps)	47	50	53	%
		FOUTvco at any frequency	45	50	55	%

Notes :

①:REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value

②Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.

③Current scale as $(Fvco/1GHz)^{1.5}$

1.5.7 Electrical Characteristics for SAR-ADC

Table 1-17 RK3126 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution				10		bits
Conversion speed	Fs				1	MSPS
Differential Non Linearity	DNL				1	LSB
Integral Non Linearity	INL				1.5	LSB
Input Capacitance	CIN			1		pF
Sampling Clock	SOC				1	MHz
Main Clock Frequency	CLK				11	MHz
Data Latency				10		Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=1.03K Fin=499K		59.56 57.03		dB
Spurious-Free Dynamic Range	SFDR	Fin=1.03K Fin=499K		78.59 65.75		dB
Second-Harmonic Distortion	2HD	Fin=1.03K Fin=499K		-93.32 -70.76		dB
Third-Harmonic Distortion	3HD	Fin=1.03K Fin=499K		-88.16 -65.75		dB
Effective Number of Bits	ENOB	Fin=1.03K Fin=499K		9.55 9.18		Bits
Analog Supply Current(SARADC_AVDD)				580		uA
Digital Supply Current				30		uA
Power Down Current				0.5		uA

1.5.8 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 1-18 RK3126 Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output resistance	Rout	Classic mode HS mode	40.5	45	49.5	ohm
Output Capacitance	Cout				3	pF
Differential output signal high	Voh	Classic(LS/FS),Io=0mA	2.97	3.3	3.63	V
		Classic(LS/FS),Io=6mA	2.2	2.7		V
		HS mode,Io=0mA	360	400	440	mV
Differential output signal low	Vol	Classic(LS/FS),Io=0mA	-0.33	0	0.33	V
		Classic(LS/FS),Io=6mA		0.3	0.8	V
		HS mode,Io=0mA	-40	400	40	mV
Output Common Mode Voltage	VM	Classic(LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Rise and fall time	Tr/Tf	LS mode	75	87.5	300	ns
		FS mode	4	12	20	ns
		HS mode	0.8	1.0	1.2	ns

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Propagation delay(data to D+/D-)		LS mode	30		300	ns
		FS mode	0		12	ns
		HS mode		TBD		ns
Propagation delay(tx_en to D+/D-)	Tpzh/Tpzl	Classic(LS/FS) mode			2	ns
		HS mode			2	ns
Receiver sensitivity	Rsens	Classic(LS/FS) mode		±250		mV
		HS mode		±250		mV
Receiver common mode	RCM	Classic(LS/FS) mode	0.8	1.65	2.5	V
		HS mode(differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode(disconnect comparator)	0.5	0.6	0.7	V
Input capacitance	Cin	Seen at D+ or D-			3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	Voh			1.1		V
Low output level	Vol			0		V
Pulldown Resistor on DP/DM	Rpu		14.5	15	16	Kohm
Pullup Resistor on DP/DM	Rpd		2.35	2.4	2.5	Kohm
UID Pullup resistor			160	200	240	Kohm

1.5.9 Electrical Characteristics for DDR IO

Table 1-19 RK3126 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	DDR IO power standby current, ODT OFF		@ 1.5V , 125℃	N/A	N/A	N/A	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	N/A	N/A	uA
DDR IO @LVDDR3 mode	Input leakage current		@ 1.35V , 125℃	N/A	N/A	N/A	uA
	DDR IO power quiescent current		@ 1.35V , 125℃	N/A	N/A	N/A	uA

1.5.10 Electrical Characteristics for LVDS

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output voltage low, Voa or Vob	Vol	Rload=100ohm ±1%	925		N/A	mV
Output voltage high, Voa or Vob	Voh	Rload=100ohm ±1%	N/A		1475	mV
Output differential voltage	|Vod|	Rload=100ohm ±1%,Rs=0V	250		450	mV
		Rload=100ohm ±1%,Rs=VDD	150		250	mV
Output offset voltage	Vos	Rload=100ohm	1125		1375	mV

Parameters	Symbol	Test condition	Min	Typ	Max	Units
		±1%				
Change in |Vod| between '0' and '1'	|△Vod|	Rload=100ohm ±1%			50/150	mV
change in Vos between '0' and '1'	△Vos	Rload=100ohm ±1%			50	mV
Output current	Isa,Isb	Transmitter shorten to ground			24	mA
Output current	Isab	Transmitter shorten to ground			12	mA
Leakage current	Ileakage	Power down	-10			uA
Clock in/out frequency	Clk_freq		20		170	MHz
Clock out duty cycle	Clk_dco			57		%
Data(Dn_m) setup to CK_REF	Tts		2			ns
Data(Dn_m) hold to CK_REF	Tth		0.5			ns
Serial-Data Skew to Clkout edge	SDsdew		-200	0	200	ps

1.5.11 Electrical Characteristics for eFuse

Table 1-20 RK3126 Electrical Characteristics for eFuse

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Burn voltage	VQPS		2.25	2.5	2.75	V
Programming voltage	Vpgm			VQPS		V
Active mode	Iactive	STROBE high		2.53		mA
standby mode	Istandby			0.4		uA
Peak program current	Iprog			20.8		mA

1.6 Hardware Guideline

1.6.1 Reference design for RK3126 oscillator PCB connection

RK3126 only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram ,Rf is used to bias the inverter in the high gain region. The recommend value is 1Mohm.
Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Rd of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.
C1 and C2 are deciding regard to the crystal or resonator CL specification.
the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model .

In RK3126, the crystal oscillator I/O cells have embedded internal resistor, so we need not add feedback resistor (Rf) as above description.

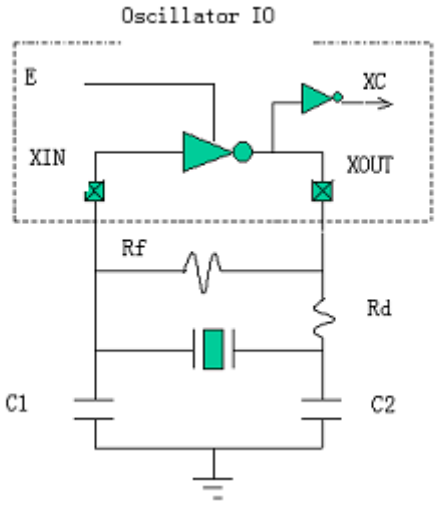


Fig.1-6 External Reference Circuit for 24MHzOscillators

1.6.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK3126.
For optimal jitter performance it is suggested to place external decoupling capacitors on the board between PLL_DVDD-VSS(XVSS) and PLL_VCCIO-VSS(XVSS) . VDDREF is typically connected to the global chip supply and does not require dedicated decoupling.
It is recommended to use at least one large capacitor (e.g. 4.7uF) capacitor for each separate supply.Additionally, a 100nF and 10nF capacitor may be placed in parallel since the lead inductance of the 4.7uF capacitor may be large.
Capacitors with minimal lead inductance should be selected. Ceramic type capacitors work well.The capacitors should be placed as close to the package pins as possible. No series impedance should be added anywhere on the board, and impedance to the voltage source should be minimized.

1.6.3 Reference design for USB OTG/Host2.0 connection

In RK3126 there are USB OTG and USB Host2.0 interface, and they share a common PHY.

- Decouple Capacitance

We should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 1-9. Place these components as closely as possible to the power pins.

- Differential Lines

The differential lines should be routed together, minimizing the number of vias through which the signal lines are routed. Layout the differential pairs with controlled impedance of 90 ohm differential.

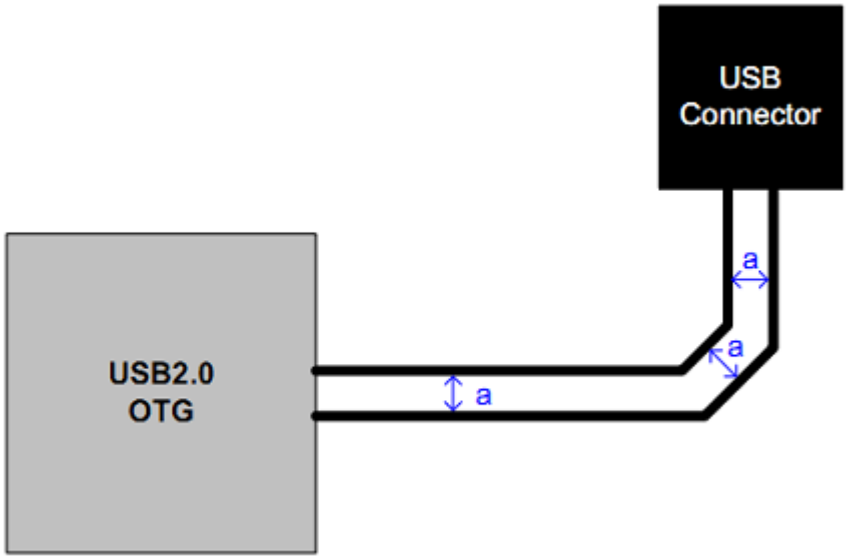


Fig.1-7 RK3126 USB OTG/Host2.0 differential lines requirement.

If high-speed signals are routed on the Top layer, best results will be obtained if the Layer 2 is a Ground plane. Furthermore, there must have only one ground plane under high-speed signals in order to avoid the high-speed signals to cross another ground plane.

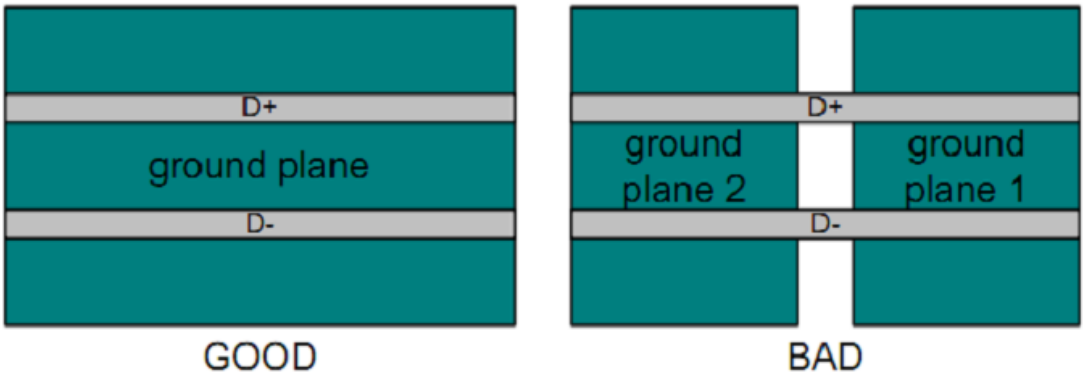


Fig.1-8 RK3126 USB OTG/Host2.0 ground plane guide.

- Component Placement

  It is very important to not create stubs on the high-speed lines, to avoid that, the placement of component should be the closed as possible from D+ and D- lines, like shown in the following figure.

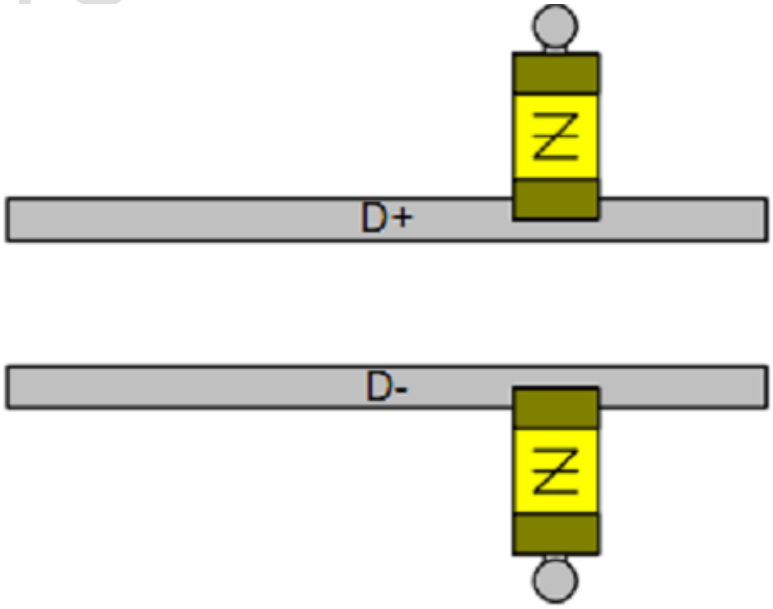


Fig.1-9 RK3126 USB OTG/Host2.0 component placement.

1.6.4 Reference design for Audio Codec connection

In RK3126, the following diagram shows external PCB reference design for Audio Codec.

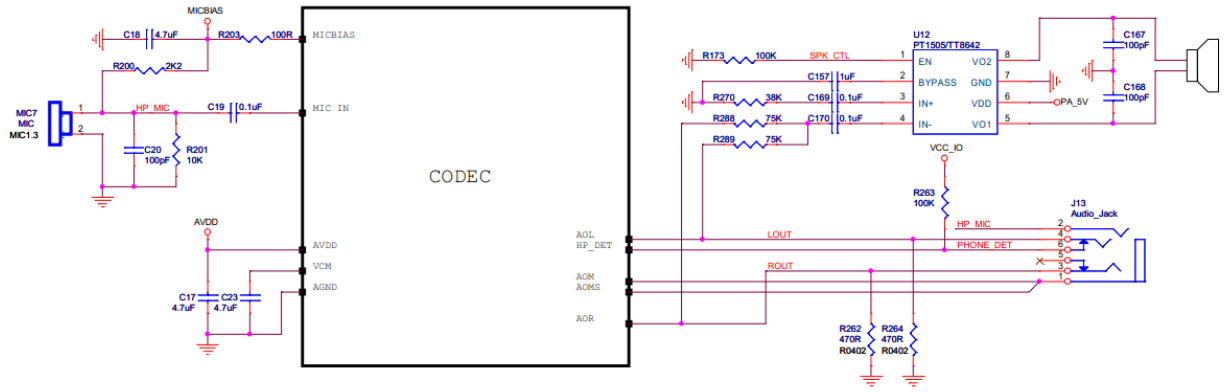


Fig.1-10 RK3126 Audio Codec interface reference connection

As above diagram shows, the MIC_IN connected with a MIC through a 0.1uf CAP. The R203 and C18 are formed a filter for the MIC. The MIC_BIAS is used for bias the MIC through a resistor. The resistor value should be changed according the MIC type. The AVDD should be supplied by 3.3V. The CAP connected with AVDD should be placed as close as possible The VCM is connected with GND through a 4.7Uf CAP. The CAP should be placed as close as possible. The AOL and AOR could be connected with a speaker or an earphone.

1.6.5 RK3126 Power on reset descriptions

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstndeassert, andthe PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

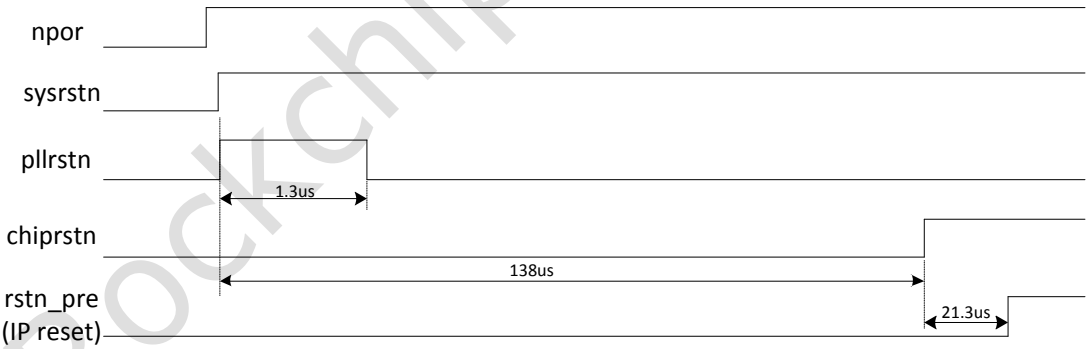


Fig.1-11 RK3126 reset signals sequence