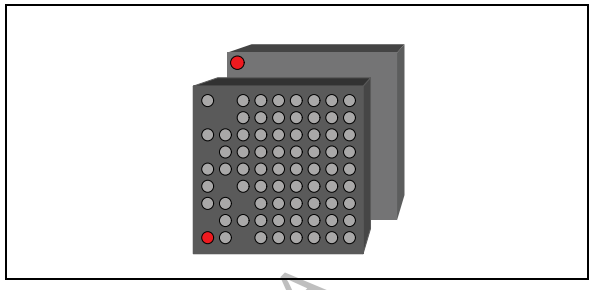
CX1001

802.11n WLAN system-on-chip

Features

- Compliant with IEEE 802.11n, 11b, 11j, 11g
- Depopulated 73-pin lead-free/RoHS compliant WLCSP 3.90 mm x 3.84 mm x 0.6 mm with 0.4 mm pitch
- Reference design using 16 external components: 1 SP3T antenna switch, 1 coexistence filter, 13 capacitors and one inductor in a PCB footprint of 50 mm2
- Enhanced integrated Bluetooth coexistence
  - IEEE 802.15.2 support (standard PTA)
  - ePTA: proprietary enhanced coexistence hardware and algorithms
- Power supply
  - Integrated SMPS for direct battery connection
  - Software adjustable output voltage to minimize power consumption
- Clocks
  - Reference clock input (digital or sine wave)
  - Low power clock input at 32.768 kHz
  - Direct external crystal input for reference clock
- Various on-chip auto calibration features
- Support for 6 to 65 Mbps OFDM, 11 and 5.5 Mbps CCK and legacy 2 and 1 Mbps DSSS data rates
- WLAN solution with fully integrated:
  - Zero IF (ZIF) transceiver
  - OFDM and CCK baseband processors
  - ARM9 media access controller (MAC)
  - SPI serial host interface
  - SDIO (1-bit, 4-bit) serial host interface



- Intelligent power control, including 802.11 power save mode
- Supports MAC enhancements including:
  - 802.11d - Regulatory domain operation
  - 802.11e - QoS including WMM
  - 802.11h - Transmit power control dynamic and frequency selection
  - 802.11i - Security including WPA2 & WAPI
  - 802.11k - Radio resource measurement
  - 802.11r - Roaming
  - 802.11w - Management frame protection

Description

The CX1001 is an IEEE 802.11b/g/j/n WLAN single-chip solution fully optimized for mobile applications such as mobile phones, smart phones, PDAs and portable media players. The extremely low power consumption and intelligent host off loading of beacon as well as the packet processing ensure industry leading battery life. High levels of integration allow for very compact and cost effective reference designs delivering fast time-to-market for new WLAN enabled products.

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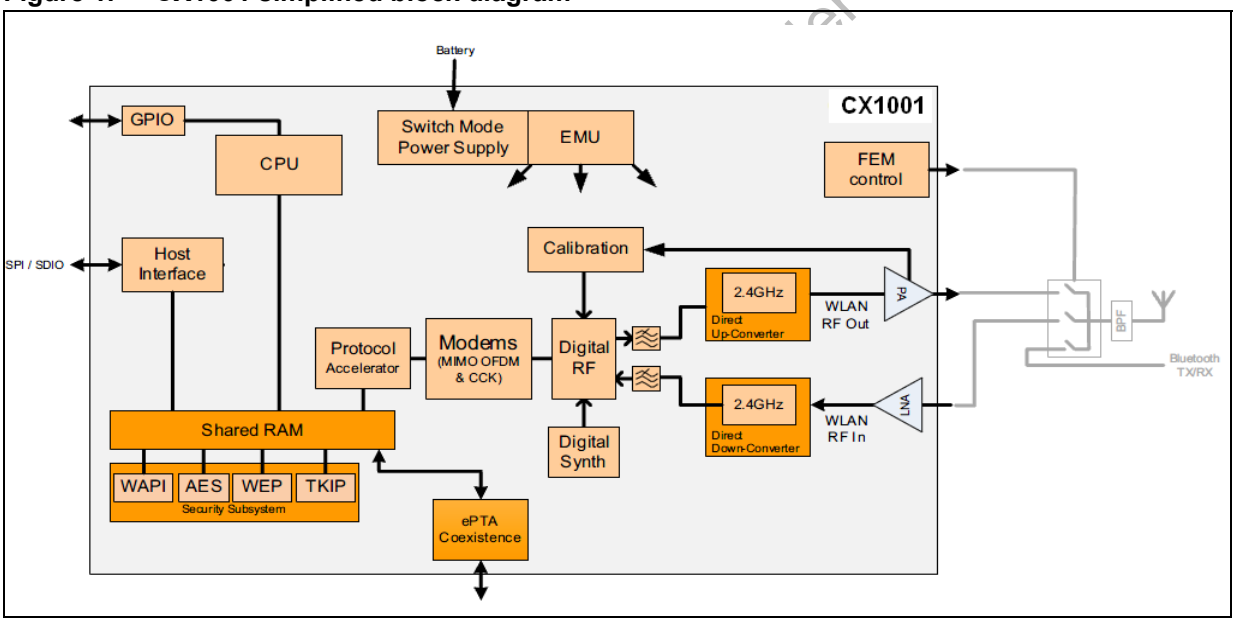
1 Introduction

The CX1001 is an IEEE 802.11b/g/j/n WLAN single-chip solution fully optimized for mobile applications such as mobile phones, smart phones, PDAs and portable media players. The extremely low power consumption and intelligent host off loading of beacon as well as the packet processing ensure industry leading battery life. High levels of integration allow for very compact and cost effective reference designs delivering fast time-to-market for new WLAN enabled products. Built on the CX1001 successful predecessors, the STLC4370 and the STLC4560, the CX1001 integrates a power amplifier and switch mode power supply. All RF ports are single ended. CX1001 is an ideal partner for ST-Ericsson CX2001 GPS/BT/FM system on chip. The CX1001 offers proprietary enhanced BT/WLAN coexistence power consumption and shared power supply and clock reducing WGBF BOM costs. A comprehensive suite of software is provided, which includes proven drivers for Symbian/S60, Linux/Android, Windows CE and Windows Mobile along with production test and engineering software utilities.

The CX1001 is a system-on-chip WLAN device packed in Wafer Level Chip Scale Package (WLCSP) of 3.90 mm x 3.84 mm x 0.6 mm with 0.4 mm pitch.

Figure 1. CX1001 simplified block diagram



The CX1001 SoC is built on the proven success of integrating previous generation WLAN devices into cellular handsets providing the lowest power consumption, best-in-class BT/WLAN co-existence mechanism in addition to high throughput performance and better range. The CX1001 supports a comprehensive range of 802.11 standards and amendments:

- Enhanced throughput and range through 802.11n support - single stream with support for WiFi 802.11n certification including STBC Rx and STBC control frame optional features
- 2.4 GHz operation compliant to 802.11g and 802.11b
- QoS support compliant to 802.11e/WMM/WMM-PS standards
- Robust security based on 802.11i/WPA/WPA2 standards
- Regulatory domain operation support based on 802.11d operation
- Radio resource measurements support based on 802.11k standard
- Fast BSS transition support based on 802.11r standard
- Protected management frame support based on 802.11w standard

The CX1001 supports also the CCX version 5.

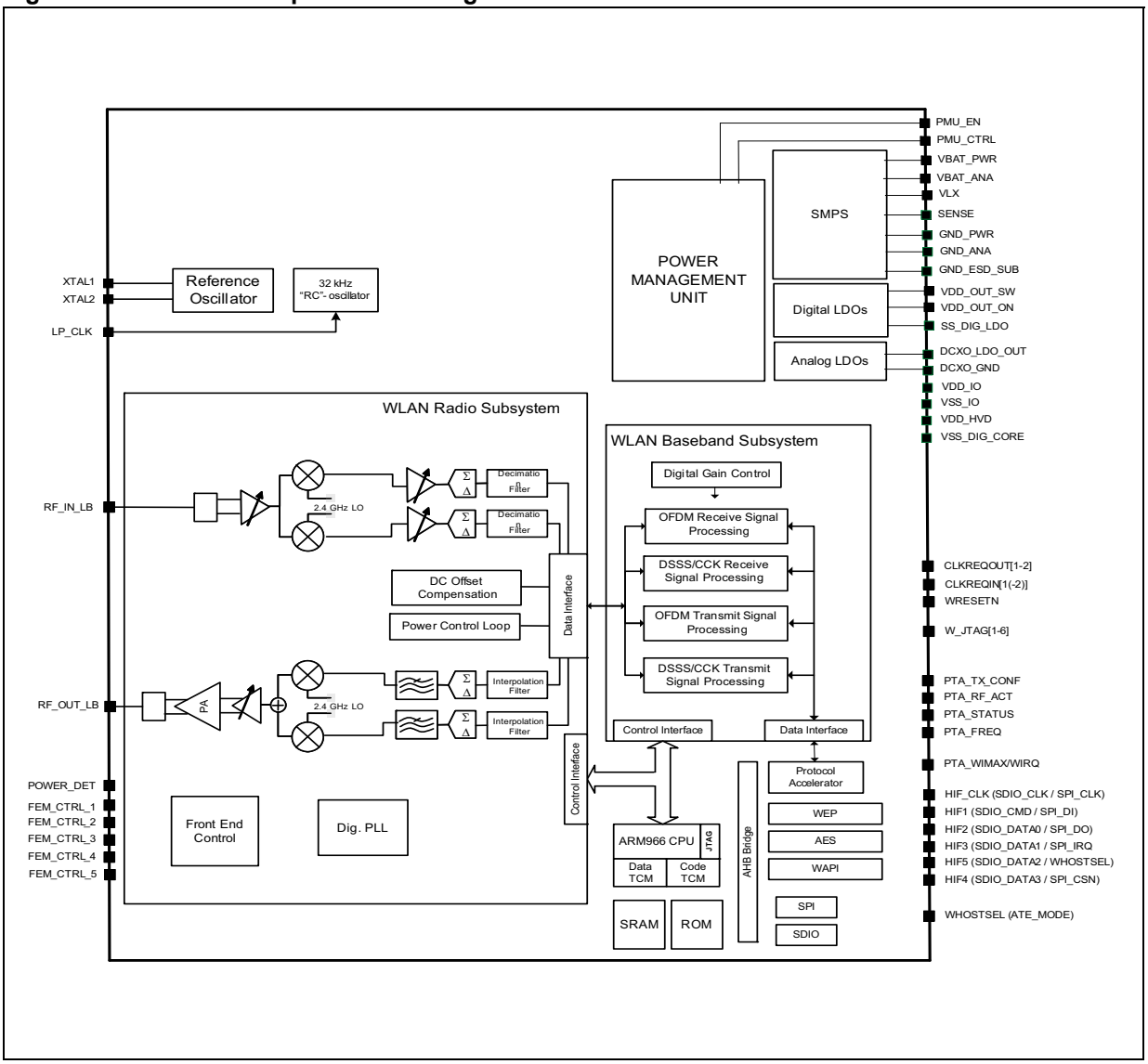
The WLAN subsystem includes a ZIF transceiver, RF synthesizer/VCO, high-speed data converters, an OFDM/CCK digital baseband processor, a power amplifier, switch mode power supply and an ARM9-based MAC.

A comprehensive single band reference design is provided that includes a switch that combines the TX and RX ports from the WLAN with the RF port from a Bluetooth device onto one 2.4 GHz antenna. A band-pass filter is added between the switch and the antenna depending on the presence of other wireless devices in the same application.

2 General hardware description

2.1 Block diagram

Figure 2. CX1001 complete block diagram



2.2 Electrical data

2.2.1 Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Vbat	Direct battery connect supply voltage	-0.3	5.5	V
VDD_HV	Supply voltages	-0.3	2.0	V
VDD_IO	Supply voltage I/O	-0.3	2.0	V
Vin	Input voltage on any digital pin	-0.3	2.0	V
Vssdiff	Maximum voltage difference between different types of Vss pins	-0.3	0.3	V
Tstg	Storage temperature	-65	+150	°C

2.2.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 2. Operating ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature	-40	25	+85	°C
Vbatt	Direct battery connect supply voltage: – All specs guaranteed – All specs guaranteed with output power back-off – Device functional with reduced performances (see section *Section 4.2.1*)	 3.6 2.7 2.3		 4.8 3.6 2.7	 V V V
VDD_ HVD	Supply voltages – All specs guaranteed – Device functional with reduced performances	 1.65 -	 1.8 1.5	 1.95 -	 V V
VDD_IO	I/O supply voltage 1.8 V mode	1.65	1.8	1.95	V
	I/O supply voltage 1.2 V mode	1.1	1.2	1.3	V

2.2.3 Digital I/O specifications

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7. The tables below summarize these specifications.

Table 3. DC and AC input specification

Symbol	Parameter	Min	Typ	Max	Unit
Input levels					
V_{IL}	Low level input voltage	0		0.35 * VDD_IO	V
V_{IH}	High level input voltage	0.65 * VDD_IO			V
V_{hyst}	Schmitt trigger hysteresis	150			mV
T_r/T_f	Rise and fall time that can be present on inputs			25	ns
R_i	Input resistance	1			MΩ
C_i	Input capacitance			5	pF
Output levels					
V_{OL}	Low level output voltage (@ 100 µA)	0		0.2	V
V_{OH}	High level output voltage (@ -100 µA)	VDD_IO - 0.2		VDD_IO	V
T_r/T_f	Rise and fall time that can be present on outputs at cload = 20 pF max			10	ns

Table 4. Pull-up and pull-down characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Equivalent pull-up resistance	VDD_IO_x = 0 V		50		kΩ
R_{PD}	Equivalent pull-down resistance	VDD_IO_x = 1.8 V		50		kΩ

Table 5. IOL and IOH characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Sink current	V_{OL} = Max	X(1)			mA
I_{OH}	Source current	V_{OH} = Min	X(1)			mA

1. X can be 2, 4 or 8 depending on the type of the I/O (X denotes the drive strength of output stage).

If the VDD_IO supply is down, external activity on the IOs is not allowed.

2.2.4 Handling information

Inputs and outputs are protected against electrostatic discharges during handling and mounting. All pins withstand the following threshold voltages.

Table 6. ESD threshold voltages

Parameter	Method	Value	Class
ESD threshold voltage	HBM (JESD22-A114-F)	±1 kV(1)	Class Ic
	CDM (JESD22-C101-D)	±200 V(1)	Class II

1. The weakest pins are RF_IN_LB and RF_IN_HB.

2.2.5 Thermal characteristics

Table 7. Package thermal resistance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Θ_{J-A}	Junction-to-air thermal resistance	Eight layers PWB construction Board dimensions = 76 x 102 x 1 mm Natural convection	33(1)		46(2)	°C/W
Ψ_{J-B}	Junction-to-board thermal resistance		20(1)		28(2)	°C/W

1. NVTTE V4 with top side heat spreader (50 x 50 x 1 mm)
2. NVTTE V2

2.2.6 Clock specifications

For more details on the clocks see *Section 2.5*.

The CX1001 uses two clocks: a reference clock and a low power clock. For the reference clock, CX1001 can either use an external reference clock source or generate its own reference using a XTAL and a built-in oscillator. The low-power clock always has to come from an external source.

Table 8. Reference clock overall specifications

Symbol	Parameter	Min	Typ	Max	Unit
Using an external reference clock					
F_{IN}	Clock input frequency list	13, 16, 16.8, 19.2, 26, 33.6, 38.4, 40, 52			MHz
F_{INTOL}	Tolerance on input frequency	-20		20	ppm
t_{STABLE}	Clock stabilization time(1)		<10	15(2)	ms
Using one XTAL and the built-in oscillator					
F_{IN}	Clock input frequency list	38.4, 40, 52			MHz
F_{INTOL}	Combined inaccuracies of the XTAL after tuning(3)	-20		20	ppm

1. Time between clock request signal asserted by the IC until reference clock is stable. It is recommended that the system provides a stable clock in less than 10 ms.
2. Software programmable waiting time up to maximum 15 ms by discrete steps.

3. See *Section 2.5.2*

Table 9. Low power clock specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequencies		32.768		kHz
F_{INTOL}	Tolerance on input frequency	-1000		1000	ppm

2.2.7 Current consumption

Table 10. CX1001 current consumption

State	Vbat (Inc PA)		Vbat (Excl PA)		VIO		Unit
	Typ	Max	Typ	Max	Typ	Max	
Tamb = 25°C, 26 MHz digital clock, Vbat = 3.6 V, VDD_HV = 1.8 V, VDD_IO = 1.8 V.							
Complete power down(1) (WRESETN low, PMU_EN high)	61	-	56	-	7		µA
Complete power down(1) (WRESETN low, PMU_EN low)	10	-	5	-	7	-	µA
Sleep(1)	80	-	75	-	25	-	µA
Power save (beacon period (including DTIM) 100 ms, beacon length 1 ms) – proprietary power saving features disabled – proprietary power saving features enabled	 1.02 0.85	 - -	 1.01 0.85	 - -	 0.06 0.03	 - -	 mA mA
RX (Idle(2)), 2.4 GHz	72	-	72	-	0.07	-	mA
RX (Active(3), 2.4 GHz, OFDM)	75	-	75	-	0.87	-	mA
TX (Active(3), 2.4 GHz, OFDM), 17.5 dBm @ chip pin output(4)	294	-	112	-	0.67	-	mA
TX (Active(3), 2.4 GHz, OFDM), 21 dBm @ chip pin output(4)	366	-	112	-	0.67	-	mA
A VoIP call using a standard codec G.711 (64Kb/s, 320 byte packets) and U-APSD (WMM Power Save) power-saving mode	5.18	-	4.10	-	0.04	-	mA
Video Streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example MPEG-4 @ 2 Mbps)	15.03	-	13.16	-	0.10	-	mA
Ipeak: system maximum peak current draw(5)	-	398	-	-	-	4(6)	mA
Tamb = 25°C, 26 MHz digital clock, Vbat = 3.6 V, VDD_HV = 1.5 V, VDD_IO = 1.8 V.							
Complete power down(1) (WRESETN low, PMU_EN high)	60	-	55	-	7	-	µA
Complete power down(1) (WRESETN low, PMU_EN low)	10	-	5	-	7	-	µA
Sleep(1)	76	-	71	-	25	-	µA
Power save (beacon period (including DTIM) 100 ms, beacon length 1 ms) – proprietary power saving features disabled – proprietary power saving features enabled	 0.89 0.74	 - -	 0.88 0.74	 - -	 0.06 0.03	 - -	 mA mA

Table 10. CX1001 current consumption (continued)

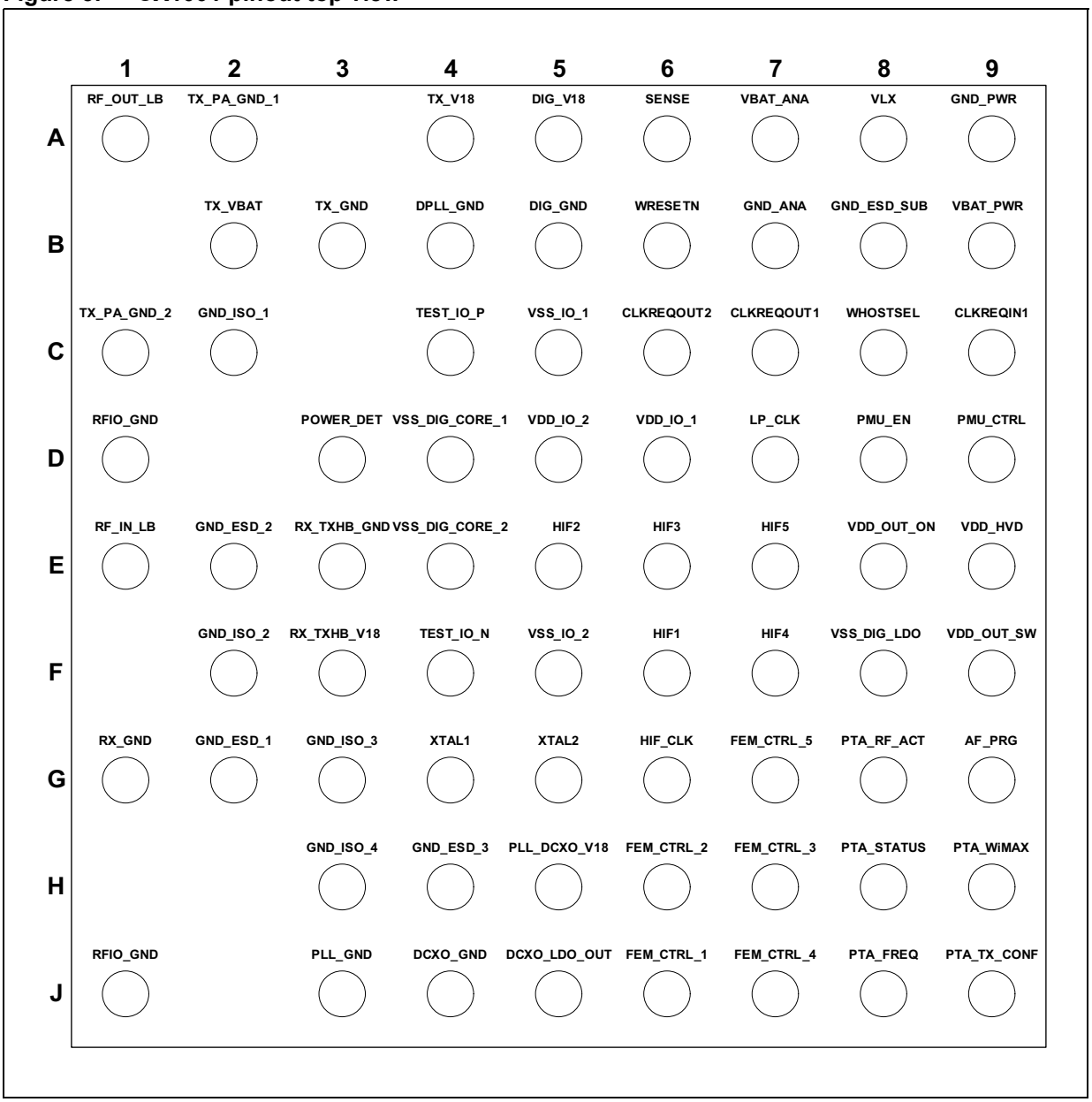
State	Vbat (Inc PA)		Vbat (Excl PA)		VIO		Unit
	Typ	Max	Typ	Max	Typ	Max	
RX (Idle[2]), 2.4 GHz	62	-	62	-	0.07	-	mA
RX (Active[3], 2.4 GHz, OFDM)	65	-	65	-	0.87	-	mA
TX (Active[3], 2.4 GHz, OFDM), 14.0 dBm @ ANT output [4]	279	-	97	-	0.67	-	mA
A VoIP call using a standard codec G.711 (64 Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode	4.61	-	3.54	-	0.04	-	mA
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example MPEG-4 @ 2 Mbps	13.21	-	11.34	-	0.10	-	mA
Ipeak: system maximum peak current draw[5]	-	378	-	-	-	4[6]	mA

1. See *Table 30* for a detailed explanation.
2. All RX circuitry is enabled but there is no signal to be received
3. 100% of the time
4. Those are the maximum output power levels allowed by the system at 6 Mbps (BPSK 1/2) and 54 Mbps (64QAM 3/4). See *Table 44* for details.
5. Including all power rails of CX1001 connected directly or indirectly (through SMPS) to Vbat. Excluding the additional draw from Vbat due to (an)other circuit(s) supplied by the SMPS output.
6. Including 1 mA to drive the external switch control.

2.3 Pinout

2.3.1 Pin layout

Figure 3. CX1001 pinout top view



2.3.2 Pin functions

Table 11. CX1001 functional and supply pin list

Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
Clock signals						
XTAL1	G4	I/O	I/O	None	Reference clock input or XTAL inputs	
XTAL2	G5	I/O	I/O	None		
LP_CLK	D7	I	I	None	Low power clock input	
Control signals						
WRESETN	B6	I	I	PD	Reset - active low	
WHOSTSEL	C8	I	I	None	Test mode selection - active high	
CLKREQIN1	C9	I/O	I	PD	Programmable pin	CLK_REQ_IN
CLKREQOUT1	C7	I/O	I	PD		CLKREQOUT
CLKREQOUT2	C6	I/O	I	PU		CLKREQOUTN
PMU_EN	D8	I/O	I	None(1)		SMPS enable(2)
PMU_CTRL	D9	I/O	I	PD		SMPS mode control
Digital interfaces						
HIF1	F6	I/O	I	None	Programmable pin	SDIO_CMD / SPI_DI
HIF2	E5	I/O	I	None		SDIO_DATA0 / SPI_DO
HIF3	E6	I/O	I	None		SDIO_DATA1 / WIRQ
HIF4	F7	I/O	I	None		SDIO_DATA3 / SPI_CSN
HIF5	E7	I/O	I	None		SDIO_DATA2 / HIF selection(3)
HIF_CLK	G6	I/O	I	None		SDIO_CLK / SPI_CLK
PTA_TX_CONF	J9	I/O	I	PD		PTA_TXCONF
PTA_RF_ACT	G8	I/O	I	PD		PTA_RF_ACT(4)
PTA_STATUS	H8	I/O	I	PD		PTA_STATUS
PTA_FREQ	J8	I/O	I	PD		PTA_FREQ
PTA_WIMAX	H9	I/O	I	None		PTA_WIMAX/WIRQ
RF interfaces						
POWER_DET	D3	I (analog)		None	FEM power detector interface	
RF_IN_LB	E1	I (RF)		None	RX 2.4 GHz inputs	
RF_OUT_LB	A1	O (RF)		None	TX 2.4 GHz output	

Table 11. CX1001 functional and supply pin list (continued)

Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
FEM control interfaces						
FEM_CTRL_1	J6	O	I	PD	Programmable pin	FEM controls
FEM_CTRL_2	H6	O	I	PD		
FEM_CTRL_3	H7	O	I	PD		
FEM_CTRL_4	J7	O	I	PD		
FEM_CTRL_5	G7	O	I	None		Bluetooth FEM control(5)
RF power supplies						
PLL_DCXO_V18	H5	-			1.8 V DCXO supply pin	
TX_V18	A4	-			1.8 V supply for WLAN RF transmit	
RX_TXHB_V18	F3	-			1.8 V supply	
TX_VBAT	B2	-			Supply for analog integrated PA (3.6 V)	
DIG_V18	A5	-			Supply for WLAN RF digital LDOs (1.8 V)	
DCXO_LDO_OUT	J5	-			Internal supply decoupling/regulator output	
GND_ESD_1	G2	-			Ground for WLAN analog	
GND_ESD_2	E2	-				
GND_ESD_3	H4	-				
DCXO_GND	J4	-				
GND_ISO_1	C2	-				
GND_ISO_2	F2	-				
GND_ISO_3	G3	-				
GND_ISO_4	H3	-				
TX_GND	B3	-			Ground for WLAN RF	
RX_GND	G1	-				
RX_TXHB_GND	E3	-				
TX_PA_GND_1	A2	-				
TX_PA_GND_2	C1	-				
RFIO_GND	D1					
RFIO_GND	J1					
DIG_GND	B5	-			Ground for WLAN RF digital	
DPLL_GND	B4	-				
PLL_GND	J3	-			Ground for WLAN PLL	

Table 11. CX1001 functional and supply pin list (continued)

Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
Digital power supplies						
VDD_IO_1	D6	-			Supply for digital I/Os (1.8 V)	
VDD_IO_2	D5	-				
VDD_HVD	E9	-			Supply for WLAN digital LDOs (1.8 V)	
VDD_OUT_SW	F9	-			Internal supply decoupling/regulator output (1.2 V)	
VDD_OUT_ON	E8	-			Internal supply decoupling/regulator output (1.2 V)	
VSS_IO_1	C5	-			Ground for digital	
VSS_IO_2	F5	-				
VSS_DIG_LDO	F8	-				
VSS_DIG_CORE_1	D4	-				
VSS_DIG_CORE_2	E4	-				
Other pins						
AF_PRG	G9	-			High voltage pad for antifuse programming (leave unconnected)	
TEST_IO_P	C4	-			WLAN ANA test I/O (connected to VSS_W_ANA)	
TEST_IO_N	F4	-				
SMPS						
VBAT_PWR	B9				Power stage supply pin	
VBAT_ANA	A7				Analog supply pin	
GND_PWR	A9				Power stage ground pin	
GND_ANA	B7				Analog ground	
GND_ESD_SUB	B8				ESD substrate ground	
SENSE	A6				Voltage sense across external capacitor	
VLX	A8				Pin for inductor connection (switch output)	
No Ball						
No ball	A3, B1, C3, D2, F1, H1, H2, J2				Those places in the grid are intentionally not occupied by any ball	

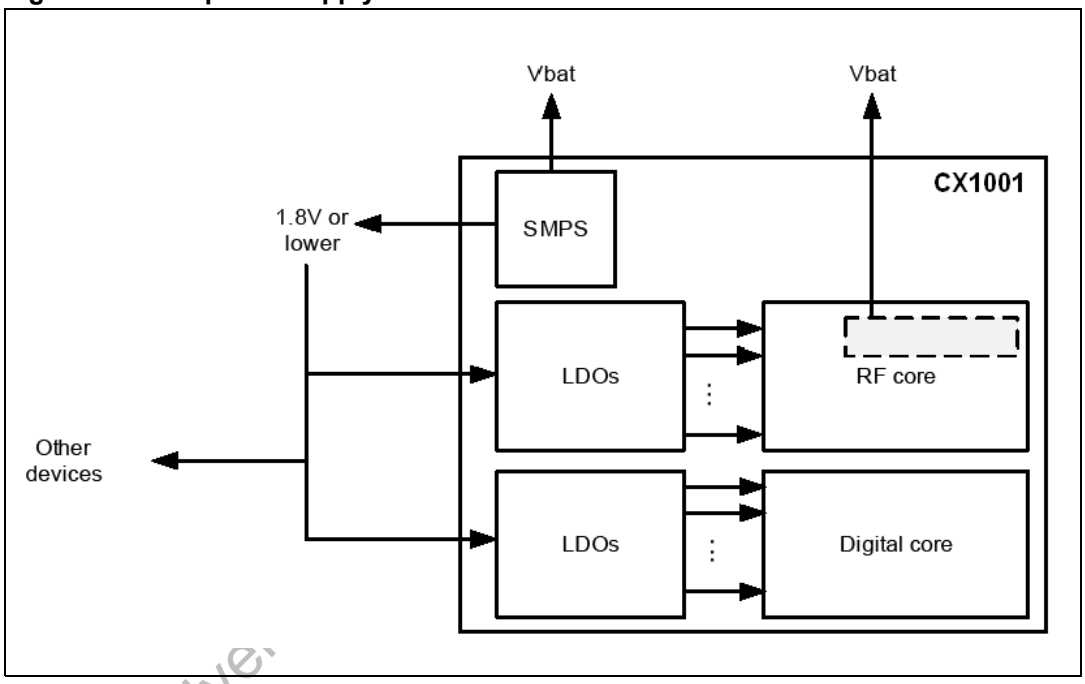
1. Input with PD when External SMPS used (VBAT_PWR and VBAT_ANA connected to GND), Input without pull when Internal SMPS used (VBAT_PWR and VBAT_ANA connected to Vbat).
2. PMU_EN maintains some functionality when the CX1001 is reset. See *Section 2*.

3. See *Section 2.6.1: General control signals* for the host interface mode selection mechanism.
4. PTA_RF_ACT maintains some functionality when CX1001 is reset. See *Section 2.6.5*
5. FEM_CTRL_5 maintains some functionality when CX1001 is reset. See *Section 2.6.4*..

2.4 Power supply

All circuits inside the CX1001 but the IOs are supplied by a single battery connection. The IOs are supplied by a regulated 1.8 V source assumed to be available from the platform and on which the consumption does not exceed a few mA (see *Table 10*). A simplified view of the supply distribution architecture is depicted in *Figure 4*. See *Section 2.2.1* about the absolute maximum ratings and operating conditions.

Figure 4. Simplified supply distribution architecture



2.4.1 SMPS

Features

- 2 switching modes are supported:
  - PWM mode optimizes efficiency while minimizing ripple and noise for large current outputs
  - PFM mode optimizes efficiency for small current outputs
- 2 output voltages are supported:
  - 1.8 V in order to support CX1001 in combination with (an)other component(s) like for instance ST-Ericsson's BT/FM/GPS device CX2001.
  - A SW-programmable voltage between 1.8 V and 1.4 V that minimizes CX1001 consumption. This second case can be used when no other component requires 1.8 V from the built-in SMPS
- Possibility to disable the SMPS in order to use an external SMPS
- High switching frequency allows the use of a small inductor value (hence a compact footprint) while maintaining a very low ripple at the output

SMPS use cases

Table 12. SMPS use cases

Use case	Configuration	Description
1	VBAT_PWR and/or VBAT_ANA connected to GND (1)	An external SMPS is used to supply CX1001. The built-in SMPS is disabled.
2	VBAT_PWR and VBAT_ANA connected to battery	The built-in SMPS is enabled. The selection of the output voltage (high or low, see *Table 16*) is done in SW, taking into account the state of PMU_EN. PMU_CTRL forces the SMPS in a PWM mode. For optimum operation, strap to GND. The SMPS will automatically switch from PWM to PFM depending on the current draw.

1. It is good practice to connect both to GND

SMPS control signals

Table 13. SMPS control signals

Signal	Use case[1]	Direction	Function
PMU_EN	1	Output	PMU_EN indicates the WLAN transceiver's power request. Active high.
	2	Input	PMU_EN enables the SMPS. PMU_EN is internally combined (OR) with the WLAN transceiver power request. The circuitry behind PMU_EN is supplied by VDD_IO_x. It remains functional when the WLAN transceiver is reset (WRESETN=low) or when it's core is not supplied. Multiple request can be combined externally by a wired-OR. Active high.
PMU_CTRL	1	Output	PMU_CTRL indicates CX1001 requests to an external SMPS to go in PWM mode.
	2	Input	PMU_CTRL forces the SMPS in a PWM mode. PMU_CTRL is internally combined with the CX1001 low noise supply requirement. Multiple request can be combined externally by a wired-OR. Active high strap to GND for optimum operation.

1. See section *SMPS use cases*.

SMPS other signals

Table 14. SMPS other signals

Signal	Direction	Function
VBAT_PWR	Supply	Power stage supply pin. Electrical path to decoupling should be kept minimal.
VBAT_ANA	Supply	Analog supply pin.
GND_PWR	GND	Power stage GND pin. Electrical path to decoupling should be kept minimal.
GND_ANA	GND	Analog GND pin.
GND_ESD_SUB	GND	ESD substrate GND pin.
SENSE	Input	It senses the voltage across the output capacitor. See *Figure 6* on precautions regarding this signal.
VLX	Output	SMPS output to be routed directly to the external LC.

External components

Figure 5. External components around the SMPS

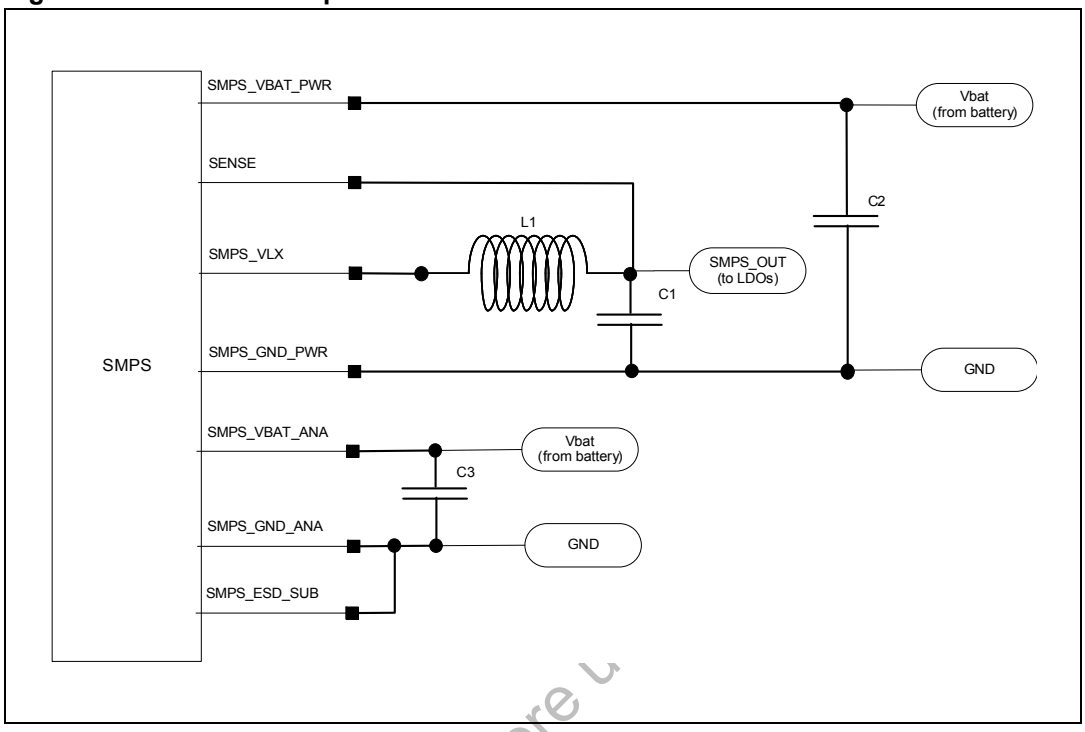
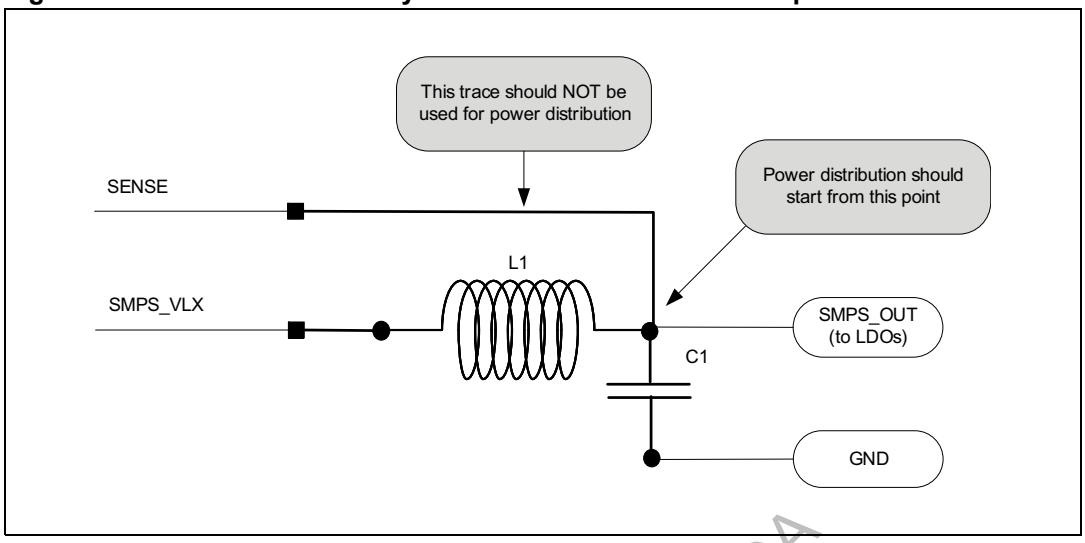


Table 15. External components around the SMPS

Component reference	Requirements	Suggested parts
L1	L = 1 µH I sat > 750 mA Rs < 200 mΩ	0603: Murata LQM18PN1R0NF0 0603: TDK GLCR1608T1R0M 0805: Murata LQM21PN1R0MC0
C1	C = 4.7 µF Rated voltage > 2.5 V Rs < 200 mΩ Ls < 0.750 pH	0402: Murata GRM155R60G475M / GRM155R60J475M
C2	C = 2.2 µF (or higher), Rated voltage ≥ 6.0 V Ls < 200 pH	0402: GRM155F50J225Z / GRM155R61A225K
C3	C = 100 nF Rated voltage ≥ 6.0 V	0201: GRM0336R0J104K

Figure 6. Precaution in the layout of the SMPS external components



SMPS performances

Table 16. SMPS performances (measured across the output capacitor unless otherwise specified)

Specification	Conditions	Min	Typ	Max	Unit
Input voltage					
See operating ranges in *Table 2*					
Output voltage					
Vout (output high)	± 5% accuracy	1.71	1.8	1.89	V
Vout (output low)	± 5% accuracy	Programmable in SW			
Vout ripple (output high)(1)	PWM			10	mVpp
	PFM			40	mVpp
Vout load regulation	From 10% to 90% of Iload max or vice versa	-50		50	mVpp
Vout line regulation	Input voltage drops 400 mv during GSM PA bursts	-50		50	mVpp
Currents					
Ileak			1		µA
Iload max	Maximum peak current through L1 before hitting overload protection	675	750	825	mA

Table 16. SMPS performances (measured across the output capacitor unless otherwise specified) (continued)

Specification	Conditions	Min	Typ	Max	Unit
Switching					
Fswitch	PWM switching frequency range. SW programmable	9	10	11	MHz
Efficiency and mode of operation					
Efficiency	PFM	80			%
	PWM	85			%
Iswitch	PFM if Iout ≤ Iswitch PWM if Iout > Iswitch		70		mA

1. The actual ripple on the supplied components is lowered by the presence of additional decoupling capacitors.

2.4.2 Power-up/power-down

Reset and power-up

There is no constraint on the power supplies (VDD_HVx, and VDD_IO_x) activation sequence.

The device is able to start up without the reference clock being present. The chip shall request it through the use of one of the CLKREQOUTx signals. The platform is than expected to provide a stable clock within *Tstable* ms (see *Table 17*) unless the built-in XTAL oscillator is used.

A valid reset shall be obtained by maintaining WRESETN active (low) for at least two cycles of LP_CLK after VDDIO is stable within it operating range. There is no constraint on the activation of the other supplies during this process. The reset is propagated to the core during the startup sequence described below.

A typical startup for the WLAN system is as follows:

- VDDIO is applied
- LP_CLK (low power clock) is running and stable
- WRESETN pin is released after at least two LP_CLK cycles
- PMU_EN is asserted in case the internal SMPS is not used. The built-in SMPS is activated in case it is used. In both cases, VDD_W_HV_x and VDD_W_CORE_x shall get a valid supply within 20 ms
- The host should wait 30 ms after the WRESETN release for the on-chip LDO to stabilize
- The chip is now in the sleep state
- The host should now wake the device by writing over the host interface, SPI or SDIO, to WUP bit
- The device asserts CLKREQOUTx to request the reference clock
- Within *Tstable* ms, the reference clock should be stable and the system can start using it
- The device will set the RDY (ready) bit and assert IRQ to the host
- The host can download the firmware and release the CPU reset by further SPI/SDIO write
- The host now waits for the CX1001 sub-system to initialize and can clear the WUP bit
- Once initialized, which includes a series of message passing between the host and the WLAN, the WLAN may not have anything further to do and will enter the sleep state

More detailed information on this startup sequence and the required host commands can be found in the hardware user manual.

The power down of the device does not imply any constraint. It is also recommended that the platform activates the RESETN at least 2 LP_CLK cycles before powering-off of the supplies.

2.5 Clocks

2.5.1 Reference clock (system clock)

The reference clock is the main clock of the CX1001. It is provided to the chip either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using a crystal directly connected to the device.

Table 17. Reference clock overall specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequency list Using an external clock source	13, 16, 16.8, 19.2, 26, 33.6, 38.4, 40, 52			MHz
	Clock input frequency list Using a XTAL and the built-in oscillator	38.4, 40, 52			MHz
F_{INTOL}	Tolerance on input frequency without trimming(1)	-20		20	ppm

Table 17. Reference clock overall specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit
$F_{INTTRIM}$	Tolerance on input frequency with trimming(1)(2)	-50		50	ppm
Tstable	Clock stabilization time(3)		< 10	15(4)	ms
I_{LEAK}	Input leakage current, both for analog and digital			1	µA

1. See *Trimming*.
2. This is the initial acceptable range. Variation over time will however meet the FINTOL requirements.
3. Time from the moment the clock request signal is asserted by the IC until the reference clock is stable. It is recommended that the system provides a stable clock in less than 10 ms
4. Wait for the software programmable time up to a max of 15 ms by discrete steps

Clock frequency detection

An integrated automatic detection algorithm detects the reference clock frequency using the low power clock after a hardware reset.

Clock source detection

An integrated automatic detection mechanism detects the clock source from the connections of the XTAL1 and XTAL2 pins:

- When an external reference clock source is used, the clock input pin is XTAL2. The CX1001 supports both an analog or digital source. An analog source shall be AC coupled to XTAL2 while a digital source shall be DC coupled to XTAL2. In both cases XTAL1 shall be DC grounded
- When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to XTAL1 and XTAL2

External clock source

- Requirements

Table 18. External clock requirements

Symbol	Parameter	Min	Typ	Max	Unit
AC coupled analog signal					
V_{APP}	Peak-to-peak voltage range of the AC coupled analog input	0.4	0.5	1.2	Vpp
DC coupled digital signal					
V_{IL}	CX1001 input low voltage on XTAL1 and XTAL2(1)	0		0.3* VDDIO	V
V_{IH}	CX1001 input high voltage on XTAL1 and XTAL2(1)	0.7* VDDIO		VDDIO	V
T_r/T_f	10%-90% Rise and fall time	1		5	ns
Duty cycle		35	50	65	%

Table 18. External clock requirements (continued)

Symbol	Parameter	Min	Typ	Max	Unit
Both analog and digital signals					
Z_{INRe}	Real part of parallel AC input impedance at pin	30	100		kΩ
Z_{INIm}	Imaginary part of parallel AC input impedance at pin		2	4.7	pF
Z_{IDRe}	Change in real part of parallel impedance at pin when changing mode(2) (expressed in equivalent parallel resistance added or removed)	150			kΩ
Z_{IDIm}	Change in imaginary part of parallel impedance at pin when changing mode(2)(expressed in equivalent parallel resistance added or removed)			0.5	pF
Z_{DC}	DC input impedance	10			MΩ
$Jitter_{cc}$	Cycle-to-cycle jitter, 6 sigma value			250	ps
$Jitter_{pp}$	Peak-to-peak jitter during clock activation to ensure that PLL stays locked			1	ns
Phase noise	RefClk @ 26 MHz, 2.4 GHz 802.11 b/g/n @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz			 -123 -133 -138 -138	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz

1. Those are not the same as the VIH and VIL of other digital IOs.
2. When changing from a mode where the clock is used (active for instance) to a mode where it is not used (deep sleep for instance)

- Trimming

  The WLAN system supports a default inaccuracy of its system clock (hence the radio LO) of up to ± 20 ppm. The CX1001 chip is able to handle a higher inaccuracy of its reference clock up to ± 50 ppm. A correction is then applied in the block that derives the system clock from the reference clock. In this case, the correction value needs to be provided to the CX1001. This trimming is supported in the three cases; when this clock is provided to the chip either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using a crystal directly connected to the device.

- Clock request signals

  To minimize power consumption, a clock request output feature is available so that the reference clock can be stopped when not needed by the WLAN system. The clock request output signal can be active high or active low, and the CX1001 supports internal propagation of a clock request input signal coming from another device in the system. The clock request input shall always be active high. When the reference clock is generated from an external crystal directly connected to the chip, these clock request signals are not used.

  Different configurations as described below are supported immediately after reset and in all modes of operation, provided that VDD_IO is available.

  The clock request functionality is based on three signals: CLKREQOUT1, CLKREQOUT2 and CLKREQIN1, with the following function:

  – CLKREQOUT1: active high clock request output. Support for either push-pull or open drain output
  – CLKREQOUT2: active low clock request output. Support for either push-pull or open drain output
  – CLKREQIN1: active high clock request input from another device

Built-in oscillator and XTAL

Table 19. External crystal characteristics requirements

Parameter	Conditions	Min	Typ	Max	Unit
Crystal nominal frequency		38.4, 40, 52			MHz
Crystal mode		Series			
Crystal drive level				100	µW
Crystal ESR				50	Ω
Crystal frequency accuracy at nominal temperature	Reference: 25 °C	-10	0	+10	ppm
Crystal pullability		10		150	ppm/pF
Crystal drift due to ageing	After 5 years	-3	0	+ 3	ppm
Crystal drift due to temperature	Reference: 25 °C Range: -30 to +85 °C	-12	0	+12	ppm
Load capacitance			8		pF

The XTAL oscillator is a DCXO. With the XTAL properties mentioned in *Table 19*, the initial frequency accuracy can be tuned down to 2 ppm. Combined with the ageing and temperature drift, this leads to a 20 ppm maximum offset of the local oscillator. This tuning requires an accurate reference that can be provided during production for instance.

2.5.2 Low power clock (sleep clock)

This clock is used for the low power modes of WLAN systems. If an external low power clock source is used, it must be available after power-up and before the reset is released. It must also remain active all the time until the chip is powered off. If no such external clock source is detected when the reset is released, an internal oscillator will be started and used a low power clock source.

This clock is provided to the chip through a standard digital input, LP_CLK, with default characteristics. The input contains a Schmitt trigger and does not contain any pull.

Table 20. Low power clock requirements

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Frequency		32.768		kHz
F/F_{IN}	Frequency accuracy	-1000		1000	ppm
Duty cycle		30		70	%
Rin	Input resistance	1			MΩ
Cin	Input capacitance			5	pF
Jitter	Cycle-to-cycle	-40		+40	ns
V_{IL}	CX1001 input low voltage on LPCLK	0		0.2	V
V_{IH}	CX1001 input high voltage on LPCLK	VDDIO-0.2		VDDIO	V
Tr/Tf	Rise and fall time			500	ns

2.6 Digital interfaces

2.6.1 General control signals

The CX1001 supports several control signals that have impact on the operation of the full device (not dedicated to a specific function). Some of these signals are available by default on a pin, others can be mapped to a programmable pin.

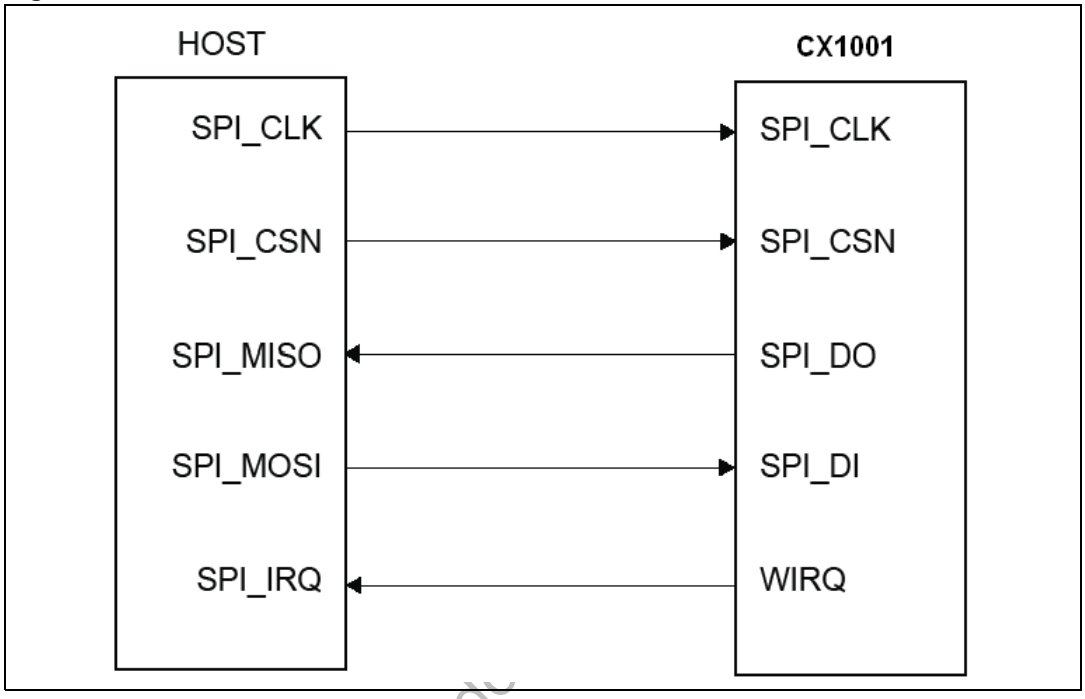
Table 21. Control signals

Signal	Direction	Function
WRESETN	Input	RESET of the WLAN subsystem.
CLKREQOUT[1: 2]	(open drain) Output	Signal that requests the reference clock only when needed to allow power saving. An active high and an active low version of this signal are available, CLKREQOUT1 and CLKREQOUT2 respectively. See *External clock source* for details on the signal behavior. If the active high version is used, the active low can be used for another function after reset, and vice versa. Both versions can be reused after reset when a XTAL is used. When the signal is not asserted, the output is converted to a high Z mode. This way, several clock requests can be combined with a passive resistor.
CLKREQIN1	Input	Signal that allows the sharing of the reference clock between several devices on a board without the need of external components for the control of the enable of this clock. If this function is not used, the pin may be reused for other functions after reset. See *External clock source* for details on the signal behavior.
WHOSTSEL	Input	Configuration pin used to select the ATE test mode. This pin shall be strapped to GND for normal operation.
HIF5	Input/output	The state of this pin is monitored on the rising edge of WRESETN. – LOW selects SPI – HIGH selects SDIO Setup and hold time are those of the SDIO interface (see *Table 23*).

2.6.2 SPI interface

The physical SPI interface is a 5-wire data interface (SPI_CSN, SPI_CLK, SPI_DO, SPI_DI and SPI_INT).

Figure 7. SPI interface



The five signals of the SPI interface are the following:

- SPI_CSN: device select allows the use of multiple slaves (1 device select per slave). This signal is active low. This signal is mandatory, even with only one slave, because the host must drive this signal to indicate SPI frames
- SPI_CLK: clock signal, active for a multiple of data length cycles during an SPI transfer (SPI_CSN active). The clock is allowed to be active when SPI_CSN is not active, in order to serve other slaves
- SPI_DO: data transfer from slave to master. Data is generated on the negative edge of SPI_CLK by the slave and sampled on the positive edge of SPI_CLK. When SPI_CSN is inactive, this CX1001 output is in tristate mode
- SPI_DI: data transfer from master to slave. Data is generated on the negative edge of SPI_CLK by the master and sampled on the positive edge of SPI_CLK
- SPI_IRQ: interrupt from the slave, used to request an SPI transfer by the slave to the master. The signal is active high (host input must be level sensitive)

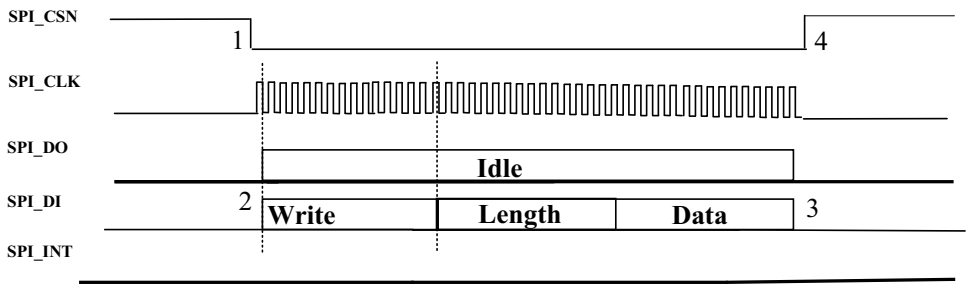
The SPI interface has the following characteristics:

- The maximum operating frequency is 52 MHz. The SPI interface in CX1001 supports the timings defined below
- The SPI interface is operating in half duplex mode
- The SPI interface is master at the host side, and slave at the CX1001 side
- The SPI data length, endianness and flow control are configurable. The host can change the configuration by writing in the SPI configuration register
- 16 and 32 bit word lengths are supported including the following configurable modes where [bn] is the bit transmission order from left to right:
  - 32-bit Mode0: [b15-b8], [b7-b0], [b31-b24], [b23-b17]
  - 32-bit Mode1: [b31-b24], [b23-b17], [b15-b8], [b7-b0]
  - 32-bit Mode2: [b7-b0], [b15-b8], [b23-b17], [b31-b24]
  - 16-bit Mode0: [b15-b8], [b7-b0]
  - 16-bit Mode1: [b7-b0], [b15-b8]
- Rising clock edge is used for sampling. Active clock edge for shifting is configurable (rise/fall)
- Supports automatic indirect addressing of device internal memory via fixed address SPI register to facilitate bulk DMA transfer
- Supports host wake up of the WLAN block by SPI register access

The default WLAN SPI configuration is:

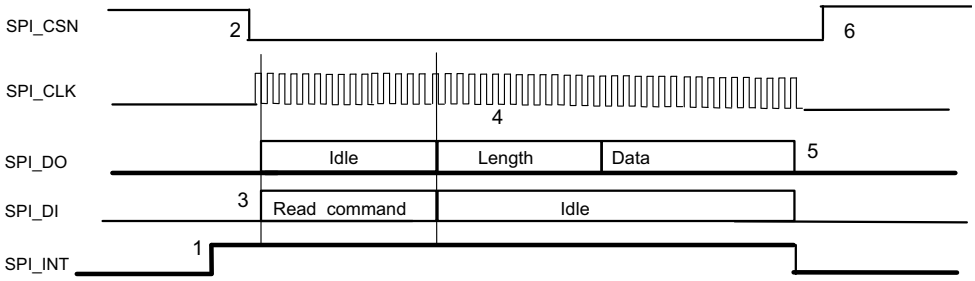
- 32 bit data length
- Most significant byte first, default is little endian
- Most significant bit first
- Flow control on SPI_DO and in a register

Figure 8. Default SPI data transfer from the host (master) to the CX1001 (slave)



1: Master selects the Slave
2: Master sends Write command and data to Slave
3: All data have been transmitted
4: Master de selects Slave

Figure 9. Default SPI data transfer from the CX1001 (slave) to the host master



1: Slave requests the bus
2: Master selects the Slave
3: Master sends Read command to Slave
4: Slave sends back Length and Data
5: All data has been transmitted
6: Master de -selects the Slave

Figure 10. SPI setup and hold timing

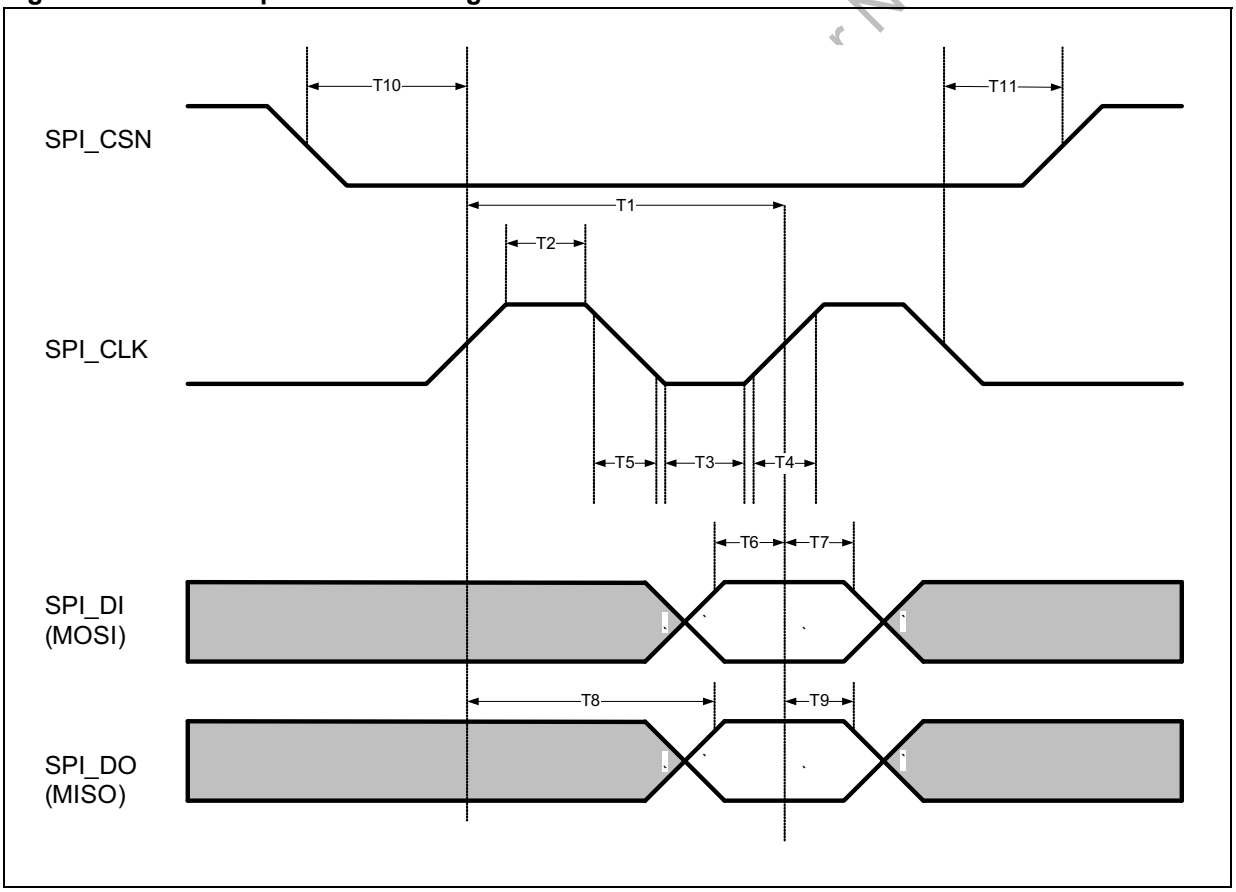


Table 22. SPI timing parameters

Symbol	Description	Min	Typ	Max	Unit
T1	Clock period	19.23(1)			ns
T2 & T3	Clock high and low duration	(0.45*T1)-T4		(0.55*T1)-T4	ns
T4 & T5	Clock rise and fall time (10% to 90%)	1		2.5	ns
T6	Input setup time (SPI_DI valid to SPI_CLK active edge)	5.0		-	ns
T7	Input hold time (SPI_CLK active edge to SPI_DI invalid)	5.0		-	ns
T8	Output setup time (SPI_CLK active edge SPI_DO valid)	-		14.23 (2)	ns
T9	Output hold time (SPI_CLK active edge to SPI_DO invalid)	5.0		-	ns
T10	CSN to clock (CSN fall to 1st rising edge)	5.0			ns
T11	Clock to CSN (Last falling edge of SPI_CLK to CSN rising edge)	1.0		-	ns

1. 19.23 ns = 1/52 MHz
2. 14.23 ns = 19.23 ns - 5 ns

2.6.3 SDIO interface

The SDIO interface is a 4 to 6-wire data interface (SDIO_CLK, SDIO_CMD, SDIO_DATA0, SDIO_DATA1/INT, optional SDIO_DATA2 and SDIO_DATA3). The SDIO interface is compatible with the SDIO specification version 1.10 *[3]*, with the exception that a) the voltage range is not SD compatible, but is compatible with the standard I/O levels defined in this document b). Interrupt may be generated to the host in 4-bit SDIO mode even with no SDIO clock, max clock frequency is 26 MHz.

The 6 signals of the SDIO interface are the following:

- SDIO_CLK: clock signal
- SDIO_CMD: bidirectional SDIO command line
- SDIO_DATA0: bidirectional data line
- SDIO_DATA1/INT: bidirectional data line. When no data is present on the line, it is used as interrupt from the slave, used to request an SDIO transfer from the slave to the master
- SDIO_DATA2: optional bidirectional data line
- SDIO_DATA3: optional bidirectional data line

In case the host does not support an in-band interrupt signal, an optional 7th signal can be used for that purpose:

- WLAN_IRQ (multiplexed on PTA_WiMAX) may optionally compliment (duplicate) the interrupt function of SDIO_DATA1

The SDIO interface has following characteristics:

- The maximum operating frequency is 26 MHz. The SDIO interface in CX1001 supports the timings defined below
- The SDIO interface is master at the host side, and slave at the CX1001 side
- Operation in SD mode from 1 to 4 data bits

Figure 11. SDIO interface timing

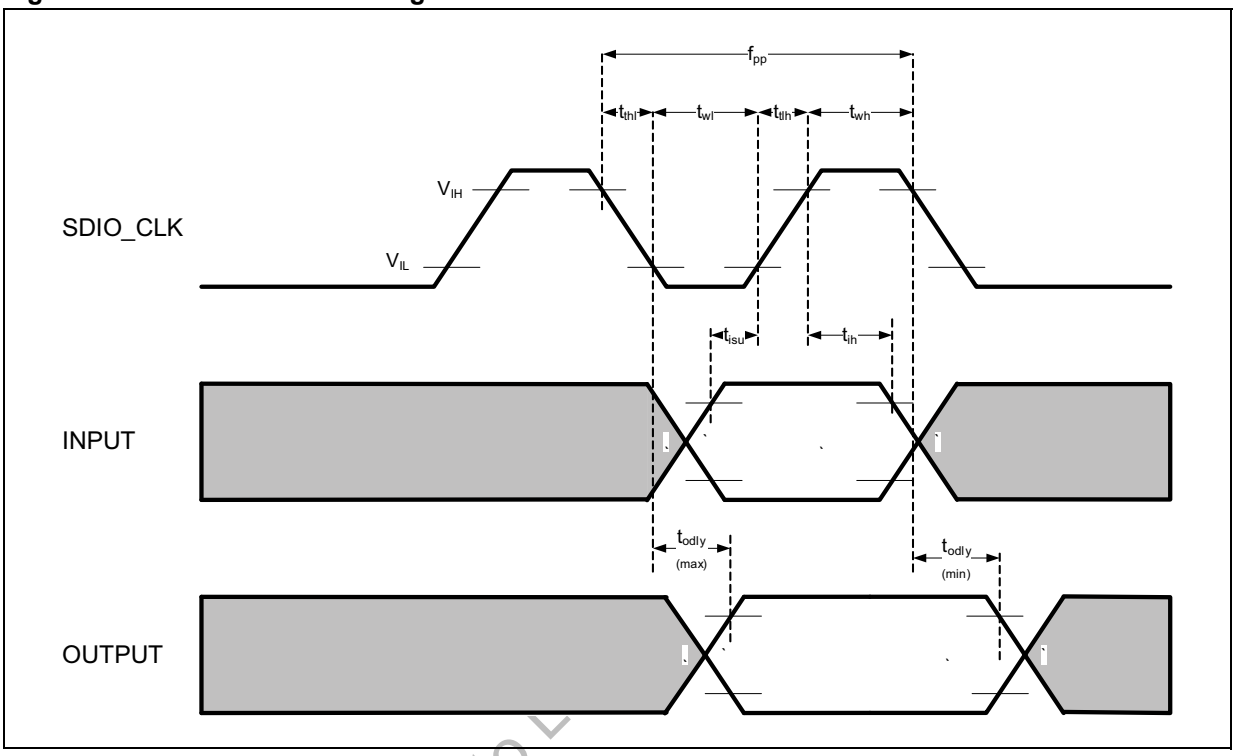


Table 23. SDIO interface timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{pp}	Clock frequency (data transfer mode)	0		26	MHz
t_{thl}	Clock fall time			9	ns
t_{tlh}	Clock rise time			9	ns
t_{wl}	Clock low time	10			ns
t_{wh}	Clock high time	10			ns
t_{isu}	Input setup time	5			ns
t_{ih}	Input hold time	5			ns
t_{odly}	Output delay time (during data transfer mode)			14	ns

2.6.4 FEM control signals

The CX1001 has 5 dedicated IOs to control the state of the Front-End Module and or antenna switch.

Four of the IOs are reserved to control the TX/RX antenna switch for the 2.4 GHz frequency band. The matching of the four IOs to the four functions is programmable software. Typically the four IOs will be allocated in a way that makes the board layout easier. The behavior of those IOs is controlled by PTA (see *Section 2.6.5*) during normal operation. All IOs are configured as input and kept low by a pull-down resistor when the CX1001 is reset.

The fifth IO is reserved for the control of the BT switch. The behavior of this IO is controlled by the PTA block (see *Section 2.6.5*) even when CX1001 is reset. This guarantees that BT can access the media on request when WLAN is reset.

Table 24. Control signals

Signal	Direction	Function (control of antenna switch)
FEM_CTRL_1 FEM_CTRL_2 FEM_CTRL_3 FEM_CTRL_4	Output	2.4 GHz TX or 2.4 GHz RX; software programmable
FEM_CTRL_5	Output	BT

2.6.5 (e)PTA interface

Bluetooth and WLAN occupy the same 2.4 GHz ISM band which may lead to interference when operating concurrently. The IEEE standard 802.15.2 recommends a collaborative coexistence mechanism of Packet Traffic Arbitration (PTA) based on time-sharing BT and/or WLAN requesting the medium before any communication. In case of conflict, PTA decides whom to award the medium to, based on priority of the BT and WLAN traffic and their current status. By using the coexistence mechanism it is possible to dynamically allocate bandwidth to the two devices when simultaneous operations is required while the full bandwidth can be allocated to one of them in case the other does not require activity.

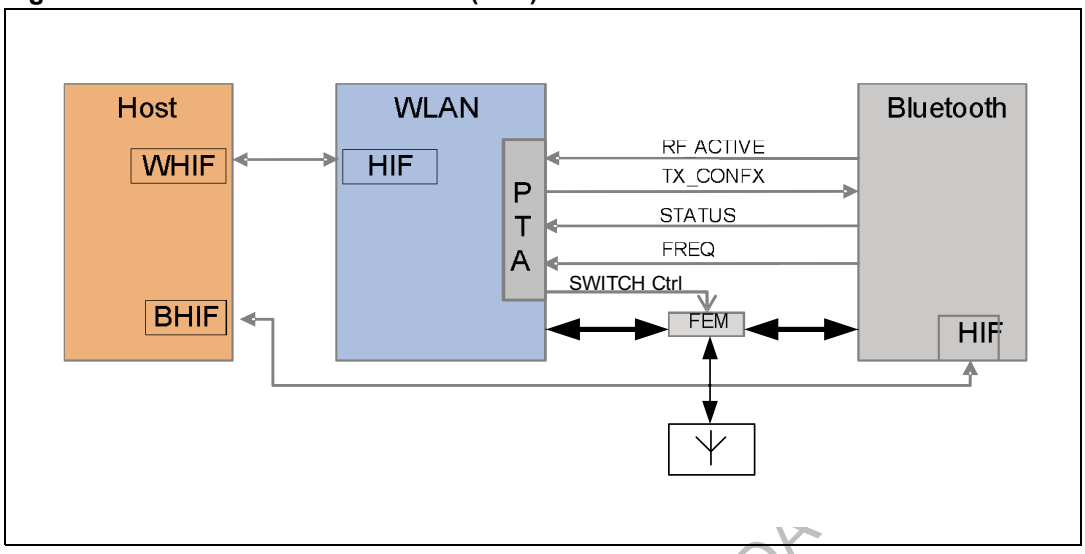
The combination of time division multiplexing and the priority mechanism avoids the interference due to packet collision. It also allows the maximization of the 2.4 GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link. A typical application would be to guarantee optimal quality to the Bluetooth voice communication while an intensive WLAN communication is ongoing.

CX1001 implements the IEEE 802.15.2 recommended practices referred to as standard PTA. CX1001 also implements further enhancements based on proprietary hardware and algorithms, known as ePTA. CX1001 also implements other simpler alternatives for compatibility with less advanced counter-parts.

Description of standard PTA

The standard PTA implementation in CX1001 uses a four-wire interface. The polarity of the signals is programmable.

Figure 12. Packet traffic arbitration (PTA) between BT and WLAN



Signal **RF_ACTIVE**, output from BT and input to PTA, is asserted prior to any BT transaction and it remains active for the duration of the transaction. The signal RF_ACTIVE synchronizes the PTA to the BT slots by occurring a fixed pre-defined period before the next BT slot. RF_ACTIVE will be de-asserted by BT as soon as possible at the end of the transaction.

The **STATUS** line, output from BT and input to PTA, is used to signal both the priority of the pending BT transaction and also the RX/TX status during the transaction. The priority of the transaction is signaled by the STATUS signal for a defined duration after the RF_ACTIVE is asserted. The PTA should sample the priority status during this defined window. After signaling of the priority, the STATUS line “may” signal the RX/TX mode of the BT.

The **FREQ** signal, output from BT, is optional, and is asserted when the BT transceiver hops into the restricted channels defined by the host.

The signal **TX_CONFX**, output from PTA and input to BT, is de-asserted when the PTA module wants to prevent BT transmission. The BT module shall not initiate a transmission when the TX_CONFX is de-asserted. The BT device samples the TX_CONFX prior to a TX slot. If TX_CONFX is de-asserted during an on-going BT transmission, the BT transmission may be continued to the end as scheduled.

When CX1001 is reset, the signal **TX_CONFX** will be kept low by a pull-down resistor in order not to block BT access to the media. The input **RF_ACTIVE** will be kept operational (including it's effect on the control of the antenna switch) when CX1001 is reset.

Figure 13. Timing diagram for the standard PTA signals

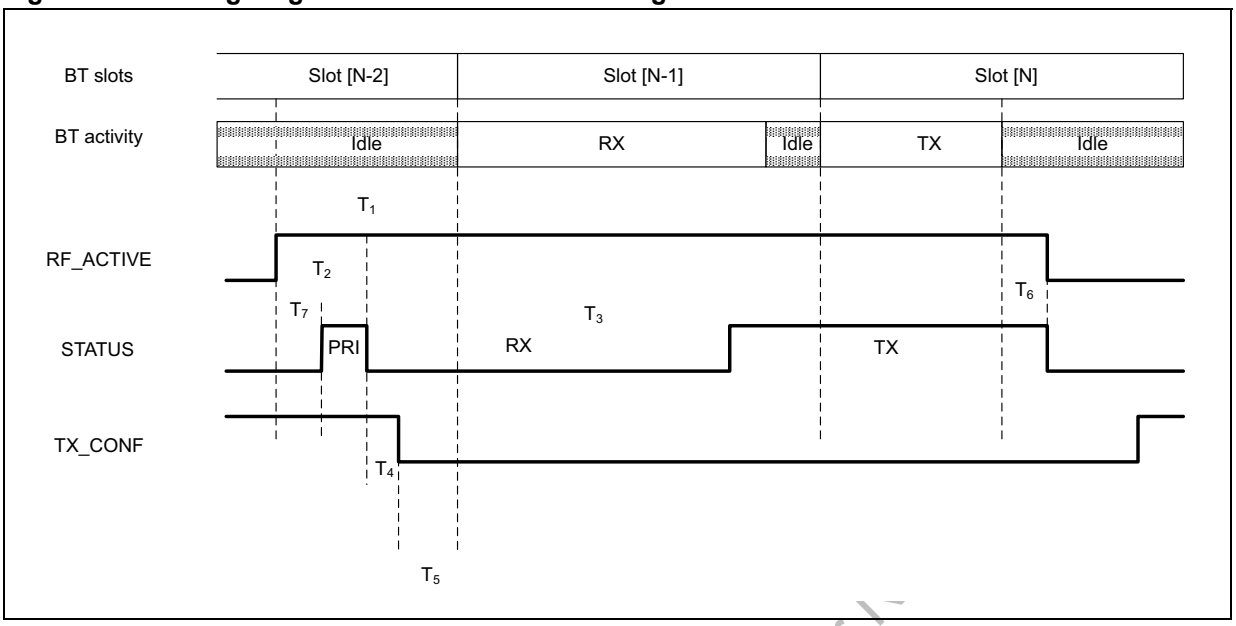


Table 25. Details on the timing constraints for PTA signals

Parameter	Min (µs)	Max (µs)	Description
T_1	100	200	RF_ACTIVE will be asserted no earlier than 200 µs and no later than 150 µs before the medium is required
T_2	15	20	The STATUS signal indicates the priority of a transaction for the duration of [T2-T7] after RF_ACTIVE is asserted. After T_2 STATUS line MAY indicate TX/RX mode of the subsequent slot(s)
T_3	0	475	If the STATUS signal will convey TX/RX mode, the STATUS signal shall be set to reflect the RX/TX mode for the slot N no later than 475 µs from the start of N-1 slot
T_4			For reference only
T_5	75		If ePTA wishes to prevent a BT transmission, then it must de-assert (logic high) the TX_CONFX signal at least 75 µs before the start of the BT transmit slot. The BT device will sample the TX_CONFX signal T_5 (or shortly after) before the start of the transmit slot in order to determine whether transmit is allowed. Whenever RF_ATIVE is asserted, ePTA shall not change the TX_CONFX inside the T_5 window prior to start of a TX slot
T_6		25	RF_ACTIVE shall be de-asserted within 25 µs after last RX or TX activity of the transaction has ended
T_7		1	The STATUS signal will indicate priority of the signal no later than 1 µs after RF_ACTIVE is asserted
T_8		20	If the BT device de-asserts RF_ACTIVE whilst TX_CONFX is de-asserted (e.g. in response to ePTA blocking BT TX), the ePTA must re-assert TX_CONFX line within T_8. This is incase the BT device immediately schedules a new transaction and asserts RF_ACTIVE

The PTA mechanism relies on both hardware and software parts. The PTA packet-wise arbitrator (hardware) can be programmed to implement multiple protections and ways to grant access to the medium to one system over the other (or to both simultaneously in RX sometimes). The high level controller (PTA firmware) controls the HW parameters and monitors the number of grant/access-denied/aborts of BT and WLAN traffic to ensure that the medium is shared efficiently and fairly over time.

Simplified description of enhanced PTA (or ePTA)

ST-Ericsson ePTA is an extension of the standard PTA protocol to increase the amount of information exchanged between BT and WLAN. A serial communication bus is multiplexed with the PTA signals and the FREQ line to transport additional information, optimizing the use of the existing bus.

FREQ line: on top of the TX/RX and priority information, the ePTA protocol foresees the transmission of a multiple-bit LinkID and periodicity. Each LinkID is mapped with an accurate priority rating in the ePTA while the periodicity further informs the ePTA about the type of BT traffic.

Serial Link: in addition to LinkID and periodicity, ST-Ericsson ePTA extension allows non real-time messages to be transferred between BT and ePTA, using an I2C based serial-link. These messages are transmitted only when the RF_ACTIVE signal is de-asserted. The pin map for this serial link is shown in *Table 26*.

Table 26. Multiplexing of serial link over STATUS, FREA and TX_CONF signals

Regular name	Direction	Serial link name	Serial bus function
RF_ACTIVE	BT to WLAN	SERIAL_ACTIVE_N	Low means serial link is active
STATUS	BT to WLAN	SERIAL_CLK	Serial interface clock
FREQ	Bi-directional	SERIAL_DATA	Serial interface data
TX_CONFX	Bi-directional	SERIAL_REQ or ACK	Request to transfer or ACK

The combination of LINKID/periodicity accompanying each BT request and the messages from BT on the serial-link, means that a lot more information is available to ePTA to improve its arbitration policies. This is over and above the decent quality of coexistence that we achieve already using the standard PTA

Simpler and alternative PTA interfaces

In addition to the four-wire standard PTA interface and ST-Ericsson ePTA extensions to it, CX1001 also embodies other simpler/alternative interface to BT as illustrated in.

Table 27. Alternative PTA interfaces

Mode	PIN_1 (in)	PIN_2 (in)	PIN_3 (in-out)	PIN_4 (in-out)	Description
PTA_1W_WLM	-	-	-	BT_RF_NALL	1-wire interface. WLAN is master. PTA asserts BT_RF_NALL when WLAN is active
PTA_1W_BTM	WL_RF_NALL	-	-	-	1-wire interface. BT is master. WLAN suspends communication if BT asserts WL_RF_NALL
PTA_2W_PRI_TX	BT_PRI	-	-	WL_TX	2-wire. BT asserts BT_PRI when it wants to transmit priority traffic. WL_TX is asserted if WLAN is in TX
PTA_3W_RGA	BT_RF_ACTIVE	-	ABORT	TX_CONFX	3-wire. BT makes explicit request before communication. PTA may assert abort anytime while BT is in TX/RX and WLAN wins
PTA_3W_RGS	BT_RF_ACTIVE	BT_STATUS	-	TX_CONFX	3-wire standard PTA (excluding FREQ line)
PTA_4W_RGSF	BT_RF_ACTIVE	BT_STATUS	BT_FREQ	TX_CONFX	4-wire standard PTA
PTA_4W_RGSFLID	BT_RF_ACTIVE	BT_STATUS	BT_FREQ	TX_CONFX	4-wire ST extension to standard PTA. Serial link multiplexed when RF_ACTIVE de-asserted

2.7 RF inputs and outputs

2.7.1 Electrical characteristics

Table 28. Electrical characteristics of the RF inputs and outputs

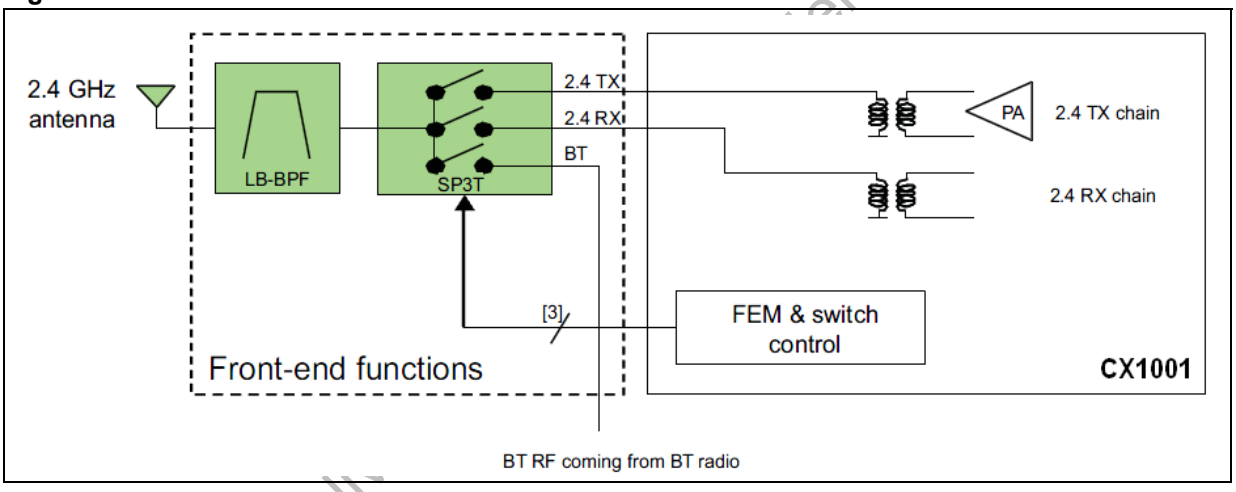
Ball name	Type	ZTyp, ohm(1)	Dedicated frequency range (GHz)
RF_IN_LB	Single-ended	50	2.4 - 2.4835
RF_OUT_LB	Single-ended	50	2.4 - 2.4835

1. This part of the circuit is biased. When unused portions of the circuit are powered down. Impedance may change.

2.7.2 Reference schematic

Figure 14 shows a simplified view of the components to be placed between the RF ports and the antenna. The assumption is made that a Bluetooth device shall share the 2.4 GHz antenna and BPF. For more details on the possible implementations, see the CX1001 Performance and architecture application note.

Figure 14. Schematic of the antenna interface



3 WLAN functional description

The WLAN subsystem implements the MAC and physical layer functionalities of the 802.11 specification and amendments. The radio is capable of operation in all of the available channels in the 2.4 frequency band.

The WLAN radio is based on a direct conversion architecture with two RF front-ends for operation in 2.4 band and a common analog and digital baseband.

The digital transceiver implements the OFDM (802.11n) and DSSS/CCK (802.11b/g) functions, supporting the following PHY features:

- OFDM:
  - Bandwidth: 20 MHz
  - Modulations: BPSK, QPSK, 16QAM and 64QAM
  - Code rates: ½, $^{2}/_{3}$, ¾, $^{5}/_{6}$
  - Preambles: legacy, greenfield and mixed mode preambles
  - Single convolutional encoder
  - Reception of 802.11n 2x1 STBC encoded signals for range enhancement
  - Reception of 802.11n beam formed and channel sounding packets (support for maximum of two transmitter preambles)
  - RIFS of 2 µs (802.11n only)
- DSSS/CCK:
  - Modulations: DBPSK, DQPSK, CCK
  - Preambles: long and short

3.1 Modem receiver

The low and high band signals are demodulated by separate RF front-ends. The radio signal from the balanced 2.4 RF input is amplified by an LNA. The passive receive switching mixers are driven by quadrature LO signals supplied by the on-device RF PLL. The amplified mixer output is fed to a common analog baseband circuit. The analog baseband receiver performs part of the channel filtering and further signal amplification, such that the signal is presented at the correct range of the A/D converter. High speed sigma delta A/D converters are employed for signal sampling. High over-sampling ratio and noise shaping techniques provide high dynamic range, thereby reducing the analog complexity. The rest of the channel filtering and gain amplification is performed in the digital domain. DC compensation is performed partly in the analog and partly in the digital domain. AGC Control, DC tracking and control, quadrature imbalance tracking and control are implemented digitally. The RC time constants for the analog filters are calibrated automatically.

OFDM and DSSS/CCK signals are coherently demodulated and decoded by the digital modem. The digital modem also implements the CCA 802.11k functions to collect the link statistics like RSSI, RPI, IPI and RSNI.

3.2 Modem transmitter

The digital modem implements the OFDM and DSSS/CCK modulation for all frame-formats specified for a single layer/transmitter. The OFDM and DSSS/CCK modulated I/Q signals use a common circuit for digital up-sampling, filtering, quadrature imbalance compensation, LO leakage correction and digital power scaling. High speed sigma delta D/A converters are employed for digital to analog conversion reducing the analog complexity. The filtered analog I/Q signals are then up-converted using a modulator. The modulator is driven by the signal from the LO buffer/dividers supplied by the VCO. The up-converted RF signals are further amplified by a digitally controlled amplifier and a 21 dBm power amplifier, eliminating the need for any external amplification between the transceiver and the antenna.

Transmit I/Q calibration is implemented partly in both the analog and digital domains. The transmitter implements automatic level control by averaging the reading of the integrated power detector at the PA output. Both bands share the integrated ADC used to samples the power detector output. The power detector for the low-band is integrated inside CX1001 optimizing the coupling with the integrated PA.

3.3 RF PLL

A single RF LC oscillator PLL provides the quadrature LO signals to the up and down converters. A fractional synthesizer design is employed to accommodate different reference frequencies. The loop filter is fully integrated inside the CX1001.

3.4 WLAN controller

The main components of the WLAN controller are the CPU subsystem, the MAC protocol accelerator subsystem, the encryption/decryption engines, the host interfaces and an enhanced PTA for WLAN/BT coexistence.

3.5 IEEE 802.11 standard compliance and support

3.5.1 General support

Support for operation in 802.11n, 802.11b and 802.11g networks, meaning support for basic mandatory MAC features and for the mandatory modes of:

- Clause 15, DSSS PHY (basic 802.11)
- Clause 18, HR/DSSS PHY (802.11b)
- Clause 19, ERP PHY (802.11g)
- Clause 21, HT PHY (802.11n), Compliant to WiFi Handset Profile

Support for operation as a wireless station (STA) in both infrastructure and ad-hoc networks; in particular, the module supports IBSS operation and also implements support for IBSS power save mode.

3.5.2 International regulatory support

Supports the IEEE 802.11d standard amendment for regulatory domain identification.

3.5.3 Radio resource management support

Supports the mandatory aspects introduced in the IEEE 802.11k amendment to the standard.

3.5.4 Security support

Support for basic WEP:

- Key lengths of 40, 104 bits for WEP encryption (IV generation and ICV verification) are supported
- Open and shared key authentication
- Cryptographically weak IVs are avoided

Supports the MAC mandatory aspects of RSNA security including TKIP and AES-CCMP and the following optional security features:

- RSNA for IBSS is supported

Supports protected management frames introduced in IEEE 802.11w amendment to the standard:

- CCMP for unicast management frames
- BIP for broadcast/multicast management frames

Supports fast BSS transition in a RSNA introduced in the IEEE 802.11r amendment to the standard.

3.5.5 Quality of service

Supports the EDCA medium access method, four access categories, and TSPEC signalling.

3.5.6 Power saving

Support for basic PSM.

Support for Unscheduled Automatic Power Save Delivery (U-APSD) as defined by WMM-PS.

3.5.7 Fast roaming

Supports fast BSS transition introduced in the IEEE 802.11r amendment to the standard.

3.5.8 802.11n

Supports MAC enhancements for higher throughput as defined in the IEEE 802.11n amendment to the standard.

In addition to the above, the reference driver and associated software implement aspects of RSNA, CCX, 802.11w, 802.11k, Tspec setup and 802.11r not contained in the MAC but necessary to complete the system for reference or demonstration purposes, for example the supplicant necessary for RSNA security.

3.5.9 WiFi alliance interoperability testing

General support

The device when built into a system has sufficient features and performance to be passed by WiFi as an ASD device (Application Specific Device).

International regulatory support

Support for 802.11d.

Security support

Support for WEP, WPA (RSNA using TKIP & MIC), WPA2 (RSNA using CCMP).

The device supports the features that the new formed security marketing task group will define in the next TGw MRD.

Quality of service

Support for WMM (EDCA from 802.11e), WMM-PS (U-APSD from 802.11e, with interface for Tspec negotiation by upper layers).

High throughput

The device supports the mandatory features defined in the TGn MRD for the HH (HandHeld) market segment.

WiFi protected setup

For easy configuration.

3.5.10 CCX™

Note: CCX is a trade mark of Cisco Inc.

General support

The device when built into a system has sufficient features and performance to be passed by Cisco's nominated testing house as a CCX capable device in the category of ASD devices.

Support for CCX version 5, with interoperability with AP's down to CCX version 1.

Interoperability

Compatible with all the applicable features defined by Cisco CCX version 5 specification. CCX standards specify certain features (such as EAP methods) which require support on the host platform OS in which the CX1001 is integrated. CX1001 software provides necessary interfaces in such instances to realize full CCXv5 support for the ASD

Security support

Support for encryption WEP, RSNA using TKIP & MIC, RSNA using AES-CCMP.

Support for authentication methods (Cisco LEAP, PEAP with EAP-GTC support, CCKM with EAP-FAST) depends on the host platform.

Quality of service

Support for WMM (EDCA from 802.11e), WMM-PS (U-APSD from 802.11e, with interface for Tspec negotiation by upper layers).

Interoperability with pre-standard EDCA, CCX certified equipment is maintained.

Network management

AP-assisted roaming.

Radio environment reporting.

AP-specified maximum transmit power (through support for TPC).

Other features of CCX are dependant on the host platform

Proxy ARP.

Cisco compatible version control.

Interoperability with APs that support multiple SSIDs.

3.6 Regional regulatory standards compliance

Below is a non-exhaustive list of regional regulatory standards which the CX1001 complies with. For some of those standards, it is assumed that the CX1001 is used together with the approved components part of the reference design (see CX1001 hardware user manual).

Table 29. Regional regulatory approvals

Region	Regulatory authority	Specification	Reference in FCC, ETSI/EN and TELEC standards
US	FCC	FCC Part 15, Subpart	Section 15.35 Measurement methods
			Section 15.205: Restricted bands of operation
			Section 15.209: Radiated emission limits, general requirements (EIRP)
			Section 15.247: Operation within the bands 902 - 928 MHz, 2400 - 2483.5 MHz, and 5725 - 5850 MHz
			Section 15.407
EU & Canada	ETSI / EN	EN300 328 (V1.7.1): 2.4 GHz ISM band operation	Section 4.3.1 to 4.3.3:Maximum transmit power
			Maximum EIRP spectral density, Frequency range
			Section 4.3.6 to 4.3.7: Transmit and receive spurious emissions
Japan	TELEC (former MKK)	ARIB STD T66 (b/g)	Section 3.1, 3.2, 3.3: Technical requirements on radio equipment, general, TX and RX
		RCR STD T33 (b)	

3.7 Low power modes

Table 30. WLAN low power modes

Low power mode	Description
Standby (complete power down)	W_RESETN is active and WLAN subsystem is effectively powered down
Sleep	The WLAN subsystem – Is largely powered down – Operates from the low power clock (sleep clock) (32 kHz) – Preserves the value of internal state variables and the CPU firmware – Does not accept commands from host – Limited access to clock stabilization time, interrupt source to host, WLAN wakeup registers – Reference clock is not active in any part of the design
PSM	The WLAN subsystem – Is partly powered down depending on the WLAN activity – Accepts commands from the host – Reference clock is active depending on active mode – Dynamically switches between sleep and active mode when needed
Active	The WLAN subsystem – The CPU subsystem and host interface are active – The system is transmitting or receiving
Rx-Idle	The WLAN subsystem – Is listening to the channel. All TX circuits are disabled (clocks are switched off). Only minimum necessary RX circuits are enabled

3.8 Host interface

The WLAN host interface uses either the SPI interface defined in *Section 2.6.2* or the SDIO interface defined in *Section 2.6.3*.

3.9 FEM control interface

See *Section 2.6.4*.

3.10 Bluetooth - WLAN coexistence and 802.15.2 compliance

Bluetooth and WLAN 802.11b and 802.11g technologies occupy the same 2.4 GHz ISM band. The CX1001 implements a set of mechanisms to avoid interference in a collocated scenario:

- When configured according to “standard PTA”, CX1001 implements the recommendation of IEEE 802.15.2.
- When configured according to “enhanced PTA”, CX1001 implements proprietary features that further optimize coexistence. Advanced information on the Bluetooth traffic is communicated via a serial protocol on the 4 wires defined for standard PTA.
- CX1001 also implements simpler coexistence interfaces.

See *Section 2.6.4* for more details on how the interface operates.

3.11 WLAN - WiMAX coexistence

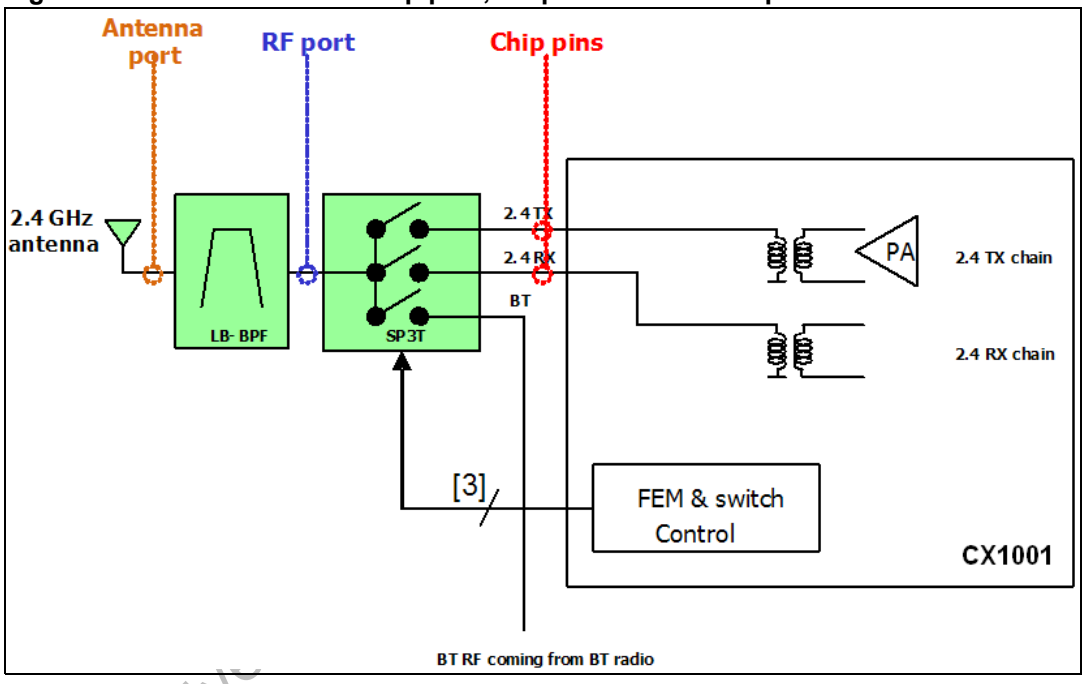
Assertion of the WiMAX ‘disable pin’ notifies WLAN that WiMAX is active.

4 WLAN transceiver performances

4.1 RF receiver performance

This section specifies the performances of the RF receiver referred to the input pins of the CX1001 (called chip pins) and gives indications of the performances at the antenna port or the RF port depending on which is the most relevant. This indication is obtained considering an attenuation of 3.5 dB between the antenna port, and chip pins and 0.7 dB between the RF port and chip pins. This corresponds to what is measured on the reference design described in the CX1001 hardware user manual including a switch, a band-pass filter, and track losses.

Figure 15. Definition of the chip pins, RF port and antenna port



4.1.1 Maximum input signal level

Table 31. Maximum input signal levels at CX1001 pins

Mode	Parameter	Conditions/comments	Specification at CX1001 pin			
			Min	Typ	Max	Unit
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 8% for CCK/DSSS			-20	dBm
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 10% for OFDM			-20	dBm

Table 32. Maximum input signal levels at RF port

Mode	Parameter	Conditions/comments	Indication at RF port(1)			
			Min	Typ	Max	Unit
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 8% for CCK/DSSS			-19	dBm
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 10% for OFDM			-19	dBm

1. Under the assumption that CX1001 is used see comments in combination with the components specified in CX1001 hardware user manual section 4.1

4.1.2 Minimum input signal level (sensitivity)

All power levels rounded to 0.5 dB granularity.

Table 33. 2.4 GHz sensitivity (minimum input level) at CX1001 pins

Band	Standard	Rate	Modulation	Coding	Conditions	Specification at CX1001 pin			Unit
		Mbps				Min	Typ	Max(1)	
2.4 GHz	DSSS/CCK	1	DSSS	--	@ FER < 8% 1024 bytes per frame, full operating range		-98.5	-96.5	dBm
		2	DSSS	--			-96	-94	dBm
		5.5	CCK	--			-94	-92	dBm
		11	CCK	--			-89	-87	dBm
	11g/n (20 MHz, OFDM)	6	BPSK	1/2	@ PER < 10% 1000 bytes per frame, full operating range		-94.5	-92.5	dBm
		9	BPSK	3/4			-92.5	-90.5	dBm
		12	QPSK	1/2			-91.5	-89.5	dBm
		18	QPSK	3/4			-89	-87	dBm
		24	16QAM	1/2			-86	-84	dBm
		36	16QAM	3/4			-83	-81	dBm
		48	64QAM	2/3			-78.5	-76.5	dBm
		54	64QAM	3/4			-77	-74.5	dBm
	11n (OFDM, 20 MHz)(2)	6.5	BPSK	1/2	@ PER < 10% 4096 bytes per frame, full operating conditions		-92.5	-90.5	dBm
		13	QPSK	1/2			-89.5	-87.5	dBm
		19.5	QPSK	3/4			-87	-85	dBm
		26	16QAM	1/2			-84.5	-82.5	dBm
		39	16QAM	3/4	@ PER < 10% 4096 bytes per frame, full operating range		-81	-79	dBm
		52	64QAM	2/3			-77	-75	dBm
		58.5	64QAM	3/4			-75.5	-73	dBm
		65	64QAM	5/6			-73.5	-71	dBm

1. There is a degradation of the sensitivity on channel 1 by 1.5 dB
2. Assuming the smoothing bit in HT-SIG of the received frames is set to 1.

Table 34. 2.4 GHz sensitivity (minimum input level) at RF port

Band	Standard	Rate	Modulation	Coding	Conditions	Indication at RF port (1)			Unit
		Mbps				Min	Typ	Max(2)	
2.4 GHz	DSSS/CCK	1	DSSS	--	@ FER < 8% 1024 bytes per frame, full operating range		-98	-95.5	dBm
		2	DSSS	--			-95	-93	dBm
		5.5	CCK	--			-93	-91	dBm
		11	CCK	--			-88	-86	dBm
	11g/n (20 MHz, OFDM)	6	BPSK	1/2	@ PER < 10% 1000 bytes per frame, full operating range		-93.5	-91.5	dBm
		9	BPSK	3/4			-91.5	-89.5	dBm
		12	QPSK	1/2			-90.5	-88.5	dBm
		18	QPSK	3/4			-88	-86	dBm
		24	16QAM	1/2			-85.5	-83	dBm
		36	16QAM	3/4			-82	-80	dBm
		48	64QAM	2/3			-78	-75.5	dBm
		54	64QAM	3/4			-76.5	-74	dBm
	11n (OFDM, 20 MHz)(3)	6.5	BPSK	1/2	@ PER < 10% 4096 bytes per frame, full operating range		-92	-89.5	dBm
		13	QPSK	1/2			-89	-86.5	dBm
		19.5	QPSK	3/4			-86.5	-84	dBm
		26	16QAM	1/2			-84	-81.5	dBm
		39	16QAM	3/4			-80.5	-78	dBm
		52	64QAM	2/3			-76.5	-74	dBm
		58.5	64QAM	3/4			-74.5	-72	dBm
		65	64QAM	5/6			-73	-70	dBm

1. Under the assumption that CX1001 is used in combination with the components specified in the CX1001 hardware user manual
2. There is a degradation of the sensitivity on channel 1 by 1.5dB
3. Assuming the smoothing bit in HT-SIG of the received frames is set to 1.

The specified throughput and sensitivity is achieved under the following multi-path delay spread conditions:

Table 35. Multi-path delay spread requirements for DSSS/CCK

Data rate [Mbps]	Spread [ns]
1	> 350
2	> 300
5.5	> 200
11	> 50

Table 36. Multi-path delay spread requirements for OFDM

Data rate [Mbps]	Spread [ns]
6	> 400
9	> 250
12	> 250
18	> 220
24	> 160
36	> 100
48	> 90
54	> 70
65	> 50

4.1.3 Adjacent channel rejection and blockers

Table 37. 802.11g adjacent channel rejection at antenna port

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port(1)			
				Min	Typ	Max	Unit
OFDM (802.11g)	BPSK ½	-82	Tests as specified in IEEE 802.11, Clause 17.3.10.2	16	21		dBc
	BPSK ¾	-81		15	20		dBc
	QPSK ½	-79		13	18		dBc
	QPSK ¾	-77		11	16		dBc
	16QAM ½	-74		8	13		dBc
	16QAM ¾	-70		4	9		dBc
	64QAM ⅔	-66		0	5		dBc
	64QAM ¾	-65		-1	4		dBc

1. Under the assumption explained in *Section 4.1*.

Table 38. 802.11n adjacent channel rejection at antenna port

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port(1)			
				Min	Typ	Max	Unit
OFDM (802.11n)	BPSK ½	-82	Tests as specified in IEEE P802.11n Draft	16	21		dBc
	QPSK ½	-79		13	18		dBc
	QPSK ¾	-77		11	16		dBc
	16QAM ½	-74		8	13		dBc
	16QAM ¾	-70		4	9		dBc
	64QAM $^{2}/_{3}$	-66		0	5		dBc
	64QAM ¾	-65		-1	4		dBc
	64QAM $^{5}/_{6}$	-64		-2	3		dBc

1. Under the assumption explained in *Section 4.1*.

Table 39. DSSS/CCK (802.11b/g) adjacent channel rejection

Mode	Data rate	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port(1)			
				Min	Typ	Max	Unit
DSSS/CCK	11 Mbps	-76	At 25 MHz offset, 11 Mbps	35	38	--	dBc

1. Under the assumption explained in *Section 4.1*.

4.1.4 Non-adjacent channel rejection

Table 40. 802.11g non-adjacent channel rejection

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port(1)			
				Min	Typ	Max	Unit
OFDM (802.11g)	BPSK ½	-82	Tests as specified in IEEE 802.11, Clause 17.3.10.3	32	39		dBc
	BPSK ¾	-81		31	38		dBc
	QPSK ½	-79		29	36		dBc
	QPSK ¾	-77		27	34		dBc
	16QAM ½	-74		24	31		dBc
	16QAM ¾	-70		20	27		dBc
	64QAM $^{2}/_{3}$	-66		16	23		dBc
	64QAM ¾	-65		15	22		dBc

1. Under the assumption explained in *Section 4.1*.l

Table 41. 802.11n non-adjacent channel rejection

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port(1)			
				Min	Typ	Max	Unit
OFDM (802.11n)	BPSK ½	-82	Tests as specified in IEEE P802.11n Draft	32	39		dBc
	QPSK ½	-79		29	36		dBc
	QPSK ¾	-77		27	34		dBc
	16QAM ½	-74		24	31		dBc
	16QAM ¾	-70		20	27		dBc
	64QAM $^{2}/_{3}$	-66		16	23		dBc
	64QAM ¾	-65		15	22		dBc
	64QAM $^{5}/_{6}$	-64		14	21		dBc

1. Under the assumption explained in *Section 4.1*.

4.1.5 Cellular blocker tolerance

Immunity against a blocker signal is given in *Table 42* under the condition that the WLAN receiver's sensitivity is not degraded by more than 1 dB. Power levels specified are RMS figures. For WCDMA a large crest factor of up to 12 dB applies. When the blocker band overlaps with WLAN band, the coexistence is assumed to be solved by packet traffic arbitration or PTA. See *Section 2.6.5* for more details.

RF coexistence is dependant on the reference design and its band pass filter characteristics. The figures at the antenna port are given as an indication and are based on. The reference design implementation given in the CX1001 hardware user manual under the worst case conditions (lowest attenuation of the BPF).

Table 42. Cellular blocker tolerance at the CX1001 pins and antenna port

Mode	Band	Frequency [MHz]		Specification at CX1001 pin		Indication at ANT port(1)		Unit
		Min	Max	Min	Typ	Min	Typ	
2.4 GHz	3GPP band 12 FDD uplink	698	716	-28		12		dBm
2.4 GHz	3GPP band 13 FDD uplink	776	798	-28		12		dBm
2.4 GHz	GSM850 FDD uplink	824	849	-19		21		dBm
2.4 GHz	3GPP band 5 FDD uplink	824	849	-28		12		dBm
2.4 GHz	3GPP band 6 FDD uplink	824	849	-28		12		dBm
2.4 GHz	EGSM900 FDD uplink	880	915	-19		21		dBm
2.4 GHz	3GPP band 8 FDD uplink	880	915	-28		12		dBm
2.4 GHz	3GPP band 11 FDD Uplink	1427	1452	-28		12		dBm
2.4 GHz	3GPP band 4 FDD uplink	1710	1755	-28		12		dBm
2.4 GHz	3GPP band 10 FDD uplink	1710	1770	-28		12		dBm
2.4 GHz	DCS1800 FDD uplink	1710	1785	-22		18		dBm

Table 42. Cellular blocker tolerance at the CX1001 pins and antenna port (continued)

Mode	Band	Frequency [MHz]		Specification at CX1001 pin		Indication at ANT port(1)		Unit
		Min	Max	Min	Typ	Min	Typ	
2.4 GHz	3GPP band 3 FDD uplink	1710	1785	-28		12		dBm
2.4 GHz	3GPP band 9 FDD uplink	1750	1785	-28		12		dBm
2.4 GHz	PCS1900 FDD uplink	1850	1910	-22		18		dBm
2.4 GHz	3GPP band 2 FDD uplink	1850	1910	-28		12		dBm
2.4 GHz	3GPP band 35 TDD	1850	1910	-28		12		dBm
2.4 GHz	3GPP band 39 TDD	1880	1920	-28	-	12	-	dBm
2.4 GHz	3GPP band 33 TDD	1900	1920	-28	-	12	-	dBm
2.4 GHz	3GPP band 37 TDD	1910	1930	-28	-	12	-	dBm
2.4 GHz	3GPP band 1 FDD uplink	1920	1980	-28	-	12	-	dBm
2.4 GHz	3GPP band 36 TDD	1930	1990	-28	-	12	-	dBm
2.4 GHz	3GPP band 34 TDD	2010	2025	-28	-	12	-	dBm
2.4 GHz	3GPP band 40 TDD	2300	2400	-43	-	-40.4	-	dBm
2.4 GHz	WiMAX BC2	2305	2360	-43	-	-40.4	-	dBm
2.4 GHz	BT	2402	2480	NA	-	NA	-	dBm
2.4 GHz	WiMAX BC3	2496	2690	-43	-	-40.4	-	dBm
2.4 GHz	3GPP band 7 FDD uplink	2500	2570	-43	-	-40.4	-	dBm
2.4 GHz	3GPP band 38 TDD	2570	2620	-43	-	-40.4	-	dBm
2.4 GHz	WiMAX BC5	3300	3900	-31	-	-15.4	-	dBm
2.4 GHz	UWB G1	3168	4752	-51	-	-21	-	dBm
2.4 GHz	UWB G3	6336	7920	-51	-	-21	-	dBm
2.4 GHz	UWB G6	7392	8976	-51	-	-21	-	dBm

1. Under the assumption explained in *Section 4.1*.

4.1.6 RSSI and RCPI

Table 43. RSSI and RCPI accuracy at CX1001 pins

Parameter	Conditions	Typ	Max	Unit
RSSI accuracy at CX1001 pins	VBAT ≥ 3.6 V, 25°C, excluding insertion loss variations between the ANT and CX1001 pins	± 2	± 3.5	dB
RCPI accuracy at CX1001 pins		± 2	± 3.5	dB

4.2 RF transmitter performance

This section specifies the performances of the RF transmitter referred to the input pins of the CX1001 (called chip pins) and gives indications of the performances at the antenna port or the RF port depending on which is the most relevant. This indication is obtained considering an attenuation of 3.5 dB between the antenna port and the chip pins and 0.7dB between the RF port and the chip pins. This corresponds to what is measured on the reference design described in the CX1001 hardware user manual including a switch, a band-pass filter and track losses. The chip pins, RF port, and antenna port are defined in *Figure 15*.

4.2.1 Output power

The output power is specified as average conducted power at the antenna connector. The output power specifications are met over frequency, temperature and a battery voltage of 3.6 V upwards according to the full spec operating range (see *Section 2.2.2*). In the full specification with output power backed-off (2.7 V < Vbat < 3.6 V) and the functional with reduced performance (2.3 V < Vbat < 2.7 V) operating ranges. The output power needs to be backed-off to sustain the transmit EVM, spectral mask, harmonic level and spurious emissions specifications.

Table 44. Coding rate dependent output power vs. EVM at CX1001 pins for 802.11b/g

Modulation	Coding rate	Conditions	Specification at CX1001 pins				EVM		EVM	
			Min	Typ	Max	Unit	Max	Unit	Max	Unit
DSSS/CCK	--	All conditions typical: Vbat ≥ 3.6 V, 25 C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general	20	21	-	dBm	-14.5	dB	18.84	%
BPSK	1/2		20	21	-	dBm	-14.5	dB	18.84	%
BPSK	3/4		20	21	-	dBm	-14.5	dB	18.84	%
QPSK	1/2		20	21	-	dBm	-14.5	dB	18.84	%
QPSK	3/4		20	21	-	dBm	-14.5	dB	18.84	%
16QAM	1/2		19.5	20.5	-	dBm	-17.5	dB	13.34	%
16QAM	3/4		18.5	19.5	-	dBm	-20.5	dB	9.44	%
64QAM	2/3		17.5	18.5	-	dBm	-23.5	dB	6.68	%
64QAM	3/4		16.5	17.5	-	dBm	-25.5	dB	5.31	%

Table 45. Coding rate dependent output power vs. EVM at CX1001 pins for 802.11n

MCS	Conditions or comments	Specification at CX1001 pins				EVM		EVM	
		Min	Typ	Max	Unit	Max	Unit	Max	Unit
MCS-0	All conditions typical: Vbat ≥ 3.6 V, 25 °C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in genera	20	21	-	dBm	-14.5	dB	18.84	%
MCS-1		20	21	-	dBm	-14.5	dB	18.84	%
MCS-2		20	21	-	dBm	-14.5	dB	18.84	%
MCS-3		19.5	20.5	-	dBm	-17.5	dB	13.34	%
MCS-4		18.5	19.5	-	dBm	-20.5	dB	9.94	%
MCS-5		17.5	18.5	-	dBm	-23.5	dB	6.68	%
MCS-6		16.5	17.5	-	dBm	-25.5	dB	5.31	%
MCS-7		15.5	16.5	-	dBm	-28.5	dB	3.76	%

Table 46. Coding rate dependent output power vs. EVM at RF port for 802.11b/g

Modulation	Coding rate	Conditions	Indication at RF port(1)				EVM		EVM	
			Min	Typ	Max	Unit	Max	Unit	Max	Unit
BPSK	1/2	All conditions typical: Vbat ≥ 3.6 V, 25 °C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general	19	20		dBm	-14.0	dB	19.95	%
BPSK	3/4		19	20		dBm	-14.0	dB	19.95	%
QPSK	1/2		19	20		dBm	-14.0	dB	19.95	%
QPSK	3/4		19	20		dBm	-14.0	dB	19.95	%
16QAM	1/2		18.5	19.5		dBm	-17.0	dB	14.13	%
16QAM	3/4		17.5	18.5		dBm	-20.0	dB	10.00	%
64QAM	2/3		16.5	17.5		dBm	-23.0	dB	7.08	%
64QAM	3/4		15.5	16.5		dBm	-25.0	dB	5.62	%

1. Under the assumption explained in *Section 4.2*.

Table 47. Coding rate dependent output power vs. EVM at RF port for 802.11n

MCS	Conditions or comments	Indication at RF port(1)				EVM		EVM	
		Min	Typ	Max	Unit	Max	Unit	Max	Unit
MCS-0	All conditions typical: Vbat ≥ 3.6 V, 25 °C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general	19	20	-	dBm	-14	dB	19.95	%
MCS-1		19	20	-	dBm	-14	dB	19.95	%
MCS-2		19	20	-	dBm	-14	dB	19.95	%
MCS-3		18.5	19.5	-	dBm	-17	dB	14.13	%
MCS-4		17.5	18.5	-	dBm	-20	dB	10.00	%
MCS-5		16.5	17.5	-	dBm	-23	dB	7.08	%
MCS-6		15.5	16.5	-	dBm	-25	dB	5.62	%
MCS-7		14.5	15.5	-	dBm	-28	dB	3.98	%

1. Under the assumption explained in *Section 4.2*

Power back-off

- When 2.7V < VBAT < 3.6V, the output power shall be backed off by 0.8 dB per 300 mV drop of Vbat below 3.6 V to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general.
- When 2.3V < VBAT < 2.7V, an additional back-off of the output power is needed to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general.
- When the load is not 50 Ω, the output power is backed off to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general. The amount of back-off needed is given in *Table 48* as a function of VSWR.

Table 48. Power back-off as a function of the VSWR at the CX1001 pins

Power back-off		VSWR			
Modulation	**Coding rate**	**1.3:1**	**1.5:1**	**2:1**	**3:1**
DSSS / CCK	-			2 dB	3 dB
BPSK	1/2	0.3 dB	0.5 dB	1 dB	2 dB
64QAM	3/4	0.4 dB	0.7 dB	1.5 dB	4 dB

- The device is able to withstand a VSWR of up to 12:1 without any damage.
- When the temperature increases from +25°C to +85°C, the output power shall be backed off by 0.25 dB per 10°C increase to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general.

Power control

Table 49. Output power control

Mode	Parameter	Note	Min	Typ	Max	UNit
2.4 GHz	Power control range	At antenna	15	-	-	dB
	Power resolution	At maximum power	-	0.25	-	dB
	Power accuracy	At maximum power (closed loop)	-1	0	+1	dB

The typical value of Pout can be adjusted in software within the limits defined by *Table 44* to *Table 47* and *Table 49*. See the ETF Software Delivery Note for details.

4.2.2 Spectral mask

Table 50. Transmit spectral mask at CX1001 pins and antenna port

Mode	Parameter	Conditions/ Comments	Specification at CX1001 pins			
			Min	**Typ**	**Max**	**Unit**
DSSS/CCK Tx (11b)	Spectral mask	± 11 ~ 22 MHz	-	-	-30	dBr
	Spectral mask	> ± 22 MHz	-	-	-50	dBr

Table 50. Transmit spectral mask at CX1001 pins and antenna port

Mode	Parameter	Conditions/ Comments	Specification at CX1001 pins			
			Min	Typ	Max	Unit
OFDM Tx (11g/n)	Spectral mask	± 11 MHz	-	-	-20	dBr
	Spectral mask	± 20 MHz	-	-	-28	dBr
	Spectral mask	± 30 MHz	-	-	-45	dBr

4.2.3 Harmonic levels

Table 51. Harmonic levels

Band	Harmonic	Freq [MHz]		Emissions		Unit
		Min freq	Max freq	Specification at CX1001 pins	Indication at antenna port(1)	
				Max	Max	
2.4 GHz	2nd	4824	4968	-9	-44	dBm/MHz
	3rd	7236	7452	-17	-47	dBm/MHz
	4th	9648	9936	-24	-44	dBm/MHz
	5th	12060	12420	-29	-47	dBm/MHz

1. Under the assumption explained in *Section 4.2*.

4.2.4 Spurious emissions

Table 52. TX spurious emissions at CX1001 pins

Band	Frequency (MHz)		RBW (MHz)	Specification at CX1001 pins	Unit
	Min	Max		Max	
VHF1	0	67	10^{-1}	-60	dBm
FM band 2	67	108	2.10^{-1}	-71	dBm
VHF2	108	170	10^{-1}	-60	dBm
DAB band III	170	230	1.5	-65	dBm
DVB-H UHF	470	862	8	-58	dBm
3GPP band 12 FDD downlink	728	746	1	-63	dBm
3GPP band 13 FDD downlink	747	762	1	-63	dBm
UHF1	798	824	10^{-1}	-60	dBm
GSM850 FDD downlink	869	894	2.10^{-1}	-70	dBm
3GPP band 5 FDD downlink	869	894	2.10^{-1}	-70	dBm
3GPP band 6 FDD downlink	875	885	2.10^{-1}	-70	dBm
UHF2	915	925	10^{-1}	-60	dBm

Table 52. TX spurious emissions at CX1001 pins (continued)

Band	Frequency (MHz)		RBW (MHz)	Specification at CX1001 pins	Unit
	Min	Max		Max	
EGSM900 FDD downlink	925	960	2.10^{-1}	-70	dBm
3GPP band 8 FDD downlink	925	960	2.10^{-1}	-70	dBm
UHF3	960	1427	1	-50	dBm
DAB L band	1452	1492	1.5	-61	dBm
3GPP band 11 FDD downlink	1475	1500	2.10^{-1}	-70	dBm
GPS	1570	1580	5.10^{-2}	-90	dBm
GLONASS	1592	1610	5.10^{-2}	-85	dBm
UHF4	1610	1670	1	-50	dBm
DVB-H USA band	1670	1675	8	-54	dBm
DCS1800 FDD downlink	1805	1880	2.10^{-1}	-70	dBm
3GPP band 3 FDD downlink	1805	1880	2.10^{-1}	-70	dBm
3GPP band 9 FDD downlink	1845	1880	2.10^{-1}	-70	dBm
3GPP band 35 TDD	1850	1910	1.25	-62	dBm
3GPP band 39 TDD	1880	1920	1.25	-52	dBm
3GPP band 33 TDD	1900	1920	4	-52	dBm
3GPP band 37 TDD	1910	1930	1.25	-52	dBm
UHF5	1990	2010	1	-50	dBm
PCS1900 FDD downlink	1930	1990	2.10^{-1}	-66	dBm
3GPP band 2 FDD downlink	1930	1990	2.10^{-1}	-66	dBm
3GPP band 36 TDD	1930	1990	1.25	-58	dBm
3GPP band 34 TDD	2010	2025	1.25	-62	dBm
UHF6	2025	2110	1	-50	dBm
3GPP band 4 FDD downlink	2110	2155	4	-59	dBm
3GPP band 1 FDD downlink	2110	2170	4	-59	dBm
3GPP band 10 FDD downlink	2110	2170	4	-59	dBm
UHF7	2170	2305	1	-50	dBm
3GPP band 40 TDD	2300	2400	1.25	-55	dBm
WiMAX BC2	2305	2360	4	-50	dBm
BT	2402	2480	-	-	dBm
WiMAX BC3	2496	2690	4	-50	dBm
3GPP band 38 TDD	2570	2620	4	-55	dBm
3GPP band 7 FDD downlink	2620	2690	4	-55	dBm
WiMAX BC5	3300	3900	4	-67	dBm

Table 52. TX spurious emissions at CX1001 pins (continued)

Band	Frequency (MHz)		RBW (MHz)	Specification at CX1001 pins	Unit
	Min	Max		Max	
UWB G1	3168	4752	10^{-6}	-118	dBm
UWB G3	6336	7920	10^{-6}	-133	dBm
UWB G6	7392	8976	10^{-6}	-133	dBm
SHF	2480	12700	1	-50	dBm

Table 53. TX spurious emissions at antenna port (indication)

Band	Frequency (MHz)		RBW (MHz)	Indication at antenna port(1)	Unit
	Min	Max		2.4 GHz	
				Max	
VHF1	0	67	10^{-1}	-101	dBm
FM band 2	67	108	2.10^{-1}	-112	dBm
VHF2	108	170	10^{-1}	-101	dBm
DAB band III	170	230	1.5	-105	dBm
DVB-H UHF	470	862	8	-98	dBm
3GPP band 12 FDD downlink	728	746	1	-104	dBm
3GPP band 13 FDD downlink	747	762	1	-104	dBm
UHF1	798	824	10^{-1}	-101	dBm
GSM850 FDD downlink	869	894	2.10^{-1}	-111	dBm
3GPP band 5 FDD downlink	869	894	2.10^{-1}	-111	dBm
3GPP band 6 FDD downlink	875	885	2.10^{-1}	-111	dBm
UHF2	915	925	10^{-1}	-101	dBm
EGSM900 FDD downlink	925	960	2.10^{-1}	-111	dBm
3GPP band 8 FDD downlink	925	960	2.10^{-1}	-111	dBm
UHF3	960	1427	1	-91	dBm
DAB L band	1452	1492	1.5	-102	dBm
3GPP band 11 FDD downlink	1475	1500	2.10^{-1}	-111	dBm
GPS	1570	1580	5.10^{-2}	-130	dBm
GLONASS	1592	1610	5.10^{-2}	-123	dBm
UHF4	1610	1670	1	-91	dBm
DVB-H USA band	1670	1675	8	-95	dBm
DCS1800 FDD downlink	1805	1880	2.10^{-1}	-111	dBm
3GPP band 3 FDD downlink	1805	1880	2.10^{-1}	-111	dBm

Table 53. TX spurious emissions at antenna port (indication) (continued)

Band	Frequency (MHz)		RBW (MHz)	Indication at antenna port(1)	Unit
	Min	Max		2.4 GHz	
				Max	
3GPP band 9 FDD downlink	1845	1880	2.10^{-1}	-111	dBm
3GPP band 35 TDD	1850	1910	1.25	-103	dBm
3GPP band 39 TDD	1880	1920	1.25	-93	dBm
3GPP band 33 TDD	1900	1920	4	-93	dBm
3GPP band 37 TDD	1910	1930	1.25	-93	dBm
UHF5	1990	2010	1	-91	dBm
PCS1900 FDD downlink	1930	1990	2.10^{-1}	-107	dBm
3GPP band 2 FDD downlink	1930	1990	2.10^{-1}	-107	dBm
3GPP band 36 TDD	1930	1990	1.25	-99	dBm
3GPP band 34 TDD	2010	2025	1.25	-103	dBm
UHF6	2025	2110	1	-86	dBm
3GPP band 4 FDD downlink	2110	2155	4	-90	dBm
3GPP band 1 FDD downlink	2110	2170	4	-90	dBm
3GPP band 10 FDD downlink	2110	2170	4	-90	dBm
UHF7	2170	2305	1	-71	dBm
3GPP band 40 TDD	2300	2400	1.25	-58	dBm
WiMAX BC2	2305	2360	4	-53	dBm
BT	2402	2480	-	-	dBm
WiMAX BC3	2496	2690	4	-53	dBm
3GPP band 38 TDD	2570	2620	4	-58	dBm
3GPP band 7 FDD downlink	2620	2690	4	-58	dBm
WiMAX BC5	3300	3900	4	-82	dBm
UWB G1	3168	4752	10^{-6}	-149	dBm
UWB G3	6336	7920	10^{-6}	-163	dBm
UWB G6	7392	8976	10^{-6}	-163	dBm
SHF	2480	12700	1	-53	dBm

1. Under the assumption explained in *Section 4.2*.

5 Package mechanical data

The device CX1001 is in lead-free/RoHS-compliant 73-pin WLCSP package. *Figure 16* shows the package drawing and dimensions.

Figure 16. WLCSP with depopulated pitch and 0.25 mm ball - bottom view

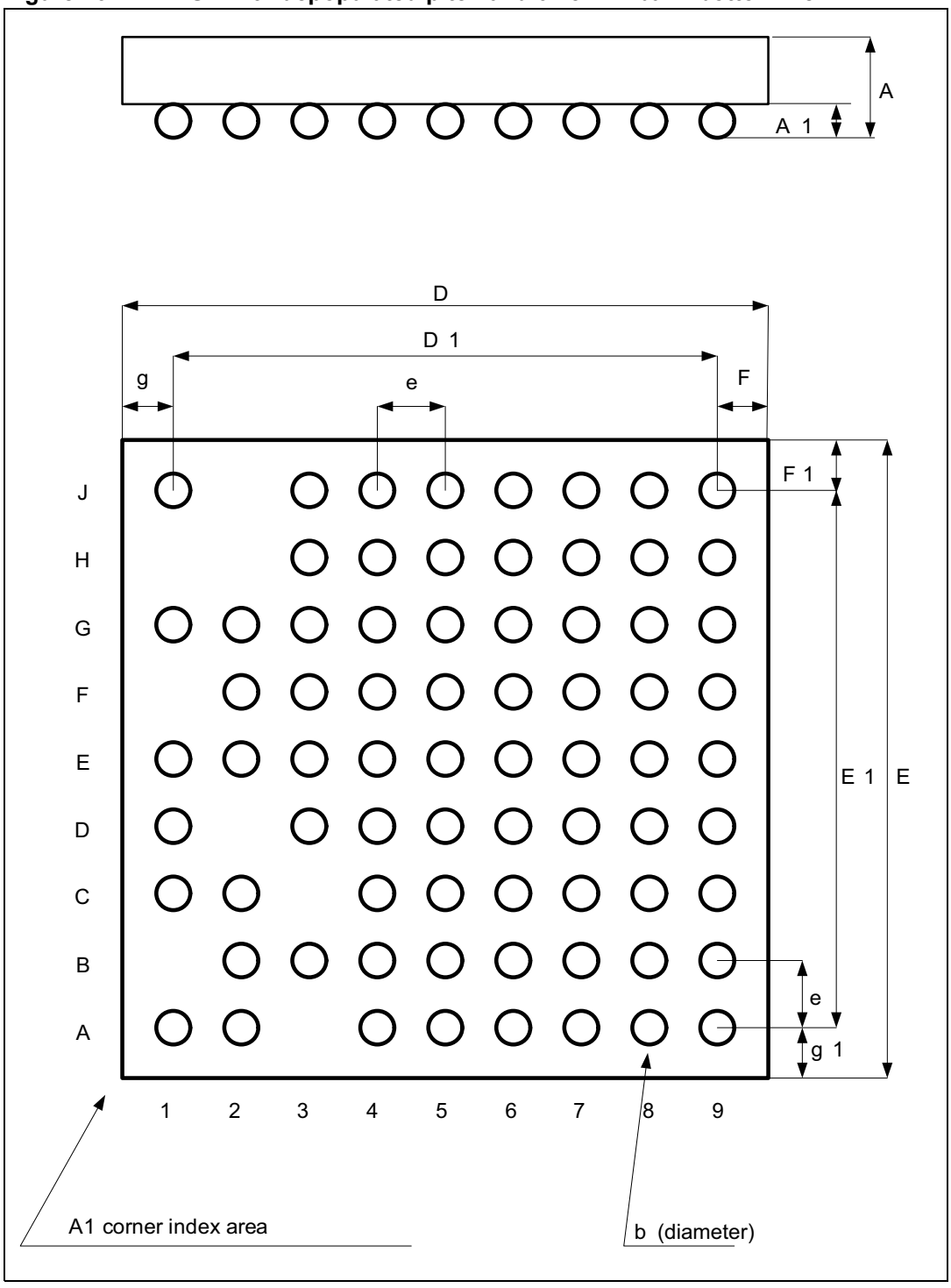


Table 54. Package dimensions

Databook (mm)				
Reference	**Min**	**Typ**	**Max**	**Notes**
A	0.490	0.545	0.60	Height
A1	0.17	0.20	0.23	
b	0.23	0.26	0.29	(1)
D	3.86	3.90	3.94	
D1	-	3.20	-	
E	3.80	3.84	3.88	
E1	-	3.20	-	
e	-	0.40	-	
F	-	0.40	-	(2)
F1	-	0.32	-	(2)
g	-	0.30	-	(2)
g1	-	0.32	-	(2)

1. The typical ball diameter before mounting is 0.25 mm
2. The matrix ball array is not centered

Table 55. Package marking

Item	Description	Format	Value
A	Component identification		1100-3
B	Diffusion lot		-
C	CAP assembly lot	assy plant # (AP), Y, WW	
D	tracebility information	wafer ID	
E	tracebility information	row-col	row-col
F	tracebility information		VQ TWN

Table 56. Ordering information

Order code	Description	Package(1)
CX100101UKTM	802.11bgn WLAN	Package CSP without BSC

1. Back-Side Coating: It is a tape of 40 micron thickness, used for protecting and reinforcing the chip surface.

6 References

[1] EEE 802.15.2, IEEE recommended practice for telecommunications and Information exchange between systems - Local and metropolitan area networks specific requirements - Part 15.2: coexistence of wireless personal area networks with other wireless devices operating in unlicensed frequency band, august 2003, IEEE

[2] The I2C-bus specification, version 2.1, january 2000, philips semiconductors

[3] SD Specification, part E1, SDIO specification, version 1.10, august 2004, SD association

[4] IEEE802.11-2007
Wireless LAN medium access control (MAC) and physical layer (PHY) specifications
Includes amendments 11b, 11d, 11e, 11g, 11h, 11i, 11j

[5] IEEE P802.11k-2008
Amendment 1: radio resource management

[6] IEEE P802.11r-2008
Amendment 2: Fast BSS transition

[7] EEE P802.11n/D6.0
Amendment: Enhancements for higher throughput

[8] IEEE P802.11w/D6.0
Amendment: protected management frames

[9] FCC regulations, PART 15 - RADIO FREQUENCY DEVICES, Subpart C - Intentional radiators, version from 7-10-2008.

[10] EN300 328: electromagnetic compatibility and radio spectrum matters (ERM); wide band transmission systems; data transmission equipment operating in the 2,4 GHz ISM band and using wide band ondulation techniques; harmonized EN covering essential requirements under article 3.2 of the R&TTE directive V1.7.1 (2006-05)

[11] EN 301 893: broadband radio access networks (BRAN); 5 GHz high performance RLAN; harmonized EN covering the essential requirements of article 3.2 of the R&TTE directive; V1.5.1 (2008-08)

[12] ARIB STD T66

[13] ARIB STD T71

7 Glossary

Table 57. Glossary

Acronym	Definition
A/D	Analog to Digital
AC	Alternating Current
AES	Advance Encryption System
AF	Alternative frequency
AGC	Automatic Gain Control
AHB	Advanced High-performance Bus
AMBA	Advanced Micro-controller Bus Architecture
AMR	Absolute Maximum Rating
AP	Access Point
APB	Advanced Peripheral Bus
API	Application Program Interface
ARM9	Micro-processor
ASD	Application Specific Device
BB	Base Band
BER	Bit Error Rate
BOM	Bill Of Materials
BPSK	Binary Phase Shift Keying
BR	Basic Rate
BT	Bluetooth
BW	Band Width
C/I	Carrier-to-co-channel Interference
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCX	Cisco Compatible eXtensions
CDMA	Code Division Multiple Access
CENELEC	European Committee for Electrotechnical Standardization
CMOS	Complementary Metal Oxide Semiconductor
CODEC	COder DEcoder
CPU	Central Processing Unit
D/A	Digital to Analog
DBPSK	Differential Binary Phase Shift Keying
DC	Direct Current

Table 57. Glossary (continued)

Acronym	Definition
DCS	Digital Cellular System
DFS	Dynamic Frequency Selection
DMA	Direct Memory Access
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processing
DSSS	Direct Sequence Spread Spectrum
EAP	Extensible Authentication Protocol
EDCA	Enhanced Distributed Channel Access
EIA	Electronic Industries Association
ESD	Electro Static Discharge
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FEM	Front End Module
FM	Frequency Modulation
GPIO	General Purpose I/O pin
GSM	Global System for Mobile communications
HH	Hand Held
HW	HardWare
IBSS	Independent Basic Service Set
I/O	Input/Output
I2C	Inter-Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IPD	Integrated Passive Device
IRQ	Interrupt ReQuest
ISM	Industrial, Scientific and Medical
ITU	International Telecommunication Union
IV	Initialization Vector
JEDEC	Joint Electron Device Engineering Council
JESD	EIA JEDEC Standard
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
LO	Local Oscillator
MAC	Medium Access Control
MRD	Marketing Requirements Document
OFDM	Orthogonal Frequency Division Multiplexing

Table 57. Glossary (continued)

Acronym	Definition
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Pull-Down
PEAP	Protected Extensible Authentication Protocol
PER	Packet Error Rate
PHY	Physical (Layer)
PLL	Phase Locked Loop
ppm	parts per million
PSM	Power Saving Mode
PSMP	Power Save Multi Poll
PTA	Packet Traffic Arbitration
PU	Pull-Up
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RC	Resistance-Capacitance
RF	Radio Frequency
rms	root mean squared
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RX	Receive
SDIO	Secure Digital Input Output
SMPS	Switch Mode Power Supply
SoC	System on Chip
SPI	Serial Peripheral Interface
ST	STMicroelectronics
STA	802.11 Station or Client
STBC	Space Time Block Code
SW	SoftWare
TKIP	Temporal Key Integrity Protocol
TPC	Transmit Power Control
TX	Transmit
U-APSD	Unsolicited Automatic Power Save Delivery
VCO	Voltage Controlled Oscillator

Table 57. Glossary (continued)

Acronym	Definition
VGA	Variable Gain Amplifier
WCDMA	Wideband Code Division Multiple Access
WEP	Wired Equivalent Protection
Wi-Fi	Wireless Fidelity
WFA	Wi-Fi Alliance
WFBGA	Very Thin Profile Fine Pitch Ball Grid Array
WLAN	Wireless Local Area Network
WLCSP	Wafer-Level Chip Scale Package
WMM	WiFi Multimedia
WPA	WiFi Protected Access
ZIF	Zero Intermediate Frequency

8 Revision history

Table 58. Document revision history

Date	Revision	Changes
14-Dec-2012	1	Initial release.