Rockchip
瑞芯微电子

福州瑞芯微电子有限公司

SPECIFICATION

SPEC. NO.: ______________ REV: 1.7

DATE: 03.10. 2011

PRODUCT NAME: RK901

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

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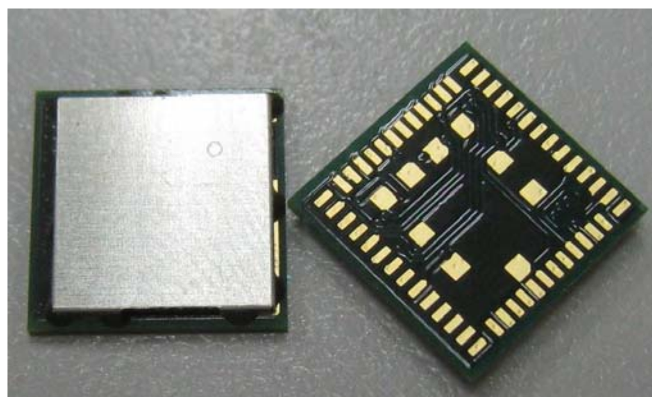
RK901

Wi-Fi SIP Module

Spec Sheet



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Revision History

Date	Revision Content	Revised By	Version
2011/08/22	-Initial released		1.0
2011/09/27	Modify physical dimensions		1.1
2011/10/19	Modify block diagram		1.2
2011/12/23	Add Power Consumption		1.3
2012/01/12	Modify dimension		1.4
2012/03/09	Add packing information		1.5
2012/03/19	More info to recommended footprint		1.6
2012/05/03	Pin description revised		1.7

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1. Introduction

Rockchip Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi functionalities. The highly integrated RK901 module makes the possibilities of web browsing, VoIP, headsets and other applications. With seamless roaming capabilities and advanced security, RK901 can also interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

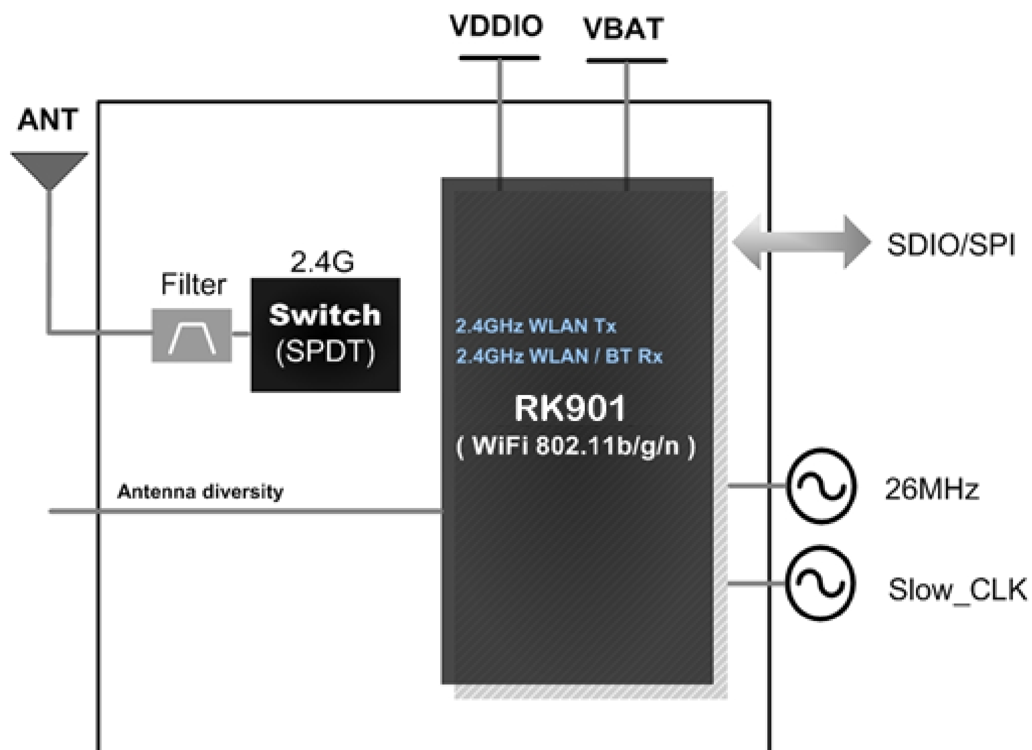
This wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi.

This compact module is a total solution for Wi-Fi technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- Single-band 2.4GHz IEEE 802.11b/g/n
- Supports standard interfaces SDIO v2.0(50MHz, 4-bit and 1-bit) and generic SPI(up to 50MHz)
- Integrated ARM Cortex-M3^{TM} CPU with on-chip memory enables running IEEE802.11 firmware that can be field-upgraded with future features.
- Supports per packet Rx antenna diversity
- Security:
    i. Hardware WAPI acceleration engine
    ii. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
    iii. WPA^{TM} – and WPA2^{TM} - (Personal) support for powerful encryption and authentication

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 Wi-Fi RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
Product Name	RK901 Wi-Fi SIP Module
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Main Chip	RK901
Host Interface	SDIO
Dimension	L x W x H: 9.5 x 9.5 x 1.5 mm
Frequency Range	2.412 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 ± 1dBm, typical
	- MCS=1 PER @ -84 ± 1dBm, typical
	- MCS=2 PER @ -82 ± 1dBm, typical
	- MCS=3 PER @ -80 ± 1dBm, typical
	- MCS=4 PER @ -77 ± 1dBm, typical
	- MCS=5 PER @ -73 ± 1dBm, typical
	- MCS=6 PER @ -71 ± 1dBm, typical
	- MCS=7 PER @ -69 ± 1dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -87 ± 1dBm, typical
	- 9Mbps PER @ -86 ± 1dBm, typical
	- 12Mbps PER @ -85 ± 1dBm, typical
	- 18Mbps PER @ -83 ± 1dBm, typical
	- 24Mbps PER @ -81 ± 1dBm, typical
	- 36Mbps PER @ -78 ± 1dBm, typical
	- 48Mbps PER @ -74 ± 1dBm, typical
	- 54Mbps PER @ -72 ± 1dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 ± 1dBm, typical
	- 2Mbps PER @ -89 ± 1dBm, typical
	- 5.5Mbps PER @ -87 ± 1dBm, typical

	- 11Mbps PER @ -84 ± 1dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6.5	V
VDDIO	Digital/Bluetooth/SDIO/SPI I/O Voltage	-0.5	4.1	V

4.2.2 Recommended Operating Ratings

Test conditions: At room temperature 25°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	3.0	3.6	5.0	V
VDDIO	1.7	1.8	1.92	V
	2.97	3.3	3.6	V

Note: The voltage of VDDIO is depended on system I/O voltage.

Test conditions: At operating temperature -10°C ~65°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	3.0	3.6	5.0	V
VDDIO	1.7	-	3.35	V

Note: VDDIO operating voltage range from 1.7V to 3.35V at operating temperature is guaranteed.

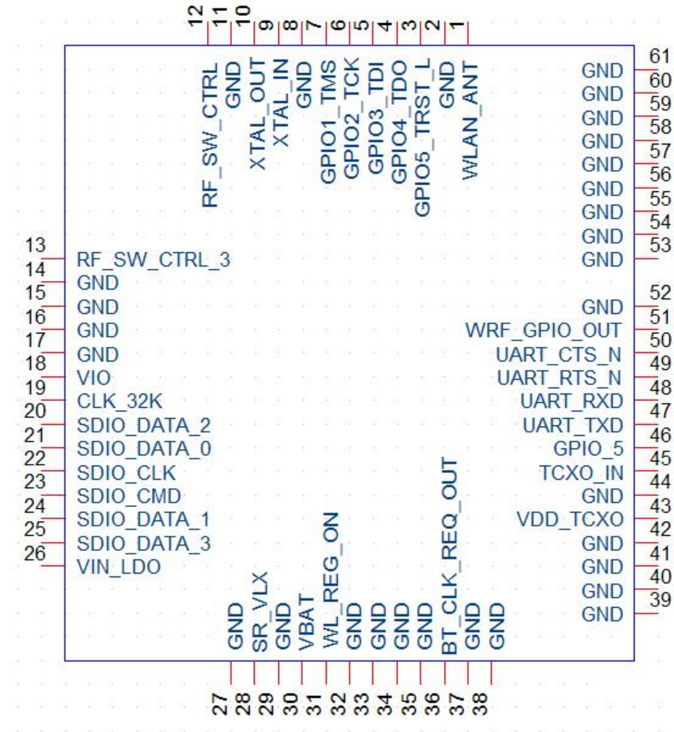
4.3 Power Consumption

Conditions: VBAT=3.0V; VDDIO=3.3V Temp=25°C

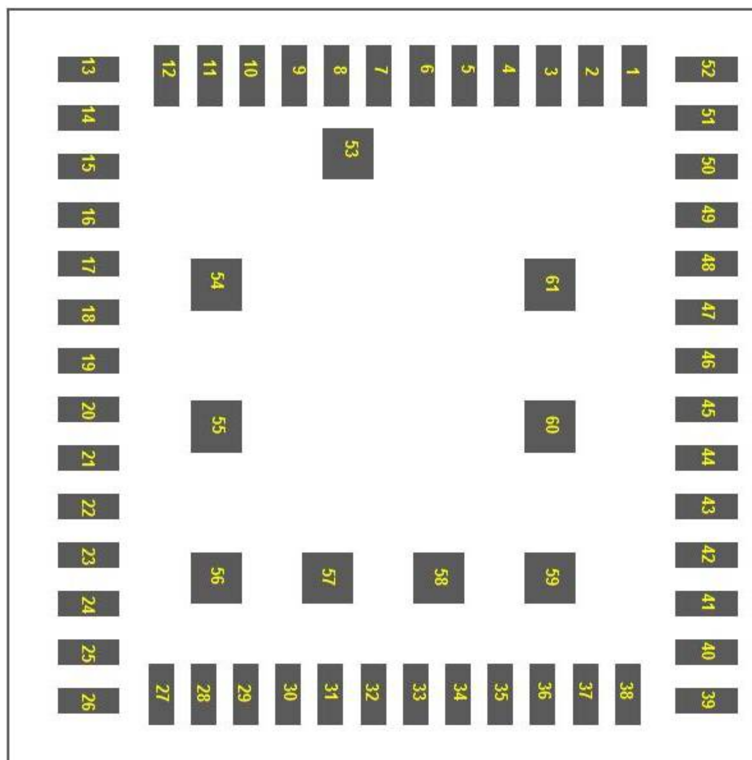
Mode	Description	Typ.	Max.	Unit
802.11B				
11Mbps, Transmit	Payload length 2304bytes, 250µs interval. @ 15 dBm	302		mA
11Mbps, Receive	-80dBm Payload length 1000Bytes	67		mA
802.11G				
54Mbps, Transmit	Payload length 2304Bytes, 250µs interval. @ 15 dBm	193		mA
54Mbps, Receive	-70dBm Payload length 1000Bytes	66		mA
802.11n				
65Mbps, Transmit	Payload length 2304Bytes, 250µs interval. @ 15 dBm	235		mA
65Mbps, Receive	-65dBm Payload length 1000Bytes	65		mA
Power save mode	OSC, BB PLL, RF PLL, AFE and Radio are powered down.	0.374		mA

5. Pin Assignments

5.1 Pin Outline



5.2 PCB Pin Outline



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5.3 Pin Definition

NO	Name	Type	Description
1	WLAN_ANT	I/O	RF signal I/O port
2	GND	—	Ground
3	JTAG_TRST_L	I	JTAG interface, if JTAG not used unconnected (NC)
4	JTAG_TDO_UART_TX	O	JTAG interface, if JTAG not used unconnected (NC) this pin. This pin is also muxed with UART_TX, which can be enabled by software
5	JTAG_TDI_UART_RX	I	JTAG interface, if JTAG not used unconnected (NC) this pin. This pin is also muxed with UART_RX, which can be enabled by software
6	JTAG_TCK	I	JTAG interface, if JTAG not used unconnected (NC)
7	JTAG_TMS	I	JTAG interface, if JTAG not used unconnected (NC)
8	GND	—	Ground
9	OSC_IN	I	XTAL oscillator input
10	OSC_OUT	I/O	XTAL oscillator output
11	GND	—	Ground
12	RF_SW_CTRL0	—	Floating (Don't connected to ground)
13	RF_SW_CTRL3	—	Floating (Don't connected to ground)
14	GND	—	Ground
15	GND	—	Ground
16	GND	—	Ground
17	GND	—	Ground
18	VIO	I	Digital I/O Voltage input
19	CLK_32K	I	Sleep clock (32.768KHz) input
20	SDIO_DATA_2	I/O	SDIO data line 2
21	SDIO_DATA_0	I/O	SDIO data line 0
22	SDIO_CLK	I	SDIO clock
23	SDIO_CMD	I/O	SDIO command line
24	SDIO_DATA_1	I/O	SDIO data line 1
25	SDIO_DATA_3	I/O	SDIO data line 3
26	VIN_LDO	I	Internal DC-DC regulator input
27	GND	—	Ground
28	SR_VLX	O	Internal DC-DC regulator output
29	GND	—	Ground
30	VBAT	I	DC voltage input
31	WL_RST_N	I	Active low WLAN reset signal

32	GND	—	Ground
33	GND	—	Ground
34	GND	—	Ground
35	GND	—	Ground
36	XTAL_PU	O	Floating (Don't connected to ground)
37	GND	—	Ground
38	GND	—	Ground
39	GND	—	Ground
40	GND	—	Ground
41	GND	—	Ground
42	GND	—	Ground
43	VDD_TCXO	—	Floating (Don't connected to ground)
44	GND	—	Ground
45	TCXO_IN	—	Floating (Don't connected to ground)
46	GPIO_5	—	Floating (Don't connected to ground)
47	GPIO_4	—	Floating (Don't connected to ground)
48	GPIO_3	—	Floating (Don't connected to ground)
49	GPIO_1	—	WL_Host Wake,
50	GPIO_0	—	Mode selection, Low for SDIO, High for SPI mode
51	WRF_GPIO_OUT	—	Floating (Don't connected to ground)
52	GND	—	Ground
53	GND	—	Ground
54	GND	—	Ground
55	GND	—	Ground
56	GND	—	Ground
57	GND	—	Ground
58	GND	—	Ground
59	GND	—	Ground
60	GND	—	Ground
61	GND	—	Ground

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6. Dimensions

6.1 Physical Dimensions

(Unit: mm)

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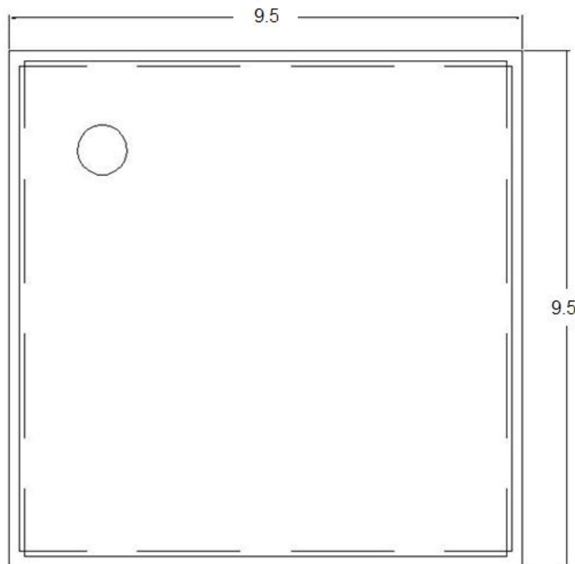
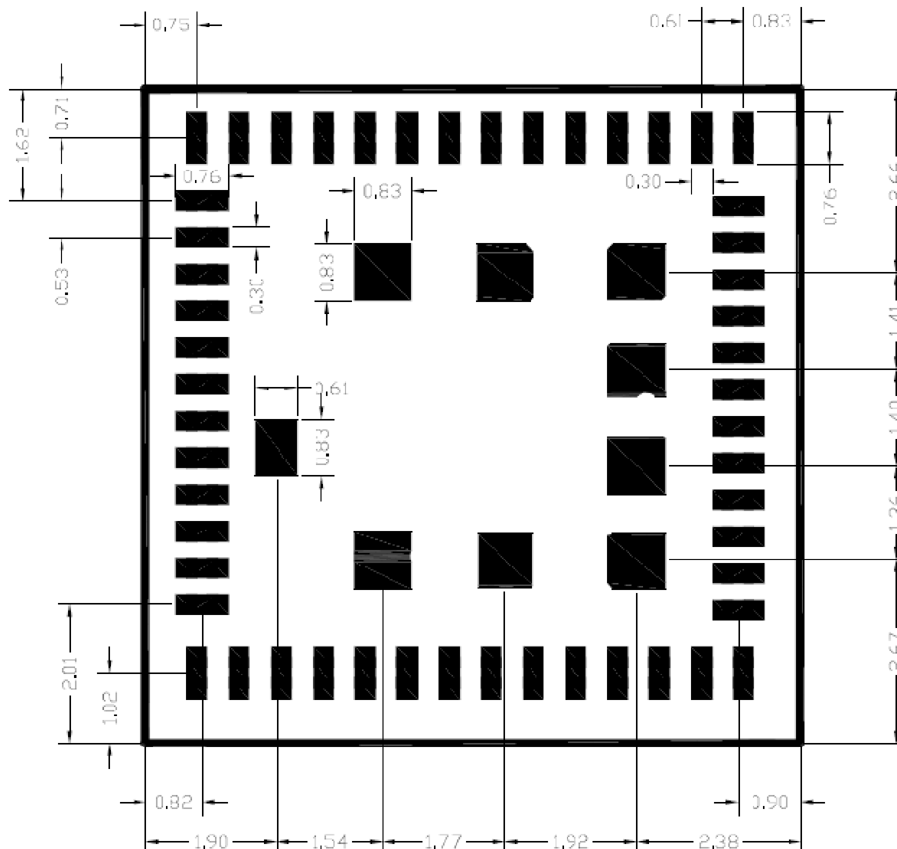


< Side View >



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6.2 Recommended Footprint

(Unit: mm)

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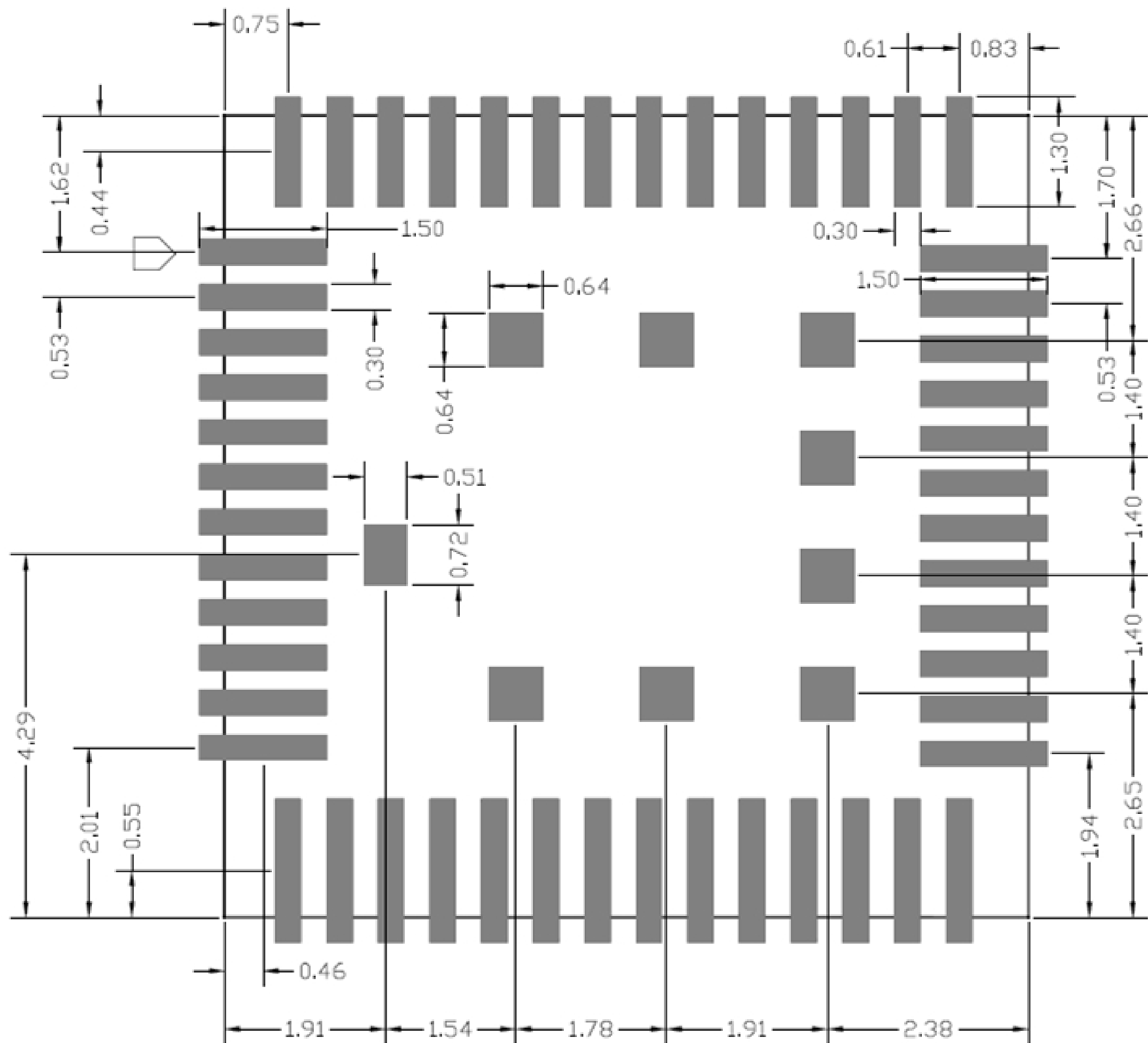


7. External clock reference

Crystal oscillator requirements and performance:

Parameter	Conditions/Notes	Crystal			TCXO			
		Min	Typ	Max	Min	Typ	Max	Units
Frequency	–	Between 12MHz and 52MHz						
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ohm
Input impedance (XTAL_IN)	Resistive	–	–	–	30k	100k	–	Ohm
	Capacitive	–	–		–	–	7.5	pF
Input impedance (TCXO_IN)	Resistive	–	–	–	30k	100k	–	Ohm
	Capacitive	–	–	–	–	–	4	pF
XTAL_IN Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
XTAL_IN Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.36	V
XTAL_IN Input voltage	AC-coupled analog signal	–	–	–	400	–	1200	mVp-p
TCXO_IN Input voltage	DC-coupled analog signal	–	–	–	400	–	3300	mVp-p
Frequency tolerance	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%

External LPO signal characteristics

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

7.1 SDIO Pin Description

The RK901 supports SDIO version 1.2 for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

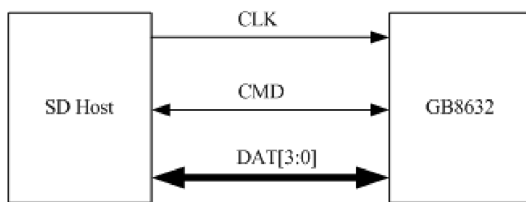
※ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)

※ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)

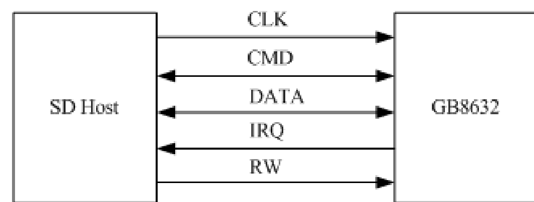
※ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize / ByteCount = 512B)

SDIO Pin Description

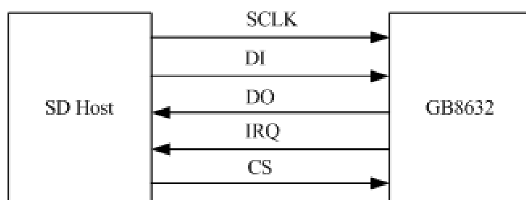
SD 4-Bit Mode		**SD 1-Bit Mode**		**SPI Mode**	
DATA0	Data Line 0	DATA	Data Line	DO	Data Output
DATA1	Data Line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data Line 2 or Read Wait	RW	Read Wait	NC	Not Used
DATA3	Data Line 3	NC	Not Used	CS	Card Select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command Line	CMD	Command Line	DI	Data Input



SD 4-Bit Mode



SD 1-Bit Mode



SPI Mode

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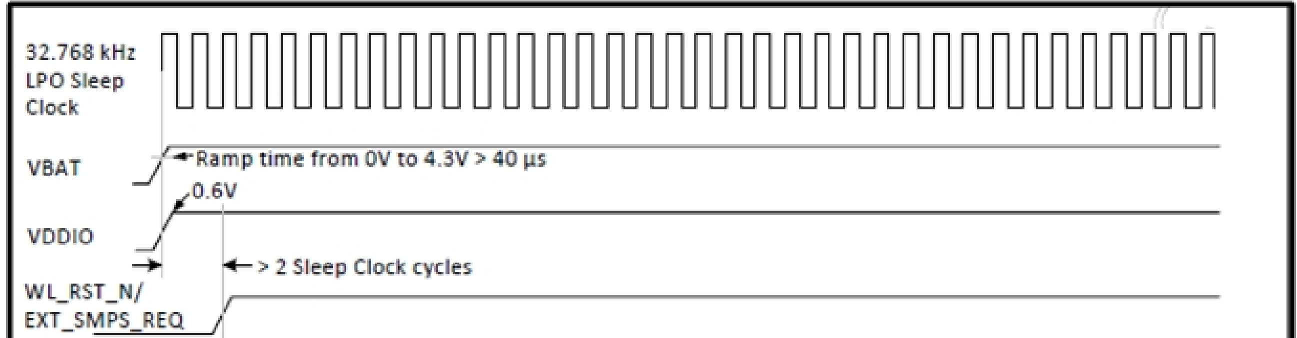
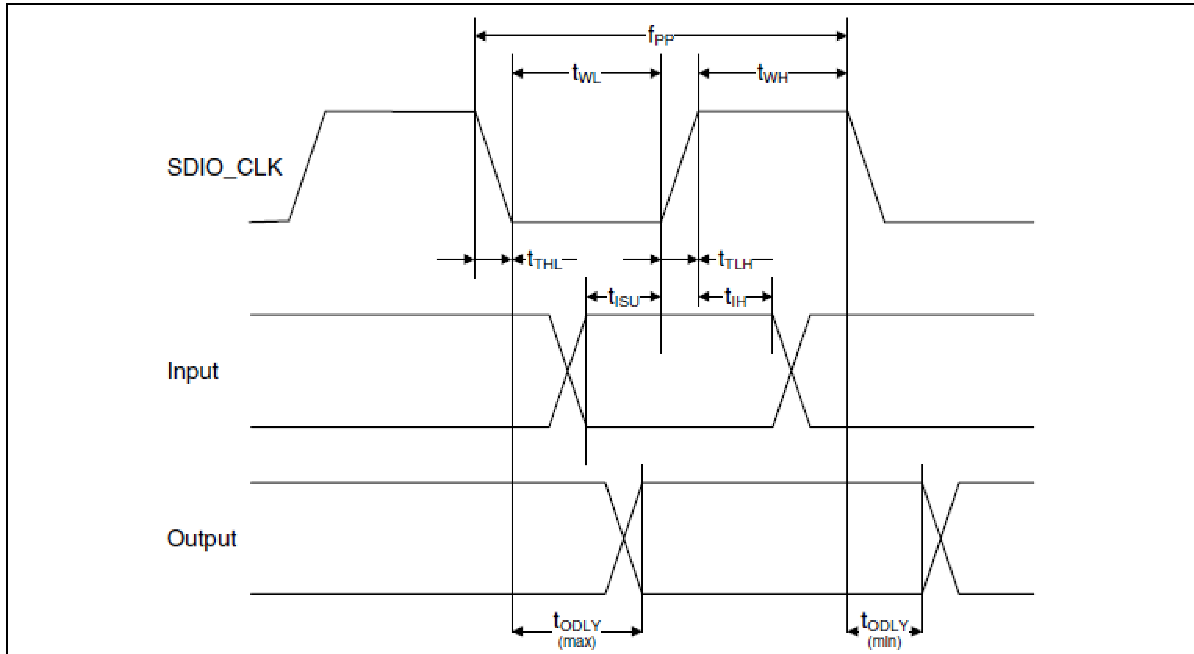
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram



※ WL_RST_N: Low asserting Reset for WLAN Core. This pin must be driven high or low (not left floating).

8.2 SDIO Default Mode Timing Diagram

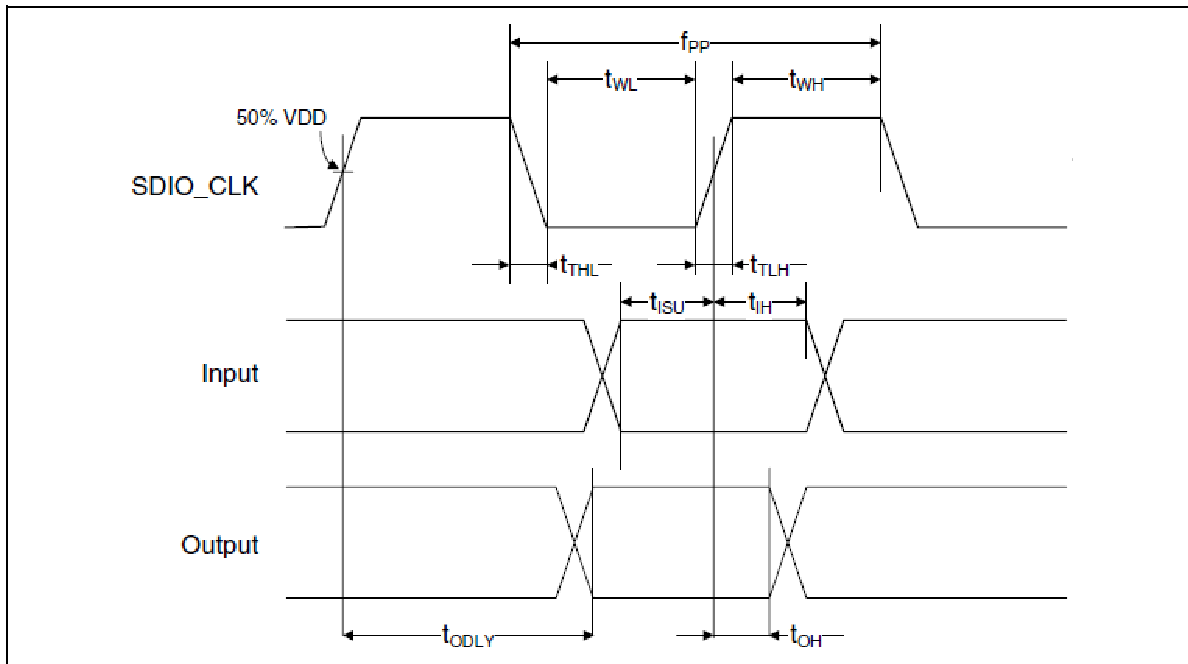


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

8.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

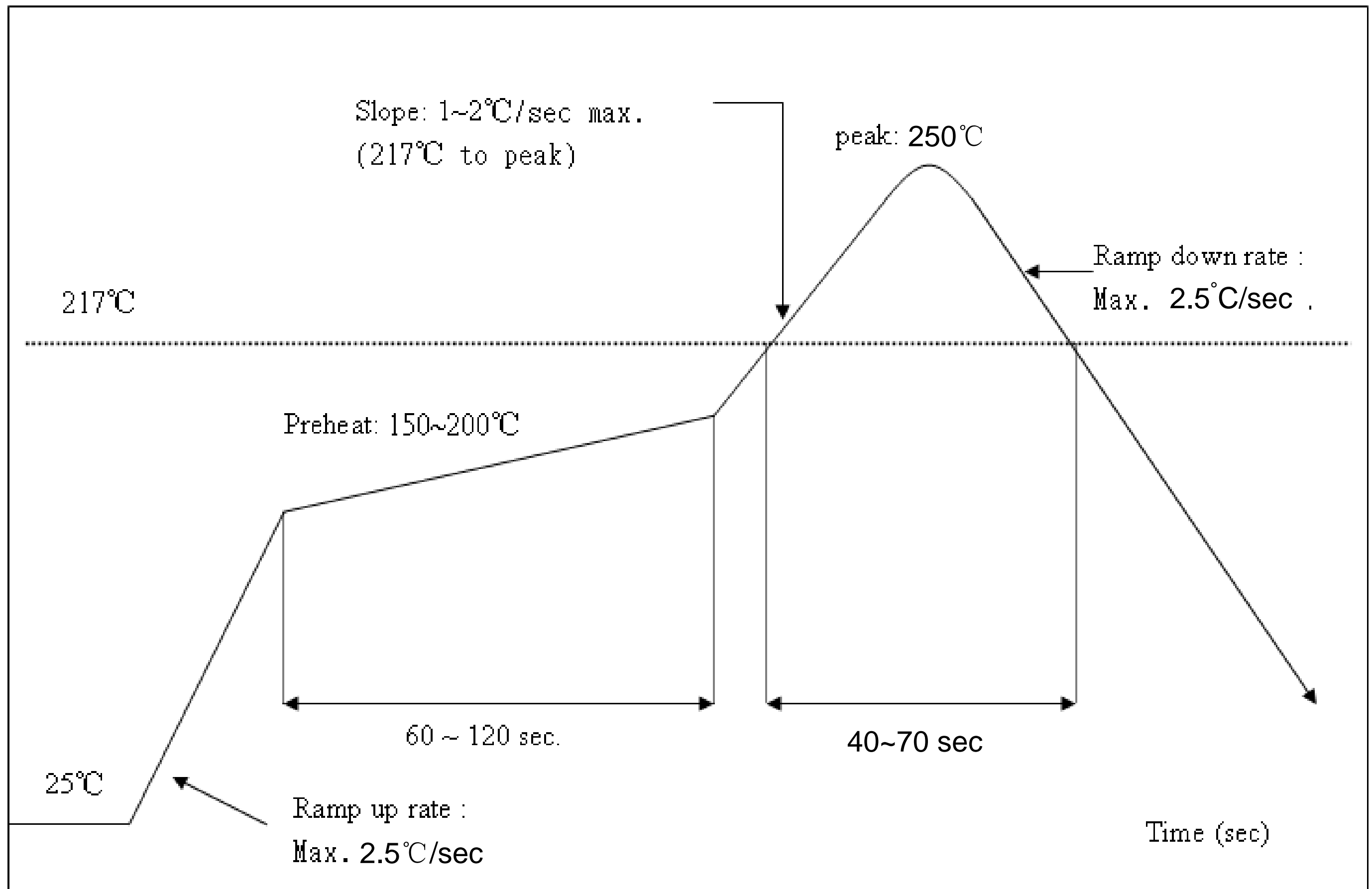
a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



10. Packing Information

10.1 Label

Label A → Anti-static and humidity notice

Label B → MSL caution / Storage Condition

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
2. Peak package body temperature: ____________ °C
   If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: ________ hours of factory conditions
   If blank, see adjacent bar code label
   ≤30°C/60% RH, or
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C
   b) 3a or 3b are not met
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: ____________________
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Label C → Inner box label .

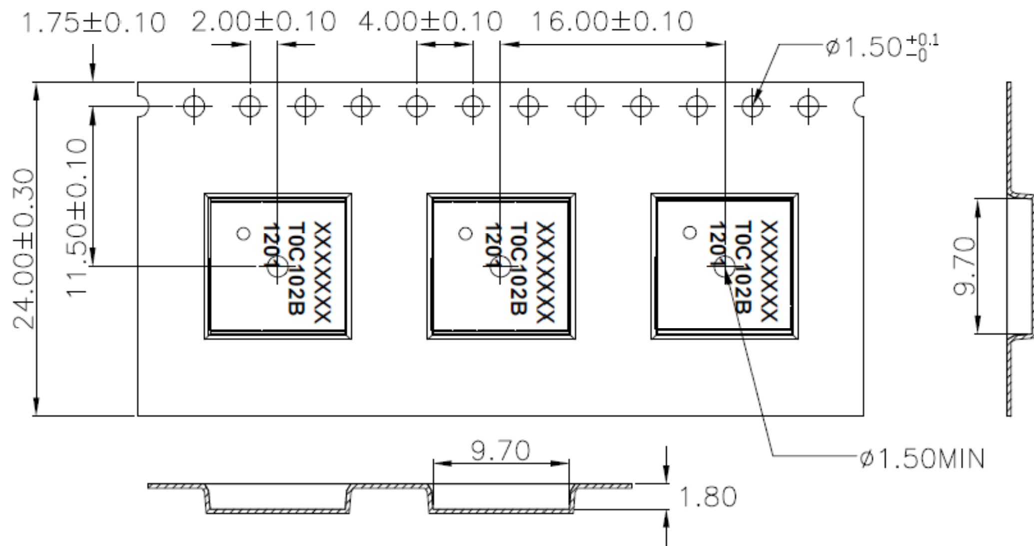
PKG S/N :	9PKG12013100001
Model:	XXXXXXXX(HF)
P/N :	99P-W01-0042R
Qty :	1500
Date Code :	1205
Lot Code :	T0C102B

Label D → Carton box label .

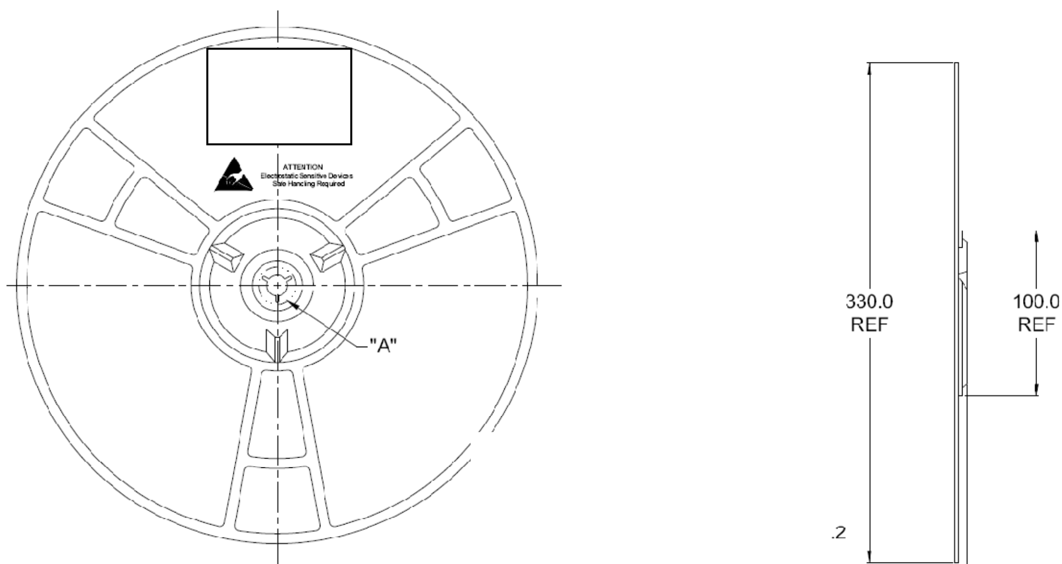
AMPAK Technology

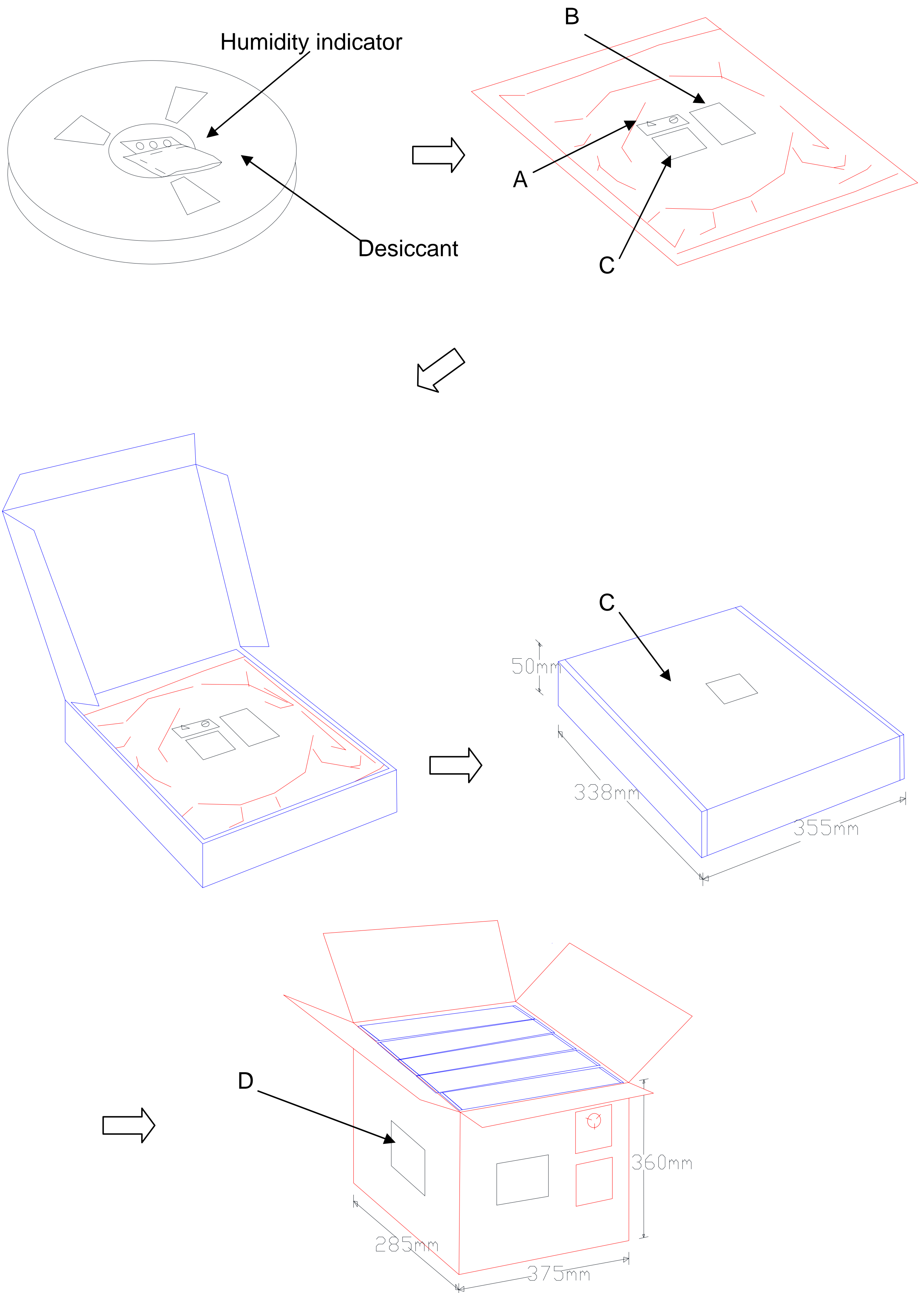
Model Name :	XXXXXXX(HF)
Part No :	99P-W01-0042R
Quantity :	7500 ea
Lot D/C :	1205
Manufacture :	2012/02/22

10.2 Dimension

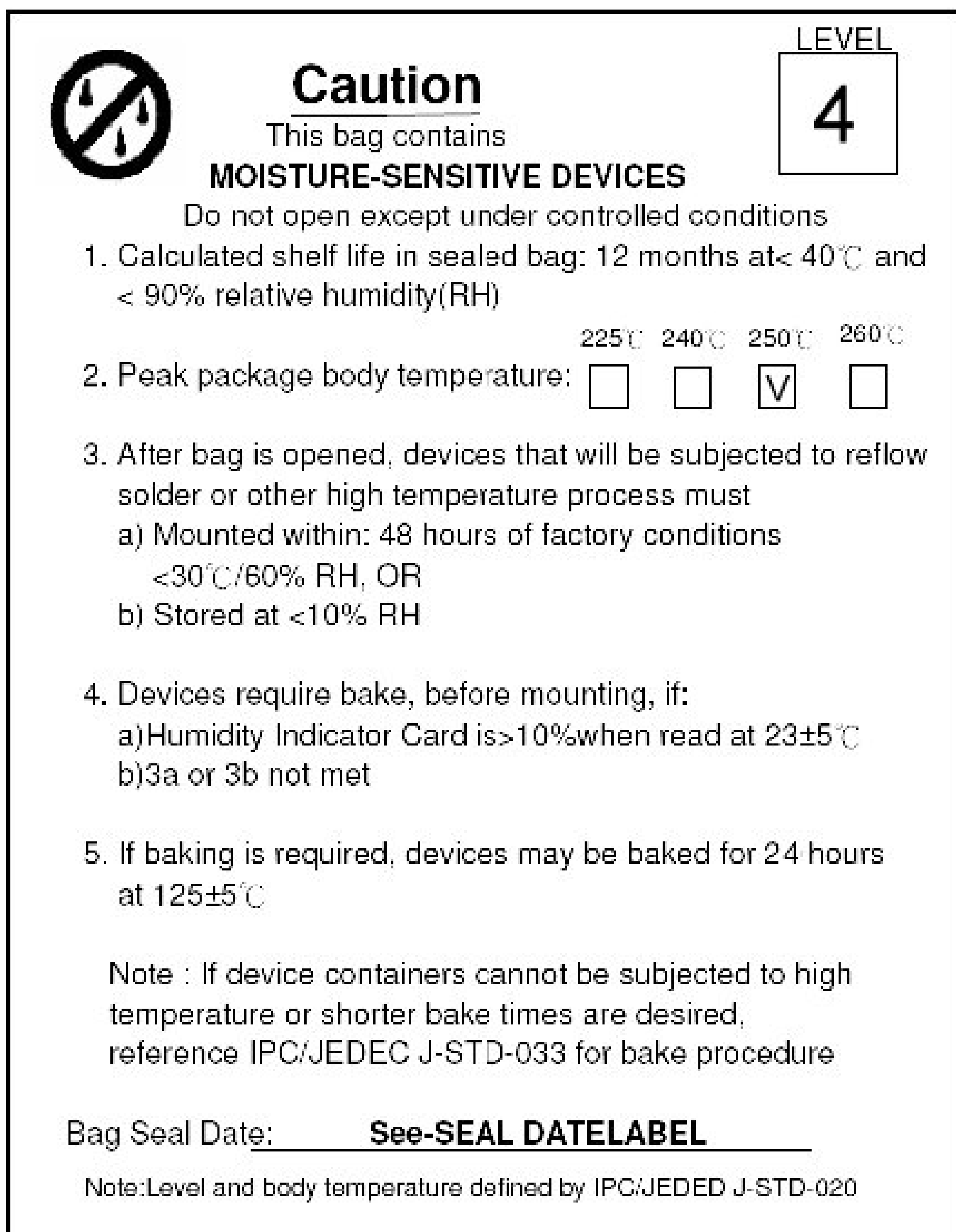


1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.




Humidity indicator
Desiccant
B
A
C
C
50mm
338mm
355mm
D
360mm
285mm
375mm

10.3 MSL Level / Storage Condition



LEVEL **4**

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and < 90% relative humidity(RH)
2. Peak package body temperature: 225℃ [ ] 240℃ [ ] 250℃ [V] 260℃ [ ]
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions <30℃/60% RH, OR
   b) Stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is>10%when read at 23±5℃
   b)3a or 3b not met
5. If baking is required, devices may be baked for 24 hours at 125±5℃

Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: **See-SEAL DATELABEL**

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs