PRODUCT DATA SHEET

RK2705

Revision A1.4
Feb, 2009

Release Note

Document Version Information

Product Version Information	
Product Name	RK2705
Version Number	A1.4
Previous Version	
Release Date	Feb 24, 2009

Document History

Version Number	Release Date	Change Notes
A 1.0	Nov 5, 2008	First release
A 1.1	Nov 5, 2008	Modify IO define
A 1.2	Dec 15, 2008	Update data book
A 1.3	Feb 13, 2009	Cancel the limit of QVGA MCU panel
A 1.4	Feb 24, 2009	Add PIN 34 (PA7/LCD_VSYNC) to support RGB panel

Product Overview

1.1 Overview

The RK2705 is an integrated system-on-chip with Dual Core architecture, which will focus on multimedia product application such as MP3, MP4, PMP etc. The Dual-Core architecture integrated ARM7EJC and DSP micro processor and by co-operating of those two CPUs, RK2705 can get high performance on Low-Power platform.

1.2 Features

- **System Operation**
  - Dual Core Architecture (ARM7EJC+DSP)
  - Support system boot sequentially from ARM7EJC to DSP
  - Selectable booting method
    - Boot from NOR Flash
    - Boot from Embedded ROM
  - Internal memory space
    - DSP IMEM 32Kwords
    - DSP DMEM 32Kwords
    - ARM7EJC Embedded Sync SRAM 4Kbytes
    - ARM7EJC Embedded Boot ROM 8Kbytes

- **Clock & Power Management**
  - Use two crystal oscillator (24MHz/32.768KHz)
  - Use three PLL (For ARM/DSP/CODEC+HSADC)
  - Support different AHB Bus and ARM7EJC clock ratio
    - 1:1 and 1:2 mode
  - Max frequency of every domain
    - ARM7EJC 240MHz (default 12MHz)
    - AHB BUS 133MHz (default 12MHz)
    - APB BUS 133MHz (default 12MHz)
    - DSP 176MHz (default 24MHz)
  - Power management mode
    - Normal, slow, idle, stop, and power-off mode

- **Processor**
  - ARM7EJC
    - ARMv5TE architecture with Jazella technology
    - 8x Java performance improvement
    - Five-stage pipeline
    - DSP extensions with 32x16 MAC
    - Small, cost-effective, processor macro cell
    - Unified Cache architecture , Size is 16KB(8words/line)
    - Two way configurable write-through cache
  - DSP
    - RISC-based four-way superscalar architecture
    - Eight-stage pipeline
    - Support 4GB address space
  - Dual-Core communication unit
    - Support dual cores system
    - Mailbox handshaking with interrupt mechanism
      - Support two AHB slave ports
      - Each mailbox element includes one data word register, one command word register, and one flag bit that can represent one interrupt
      - 4 interrupts to Host Interrupt Controller
      - 4 interrupts to Client Interrupt Controller

- **Memory controller**
  - Static/SDRAM Memory controller
    - Dynamic memory interface support
    - Asynchronous static memory device support including SRAM, ROM and Flash with or without asynchronous page mode
    - Support 1 independent AHB slave port for control register, and up to 2 individual AHB slave port for data access
    - Support 1 chip selects for SDRAM and 2 chip selects for static memory
    - support 16-bit wide SDRAM and 8-bit or 16-bit wide static memory
    - Support industrial standard SDRAM from 16MBytes to 128MBytes devices
    - 16Mbytes access space per static memory support
  - NAND Flash controller
    - Support 4 chip selects for NAND flash
    - support 8-bit wide data
    - Flexible CPU interface support
    - Embedded buffer to improve performance
    - Support internal DMA transfer from/to flash
    - 512bytes、2Kbytes、4Kbytes page size support
    - Hardware ECC
  - SD controller
    - Compliant with SD/SDHC spec. except SPI mode
    - Compliant with Multimedia Card system specification V3.3 except SPI mode, Stream R/W mode and I/O (Interrupt) mode
    - Variable SD/MMC card clock rate 0 – 25 MHz which depends on APB clock frequency
    - Controllable SD/MMC card clock to save power consumption
    - Support MMU ping-pong structure to enhance the SD/MMC data transfer performance
    - Support DMA transfer

- **LCD controller**
    - Support video data input format
      - 24bit RGB
      - 16bit RGB
      - YUV 4:2:2
      - YUV 4:2:0
    - Support serial 8bit RGB LCD panel with dummy data or not
    - Support Parallel 24bit (max) RGB LCD panel
    - Built-in 2 640x32bit buffer
    - Support DMA transfer

- **DMA Controller**
  - 3 DMA Controller on-chip
  - AHB DMA (HDMA)
    - Integrated in AHB BUS0
    - Two DMA channels support
    - 8 hardware request handshaking support
    - Built-in 32x16 data FIFO
    - Support hardware and software trigger DMA transfer mode
  - AHB-to-AHB Bridge (A2A)
    - Integrated between AHB BUS0 and AHB BUS1
    - Provide AHB-to-AHB bus protocol translation
    - Support AHB-to-AHB DMA or Single AHB DMA
    - Two DMA Channels support
    - On-the-fly mode between two level bus support
    - 4 hardware request handshaking support
    - Support hardware and software trigger DMA transfer mode
  - DW DMA

- Integrated in AHB BUS1
- Four DMA Channels support
- 8 hardware request handshaking support
- Support hardware and software trigger DMA transfer mode
- Build-in 4 data FIFO : 64bytes/64bytes/64bytes/64bytes
- Scatter/Gather transfer support
- LLP transfer support
- Two master for on-the-fly support

- **USB interface**
  - USB2.0 Device Controller
    - Complies with the Universal Serial Bus specification Rev. 2.0, Supports USB Full Speed (12Mb/sec) and High Speed (480 Mb/sec), is Backward compatible with USB1.1
    - On-chip USB2.0 PHY and Parallel Bus Interface Engine (PIE)
    - Suspend / Resume operation - Supports USB remote wake-up

- **Low speed Peripheral interface**
  - Serial Peripheral Interface (SPI) Master Controller
    - Four transfer protocols available with selectable clock polarity and clock phase
    - Different bit rates available for SCLK
    - Bi-direction mode
  - UART (16550)
    - 2 UART support
    - UART0 support modem function
    - Supports up to 3Mbps baud-rate
    - Programmable baud rate generator. This enables division of the internal clock by (1 ~ 65535 x 16) and generates an internal x16 clock
    - Standard asynchronous communication bits (start, stop and parity).
  - I2C controller
    - Multi masters operation
    - Software programmable clock frequency and transfer rate up to 400Kbit/sec
    - Supports 7 bits and 10 bits addressing modes
  - I2S
    - Support mono/stereo audio file
    - Support audio resolution: 8, 16 bits
    - Support audio sample rate from 32 to 96 KHz
    - Support I2S, Left-Justified, Right-Justified digital serial audio data interface
  - PWM
    - Built-in three 32 bit timer modulers
    - Programmable counter
    - Chained timer for long period purpose
    - 4-channel 32-bit timer with Pulse Width Modulation (PWM)
    - Programmable duty-cycle, and frequency output
  - General Purpose IO (GPIO)
    - Support 48 individually programmable input/output pins
    - Support GPIO with interrupt capability
  - Timers
    - Built-in three 32 bits timer modules
    - Programmable counter
  - Watchdog Timer (WDT)
    - Watchdog function
    - Built-in 32 bits programmable reset counter
- **Analog IP interface**
  - ADC Converter
    - 4-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
    - Supply 2.5V to 3.6V for analog and 0.9V to 1.3V for digital interface

- Very Low Power : <0.4mW power consumption at 1MSPS
- CODEC
  - Support built-in codec or external codec through I2S interface
  - Build in Stereo 24-bit Delta-Sigma DAC with on-chip headphone amplifier
  - Build in Stereo 16-bit Sigma-Delta ADC

- **Operation Frequency**
  - ARM7: up to 240MHz
  - DSP : up to 176MHz
  - AMBA AHB bus: up to 133 MHz
  - AMBA APB bus: up to 66 MHz

- **Package**
  - RK2705 LQFP128

- **Operation Temperature Range**
  - 0°C to +125°C

- **Operation Voltage Range**
  - Core: 1.25 V
  - I/O : 3.0 - 3.3V

1.3 Pin Description

1.3.1 RK2705 Pin Description

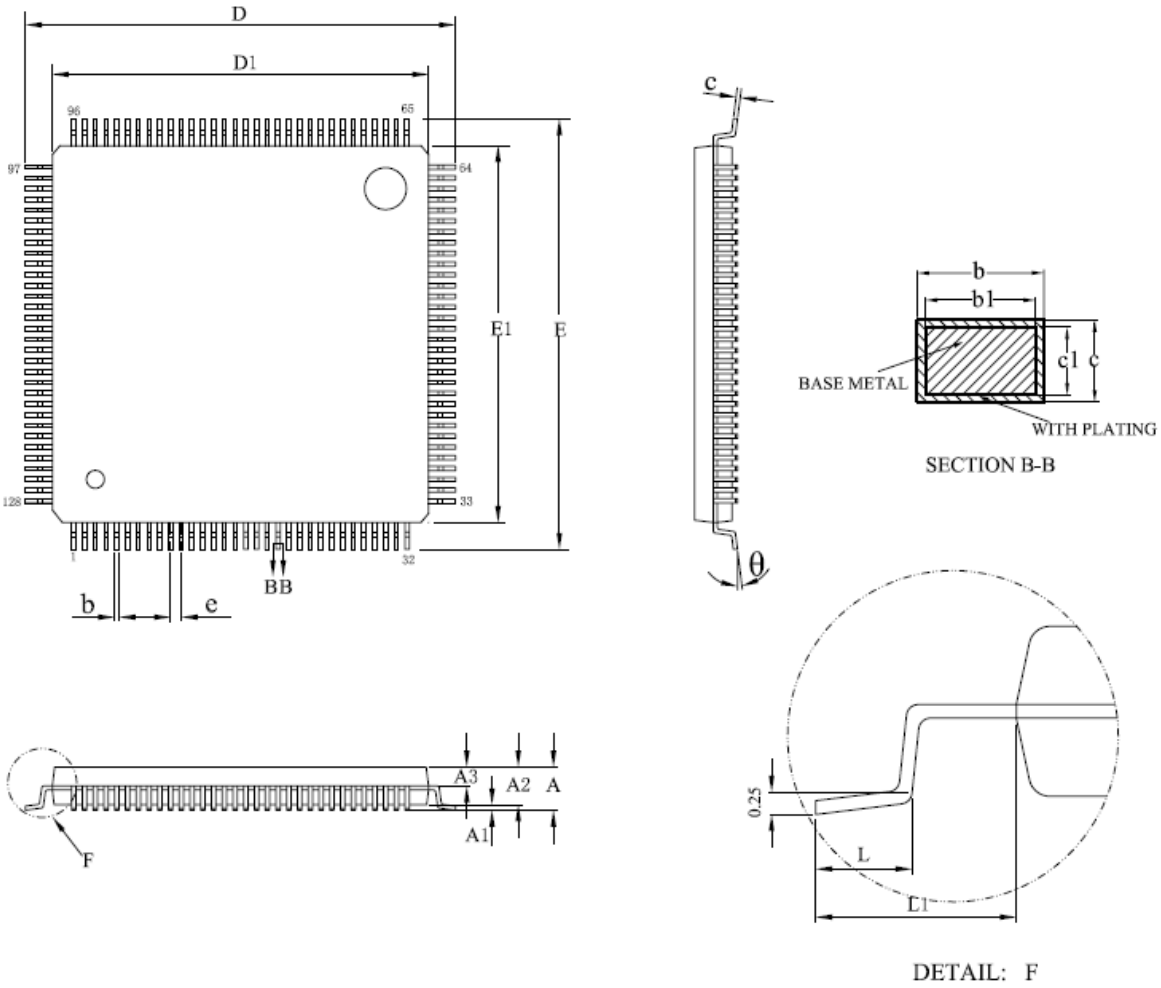
RK2705 LQFP128	Names	Direction	PIN Description
1	NPOR	I Pull up	Power on Reset
2	SDT_A6	O	SDRAM/SRAM addr[6]
3	SDT_A5	O	SDRAM/SRAM addr[5]
4	SDT_A4	O	SDRAM/SRAM addr[4]
5	SDT_A3	O	SDRAM/SRAM addr[3]
6	SDT_A2	O	SDRAM/SRAM data[2]
7	SDT_A1	O	SDRAM/SRAM data[1]
8	SDT_A0	O	SDRAM/SRAM data[0]
9	LCD_D0	O	lcd data[0]
10	LCD_D1	O	lcd data[1]
11	LCD_D2	O	lcd data[2]
12	LCD_D3	O	lcd data[3]
13	VDDIO	P	IO POWER SUPPLY 3.3V
14	VSS	P	GROUND
15	XIN24M	I OSC	Crystal 24M input
16	XOUT24M	O OSC	Crystal 24M output
17	VDD	P	CORE POWER SUPPLY 1.2V
18	LCD_D4	O	lcd data[4]
19	LCD_D5	O	lcd data[5]
20	LCD_D6	O	lcd data[6]
21	LCD_D7	O	lcd data[7]
22	PE0/LCD_D8	IO Pull up/O	GPIO E0/LCD data[8]
23	PE1/LCD_D9	IO Pull up/O	GPIO E1/LCD data[9]
24	PE2/LCD_D10	IO Pull up/O	GPIO E2/LCD data[10]
25	PE3/LCD_D11	IO Pull up/O	GPIO E3/LCD data[11]
26	PE4/LCD_D12	IO Pull up/O	GPIO E4/LCD data[12]
27	PE5/LCD_D13	IO Pull up/O	GPIO E5/LCD data[13]
28	PE6/LCD_D14	IO Pull up/O	GPIO E6/LCD data[14]
29	PE7/LCD_D15	IO Pull up/O	GPIO E7/LCD data[15]
30	PA0/LCD_D16/RXD0	IO Pull up/O/O	GPIO A1/LCD data[16]/UART0 rxd
31	PA1/LCD_D17/TXD0	IO Pull up/O/O	GPIO A1/LCD data[17]/UART0 txd
32	LCD_CLK/LCD_RS	O	RGB dot clock / MUC pannel

			RS
33	LCD_HSYNC	O	RGB HSYNC/MCU_WR
34	PA7/LCD_VSYNC	IO Pull up/O	GPIO A7/RGB_VSYNC/MCU_CS
35	FLASH_RDY	I pull up	NAND FLASH R/B
36	FLASH_RDN	O	NAND FLASH RD
37	FLASH_CS0	O	NAND FLASH CS0
38	FLASH_D7	B	nand flash data[7]
39	FLASH_D6	B	nand flash data[6]
40	FLASH_D5	B	nand flash data[5]
41	FLASH_D4	B	nand flash data[4]
42	FLASH_D3	B	nand flash data[3]
43	FLASH_D2	B	nand flash data[2]
44	FLASH_D1	B	nand flash data[1]
45	FLASH_D0	B	nand flash data[0]
46	FLASH_CLE	O	nand flash cle
47	FLASH_ALE	O	nand flash ale
48	FLASH_WRN	O	NAND FLASH WR
49	VDD	P	CORE POWER SUPPLY 1.2V
50	VSS	P	GROUND
51	VDDIO	P	IO POWER SUPPLY 3.3V
52	PB2/SDDATA0/SPI_MISO	IO Pull up/B/B	GPIO B2/SD DATA OUT/SPI_MISO
53	PB3/SDCMD/SPI_MOSI	IO Pull up/B/B	GPIO B3/SD DATA IN/SPI_MOSI
54	PB5/SDCLK/SPI_CLK	IO Pull up/O/O	GPIO B3/SD CLK/SPI_CLK
55	CODEC_AIL1	AI	L-channel analog input 1
56	CODEC_AIR1	AI	R-channel analog input 1
57	CODEC_MIC	AI	Mic input
58	CODEC_VCOM	AO	Internal biasing voltage
59	CODEC_VSSA	P	Ground for Codec
60	CODEC_VDDA	P	Power supply for CODEC, 3.3V
61	CODEC_AOHPL	AO	L-channel headphone output
62	CODEC_VSSAO	P	Ground for amplifiers
63	CODEC_VDDAO	P	Power supply for amplifiers 3.3V
64	CODEC_AOHPR	AO	R-channel headphone output
65	PA5/FLASH_CS1	IO Pull up/O	GPIO A5/FLASH CS1
66	SDA/FLASH_CS3/PB7	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS3/GPIO B7
67	SCL/FLASH_CS2/PB6	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS2/GPIO B6
68	PC0	IO Pull down	GPIO C0
69	PC1/LCD_DEN	IO Pull down/O	GPIO C1/RGB DEN
70	PC2/I2S_SCLK	IO Pull down/B	GPIO C2/I2S SCLK
71	PC3/I2S_LRCK	IO Pull down/B	GPIO C3/I2S LRCK
72	PC4/I2S_SDI	IO Pull down/I	GPIO C4/I2S DATA IN
73	PC5/I2S_SDO	IO Pull down/O	GPIO C5/I2S DATA OUT
74	PC6/I2SCLK	IO Pull down/O	GPIO C6/I2S CLOCK OUT
75	PD3/SD_CKE	IO Pull up/O	GPIO D3/SDRAM CKE
76	PD4/PWM0	IO /O	GPIO D4/PWM0
77	VDDIO	P	IO POWER SUPPLY 3.3V
78	VSS	P	GROUND
79	VDD	P	CORE POWER SUPPLY 1.2V
80	SDT_D15	B	SDRAM/SRAM data[15]
81	SDT_D14	B	SDRAM/SRAM data[14]
82	SDT_D13	B	SDRAM/SRAM data[13]
83	SDT_D12	B	SDRAM/SRAM data[12]
84	SDT_D11	B	SDRAM/SRAM data[11]
85	VBUS_DET	I Pull down	USB VBUS detect
86	LADC_AIN0	A	10bit adc channel0 input
87	LADC_AIN1	A	10bit adc channel1 input

88	LADC_AIN2	A	10bit adc channel2 input
89	LADC_VSSA	P	10bit adc analog ground
90	PHY_VDDA	P	USB PHY Analog Power 3.0V-3.3V
91	PHY_DN	A	USB DN
92	PHY_DP	A	USB DP
93	PHY_VSSA	P	USB PHY Analog Ground
94	PHY_REF	A	Resistor for USB 6.04K 1%
95	PHY_VDDP	P	USB PHY PLL POWER 1.2V
96	PHY_VSSP	P	USB PHY PLL Ground
97	SDT_D10	B	SDRAM/SRAM data[10]
98	SDT_D9	B	SDRAM/SRAM data[8]
99	SDT_D8	B	SDRAM/SRAM data[8]
100	SDT_D7	B	SDRAM/SRAM data[7]
101	SDT_D6	B	SDRAM/SRAM data[6]
102	SDT_D5	B	SDRAM/SRAM data[5]
103	SDT_D4	B	SDRAM/SRAM data[4]
104	SDT_D3	B	SDRAM/SRAM data[3]
105	SDT_D2	B	SDRAM/SRAM data[2]
106	SDT_D1	B	SDRAM/SRAM data[1]
107	SDT_D0	B	SDRAM/SRAM data[0]
108	SD_DQM1	O	SDRAM dqm[1]
109	SD_DQM0	O	SDRAM dqm[0]
110	SD_WEN	O	SDRAM wen
111	VDDIO	P	IO POWER SUPPLY 3.3V
112	VSS	P	GROUND
113	VDD	P	CORE POWER SUPPLY 1.2V
114	SD_CASN	O	SDRAM casn
115	SD_RASN	O	SDRAM rasn
116	SD_CLK	O	SDRAM clkout
117	SD_CSN	O	SDRAM csn
118	SD_BA0	O	SDRAM ba[0]
119	SD_BA1	O	SDRAM ba[1]
120	PD7	IO Pull down	GPIO D7
121	SDT_A11/PF1	O/IO Pull up	SDRAM/SRAM addr[11]/GPIO F1
122	SDT_A10	O	SDRAM/SRAM addr[10]
123	SDT_A9	O	SDRAM/SRAM addr[9]
124	SDT_A8	O	SDRAM/SRAM addr[8]
125	SDT_A7	O	SDRAM/SRAM addr[7]
126	ZPLL_VDDA	P	DSP PLL power 1.2V
127	PLL_VSSA	P	DSP PLL Ground
128	APLL_VDDA	P	ARM PLL power 1.2V
NOTE	**PC5/PD0/PD1/PD2/PD3/PD5/PD6/PF0 can not using as input IO port, only can using as output port**		
	UART1 only can using as TX mode, it can not receive data		

1.4Package outline

1.4.1 LQFP128 Package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.15	—	0.23
b1	0.14	0.16	0.19
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.40BSC		
L	0.42	0.60	0.80
L1	1.00BSC		
θ	0	—	8°

1.5 Architercture

1.5.1 Block Diagram