RK1000

Technical Reference Manual

Revision 1.4
Nov 2009

Revision History

Date	Revision	Description
2009-06-05	1.0	Initial Release
2009-06-05	1.1	Added test chip package information
2009-07-08	1.2	Add low power standby mode configuration Add CODEC pin discription
2009-07-16	1.3	Add LQFP128 package information
2009-11-3	1.4	Add RK1000-S LQFP64 package

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Chapter 1 Introduction

1.1 Overview

RK1000 is a digital-analog mixed chip which is used as a sub-chip for RK28xx or a single chip. It is designed for TVOUT, Audio-CODEC and HS-ADC functions.

This document will provide guideline on how to use RK1000 correctly and efficiently. In them , the chapter 1 will introduce the features, block diagram, signal descriptions of RK1000, the chapter 2 through chapter 7 will describe the full function of each module in detail.

1.2 Features

- **Interface**
  - I2C interface
  - RGB LCD interface
  - I2S interface

- **TV-OUT**
  - PAL/NTSC-CVBS/YPbPr traditional TV encoder
    - Support ITU-BT656/ ITU-BT601 standard
    - Support progressive RGB interface
  - 576p/480p-YPbPr SDTV encoder
  - 720p-YPbPr HDTV encoder
  - 3channel 10bit Video-DACs

- **CODEC**
  - Complete Stero/Mon Microphone interface
  - DAC and On-chip Headphone Driver
    - >20mW output power on 32Ω/3.3v
    - THD+N at 20mW, SNR>95dB with 32Ω load
    - No DC blocking capacitors required(capless mode)
  - Seperately mixed mono output
  - 256 x Fs/384 x Fs Master clock rates, up to 24MHz
  - Audio sample rates: 8 to 96kS/s
  - Less than -80dBc out-of-band Noise

- **High-Speed ADC (LQFP128 only)**
  - Two 10-bits ADCs
  - Sampling Rate: 10~60Msps
  - Input: differential, 1.8 V peak-to-peak differential
  - Power Dissipation: 12~60 mW (typical)
  - Dynamic Performance: 60 dB SFDR and 57 dB SINAD
  - Linearity: <1.5 LSB INL
    <1 LSB DNL, no missing codes
  - User-Programmable Bias Current of Pipelined Stages

- **Operation Voltage Range**
  - Core: 1.8V
  - I/O : 3.3V

- **Operating Temperature**
  - -10^{0}C ~ 60^{0}C
- **Storage Temperature**
  - -40^{0}C ~ 125^{0}C
- **Package Type**
  - RK1000 LQFP 128
  - RK1000–S LQFP 64

1.3 Block Diagram

The following figure shows block diagram of RK1000.

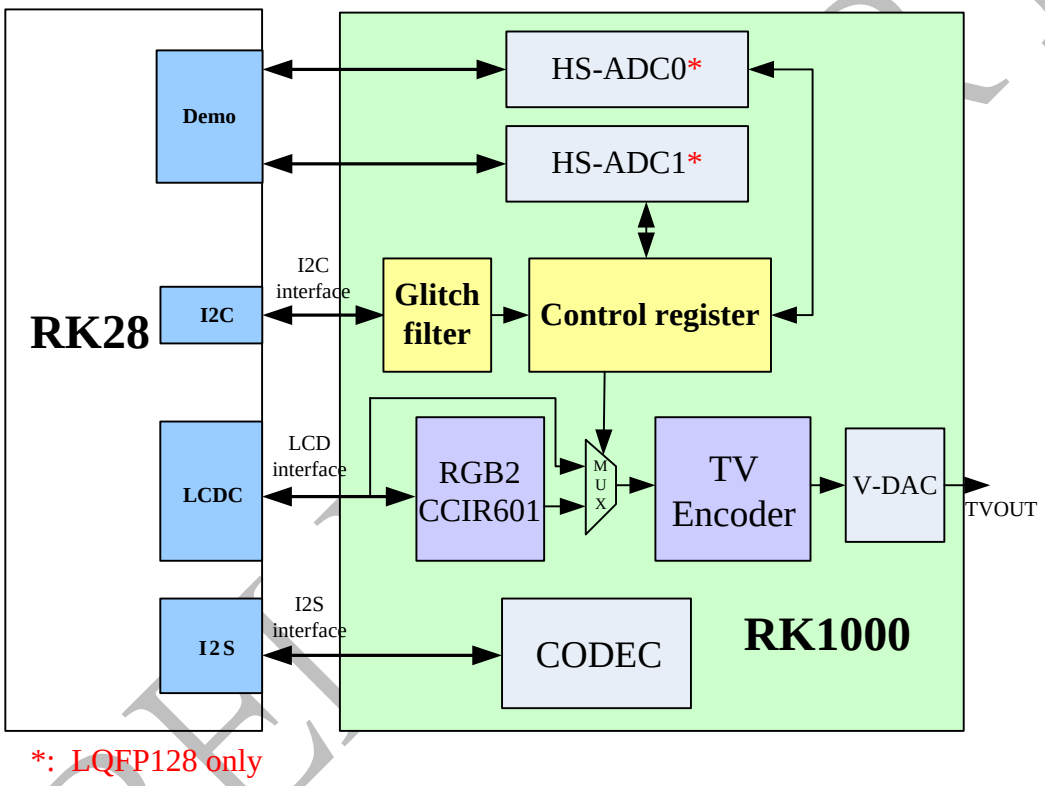


Fig. 1-1 RK1000 Block Diagram

1.4 Pin Description

1.4.1 RK1000 LQFP128 Pin description

Table 1-1 RK1000 Pin Description

PIN	PAD NAME	PIN TYPE	PULL UP/DOWN	PIN FUNCTION DESCRIPTION	
				1	2
LEFT SIDE					
1	ADC0 DOUT[0]	O	N/A	ADC0 DATA[0] OUTPUT	
2	LCDCCLKI	I	PULL UP	LCDC CLOCK INPUT	
3	HSYNCN	I	PULL DOWN	LCDC HSYNC INPUT	
4	VSYNCN	I	PULL DOWN	LCDC VSYNC INPUT	
5	LCD_D[17]	I	PULL DOWN	LCDC DATA[17] INPUT	DAC_DIN[9]
6	LCD_D[16]	I	PULL DOWN	LCDC DATA[16] INPUT	DAC_DIN[8]

7	LCD_D[15]	I	PULL DOWN	LCDC DATA[15] INPUT	DAC_DIN[7]
8	LCD_D[14]	I	PULL DOWN	LCDC DATA[14] INPUT	DAC_DIN[6]
9	LCD_D[13]	I	PULL DOWN	LCDC DATA[13] INPUT	DAC_DIN[5]
10	LCD_D[12]	I	PULL DOWN	LCDC DATA[12] INPUT	DAC_DIN[4]
11	VDDIO	P		IO POWER	
12	VSSIO	P		IO GROUND	
13	VSSCORE	P		CORE GROUND	
14	VDDCORE	P		CORE POWER	
15	LCD_D[23]	I	PULL DOWN	LCDC DATA[23] INPUT	
16	LCD_D[22]	I	PULL DOWN	LCDC DATA[22] INPUT	
17	LCD_D[21]	I	PULL DOWN	LCDC DATA[21] INPUT	
18	LCD_D[11]	I	PULL DOWN	LCDC DATA[11] INPUT	DAC_DIN[3]
19	LCD_D[10]	I	PULL DOWN	LCDC DATA[10] INPUT	DAC_DIN[2]
20	LCD_D[9]	I	PULL DOWN	LCDC DATA[9] INPUT	DAC_DIN[1]
21	LCD_D[8]	I	PULL DOWN	LCDC DATA[8] INPUT	DAC_DIN[0]
22	LCD_D[7]	I	PULL DOWN	LCDC DATA[7] INPUT	
23	LCD_D[6]	I	PULL DOWN	LCDC DATA[6] INPUT	
24	LCD_D[5]	I	PULL DOWN	LCDC DATA[5] INPUT	
25	LCD_D[4]	I	PULL DOWN	LCDC DATA[4] INPUT	
26	LCD_D[3]	I	PULL DOWN	LCDC DATA[3] INPUT	
27	LCD_D[2]	I	PULL DOWN	LCDC DATA[2] INPUT	
28	LCD_D[1]	I	PULL DOWN	LCDC DATA[1] INPUT	
29	LCD_D[0]	I	PULL DOWN	LCDC DATA[0] INPUT	
30	LCD_D[20]	I	PULL DOWN	LCDC DATA[20] INPUT	
31	LCD_D[19]	I	PULL DOWN	LCDC DATA[19] INPUT	DAC_PD
32	LCD_D[18]	I	PULL DOWN	LCDC DATA[18] INPUT	DAC_CLKIN
BOTTOM SIDE					
33	RSTN	I	PULL UP	RESET INPUT	
34	TEST	I	PULL DOWN	TEST MODE ENABLE	
35	CLK_SEL	I	PULL DOWN	LOGIC CLK SEL	
36	VDDIO	P		IO POWER	
37	VSSIO	P		IO GROUND	
38	VSSCORE	P		CORE GROUND	
39	VDDCORE	P		CORE POWER	
40	VDAC_PVSS3AP	B		ANALOG GROUD	
41	DACDVDD	P		DIGITAL POWER SUPPLY (+1.8)	
42	DACDVSS	G		DIGITAL GROUND	
43	DACB	A		DAC B CHANNEL OUTPUT	
44	DACAVD33B	P		ANALOG POWER (+3.3V) FOR CHANNEL B	
45	DACAVS33B	G		ANALOG GROUND FOR CHANNEL B	
46	DACG	A		DAC G CHANNEL OUTPUT	
47	DACAVD33G	P		ANALOG POWER (+3.3V) FOR CHANNEL G	
48	DACAVS33G	G		ANALOG GROUND FOR CHANNEL G	
49	DACR	A		R CHANNEL OUTPUT	
50	DACAVD33R	P		ANALOG POWER (+3.3V) FOR CHANNEL R	
51	DACAVS33R	G		ANALOG GROUND FOR CHANNEL R	
52	DACCOMP	A		COMPENSATION PIN. THIS PIN SHOULD BE CONNECTED THROUGH 0.01UF CERAMIC CAP PARALLEL WITH A 10UF TANTALUM CAP TO AVD33(+3.3V) EXTERNALLY	
53	DACAVDD	P		ANALOG POWER SUPPLY (+3.3)	
54	DACREXT	A		DAC EXTERNAL RESISTOR PIN. THE RESISTOR IS USED TO SET THE FULL SCALE OUTPUT CURRENT (IOFS). REXT(OHM)=VREFIN(V)*7.02 /IOFS(A).	
55	DACVREFIN	A		VOLTAGE REFERENCE INPUT	

56	DACVREFOUT	A		VOLTAGE REFERENCE OUTPUT. THIS OUTPUT 1.31V±3% REFERENCE VOLTAGE FROM BANDGAP REFERENCE BLOCK INTERNAL BANDGAP REFERENCE OUTPUT 1.31V±3%(NORMAL)	
57	DACAVSS	G		ANALOG GROUND	
58	VDAC_PVDD3AP	P		ANALOG POWER 3.3V	
60	NC				
61	NC				
62	NC				
63	NC				
64	NC				
RIGHT SIDE					
65	AIL	A		LEFT LINE IN INPUT	
66	AIR	A		RIGHT LINE IN INPUT	
67	MIC_IN	A		MICPHONE INPUT	
68	TP_MICBIAS	A		MICPHONE BIAS (VALUE=0.65*VDD OR 0.9*VDD)	
69	VDDA_REF	A		DAC REFERENCE DECOUPLING NODE(VALUE=VDD)	
70	TP_VMID	A		VMID REFERENCE DECOUPLING NODE (VALUE=VDD/2)	
71	VSSA	G		THE POWER GROUND OF CODEC ANALOG PART.	
72	VDDA	P		THE POWER SUPPLY OF CODEC ANALOG PART.	
73	AOR	A		RIGHT EARPHONE AMPLIFIER OUTPUT	
74	VSSAO	G		PA POWER GROUND	
75	AOM	A		MONO EARPHONE AMPLIFIER OUTPUT	
76	VDDAO	P		PA POWER SUPPLY	
77	AOL	A		LEFT EARPHONE AMPLIFIER OUTPUT	
78	VDDIO	P		IO POWER	
79	VSSIO	G		IO GROUND	
80	VSSCORE	G		CORE GROUND	
81	VDDCORE	P		CORE POWER	
82	ADCCLK	I	PULL UP	ADC CLOCK OUT INPUT	
83	I2CSCL	I	PULL UP	I2C CLOCK BUS	
84	I2CSDA	B	PULL UP	I2C DATA BUS	
85	I2SSDO	O		I2S DATA OUTPUT	
86	I2SSDI	I	PULL DOWN	I2S DATA INPUT	
87	ADCFRM	B	PULL DOWN	I2S LRCK FOR ADC	
88	DACFRM	B	PULL DOWN	I2S LRCK FOR DAC	
89	I2SBCLK	B	PULL DOWN	I2S BIT CLOCK	
90	I2SCLK	I	PULL UP	CODEC SYSTEM CLOCK INPUT	
91	NC				
92	NC				
93	NC				
94	NC				
95	NC				
TOP SIDE					
96	ADC1 DOUT[9]	B	N/A	ADC1 DATA OUT[9]	
97	ADC1 DOUT[8]	B	N/A	ADC1 DATA OUT[8]	
98	ADC1 DOUT[7]	B	N/A	ADC1 DATA OUT[7]	
99	ADC1 DOUT[6]	B	N/A	ADC1 DATA OUT[6]	
100	ADC1_VRP	A	N/A	POSITIVE REFERENCE VOLTAGE, EQUAL TO 1.3.CONNECT TO AN EXTERNAL 0.1UF CAP	
101	ADC1_VRN	A	N/A	NEGATIVE REFERENCE VOLTAGE, EQUAL 0.4, CONNECT TO AN EXTERNAL 0.1UF CAP.	
102	ADC1_VCM	O	N/A	COMMON MODE VOLTAGE, EQUAL TO 0.85, CONNECT TO AN EXTERNAL 0.1UF CAP IS OPTIONAL.	

103	ADC1_VIP	O	N/A	POSITIVE VOLTAGE INPUT	
104	ADC1_VIN	O	N/A	NEGATIVE VOLTAGE INPUT	
105	ADC1_VDDA	P	N/A	ANALOG POWER SUPPLY	
106	ADC1_VSSA	G	N/A	ANALOG GROUND	
107	ADC0_VRP	A	N/A	POSITIVE REFERENCE VOLTAGE, EQUAL TO 1.3.CONNECT TO AN EXTERNAL 0.1UF CAP	
108	ADC0_VRN	A	N/A	NEGATIVE REFERENCE VOLTAGE, EQUAL 0.4, CONNECT TO AN EXTERNAL 0.1UF CAP.	
109	ADC0_VCM	A	N/A	COMMON MODE VOLTAGE, EQUAL TO 0.85, CONNECT TO AN EXTERNAL 0.1UF CAP IS OPTIONAL.	
110	ADC0_VIP	A	N/A	POSITIVE VOLTAGE INPUT	
111	ADC0_VIN	A	N/A	NEGATIVE VOLTAGE INPUT	
112	ADC0_VDDA	P	N/A	ANALOG POWER SUPPLY	
113	ADC0_VSSA	G	N/A	ANALOG GROUND	
114	ADC0 DOUT[9]	O	N/A	ADC0 DATA OUT[9]	
115	ADC0 DOUT[8]	O	N/A	ADC0 DATA OUT[8]	
116	ADC0 DOUT[7]	O	N/A	ADC0 DATA OUT[7]	
117	ADC0 DOUT[6]	O	N/A	ADC0 DATA OUT[6]	
118	ADC0 DOUT[5]	O	N/A	ADC0 DATA OUT[5]	
119	ADC0 DOUT[4]	O	N/A	ADC0 DATA OUT[4]	
120	ADC0 DOUT[3]	O	N/A	ADC0 DATA OUT[3]	
121	ADC1 DOUT[5]	O	N/A	ADC1 DATA OUT[5]	
122	ADC1 DOUT[4]	O	N/A	ADC1 DATA OUT[4]	
123	ADC1 DOUT[3]	O	N/A	ADC1 DATA OUT[3]	
124	ADC1 DOUT[2]	O	N/A	ADC1 DATA OUT[2]	
125	ADC1 DOUT[1]	O	N/A	ADC1 DATA OUT[1]	
126	ADC1 DOUT[0]	O	N/A	ADC1 DATA OUT[0]	
127	ADC0 DOUT[2]	O	N/A	ADC0 DATA OUT[2]	
128	ADC0 DOUT[1]	O	N/A	ADC0 DATA OUT[1]	

1.4.2 RK1000-S LQFP64 Pin description

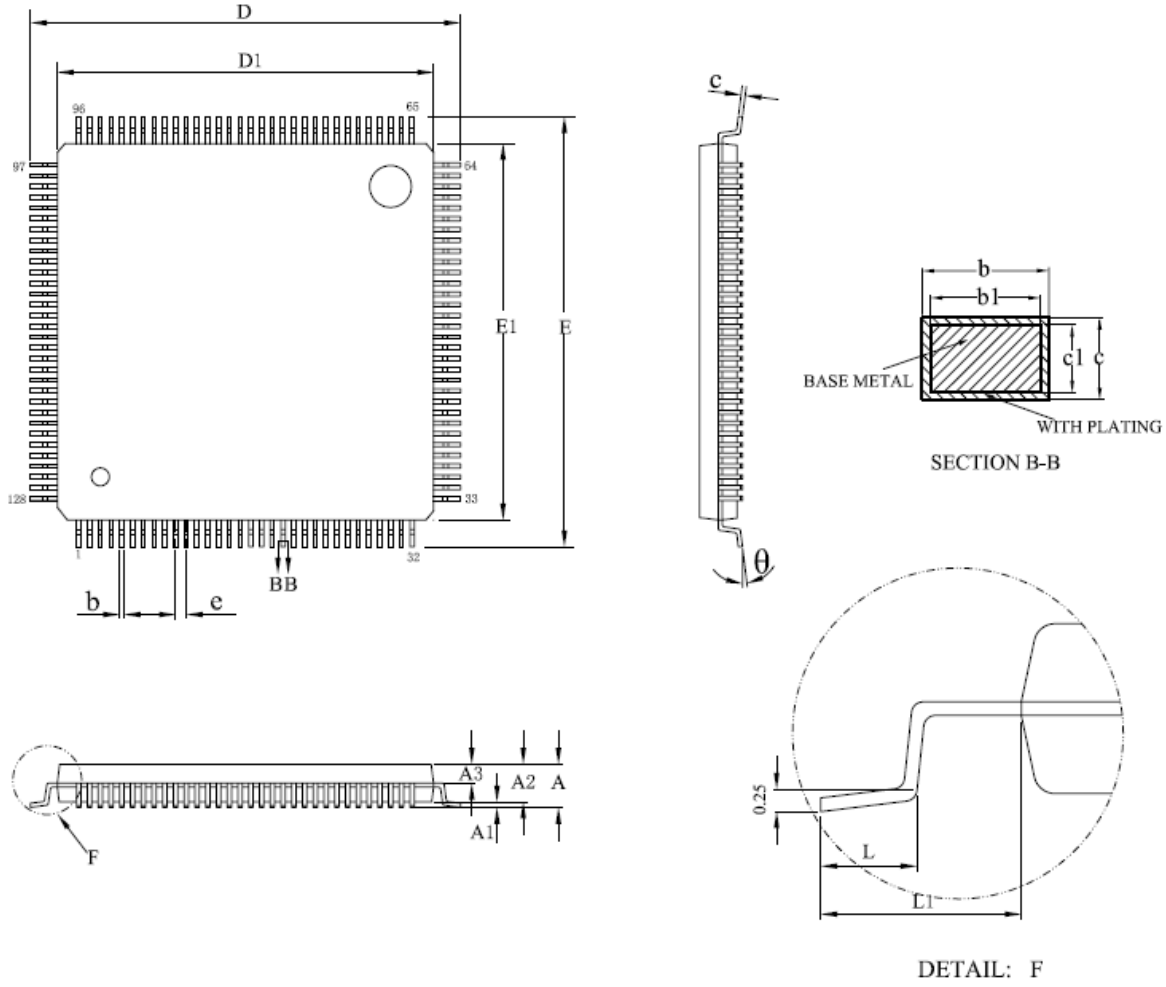
Table 1-2 RK1000-S Pin Description

Pin No.	PIN name	Pin Type	Pull Up/Down	Pin Function Description	
				1	2
Left Side					
1	LCD_D[15]	I	PULL DOWN	LCDC DATA[15] INPUT	DAC_DIN[7]
2	LCD_D[14]	I	PULL DOWN	LCDC DATA[14] INPUT	DAC_DIN[6]
3	LCD_D[13]	I	PULL DOWN	LCDC DATA[13] INPUT	DAC_DIN[5]
4	LCD_D[12]	I	PULL DOWN	LCDC DATA[12] INPUT	DAC_DIN[4]
5	VDDIO	P		IO POWER	
6	VDDCORE	P		CORE POWER	
7	LCD_D[23]	I	PULL DOWN	LCDC DATA[23] INPUT	
8	LCD_D[22]	I	PULL DOWN	LCDC DATA[22] INPUT	
9	LCD_D[21]	I	PULL DOWN	LCDC DATA[21] INPUT	
10	LCD_D[11]	I	PULL DOWN	LCDC DATA[11] INPUT	DAC_DIN[3]
11	LCD_D[10]	I	PULL DOWN	LCDC DATA[10] INPUT	DAC_DIN[2]
12	LCD_D[9]	I	PULL DOWN	LCDC DATA[9] INPUT	DAC_DIN[1]
13	LCD_D[7]	I	PULL DOWN	LCDC DATA[7] INPUT	
14	LCD_D[6]	I	PULL DOWN	LCDC DATA[6] INPUT	
15	LCD_D[5]	I	PULL DOWN	LCDC DATA[5] INPUT	

16	LCD_D[4]	I	PULL DOWN	LCDC DATA[4] INPUT	
BOTTOM SIDE					
17	LCD_D[3]	I	PULL DOWN	LCDC DATA[3] INPUT	
18	LCD_D[2]	I	PULL DOWN	LCDC DATA[2] INPUT	
19	LCD_D[1]	I	PULL DOWN	LCDC DATA[1] INPUT	
20	LCD_D[20]	I	PULL DOWN	LCDC DATA[20] INPUT	
21	LCD_D[19]	I	PULL DOWN	LCDC DATA[19] INPUT	DAC_PD
22	LCD_D[18]	I	PULL DOWN	LCDC DATA[18] INPUT	DAC_CLKIN
23	RSTN	I	PULL UP	RESET INPUT	
24	VDDIO	P		IO POWER	
25	VDDCORE	P		CORE POWER	
26	DACB	A		DAC B CHANNEL OUTPUT	
27	DACG	A		DAC G CHANNEL OUTPUT	
28	DACR	A		R CHANNEL OUTPUT	
29	DACCOMP	A		COMPENSATION PIN. THIS PIN SHOULD BE CONNECTED THROUGH 0.01UF CERAMIC CAP PARALLEL WITH A 10UF TANTALUM CAP TO AVD33(+3.3V) EXTERNALLY	
30	DACREXT	A		DAC EXTERNAL RESISTOR PIN. THE RESISTOR IS USED TO SET THE FULL SCALE OUTPUT CURRENT (IOFS). REXT(OHM)=VREFIN(V)*7.02 /IOFS(A).	
31	DACVREF	A		VOLTAGE REFERENCE, CONNNECT TO 0.1UF EXTERNAL	
32	GND	G		GROUND	
RIGHT SIDE					
33	GND	G		GROUND	
34	AIL	A		LEFT LINE IN INPUT	
35	AIR	A		RIGHT LINE IN INPUT	
36	MIC_IN	A		MICPHONE INPUT	
37	TP_MICBIAS	A		MICPHONE BIAS (VALUE=0.65*VDD OR 0.9*VDD)	
38	VDDA_REF	A		DAC REFERENCE DECOUPLING NODE(VALUE=VDD)	
39	TP_VMID	A		VMID REFERENCE DECOUPLING NODE (VALUE=VDD/2)	
40	VSSA	G		THE POWER GROUND OF CODEC ANALOG PART.	
41	VDDA	P		THE POWER SUPPLY OF CODEC ANALOG PART.	
42	AOR	A		RIGHT EARPHONE AMPLIFIER OUTPUT	
43	VSSAO	G		PA POWER GROUND	
44	AOL	A		LEFT EARPHONE AMPLIFIER OUTPUT	
45	VDDIO	P		IO POWER	
46	VDDCORE	P		CORE POWER	
47	I2CSCL	I	PULL UP	I2C CLOCK BUS	
48	I2CSDA	B	PULL UP	I2C DATA BUS	
TOP SIDE					
49	I2SSDO	O		I2S DATA OUTPUT	
50	I2SSDI	I	PULL DOWN	I2S DATA INPUT	
51	I2S_LRCK	B	PULL DOWN	I2S LRCK FOR ADC AND DAC	
52	I2SBCLK	B	PULL DOWN	I2S BIT CLOCK	
53	I2SCLK	I	PULL UP	CODEC SYSTEM CLOCK INPUT	
54	GND	G		GROUND	

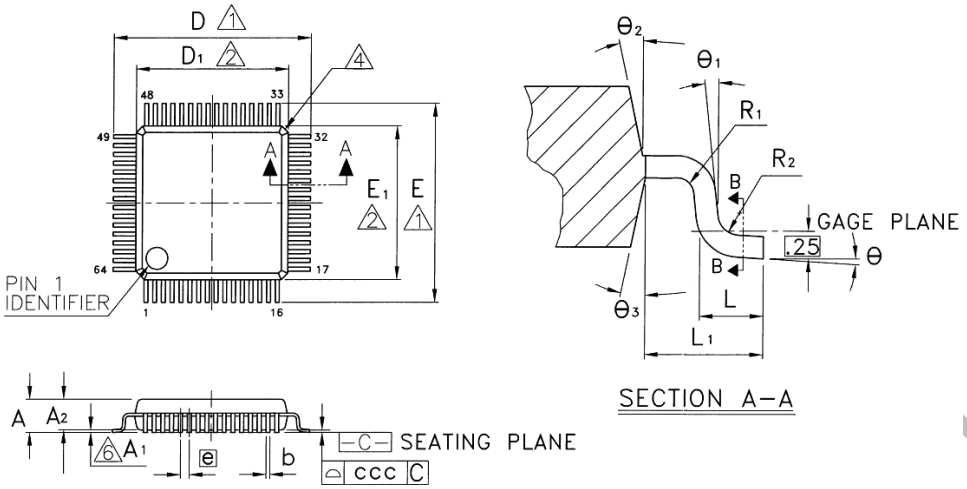
55	VDD18	B	N/A	ANALOG POWER SUPPLY	
56	NC	---			
57	AVCC	P		ANALOG POWER 3.3V FOR VDAC	
58	LCD_D[17]	I	PULL DOWN	LCDC DATA[17] INPUT	DAC_DIN[9]
59	VSYNCN	I	PULL DOWN	LCDC VSYNC INPUT	
60	HSYNCN	I	PULL DOWN	LCDC HSYNC INPUT	
61	LCDCCLKI	I	PULL UP	LCDC CLOCK INPUT	
62	NC	---			
63	NC	---			
64	NC	---			

1.5 LQFP128 Package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.15	—	0.23
b1	0.14	0.16	0.19
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.40BSC		
L	0.42	0.60	0.80
L1	1.00BSC		
θ	0	—	8°

1.5 LQFP64 Package outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Chapter 2 Control Register

2.1 I2C Interface

Control Register block is used to control other blocks of RK1000, such as HS-ADC, CODEC and TV_ENCODER. It is a I2C slave, then we can write and read those registers through I2C interaface.

There are another two I2C slaves with different slave addresses in RK1000, one in TV_ENCODER, the other one in CODEC.

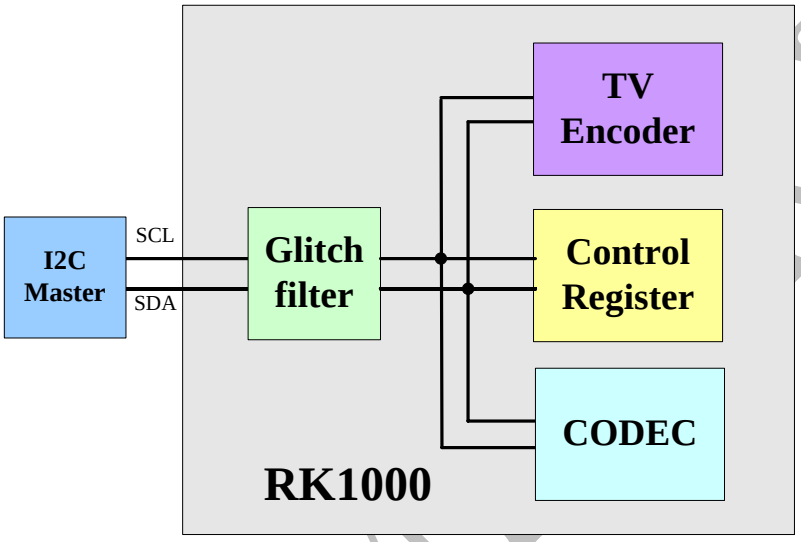


Fig. 2-1 RK1000 I2C Interface

Table 2-1 I2C slave in RK1000

I2C slave	Salve address
Control Register	7'h40
TV_ENCODER	7'h42
CODEC	7'b11xxxxx

2.2 Control Register

RK1000 control register comprises 5 r/w reisters and 1 read-only registers. This section describes the control/status registers of the design.

2.2.1 Registers Summary

Name	Offset	Size	Access	Reset Value	Description
ADC_CON	0x00	B	R/W	0x00	HS-ADC Control Register
CODEC_CON	0x01	B	R/W	0x00	CODEC Control Register
I2C_CON	0x02	B	R/W	0x00	I2C Glitch Filter Control Register
TVE_CON	0x03	B	R/W	0x00	TV-ENCODER Control Register
SRESET	0x04	B	R/W	0x00	RGB2CCIR601 soft reset
ADC_STAT	0x7	B	R	0x00	HS-ADC Status Register

2.2.2 Detail Register Description

ADC_CON
Address: I2C reg addr (0x00)
HS-ADC control register

bit	Attr	Reset Value	Description
7	R/W	0X0	Power down control signal ADC1, active HIGH
6:4	R/W	0X0	ADC1 Bias-current-Select. Set the unit bias current for pipeline stages for different conditions
3	R/W	0X0	Power down control signal ADC0, active HIGH
2:0	R/W	0X0	ADC0 Bias-current-Select. Set the unit bias current for pipeline stages for different conditions

CODEC_CON
Address: I2C reg addr (0x01)
CODEC control register

bit	Attr	Reset Value	Description
7	-	-	reserved
4	R/W	0X0	Control register module clock select 0: select I2S clock input 1: select the lcdc clock input
3	R/W	0X0	CODEC DAC lrck output enable control (Active low) 0: CODEC I2S DAC lrck output enable 1: CODEC I2S DAC lrck output disable
2	R/W	0X0	CODEC ADC lrck output enable control (Active low) 0: CODEC I2S ADC lrck output enable 1: CODEC I2S ADC lrck output disable
1	-	-	reserved
0	R/W	0X0	CODEC select control signal 0: using CODEC in RK1000 1: select to use the CODEC outside. When assert high, the I2C and I2S connect to internal CODEC will be disable

I2C_CON
Address: I2C reg addr (0x02)
I2C glitch filter control register

bit	Attr	Reset Value	Description
7:4	R/W	0X0	Rising Timeout period for I2C I2C glitch filter
3:0	R/W	0X0	Falling Timeout period register for I2C glitch filter

TVE_CON
Address: I2C reg addr (0x03)
TV_ENCODER and rgb2ccir601 control register

bit	Attr	Reset Value	Description
7	R/W	0X0	V-DAC channel R bypass 0: Disable 1: Enable
6	R/W	0X0	TVE cvbs 3 channel output enable 0: Disable 1: Enable
5:4	R/W	0X0	rgb2ccir601 input data format 00: RGB888 01: RGB666

			10: RGB565 11: YUV bypass
3	R/W	0X0	rgb2ccir601 RGB data RB swap 0: RGB 1: BGR
2	R/W	0X0	rgb2ccir601 input video format 0: Progressive 1: Interlace
1	R/W	0X0	rgb2ccir601 TV format 0: PAL(625 line) 1: NTSC(525 line)
0	R/W	0X0	rgb2ccir601 enable 0: rgb2ccir601 bypass 1: rgb2ccir601 enable

SRESET_CON
Address: I2C reg addr (0x04)
Rgb2ccir601 soft reset register

bit	Attr	Reset Value	Description
7:1	-	0X0	Reserved
0	W	0X0	Rgb2ccir601 sreset Write 1 to this bit enable Rgb2ccir601 sreset, It will be automatically cleared

ADC_STAT
Address: I2C reg addr (0x07)
HS-ADC statuus register

bit	Attr	Reset Value	Description
7:4	-	0X0	Reserved
3	R	0X0	UND,for ADC1 Digital output signal inicating the underflow condition VIP-VIN<-0.9V, UND="1",otherwise UND="0"
2	R	0X0	OVR, for ADC1 Digital output signal inicating the overflow condition VIP-VIN>0.9V, OVR="1",otherwise OVR="0"
1	R	0X0	UND,for ADC0 Digital output signal inicating the underflow condition VIP-VIN<-0.9V, UND="1",otherwise UND="0"
0	R	0X0	OVR, for ADC0 Digital output signal inicating the overflow condition VIP-VIN>0.9V, OVR="1",otherwise OVR="0"

Notes: Attr: **RW** – Read/writable, **R** – read only, **W** – write only

2.3 Functional Description

2.3.1 I2C Write/Read

1. Control Register I2C Writing

2. Control Register I2C Reading

S	SLAVE ADDR	1	A	RDATA_0#	A	·····	RDATA_N	Ā	P
	7-bits	r/w		8-bits			8-bits		

note : I2C slave addr = 7'h40*

2.3.2 Internal I2C clock

Internal I2C clock is used for handling the asynchronous I2C bus signals. It's source can be LCDC clock or I2S clock.

First, the external IO pin (IO_CLK_SEL) controls the hardware switch of Inernal I2C clock source, IF "IO_CLK_SEL = 1", the internal I2C clock always come from I2S clock, IF "IO_CLK_SEL = 0", the register bit of (I2C_CON[4]) controls the software switch of Inernal I2C clock source.

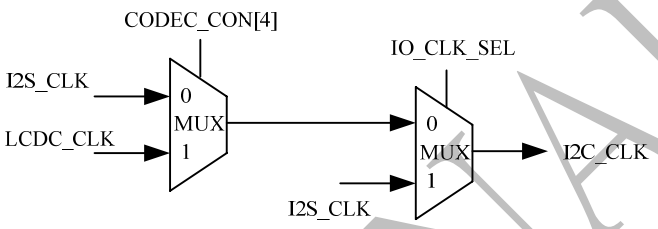


Fig. 2-2 I2C clock switch

2.3.3 I2C Glitch Filter

I2C glitch filter is designed for avoiding the I2C comunication error because of SDA and SCl signal glitches.

The SCL and SDA input signals from I2C bus are filtered(both positive edge and negtive edge) by the glitch filter block, then they are input to the three I2C slaves.

The glitch filter timeout values of both positive edge and negtive edge are setting in the control register(I2C_CON)

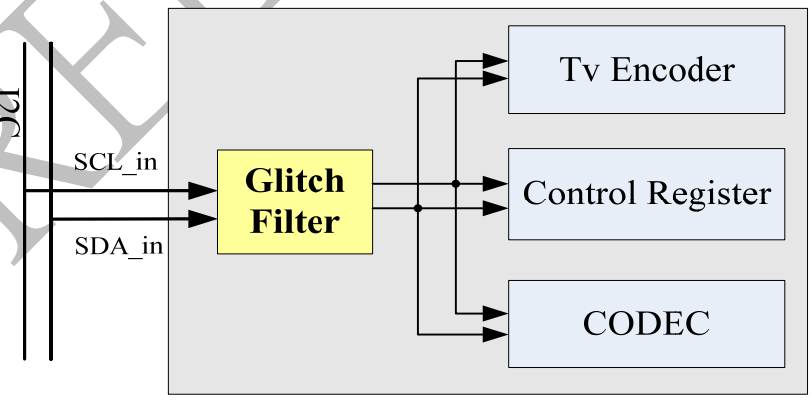


Fig. 2-3 I2C Glitch filter

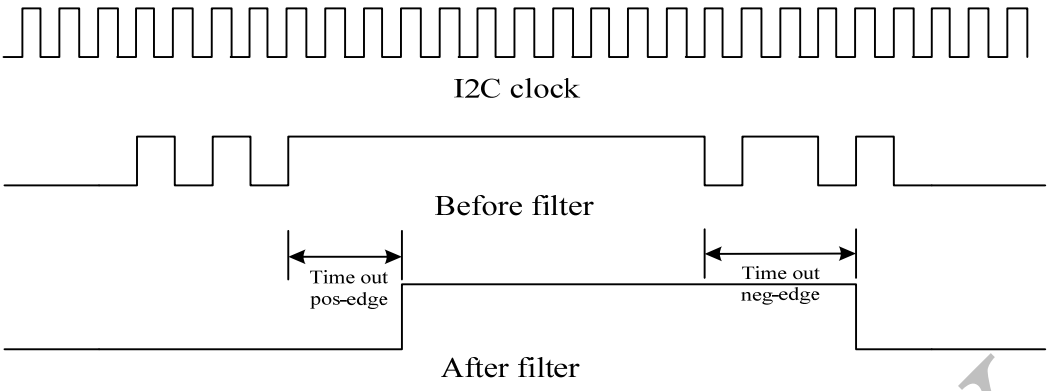


Fig. 2-4 Glitch filter wavefrom

2.3.4 RGB2CCIR601 Bypass

When the output of LCDC is RGB interface(progressive or interlace), RGB2CCIR601 module is use to transfer it to CCIR601 standard interface(interlace) for TV_ENCODER in mode of traditional TV-OUT.

If the input LCD interface is CCIR656 or TV_OUT mode is 576p/480p/720p, RGB2CCIR601 module must be bypassed.

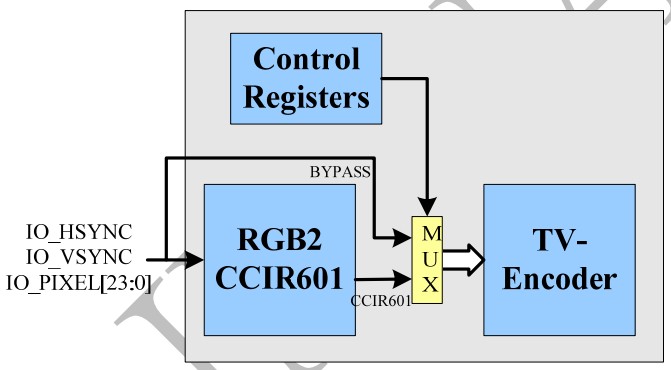


Fig. 2-5 RGB2CCIR601 Bypass

2.3.5 TVE 3-channel cvbs out

In the mode of TV_ENCODER output cvbs signals to V_DAC, 3-channel cvbs signals can be output by setting "TVE_CON[6] = 1".

2.3.6 V-DAV R-Channel Bypass

There 3 channels(RGB) 10-bits DACs in Video-DAC. The R channel DAC can be bypassed for the ustage of a signal 10-bits DAC when "TVE_CON[7]=1".

Table 2-2 V-DAC R channel bypass

I/O	IO MUX	Discription	Switch
IO_PIXEL[8]	pixel_data[8]	pixel_data[8] for TVE	default
	DAC_din[0]	bypass DAC_din[0]	reg_03[7]=1
IO_PIXEL[9]	pixel_data[9]	pixel_data[9] for TVE	default
	DAC_din[1]	bypass DAC_din[1]	reg_03[7]=1
IO_PIXEL[10]	pixel_data[10]	pixel_data[10] for TVE	default
	DAC_din[2]	bypass DAC_din[2]	reg_03[7]=1

IO_PIXEL[11]	pixel_data[11]	pixel_data[11] for TVE	default
	DAC_din[3]	bypass DAC_din[3]	reg_03[7]=1
IO_PIXEL[12]	pixel_data[12]	pixel_data[12] for TVE	default
	DAC_din[4]	bypass DAC_din[4]	reg_03[7]=1
IO_PIXEL[13]	pixel_data[13]	pixel_data[13] for TVE	default
	DAC_din[5]	bypass DAC_din[5]	reg_03[7]=1
IO_PIXEL[14]	pixel_data[14]	pixel_data[14] for TVE	default
	DAC_din[6]	bypass DAC_din[6]	reg_03[7]=1
IO_PIXEL[15]	pixel_data[15]	pixel_data[15] for TVE	default
	DAC_din[7]	bypass DAC_din[7]	reg_03[7]=1
IO_PIXEL[16]	pixel_data[16]	pixel_data[18] for TVE	default
	DAC_din[8]	bypass DAC_din[8]	reg_03[7]=1
IO_PIXEL[17]	pixel_data[17]	pixel_data[17] for TVE	default
	DAC_din[9]	bypass DAC_din[9]	reg_03[7]=1
IO_PIXEL[18]	pixel_data[18]	pixel_data[18] for TVE	default
	DAC_clkin	bypass DAC_clkin	reg_03[7]=1
IO_PIXEL[19]	pixel_data[19]	pixel_data[19] for TVE	default
	DAC_pd[0]	bypass DAC_pd	reg_03[7]=1

2.3.7 CODEC IO_MUX

The CODEC in RK1000 can be disable when setting "CODEC_CON[0]=1", In this case, external CODEC is used for Audio-CODEC solution.

IO_MUXs are inserted within the I2S intreface to disable the Internal CODEC. The I2C slave interface is also disabled.

The CODEC in RK1000 have DAC_FRM and ADC_FRM pins. if those two pins are double bonding, There are two output enable control bits from the control register (CODEC_CON[2]/CODEC_CON[3]).

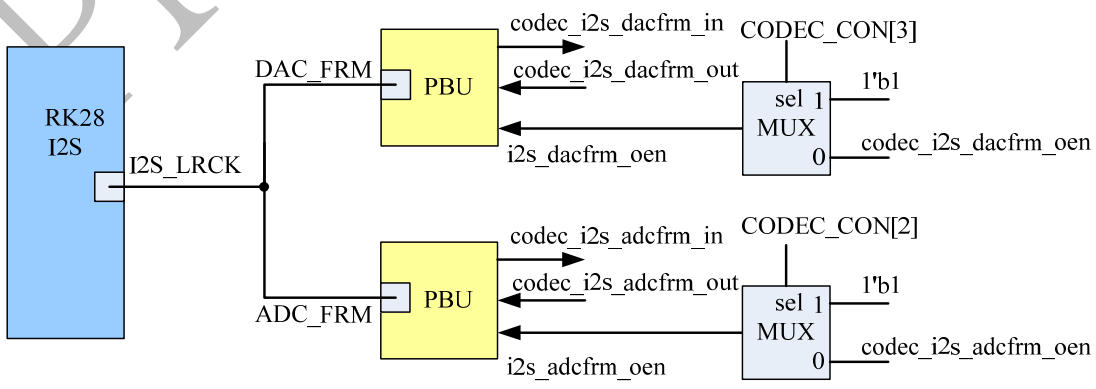


Fig. 2-6 I2SLRCK connection

2.3.8 Low power standby mode configuration

To turn RK1000 into low power standby mode,

1. Turn off the power of ADC by setting **ADC_CON to 8'hff**;
2. Bypass the RGB2CCIR601 module by setting **TVE_CON[0] to 1'b1**;
3. Turn off the power of V-DACs by setting **TVE_POWCR[2:0] to 3'b111**;
4. Bypass the internal CODEC by setting **CODEC_CON[0] to 1'b1.**

Chapter 3 RGB2CCIR601

3.1 Design Overview

3.1.1 Overview

The RGB2CCIR601 module is used to transfer RGB interface(progressive or interlace) to CCIR601 standard interface(interlace) for TV_ENCODER in mode of traditional TV-OUT(PAL/NTSC).

If the input LCD interface is CCIR656 or TV_OUT mode is 576p/480p/720p, RGB2CCIR601 module must be bypassed.

3.1.2 Features

- 27MHz input clock
- Input interface: LCD RGB Interface(720x576, 720x288, 720x480, 720x240)
- Input Data format: RGB888, RGB666, RGB565, YUV444
- Progressive to Intrelace display transfer
- Interlace to Intrelace display transfer
- Output ITU-BT601, PAL/NTSC standard

3.2 Architecture

This section provides a description about the functions and behavior under various conditions

3.2.1 Overview

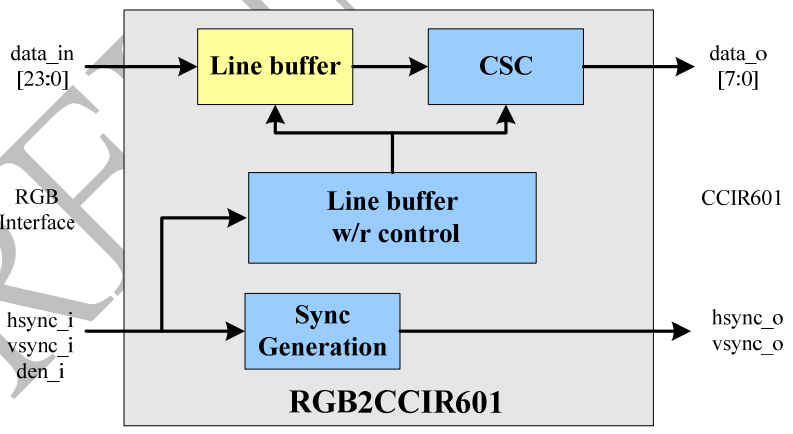


Fig. 3-1 RGB2CCIR601 diagram

3.3 Registers

The registers of RGB2CCIR601 is the register TVE_CON[5:0 in Control Rrgister module(chapter 2).

TVE_CON(Control Register)
Address: I2C reg addr (0x02)
TV_ENCODER and rgb2ccir601 control register

bit	Attr	Reset Value	Description
7	R/W	0X0	V-DAC channel R bypass 0: Disable 1: Enable
6	R/W	0X0	TVE cvbs 3 channel output enable 0: Disable 1: Enable
5:4	R/W	0X0	rgb2ccir601 input data format 00: RGB888 01: RGB666 10: RGB565 11: YUV bypass
3	R/W	0X0	rgb2ccir601 RGB data RB swap 0: RGB 1: BGR
2	R/W	0X0	rgb2ccir601 input video format 0: Progressive 1: Interlace
1	R/W	0X0	rgb2ccir601 TV format 0: PAL(625 line) 1: NTSC(525 line)
0	R/W	0X0	rgb2ccir601 enable 0: rgb2ccir601 bypass 1: rgb2ccir601 enable

Notes: Attr: **RW** – Read/writable, **R** – read only, **W** – write only

3.4 Functional Description

3.4.1 Input data format

Table 3-1 RGB2CCIR601 input data format

TVE_CON[5:4]	TVE_CON[3]	Input data format
2'b00	1'b0	RGB888: {R[23:16], G[15:8], B[7:0]}
2'b01	1'b0	RGB666: {6'b0, R[17:12], G[11:6], B[5:0]}
2'b10	1'b0	RGB565: {8'b0, R[15:11], G[10:5], B[4:0]}
2'b11	1'b0	YUV444: {U[23:16], Y[15:8], V[7:0]}
2'b00	1'b1	BGR888: {B[23:16], G[15:8], R[7:0]}
2'b01	1'b1	BGR666: {6'b0, B[17:12], G[11:6], R[5:0]}
2'b10	1'b1	BGR565: {8'b0, B[15:11], G[10:5], R[4:0]}
2'b11	1'b1	YUV444: {V[23:16], Y[15:8], U[7:0]}

3.4.2 Progressive to Interlace transfer

RGB2CCIR601 support progressive(RGB interface) to interlace(ITU_BT601) video stream transfer.

In PAL mode, 720x576p RGB interface video is transferred to 720x576i(720x288) ITU-BT601 digital interface video.

In NTSC mode, 720x480p RGB interface video is transferred to 720x480i(720x240) ITU-BT601 digital interface video.

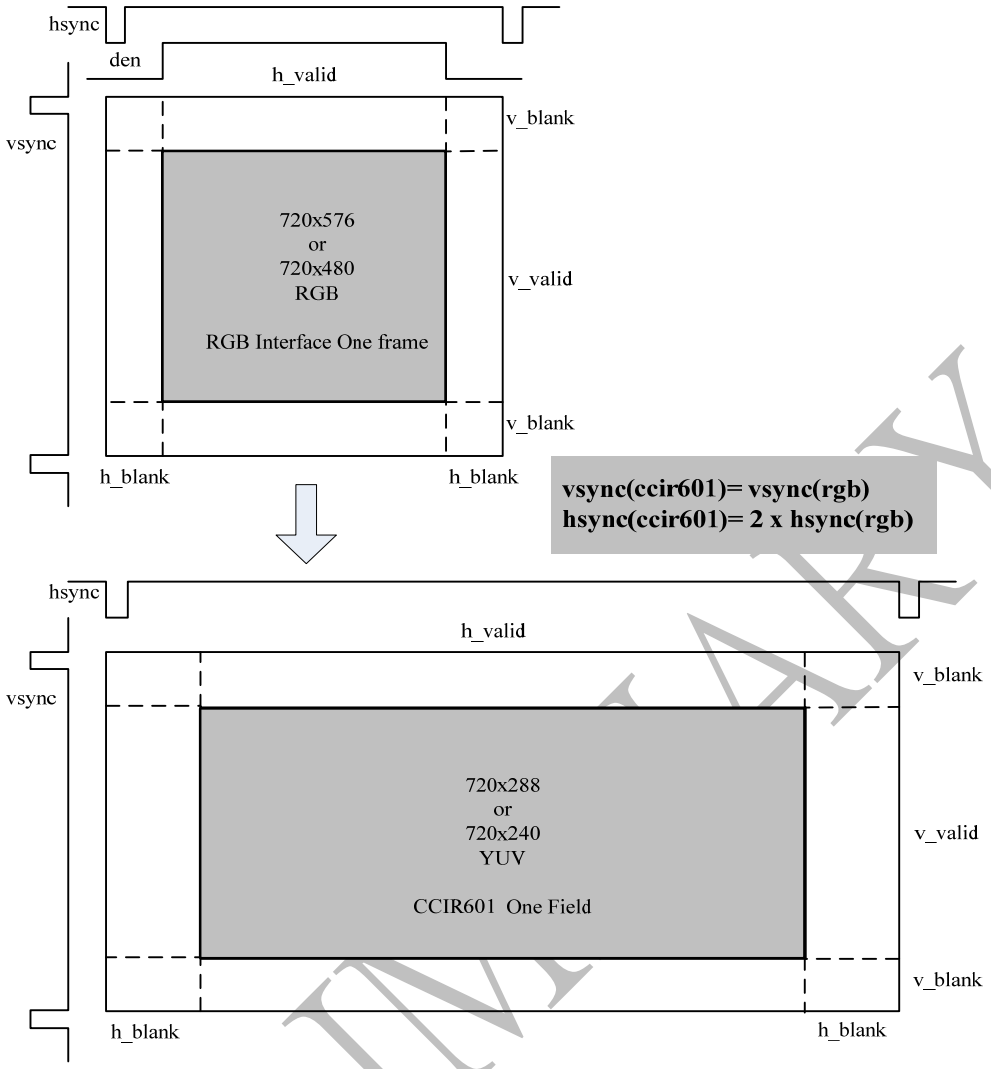


Fig. 3-2 RGB2CCIR601 P to I transfer

Timing	PAL	NTSC
V_TOTAL	625	525
V_BP	43	31
V_FP	6	14
V_PULSE	6	6
H_TOTAL	864	858
H_BP	132	122
H_FP	12	16
H_PULSE	6	6

Table 3-2 RGB Interface Timing Setting(P to I)

3.4.3 Interlace to Interlace transfer

RGB2CCIR601 support interlace(RGB interface) to interlace(ITU_BT601) video stream transfer.

In PAL mode, 720x288 RGB interface video is transferred to 720x576i(720x288) ITU-BT601 digital interface video.

In NTSC mode, 720x240 RGB interface video is transferred to 720x480i(720x240) ITU-BT601 digital interface video.

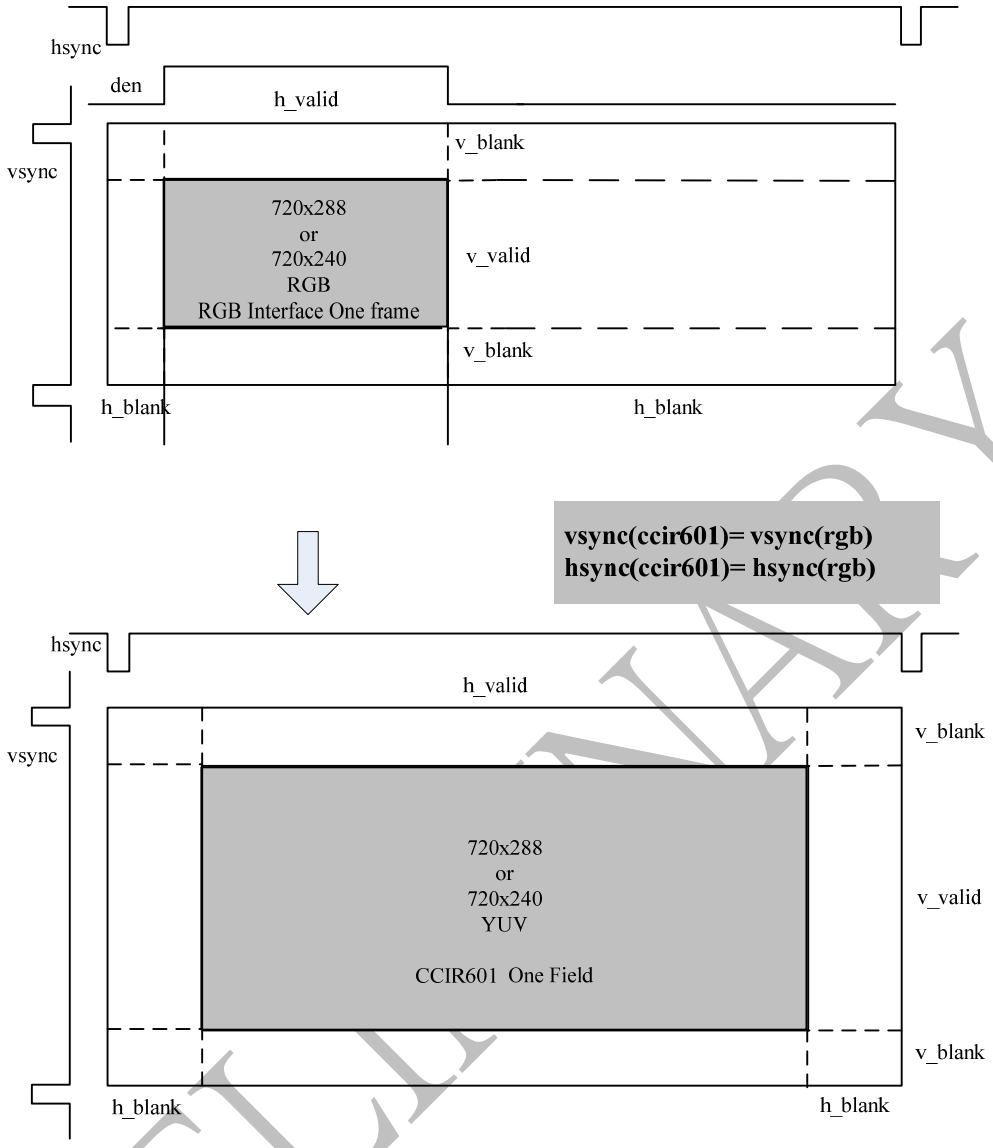


Fig. 3-3 RGB2CCIR601 I to I transfer

Timing	PAL	NTSC
V_TOTAL	312	262
V_BP	21	15
V_FP	3	7
V_PULSE	6	6
H_TOTAL	1728	1716
H_BP	132	122
H_FP	876	874
H_PULSE	6	6

Table 3-3 RGB Interface Timing Setting(I to I)

There is a problem to define the field polarity when the Interlace to Interlace transfer is running. So a soft reset function is added to reset RGB2CCIR601 module.

When RGB2CCIR601 is working and it's mode is turn to "I to I" mode, soft reset of RGB2CCIR601 and TV_ENCODER must be done(with in one frame) to make sure that the first display field is odd-field.

The soft reset of RGB2CCIR601 is writing "1" to the SRESET[0] in Control Register.

Chapter 4 TV ENCODER

4.1 Design Overview

4.1.1 Overview

TV_ENCODER is an digital video encoder. It converts digital ITU-R BT601/656 YCbCr 4:2:2video format to Composite, Y/C (S-video) and Component YUV digital video output. Video output can be programmedto be compatible with NTSC-M, NTSC-J, PAL-B,D,G,H,I,M,N and Combination N systems.

TV_ENCODER also can convert digital parallel RGB interface video to Component YcbCr SDTV/HDTV digital video output(480p/576p/720p). There are two RGB2YcbCr color space converters for ITU_BT601 and ITU_BT709.

TV_ENCODER requires a single 27 MHz(PAL/NTSC/480p/576p) or 74.25MHz(720p) clock input to support all types of video formats. A high-speed I2C compatible control interface is provided.

4.1.2 Features

COMMON:

- High-speed I2C-bus control interface
- Power-down mode for individual external video DACs

PAL/NTSC TV-OUT:

- Provide Composite, Y/C (S-video), Component YUV digital video outputs
- NTSC-M, NTSC-J, PAL-B, D, G, H, I, M, N and Combination N encoding
- Support standard ITU-R BT601 master/slave , ITU-R BT656 YCbCr 4:2:2 video input formats(NTSC/PAL)
- Programmable HSYNC and VSYNC polarity
- Support master or slave video input operation modes
- 2X over-sampling rate to improve video quality
- On-chip color-bar generator
- Single 27 MHz clock input

480p/576p/720p TV-OUT:

- Composite YCBCr digital video outputs
- 480p/576p/720p DTV encoding
- Support parallel RGB interface(RGB888 and YUV444) input formats
- 27MHz (480p/576p) or 74.25MHz(720p) clock input
- 720p-50Hz/60Hz modes
- ITU_BT601/ITU_BT709 RGB2YcbCr transfer

4.2 Architecture

This section provides a description about the functions and behavior under various conditions

4.2.1 Overview

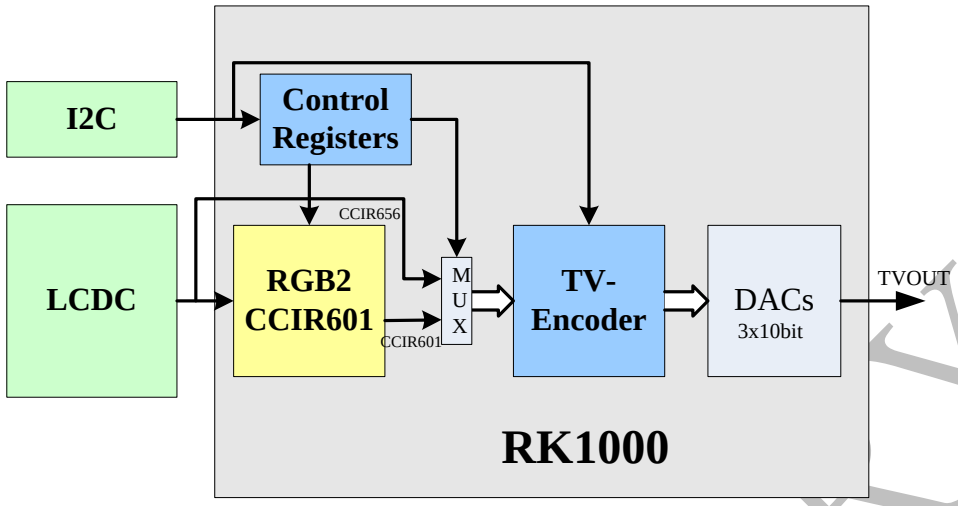


Fig. 4-1 TV_ENCODER in RK1000 diagram

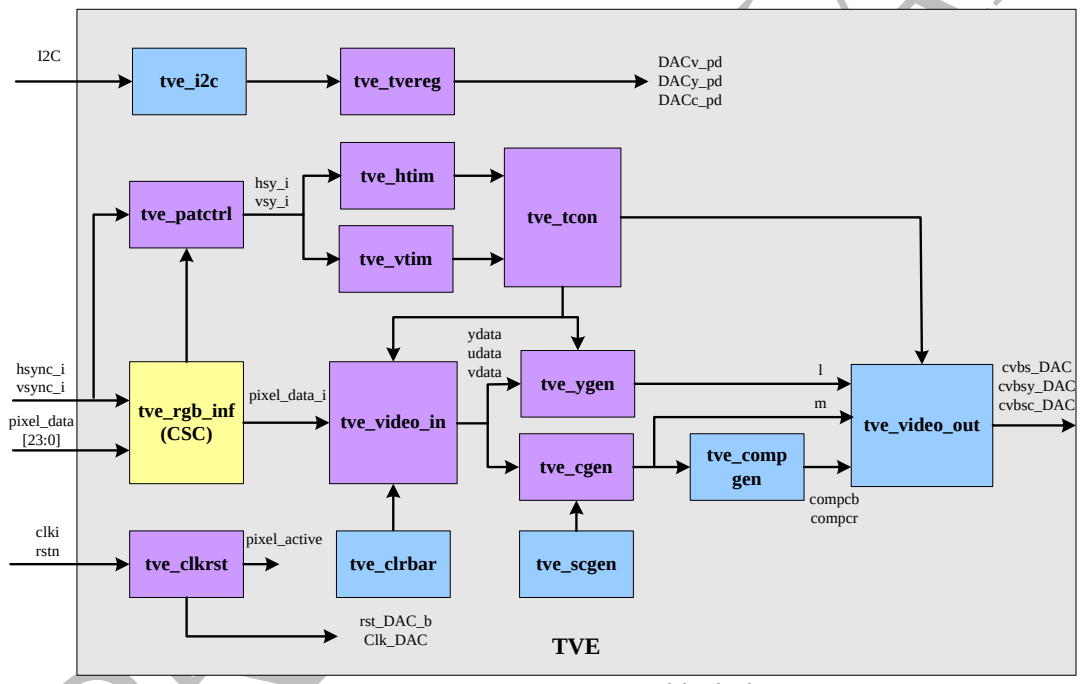


Fig. 4-2 TV_ENCODER block diagram

4.3 Registers

This section describes the control/status registers of the design.

4.3.1 Registers Summary

Name	Offset	Size	Access	Reset Value	Description
TVE_VFCR	0x00	B	R/W	0x00	Video Format Control Register
TVE_VINCR	0x01	B	R/W	0x00	Video Input Control Register
TVE_VOUTCR	0x02	B	R/W	0x00	Video Output Control

					Register
TVE_POWCR	0x03	B	R/W	0x00	Power Down Control Register
TVE_SRESET	0x04	B	R/W	0x00	Software Reset Control Register
TVE_HDTVCR	0x05	B	R/W	0x00	HDTV setting Register
TVE_YADJCR	0x06	B	R/W	0x00	HDTV Y adjustment Register
TVE_CBADJCR	0x07	B	R/W	0x00	HDTV Cb adjustment Register
TVE_CRADJCR	0x08	B	R/W	0x00	HDTV Cr adjustment Register
TVE_HVER	0x0f	B	R	0x01	Hardware Version Register

Notes:
Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access

4.3.2 Detail Register Description

TVE_VFCR
Address: reg_addr(0x00)
Video Format Control Register

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6]	R/W	0x0	**subc:**Subcarrier phase work mode 0: Reset the subcarrier phase to zero at the beginning of each field sequence. 1: Don't reset the subcarrier phase at the beginning of each field sequence.
[5:4]	-	0x0	Reserved
[3]	R/W	0x0	**vin_range:** Range of the video pixel input value 0: 16 to 235 for Y, 16 to 240 for Cb, Cr. 1: 1 to 254 for Y,Cb,Cr.
[2]	R/W	0x0	**Black0IRE:** Black level selection 0: Black level is 7.5 IRE above blanking level. 1: Black level is 0 IRE (Black level is same as blanking level).
[1:0]	R/W	0x0	**tvf[1:0]**: TV display format selection 00: NTSC-M, J (NTSC-M: black level = 7.5 IRE, NTSC-J: black level = 0 IRE). 01: PAL-M (black level = 7.5 IRE). 10:{ PAL-B, D, G, H, I, N (PAL-B, D, G, H, I: black level = 0 IRE, PAL-N: black level = 7.5 IRE). 11: PAL-NC (black level = 0 IRE).

TVE_VINCR
Address: reg_addr(0x01)
Video Input Control Register

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6:5]	R/W	0x0	**vin_d[1:0]:** Pixel data delay In video input BT601 slave mode (vinf[1:0] = 00), the first active pixel is sampled at the 245th or 265th clki

			rising edge for NTSC/PAL-M (525-line) or PAL (626-line) system respectively. vin_d is used to add delay to the duration between hsyncn_i and the first active pixel data. clki is 27 MHz. 00: Normal (no delay) 01: +1 clki cycle delay 10: +2 clki cycles delay 11: +3 clki cycles delay
[4]	R/W	0x0	**hs_p:** Polarity selection of hsyncn_i or hsyncn_o 0: hsyncn_i or hsyncn_o is falling edge active 1: hsyncn_i or hsyncn_o is rising edge active
[3]	R/W	0x0	**vs_p:** Polarity of vsyncn_i (or vsyncn_o) / FIELD 0: Low level of FIELD indicates odd fields and high level indicates even fields. (field_mode = FIELD function) vsyncn_i (or vsyncn_o) is falling edge active. (field_mode = VSYNC function) 1: High level of FIELD indicates odd fields, and low level indicates even fields. (field_mode = FIELD function) vsyncn_i (or vsyncn_o) is rising edge active. (field_mode = VSYNC function)
[2:1]	R/W	0x0	**vinf[1:0]:** Video input mode selection 00: BT601 slave mode: hsyncn_i + vsyncn_i (VSYNC/FIELD) based synchronization. 01: BT656 mode: ITU-R BT.656 format. In this mode, FTTVE100_S drives hsyncn_o and vsyncn_o (VSYNC/FIELD) output. 10: BT601 master mode: hsyncn_o + vsyncn_o (VSYNC/FIELD) based synchronization. 11: Internal 100% color bar pattern ("field_mode" should be set to "0").
[0]	R/W	0x0	**field_mode:** Select function of vsyncn_i or vsyncn_o signal 0: VSYNC function. 1: FIELD function.

TVE_VOUTCR
Address: reg_addr(0x02)
Video Output Control Register

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6]	R/W	0x0	**vof:** Output format 0: CVBS (composite) and S-video output simultaneously. 1: Component YCbCr output.
[5]	R/W	0x0	**blue:** Enable blue color output. It is used to display blue screen while there is no video input signal. 0: Normal video output 1: Blue output in all output modes.
[4]	R/W	0x0	**black:** Enable black output 0: Normal video output 1: Black output in all output modes.

[3]	R/W	0x0	**no_c:** Disable color signal 0: Normal video output 1: Color signal is disabled on CVBS output. S-video or component output is normal.
[2:0]	R/W	0x0	**y_d[2:0]:** Luma relative to chroma timing on the CVBS (composite) output. clki is 27 MHz. 000: Normal output (no delay) 001: +2 clki cycles delay 010: +4 clki cycles delay 011: +6 clki cycles delay 100: (reserved) 101: +2 clki cycles precedence 110: +4 clki cycles precedence 111: +6 clki cycles precedence

TVE_POWCR
Address: reg_addr(0x03)
Power Down Control Register

bit	Attr	Reset Value	Description
[7:5]	-	0x0	Reserved
[4]	R/W	0x0	**clki_p:** Setting this bit to logical "1" will reverse the phase of clock input clki. It is useful while the setup or hold time between clki and video input signals, including vsync, hsync, and pixel_data, is not enough. 0: The phase of internal clock is same as clki. 1: The phase of internal clock is the inverse of clki.
[3]	R/W	0x0	**DAC_clk_p:** Setting this bit to logical "0" will reverse the phase of clock output clk_DAC. It is useful while the setup or hold time between clk_DAC and video output signals is not enough. 0: The phase of clk_DAC is the inverse of internal clock. 1: The phase of clk_DAC is same as internal clock.
[2]	R/W	0x0	**DACv_pd:** Power-down the CVBS output DAC 0: Normal operation. 1: Power down the CVBS output DAC.
[1]	R/W	0x0	**DACy_pd:** Power-down the Y output DAC 0: Normal operation. 1: Power down the luminance (Y) output DAC.
[0]	R/W	0x0	**DACc_pd:** Power-down the C output DAC 0: Normal operation. 1: Power down the chrominance (C) output DAC.

TVE_SRESET
Address: reg_addr(0x04)
Software Reset Control Register

bit	Attr	Reset Value	Description
[7:1]	-	0x0	Reserved
[0]	W	0x0	**sreset:** Software reset. It will reset all registers to default reset values. 0: No reset. 1: Software reset. Writing "1" to this bit enables the

			software reset function and this bit will automatically reset to "0". It is not necessary to write "0" to disable "sreset".

TVE_HDTVCR
Address: reg_addr(0x05)
HDTV setting Register

bit	Attr	Reset Value	Description
[7:5]	-	0x0	Reserved
[4]	R/W	0x0	RGB2 YcbCr convertion mode 0: REC 601 1: REC 709
[3]	R/W	0x0	Input data format 0: RGB 1: UYV
[2]	R/W	0x0	720p mode 0: 50Hz 1: 60Hz
[1:0]	R/W	0x0	TV mode: 00: intrelace(PAL/NTSC) 01: 576p 10: 480p 11: 720p

TVE_YADJCR
Address: reg_addr(0x06)
HDTV Y adjustment Register

bit	Attr	Reset Value	Description
[7:5]	-	0x0	Reserved
[4:0]	R/W	0x10	Y adjustment control register Range: 48/64 ~ 79/64

TVE_CBADJCR
Address: reg_addr(0x07)
HDTV Cb adjustment Register

bit	Attr	Reset Value	Description
[7:5]	-	0x0	Reserved
[4:0]	R/W	0x10	Cb adjustment control register Range: 48/64 ~ 79/64

TVE_CRADJCR
Address: reg_addr(0x08)
HDTV Cr adjustment Register

bit	Attr	Reset Value	Description
[7:5]	-	0x0	Reserved
[4:0]	R/W	0x10	Cr adjustment control register Range: 48/64 ~ 79/64

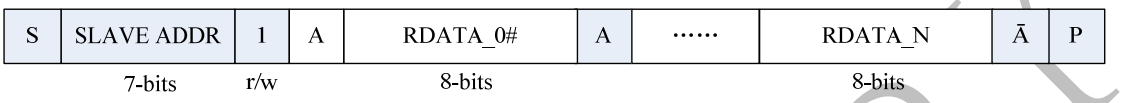
Notes:
Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access

4.4 Functional Description

4.4.1 I2C Write/Read

1. TVE I2C Writing

2. TVE I2C Reading



note : I2C slave addr = 7'h42.*

4.4.2 LCDC output timing requirememt

Table 4-1 RGB Interface HDTV Timing Setting

Timing	480P	576P	720P(50Hz)	720P(60Hz)
V_TOTAL	525	625	750	750
V_BP	42	44	25	25
V_FP	3	5	5	5
V_PULSE	5	5	5	5
H_TOTAL	858	864	1980	1650
H_BP	119	132	700	370
H_FP	19	12	0	0
H_PULSE	64	64	100	100

4.4.3 V-DACs connection

Table 4-2 TV-Encoder to V-Dacs connetion

Output Mode	V_DAC-R	V_DAC-G	V_DAC-B
Composite 0	cvbs	S video-Y	S video-C
Composite 1	cvbs	cvbs	cvbs
Component	Y	Cb	Cr

Chapter 5 Video-DAC

5.1 Design Overview

5.1.1 Overview

Video-DAC is a digital-to-analog converter for video and graph applications. There are three channels 10-bits DAC with embedded bandgap reference block. It can works up to 200MHz.

In RK1000, Video-DAC is used to a TV-DAC.

5.1.2 Features

- 10-bit 3-channel DA C
- Clock frequency: 200MHZ

5.2 Functional Description

5.4.1 DC Characteristics

Table 5-1 V-DAC DC Characteristics

(AVD33R=AVD33G=AVD33B=AVDD=3.3V; DVDD=1.8V; RL=37.5ohm, CL=10Pf; VERFIN=1.31V; Temp=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	AVD33R AVD33G AVD33B	2.97	3.3	3.63	V	
Operating voltage range	AVDD	2.97	3.3	3.63	V	
Operating voltage range	DVDD	1.62	1.8	1.98	V	
Max per channel output current	--	--	34.1	--	mA	
Max output voltage	--	--	1.278	--	V	
DAC resolution	--	--	10	--	bits	
Integral non-linearity error	INL	--	+/-1	+/-1.5	LSB	
Differential non-linearity error	DNL	--	+/-0.5	+/-1	LSB	

5.4.2 AC Characteristics

Table 5-2 V-DAC AC Characteristics

(AVD33R=AVD33G=AVD33B=AVDD=3.3V; DVDD=1.8V; RL=37.5ohm, CL=10Pf; VERFIN=1.31V; Temp=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
CK period	Tck	4.5	5	--	ns	
CK rise time	Tr	--	0.1	--	ns	
CK fall time	Tf	--	0.1	--	ns	
CK to Valid output	Tdelay	--	2.5	--	ns	
Output settling time	Tsettle	--	2.0	--	ns	

5.4.2 Application Information

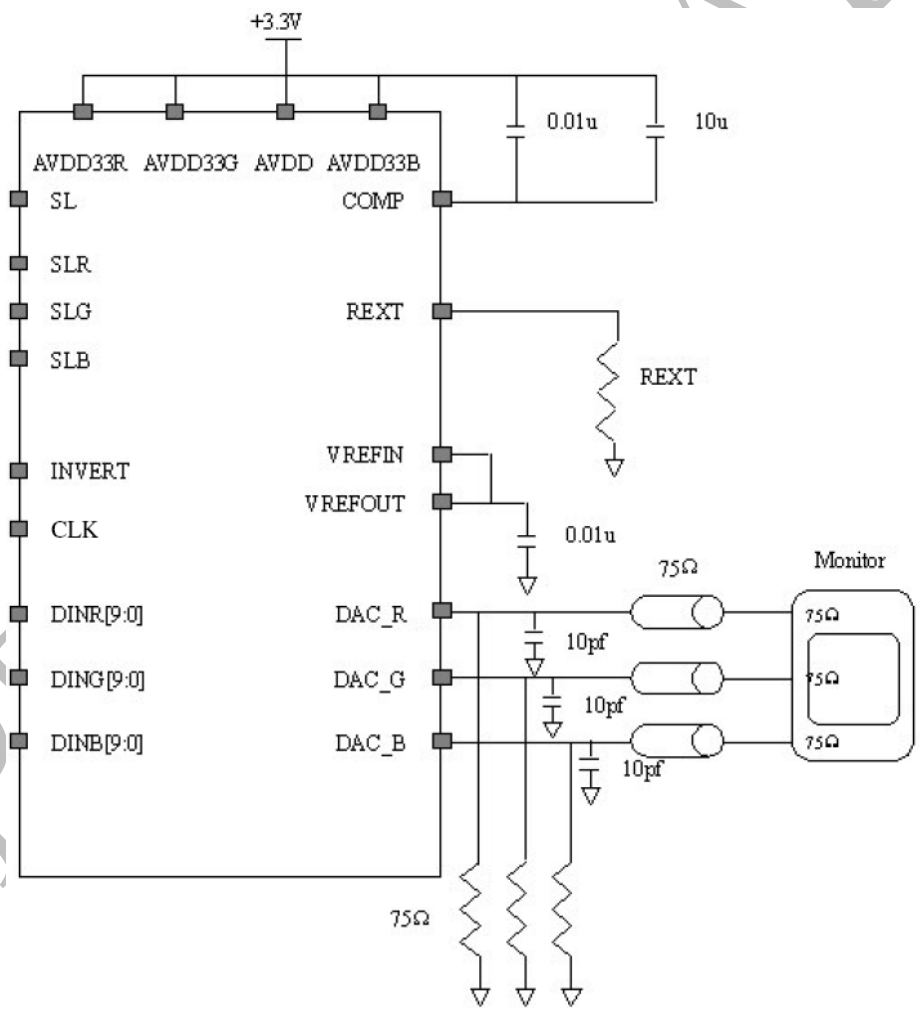


Fig. 5-1 V-DAC Application Diagram

Chapter 6 CODEC

6.1 Design Overview

6.1.1 Overview

The CODEC is a high audio quality, low power stereo CODEC IP that is well suitable for Portable Digital Audio Applications.

The device integrates interfaces to stereo/mono microphones and a stereo headphone. External component requirements are drastically reduced as no separate microphone or headphone amplifiers are required.

The CODEC can operate as a master or a slave, supporting various master clock frequencies including 12 or 24 MHz for USB devices, and standard 256fs rates (12.288 MHz, 24.576MHz, etc.). Various audio sample rates including 44.1 kHz, 48kHz, 96kHz are generated directly from the master clock. Advanced on-chip digital processing technique provides a prominent out-of-band noise suppression less than -80dBc.

The CODEC operates at the analog supply voltages down to 1.8~3.6 V, although the digital core can operate at voltages down to 1.8 V to save power. Additional power management control enables individual sections of the chip to be powered down under software control.

There is only one ADC in CODEC, the Line_in left and right channel are mixed before input to the ADC. So the Line in record only has one mixed-channel.

6.1.2 Features

- Complete Stero/Mon Microphone interfaceAHB slave interface
- ADC SNR 95dB('A' Weighted), THD -85dB at 48kHz, 3.3V
- DAC and On-chip Headphone Driver
  - >20mW output power on 32Ω/3.3V
  - THD+N at 20mW, SNR>95dB with 32Ω load
  - No DC blocking capacitors required(capless mode)
- Seperately mixed mono output
  - >20mW output power on 32Ω/3.3V
  - THD+N at 20mW, SNR>95dB with 32Ω load
  - No DC blocking capacitors required(capless mode)
- Seperately mixed mono output
- Low power consumption
  - 40mW stero playback static power(3.3V/1.5 supplies)
  - 20mW record& playback (1.8V/1.5 supplies)
- Low power supply
  - Analogue: 1.8V to 3.6V
  - Digital core: 1.7V to 1.9V
- 256 x Fs/384 x Fs Master clock rates, up to 24Mz

- Audio sample rates: 8 to 96kS/s
- Soft mute function at DAC path
- Less than -80dBc out-of-band Noise

6.2 Architecture

This section provides a description about the functions and behavior under various conditions.

6.2.1 Block Diagram

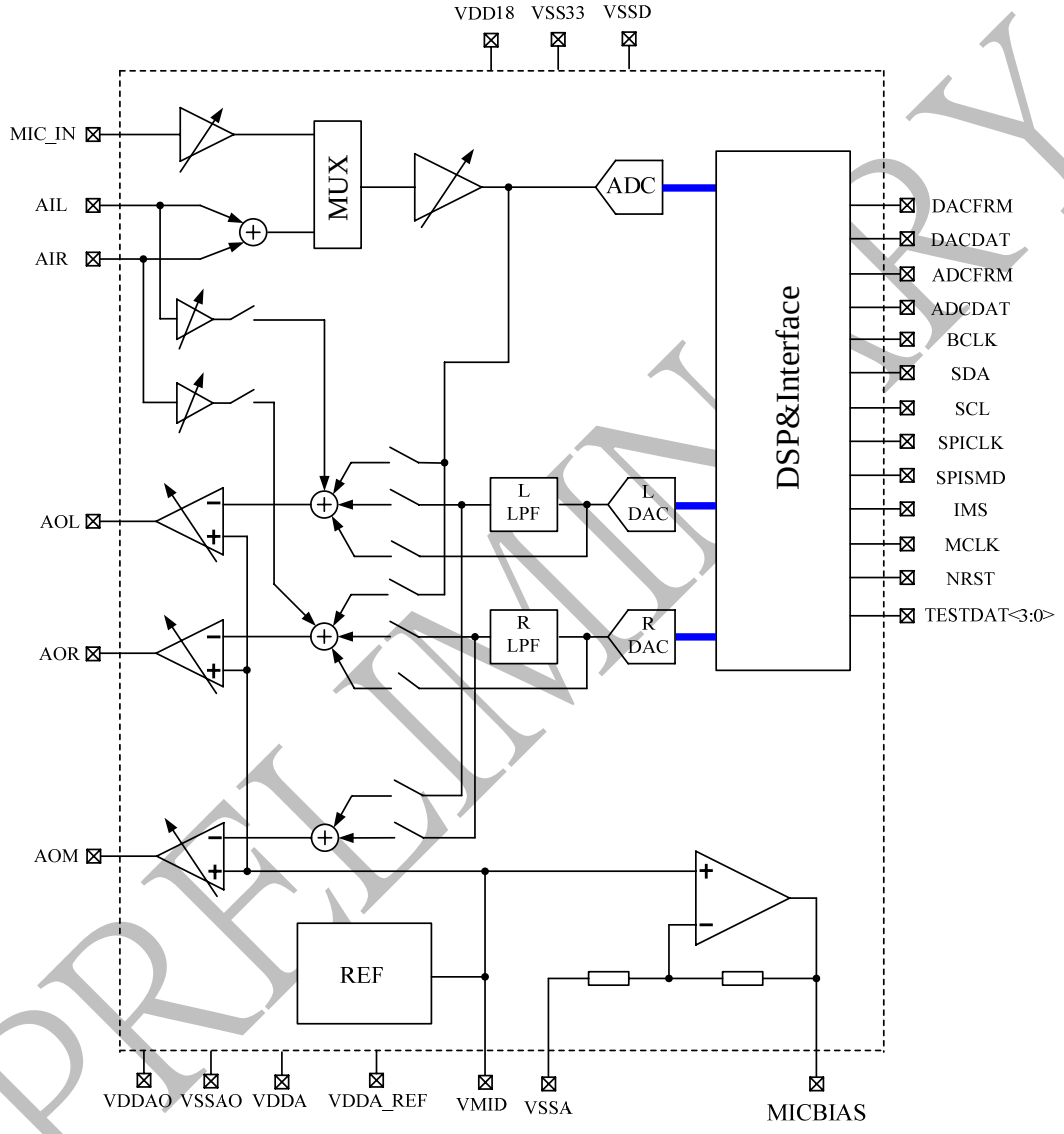


Fig. 6-1 CODEC Block Diagram

6.2.2 Pin Discription

Table 6-1 CODEC pin discription

PIN	NAME	TYPE	DESCRIPTION
1	DACFRM	BI	The frame signal of I2S DAC data
2	DACDAT	BI	The data signal of the I2S DAC data
3	ADCFRM	BI	The frame signal of the I2S ADC data
4	ADCDAT	BI	The data signal of the I2S ADC data

5	BCLK	BI	The synchronization clock of the I2S bus
6	SDA	BI	The I2C/SPI bus
7	SCL	DI	The input clock signal of the I2C/SPI bus
8	SPICLK	DI	The clock signal of the SPI bus
9	SPISMD	DO	The output data of the SPI bus
10	IMS	DI	The SPI/I2C selection bit
11	MCLK	DI	The system clock input
12	NRST	DI	The reset signal of the chip
13	VSSD	P	The digital power ground
14	TESTDAT<3>	BI	The test data
15	TESTDAT<2>	BI	The test data
16	TESTDAT<1>	BI	The test data
17	TESTDAT<0>	BI	The test data
18-23	NC		
24	AIL	AI	Left line input.
25	AIR	AI	Right line input.
26	MIC_IN	AI	Micphone input.
27	TP_MICB	AO	Micphone bias (value=0.65*vdd or 0.9*vdd)
28	VDDA_REF	AI	DAC reference decoupling node(value=vdd)
29	TP_VMID	AI	VMID reference decoupling node (value=vdd/2)
30	VSSA	P	The power ground for the CODEC analog part.
31	VDDA	P	The power supply for the CODEC analog part.
32	AOR	AO	Right Earphone amplifier output
33	VSSAO	P	PA power ground
34	AOM	AO	MONO Earphone amplifier output
35	VDDAO	P	PA power supply
36	AOL	AO	left Earphone amplifier output
37-44	NC		
45	VSSD	P	The power ground of the digital part
46	VDDD3	P	The power supply of the digital pad = 3.3 V
47	VDDD3	P	The power supply of the digital pad = 3.3 V
48	VDD18	P	The power supply of the digital core = 1.8 V

6.3 Registers

This section describes the registers of the design.

6.3.1 Registers Summary

Name	Offset	Size	Access	Reset Value	Description
CODEC_R00	0x00	B	R/W	0x05	
CODEC_R01	0x01	B	R/W	0x04	
CODEC_R02	0x02	B	R/W	0xfd	
CODEC_R03	0x03	B	R/W	0xf3	
CODEC_R04	0x04	B	R/W	0x03	
CODEC_R05	0x05	B	R/W	0x00	
CODEC_R06	0x06	B	R/W	0x00	

CODEC_R07	0x07	B	R/W	0x00	
CODEC_R08	0x08	B	R/W	0x00	
CODEC_R09	0x09	B	R/W	0x05	
CODEC_R0a	0x0a	B	R/W	0x00	
CODEC_R0b	0x0b	B	R/W	0x00	
CODEC_R0c	0x0c	B	R/W	0x97	
CODEC_R0d	0x0d	B	R/W	0x97	
CODEC_R0e	0x0e	B	R/W	0x97	
CODEC_R0f	0x0f	B	R/W	0x97	
CODEC_R10	0x10	B	R/W	0x97	
CODEC_R11	0x11	B	R/W	0x97	
CODEC_R12	0x12	B	R/W	0xcc	
CODEC_R13	0x13	B	R/W	0x00	
CODEC_R14	0x14	B	R/W	0x00	
CODEC_R15	0x15	B	R/W	0xf1	
CODEC_R16	0x16	B	R/W	0x90	
CODEC_R17	0x17	B	R/W	0xff	
CODEC_R18	0x18	B	R/W	0xff	
CODEC_R19	0x19	B	R/W	0xff	
CODEC_R1a	0x1a	B	R/W	0x9c	
CODEC_R1b	0x1b	B	R/W	0x00	
CODEC_R1c	0x1c	B	R/W	0x00	
CODEC_R1d	0x1d	B	R/W	0xff	
CODEC_R1e	0x1e	B	R/W	0xff	
CODEC_R1f	0x1f	B	R/W	0xff	

Notes:
Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access

6.3.2 Detail Register Description

CODEC_R00
Address: reg_addr(0x00)
CODEC Register 00

bit	Attr	Reset Value	Description
[7:6]	-	0x0	Reserved
[5:4]	R/W	0x0	BCM bits
[3]	R/W	0x0	DITHER_EN: Digital DSM dither enable. 0: disabled 1: enabled
[2]	R/W	0x1	SCRAMBLE_EN: Digital DSM out DEM module enable. 0: disabled 1: enabled
[1]	R/W	0x0	DSM_MODE: Digital DSM output filter select. 1: 1+z^(-3) 0: 1+z^(-1)
[0]	R/W	0x1	HPF_EN: Digital ADC high pass filter enable. 0: disabled 1: enabled

CODEC_R01
Address: reg_addr(0x01)
CODEC Register 01

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6:0]	R/W	0x04	DITHER power [22:16]

CODEC_R02
Address: reg_addr(0x02)
CODEC Register 02

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6:0]	R/W	0xfd	DITHER power [15:8]

CODEC_R03
Address: reg_addr(0x03)
CODEC Register 03

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6:0]	R/W	0xf3	DITHER power [7:0]

CODEC_R04
Address: reg_addr(0x04)
CODEC Register 04

bit	Attr	Reset Value	Description
[7:5]	R/W	0x0	SDTG_R[2:0] The gain control of the right side tone.
[4:2]	R/W	0x0	SDTG_L[2:0] The gain control of the left side tone.
[1]	R/W	0x0	INT_MUTE_R: Right interpolate filter mute enable. 0: not muted 1: muted
[0]	R/W	0x0	INT_MUTE_L: Left interpolate filter mute enable. 0: not muted 1: muted

CODEC_R05
Address: reg_addr(0x05)
CODEC Register 05

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved
[6:0]	R/W	0x00	INT_VOL_R[11:8] Right interpolate filter volume control.

CODEC_R06
Address: reg_addr(0x06)
CODEC Register 06

bit	Attr	Reset Value	Description
[7:0]	R/W	0x00	INT_VOL_R[7:0] Right interpolate filter volume control.

CODEC_R07
Address: reg_addr(0x07)
CODEC Register 07

bit	Attr	Reset Value	Description
[7]	-	0x0	Reserved

[6:0]	R/W	0x00	INT_VOL_L[11:8] Left interpolate filter volume control.

CODEC_R08
Address: reg_addr(0x08)
CODEC Register 08

bit	Attr	Reset Value	Description
[7:0]	R/W	0x00	INT_VOL_L[7:0] Left interpolate filter volume control.

CODEC_R09
Address: reg_addr(0x09)
CODEC Register 09

bit	Attr	Reset Value	Description
[7]	R/W	0x0	BCLKINV: BCLK inverted 0=not inverted 1=inverted
[6]	R/W	0x0	DCI_MS: Master mode enable. 0: disabled 1: enabled
[5]	R/W	0x0	LRSWAP: Slave mode enable. 0: output as normal 1: as slave mode
[4]	R/W	0x0	LRP Right, Left and I2S modes – LRCLK 0: normal polarity 1: invert polarity
			DSP Mode – mode A/B select 0: MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1: MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
[3:2]	R/W	0x2	DCI_WL[1:0]: Audio Data Word Length 11:32 bits 10:24 bits 01:20 bits 00:16 bits
[1:0]	R/W	0x1	FORMAT[1:0]: Audio Data Format Select 11: DSP Mode 10: I2S Format 01: Left justified 00: Right justified

CODEC_R0a
Address: reg_addr(0x0a)
CODEC Register 0a

bit	Attr	Reset Value	Description
[7]	R/W	0x0	CLK_EN: Codec CLK enable. 0: disabled 1: enabled
[6]	R/W	0x0	CLKDIV2: Master Clock Divide by 2 0: not divided 1: divided
[5:1]	R/W	0x0	CLK_SR[4:0]:

			Sample Rate Control
[0]	R/W	0x0	CLK_USB : Clocking Mode Select 0: Normal Mode 1: USB Mode

CODEC_R0b
Address: reg_addr(0x0b)
CODEC Register 0b

bit	Attr	Reset Value	Description
[7:3]	R/W	0x0	Test_mode [4:0]: Change digital in/out for test.
[2]	R/W	0x0	Test_res_mod: tst_res_pin [23:0] for analog test enable. (when enabled, DITHER_POW[22:0] has no use).
[1]	R/W	0x0	EN_INT: Interpolate filter and digital SDM enable. 0: disabled 1: enabled
[0]	R/W	0x0	EN_DEC: Decimation filter enable. 0: disabled 1: enabled

CODEC_R0c
Address: reg_addr(0x0c)
CODEC Register 0c

bit	Attr	Reset Value	Description
[7]	R/W	0x1	LINMUTE: PGA gain stage mute 0: not muted 1: muted
[6:4]	R/W	0x1	No use
[3:0]	R/W	0x7	LINVOL[3:0]: Left line input volume control 0000:0dB… 1.5dB/step… 1111:22.5dB

CODEC_R0d
Address: reg_addr(0x0d)
CODEC Register 0d

bit	Attr	Reset Value	Description
[7]	R/W	0x1	LIPMUTE: PGA gain stage mute 0: not muted 1: muted
[6:4]	R/W	0x1	No use
[3:0]	R/W	0x7	LIRVOL[3:0]: Right line input volume control 0000:0dB… 1.5dB/step… 1111:22.5dB

CODEC_R0e
Address: reg_addr(0x0e)
CODEC Register 0e

bit	Attr	Reset Value	Description

[7]	R/W	0x1	ALMUTE: microphone input mute 0: not muted 1: muted
[6:4]	R/W	0x1	No use
[3:0]	R/W	0x7	ALVOL[3:0]: microphone input volume control 0000:0dB… 1.5dB/step… 1111:22.5dB

CODEC_R0f
Address: reg_addr(0x0f)
CODEC Register 0f

bit	Attr	Reset Value	Description
[7:0]	R/W	0x97	No use

CODEC_R10
Address: reg_addr(0x10)
CODEC Register 10

bit	Attr	Reset Value	Description
[7:0]	R/W	0x97	No use

CODEC_R11
Address: reg_addr(0x11)
CODEC Register 11

bit	Attr	Reset Value	Description
[7:0]	R/W	0x97	No use

CODEC_R12
Address: reg_addr(0x12)
CODEC Register 12

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Microphone input/Line input select 0: line input 1: microphone input
[6]	R/W	0x1	No use
[5]	R/W	0x0	Microphone input amplitude boost. 0: 0dB 1: 20dB
[4]	R/W	0x0	No use
[3]	R/W	0x1	No use
[2]	R/W	0x1	No use
[1:0]	R/W	0x00	No use

CODEC_R13
Address: reg_addr(0x13)
CODEC Register 13

bit	Attr	Reset Value	Description
[7]	R/W	0x0	Left line input→ left mixer enable. 0: disabled 1: enabled
[6:4]	R/W	0x0	Left line input→ left mixer volume control.

			000:-15 dB… 3dB/step… 111:6dB
[3]	R/W	0x0	PGA output → left mixer enable. 0=disabled 1=enabled
[2:0]	R/W	0x0	PGA output→ left mixer volume control. 000:-15 dB… 3dB/step… 111:6dB

CODEC_R14
Address: reg_addr(0x14)
CODEC Register 14

bit	Attr	Reset Value	Description
[7]	R/W	0x0	Right line input→ left mixer enable. 0: disabled 1: enabled
[6:4]	R/W	0x0	Right line input→ left mixer volume control. 000:-15 dB… 3dB/step… 111:6dB
[3]	R/W	0x0	PGA output → Right mixer enable. 0=disabled 1=enabled
[2:0]	R/W	0x0	PGA output→ Right mixer volume control. 000:-15 dB… 3dB/step… 111:6dB

CODEC_R15
Address: reg_addr(0x15)
CODEC Register 15

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Right channel LPF → right mixer enable. 0: disabled 1: enabled
[6]	R/W	0x1	Left channel LPF→ left mixer enable. 0: disabled 1: enabled
[5]	R/W	0x1	Right channel LPF mute. 0: not muted 1: muted
[4]	R/W	0x1	Left channel LPF mute. 0: not muted 1: muted
[3]	R/W	0x0	Right channel DAC differential output →right mixer enable.

			0: disabled 1: enabled
[2]	R/W	0x0	Left channel DAC differential output →Left mixer enable. 0: disabled 1: enabled
[1:0]	R/W	0x1	No use

CODEC_R16
Address: reg_addr(0x16)
CODEC Register 16

bit	Attr	Reset Value	Description
[7:0]	R/W	0xf1	SCF_CTL:The control bits of the SCF DAC.

CODEC_R17
Address: reg_addr(0x17)
CODEC Register 17

bit	Attr	Reset Value	Description
[7]	R/W	0x1	left channel PA cross-zero volume update enable. 0: disabled 1: enabled
[6]	R/W	0x1	Left channel PA mute. 0: not muted 1: muted
[5:0]	R/W	0x1f	Left channel PA gain. 000000:6dB… -0.4dB/step… 111111:-60dB

CODEC_R18
Address: reg_addr(0x18)
CODEC Register 18

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Right channel PA cross-zero volume update enable. 0: disabled 1: enabled
[6]	R/W	0x1	Right channel PA mute. 0: not muted 1: muted
[5:0]	R/W	0x1f	Right channel PA gain. 000000:6dB… -0.4dB/step… 111111:-60dB

CODEC_R19
Address: reg_addr(0x19)
CODEC Register 19

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Mono channel PA cross-zero volume update enable. 0: disabled 1: enabled
[6]	R/W	0x1	Mono channel PA mute. 0: not muted

			1: muted
[5:0]	R/W	0x1f	Mono channel PA gain. 000000:6dB… -0.4dB/step… 111111:-60dB

CODEC_R1a
Address: reg_addr(0x1a)
CODEC Register 1a

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Cap-less connection support. 0: disabled 1: enabled
[6]	R/W	0x0	Right channel LPF→ Mono PA enable. 0: disabled 1: enabled
[5]	R/W	0x0	Left channel LPF→ Mono PA enable. 0: disabled 1: enabled
[4]	R/W	0x1	MICBIAS voltage select. 1: 0.9*VDDA 0: 0.6*VDDA
[3:2]	R/W	0x3	VMID ramp up control. 00: Slowest 01: Slow 10: Fast 11: Fastest
[1:0]	R/W	0x0	No use

CODEC_R1b
Address: reg_addr(0x1b)
CODEC Register 1b

bit	Attr	Reset Value	Description
[7]	R/W	0x0	No use
[5:4]	R/W	0x0	Bias current select. 00: 6u 01: 8u 10: 12u 11: 4u
[3]	R/W	0x0	PGA bias current control. When '1', bias current halved.
[2]	R/W	0x0	No use
[1:0]	R/W	0x0	Mixer bias current select. 00: default 01: +20% 10: +40% 11:-20%

CODEC_R1c
Address: reg_addr(0x1c)
CODEC Register 1c

bit	Attr	Reset Value	Description

[7]	R/W	0x0	ASDM DEM enable. 0: disabled 1: enabled
[6]	R/W	0x0	Not use
[5]	R/W	0x0	ADSM dither enable. 0: disabled 1: enabled
[4:3]	R/W	0x0	The amplitude setting of the ASDM dither. (div=vdd/48) 00: div 01: 2*div 10: 4*div 11: 8*div
[2:0]	R/W	0x0	Not use

CODEC_R1d
Address: reg_addr(0x1d)
CODEC Register 1d

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Reference power down(PD). 0: not PD 1: PD
[6]	R/W	0x1	PGA PD. 0: not PD 1: PD
[5]	R/W	0x1	No use
[4]	R/W	0x1	Micphone input Op-Amp PD. 0: not PD 1: PD
[3]	R/W	0x1	No use
[2]	R/W	0x1	PGA buffer PD. 0: not PD 1: PD
[1]	R/W	0x1	No use
[0]	R/W	0x1	VMID generator PD. 0: not PD 1: PD

CODEC_R1e
Address: reg_addr(0x1e)
CODEC Register 1e

bit	Attr	Reset Value	Description
[7]	R/W	0x1	ASDM PD 0: not PD 1: PD
[6]	R/W	0x1	No use
[5]	R/W	0x1	Left channel LPF PD. 0: not PD 1: PD
[4]	R/W	0x1	Right channel LPF PD. 0: not PD 1: PD
[3]	R/W	0x1	Left channel Mixer PD. 0: not PD

			1: PD
[2]	R/W	0x1	Right channel Mixer PD. 0: not PD 1: PD
[1]	R/W	0x1	Left channel PA PD. 0: not PD 1: PD
[0]	R/W	0x1	Right channel PA PD. 0: not PD 1: PD

CODEC_R1f
Address: reg_addr(0x1f)
CODEC Register 1f

bit	Attr	Reset Value	Description
[7]	R/W	0x1	Mono PA PD 0: not PD 1: PD
[6]	R/W	0x1	Mono Mixer PD 0: not PD 1: PD
[5]	R/W	0x1	Left channel LPF PD. 0: not PD 1: PD
[4]	R/W	0x1	Micbias PD. 0: not PD 1: PD
[3]	R/W	0x1	Not use
[2]	R/W	0x1	Left channel DAC PD. 0: not PD 1: PD
[1]	R/W	0x1	Right channel DAC PD. 0: not PD 1: PD
[0]	R/W	0x1	Not use

Notes: Attr: **RW** – Read/writable, **R** – read only, **W** – write only

6.4 Functional Description

6.4.1 I2C Write/Read

1. CODEC I2C Writing

S	2'b11	REG ADDR	0	A	WDATA	A	P
	2-bits	5-bits	r/w		8-bits		

2. CODEC I2C Reading

S	2'b11	REG ADDR	1	A	RDATA	Ā	P
	2-bits	5-bits	r/w		8-bits		

6.4.2 Headphone Volume Control PA

Each headphone output drives a 32ohm headphone load and has an analogue volume control PGA with a gain range of -60dB to +6dB in 0.4dB steps.

Table 6-2 CODEC headphone volume control

VOL_PA[5:0]						Power	Output Power
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	(dBc)	(mW)
0	0	0	0	0	0	6	79.6
0	0	0	0	0	1	5.6	72.6
0	0	0	0	1	0	5.2	66.2
0	0	0	0	1	1	4.8	60.4
0	0	0	1	0	0	4.4	55.1
0	0	0	1	0	1	4	50.2
0	0	0	1	1	0	3.6	45.8
0	0	0	1	1	1	3.2	41.8
0	0	1	0	0	0	2.8	38.1
0	0	1	0	0	1	2.4	34.8
0	0	1	0	1	0	2	31.7
0	0	1	0	1	1	1.6	28.9
0	0	1	1	0	0	1.2	26.4
0	0	1	1	0	1	0.8	24
0	0	1	1	1	0	0.4	21.9
0	0	1	1	1	1	0	20
0	1	0	0	0	0	-0.4	18.2
0	1	0	0	0	1	-0.8	16.6
0	1	0	0	1	0	-1.2	15.2
0	1	0	0	1	1	-1.6	13.8
0	1	0	1	0	0	-2	12.6
0	1	0	1	0	1	-2.4	11.5
0	1	0	1	1	0	-2.8	10.5
0	1	0	1	1	1	-3.2	9.6
0	1	1	0	0	0	-3.6	8.7
0	1	1	0	0	1	-4	8
0	1	1	0	1	0	-4.4	7.3
0	1	1	0	1	1	-4.8	6.6
0	1	1	1	0	0	-5.2	6
0	1	1	1	0	1	-5.6	5.5
0	1	1	1	1	0	-6	5
0	1	1	1	1	1	-6.4	4.6
1	0	0	0	0	0	-6.8	4.2
1	0	0	0	0	1	-7.2	3.8
1	0	0	0	1	0	-7.6	3.5
1	0	0	0	1	1	-8	3.2
1	0	0	1	0	0	-8.4	2.9

1	0	0	1	0	1	-8.8	2.6
1	0	0	1	1	0	-9.2	2.4
1	0	0	1	1	1	-9.6	2.2
1	0	1	0	0	0	-10	2
1	0	1	0	0	1	-10.8	1.7
1	0	1	0	1	0	-11.6	1.4
1	0	1	0	1	1	-12.4	1.2
1	0	1	1	0	0	-13.2	1
1	0	1	1	0	1	-14	0.8
1	0	1	1	1	0	-14.8	0.7
1	0	1	1	1	1	-15.6	0.6
1	1	0	0	0	0	-16.4	0.5
1	1	0	0	0	1	-17.2	0.4
1	1	0	0	1	0	-18	0.3
1	1	0	0	1	1	-18.8	0.3
1	1	0	1	0	0	-19.6	0.2
1	1	0	1	0	1	-20.4	0.2
1	1	0	1	1	0	-23	0.1
1	1	0	1	1	1	-26	5.00E-02
1	1	1	0	0	0	-29	2.50E-02
1	1	1	0	0	1	-32	1.30E-02
1	1	1	0	1	0	-36	5.00E-03
1	1	1	0	1	1	-40	2.00E-03
1	1	1	1	0	0	-44	8.00E-04
1	1	1	1	0	1	-49	2.50E-04
1	1	1	1	1	0	-54	8.00E-05
1	1	1	1	1	1	-60	2.00E-05

6.4.3 Interpolation Filter Volume Control

Table 6-3 CODEC Interpolation Filter volume control

VOL_INT<11:0>	Gain Value	Time (Bclk)
000000000000	0	128*0
000000000001	1	128*1
…	…	…
…	…	…
111111111110	4094	128*4094
111111111111	4095	128*4095

6.4.3 Clocking Scheme

The CODEC has an integrated clock circuit that supports flexible clocking scheme as follows:

Table 6-4 CODEC Clocking Scheme

MCLK	MCLK	ADC SAMPLE RATE	DAC SAMPLE RATE	CLK_USB	CLK_SR	BCLK
CLKDIV2=0	CLKDIV2=1	(ADCLRC)	(DACLRC)			(MS=1)
'Normal' Clock Mode						
12.288 MHz	24.576 MHz	8 kHz (MCLK/1536)	8 kHz (MCLK/1536)	0	00110	MCLK/4
		8 kHz (MCLK/1536)	48 kHz (MCLK/256)	0	00100	MCLK/4
		12 kHz (MCLK/1024)	12 kHz (MCLK/1024)	0	01000	MCLK/4
		16 kHz (MCLK/768)	16 kHz (MCLK/768)	0	01010	MCLK/4
		24 kHz (MCLK/512)	24 kHz (MCLK/512)	0	11100	MCLK/4
		32 kHz (MCLK/384)	32 kHz (MCLK/384)	0	01100	MCLK/4
		48 kHz (MCLK/256)	8 kHz (MCLK/1536)	0	00010	MCLK/4
		48 kHz (MCLK/256)	48 kHz (MCLK/256)	0	00000	MCLK/4
		96 kHz (MCLK/128)	96 kHz (MCLK/128)	0	01110	MCLK/2
11.2896MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	8.0182 kHz (MCLK/1408)	0	10110	MCLK/4
		8.0182 kHz (MCLK/1408)	44.1 kHz (MCLK/256)	0	10100	MCLK/4
		11.025 kHz (MCLK/1024)	11.025 kHz (MCLK/1024)	0	11000	MCLK/4
		22.05 kHz (MCLK/512)	22.05 kHz (MCLK/512)	0	11010	MCLK/4
		44.1 kHz (MCLK/256)	8.0182 kHz (MCLK/1408)	0	10010	MCLK/4
		44.1 kHz (MCLK/256)	44.1 kHz (MCLK/256)	0	10000	MCLK/4
		88.2 kHz (MCLK/128)	88.2 kHz (MCLK/128)	0	11110	MCLK/2
18.432MHz	36.864MHz	8 kHz (MCLK/2304)	8 kHz (MCLK/2304)	0	00111	MCLK/6
		8 kHz (MCLK/2304)	48 kHz (MCLK/384)	0	00101	MCLK/6
		12 kHz (MCLK/1536)	12 kHz (MCLK/1536)	0	01001	MCLK/6

		16kHz (MCLK/1152)	16 kHz (MCLK/1152)	0	01011	MCLK/6
		24kHz (MCLK/768)	24 kHz (MCLK/768)	0	11101	MCLK/6
		32 kHz (MCLK/576)	32 kHz (MCLK/576)	0	01101	MCLK/6
		48 kHz (MCLK/384)	48 kHz (MCLK/384)	0	00001	MCLK/6
		48 kHz (MCLK/384)	8 kHz (MCLK/2304)	0	00011	MCLK/6
		96 kHz (MCLK/192)	96 kHz (MCLK/192)	0	01111	MCLK/3
16.9344MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	8.0182 kHz (MCLK/2112)	0	10111	MCLK/6
		8.0182 kHz (MCLK/2112)	44.1 kHz (MCLK/384)	0	10101	MCLK/6
		11.025 kHz (MCLK/1536)	11.025 kHz (MCLK/1536)	0	11001	MCLK/6
		22.05 kHz (MCLK/768)	22.05 kHz (MCLK/768)	0	11011	MCLK/6
		44.1 kHz (MCLK/384)	8.0182 kHz (MCLK/2112)	0	10011	MCLK/6
		44.1 kHz (MCLK/384)	44.1 kHz (MCLK/384)	0	10001	MCLK/6
		88.2 kHz (MCLK/192)	88.2 kHz (MCLK/192)	0	11111	MCLK/3
8.192MHz	16.384MHz	8kHz (MCLK/1024)	8kHz (MCLK/1024)	0		MCLK/4
		16kHz (MCLK/512)	16kHz (MCLK/512)	0		MCLK/4
		32kHz (MCLK/256)	32kHz (MCLK/256)	0		MCLK/4
		32kHz (MCLK/256)	8kHz (MCLK/1024)	0		MCLK/4
		8kHz (MCLK/1024)	32kHz (MCLK/256)	0		MCLK/4
USB Mode						
12.000MHz	24.000MHz	8 kHz (MCLK/1500)	8 kHz (MCLK/1500)	1	00110	MCLK
		8 kHz (MCLK/1500)	48 kHz (MCLK/250)	1	00100	MCLK
		8.0214 kHz (MCLK/1496)	8.0214kHz (MCLK/1496)	1	10111	MCLK
		8.0214 kHz (MCLK/1496)	44.118 kHz (MCLK/272)	1	10101	MCLK
		11.0259 kHz (MCLK/1088)	11.0259kHz (MCLK/1088)	1	11001	MCLK
		12 kHz (MCLK/1000)	12 kHz (MCLK/1000)	1	01000	MCLK

		16kHz (MCLK/750)	16kHz (MCLK/750)	1	01010	MCLK
		22.0588kHz (MCLK/544)	22.0588kHz (MCLK/544)	1	11011	MCLK
		24kHz (MCLK/500)	24kHz (MCLK/500)	1	11100	MCLK
		32 kHz (MCLK/375)	32 kHz (MCLK/375)	1	01100	MCLK
		44.118 kHz (MCLK/272)	8.0214kHz (MCLK/1496)	1	10011	MCLK
		44.118 kHz (MCLK/272)	44.118 kHz (MCLK/272)	1	10001	MCLK
		48 kHz (MCLK/250)	8 kHz (MCLK/1500)	1	00010	MCLK
		48 kHz (MCLK/250)	48 kHz (MCLK/250)	1	00000	MCLK
		88.235kHz (MCLK/136)	88.235kHz (MCLK/136)	1	11111	MCLK
		96 kHz (MCLK/125)	96 kHz (MCLK/125)	1	01110	MCLK

Chapter 7 HS-ADC

7.1 Design Overview

7.1.1 Overview

HS-ADC is 10-bit 1.8V analog to digital converter (ADC). It features a pipelined architecture and a wideband track and hold (T/H). This ADC is optimized for high dynamic performance applications in imaging and digital communications. The HS-ADC consumes 27 mA from a 1.8V power supply while delivering a 57dB Signal to Noise Ratio Plus Distortion ratio (SINAD) at 29 MHz input frequency when operating at a sampling rate of 60MHz. It has separate power downs for adc core and reference buffers. The power consumption scales roughly linearly with operating frequency with minimum operating frequency of 10MHz and maximum operating frequency of 60MHz.

There are two HS-ADCs in RK1000 with the same input clock.

7.1.2 Features

- Sampling Rate: 10~60Msps
- Input: differential, 1.8 V peak-to-peak differential
- Power Dissipation: 12~60 mW (typical)
- Dynamic Performance: 60 dB SFDR and 57 dB SINAD
- Linearity: <1.5 LSB INL
  <1 LSB DNL, no missing codes
- User-Programmable Bias Current of Pipelined Stages

7.2 Architecture

This section provides a description about the functions and behavior under various conditions.

7.2.1 Block Diagram

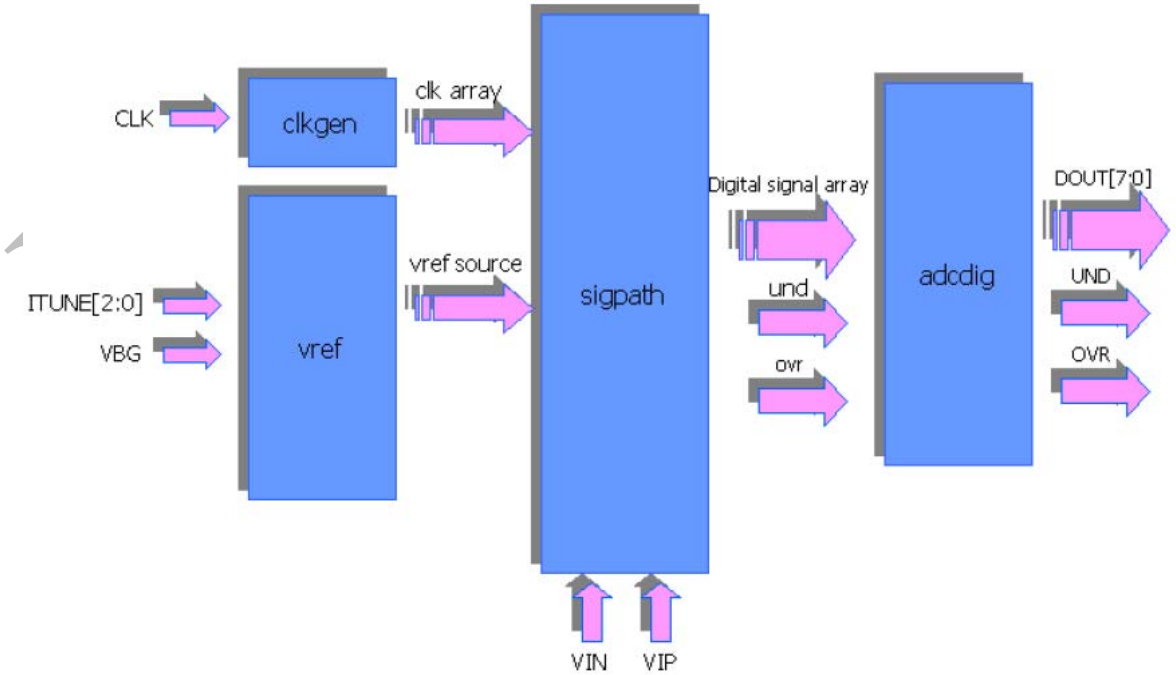


Fig. 7-1 HS-ADC Block Diagram

7.2.2 Block Descriptions

HS-ADC consists of signal path (sigpath), clock generator (clkgen), band-gap & reference generator (vref) and digital correction logic (adcdig).

HS-ADC is designed with pipelined architecture for the high-speed operation. It takes in a differential input of 1.8 V peak-to-peak and generates a 10-Bit output.(User should limit input signal amplitude to 0.9V to avoid potential saturation. Input range is dependent on the accuracy of the band gap reference)

uses a sample and hold stage followed by eight 1.5-bit compare and multiply stages, which allows for high-speed conversion while minimizing power consumption. The last stage is a 2-bit flash stage. Each sample moves through a pipeline stage every half-clock cycle. Counting the delay through the output latch, the data latency is 5 clock cycles.

7.4 Functional Description

7.4.1 Timing Characteristics

In the IP, the input sampling clock is buffered and generates two main work clocks ph1 & ph2, which are non-overlapped phase signals synchronized with the clock. The input analog signals are sampled on the falling edge of ph2, and output data are clocked out of the respective ADC's data output pins (D0 through D9) on the following falling edge of ph2.

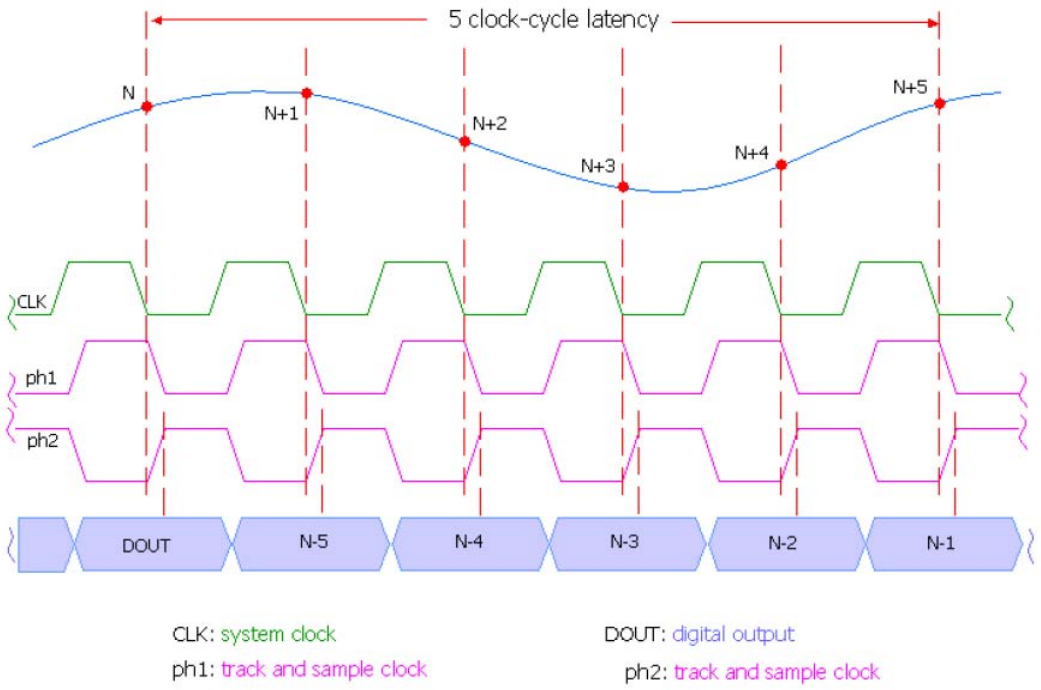


Fig. 7-2 HS-ADC Timing Characteristics

7.4.2 Bias Current Trimming

Tuning the unit bias current for pipeline stages, which is designed as 10uA, with the default setting itune="100"

Table 7-1 HS-ADC Bias Current Programming

ITUNE[2:0]	I_bias
000	60*(I_default/80)
001	65*(I_default/80)
010	70*(I_default/80)
011	75*(I_default/80)
100	I_default
101	85*(I_default/80)
110	90*(I_default/80)
111	95*(I_default/80)

7.4.3 Data Format

Due to the bipolar input differential signal, output coding is offset binary with 1LSB = FSR/1024. That means all zeros (0000000000) represent the most negative value and all ones (1111111111) represent the most positive value.

7.4.4 Electrical Characterization

Table 7-2 HS-ADC Electrical Characterization

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL				±1.5	LSB
Differential Nonlinearity	DNL				±1	LSB
Offset Error				0.03		%FS
ANALOG INPUT						
Input Range (differential)	VIN		-0.9		0.9	V
Input Resistance	RIN	Switched capacitor load	22.2	27.8	37.0	kΩ
Input capacitance	CIN		450	600	750	fF
DYNAMIC CHARACTERISTIC (FCLK=60M, T = 25, Vdda = 1.8V)						
Signal to Noise Ratio Plus Distortion	SINAD	Fin=2 M		57.8		dB
		Fin=10 M		57.1		s
		Fin=29M		56.6		
		Fin=59M		56.5		
Total Harmonic Distortion (First 5 Harmonics) *	THD	Fin=2 M		-63.2		dB
		Fin=10 M		-70.6		dB
		Fin=29M		-70		
		Fin=59M		-63.9		
Small-Signal Bandwidth						MHz
Full-Power Bandwidth	FPBW	Input at –0.5dBFS, differential inputs				MHz
Overdrive Recovery Time		For 1.5*full-scale input		20		ns
Output Noise		IN+=IN-=COM				LSBrms

CONVERSION RATE						
Maximum Clock Frequency	FCLK			60		MHz
Data latency				5		Clock
EXTERNAL REFERENCE						
Bandgap Reference	V_{BG}		1.2	1.25	1.3	V
DIGITAL INPUTS						
Input High Threshold	V_{IH}	CLK PD	$0.7V_{DD}$			V
Input Low Threshold	V_{IL}	CLK PD			$0.3V_{DD}$	V
Input Leakage	I_{IH}					μ A
	I_{IL}					
Input Capacitance	C_{IN}				0.1	pF
DIGITAL OUTPUTS (D9-D0)						
Output Voltage Low	V_{OL}				$0.3V_{DD}$	V
Output Voltage High	V_{OH}		$0.7V_{DD}$			V
POWER REQUIREMENTS						
Analog Supply Voltage	VDDA		1.7	1.8	1.9	V
Digital Supply Voltage	VDDD		1.6	1.8	2.0	V
Analog Supply Current	I_{VDDA}	Fin=29M		27		mA
Digital Supply Current	I_{VDDD}	Fin=29M		1		mA
Total Power down current	I_{VDDD}				2	uA
TIMING CHARATERISTICS						
CLK Rise to Output Data Valid	t_{DO}				1.98	ns
CLK Pulse Width High	t_{CH}			8.1		ns
CLK Pulse Width Low	t_{CL}			8.1		ns
Wake up time for core (from PDC going low to ADC functional while PDR is low, note that this is dependant on clk period, and is roughly 15 clocks)	t_{WAKEC}				120	ns
Wake up time for Reference buffers (from PDR going low to reference buffers functional, external caps is assumed to be 0.1uF)	t_{WAKER}				100	us