LC1132 Specification

V1.0.0

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Author	PMU team

Documents update Notes

Date	Owner	Version	Notes
2012-9-26	Suguobin	V0.0.1	
2012-9-30	Suguobin	V0.0.2	
2012-12-4	Wanglei	V0.0.2	1. Update pin configuration 2. Add pin description and ball location 3. Update typical application diagram 4. Add package dimension
2012-12-17	Liuyuping	V1.0.0	
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Contents

1 Overview

1.1 Features

- Handles all 2G/3G/smart phone baseband power management

Handles all voice/audio codec

- Input range: 3.0 ~ 4.5V
- Charger input of up to 15V
- 4 buck converters and 19 LDOs optimized for specific 2G/3G/smart phone subsystems
- Flexibility for various configurations of backlight LED drivers: 3 current SINK
- Read/write I2C compatible control interface
- Pre-charge indication
- Li-ion battery charging function
- Flexibility configurations of DCDC output with DVFS control or OSCEN Control
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Power-on reset and start-up timer
- Precise voltage, temperature measurement
- Automatic headphone & microphone detection
- Mono Class D 8Ω amplifier, 800 mW at 4.2V
- OCL or AC-coupled headphone operation
- 33mW stereo headphone amplifier at 1.8V
- 55mW receiver amplifier at 3.3V
- 24-bit stereo DAC and mono DAC
- 16-bit stereo ADC
- 8 kHz to 96 kHz stereo audio playback
- 8 kHz to 96 kHz mono recording
- Bidirectional IIS compatible audio interface
- Bidirectional PCM compatible audio interface
- FIR filter programmability for tone control
- Low power clock network operation if a 12 MHz or 13 MHz system clock is available
- Automatic gain control for microphone input
- Mono differential auxiliary output
- Stereo line inputs
- Differential microphone input
- Multi-function IRQ output
- 147-pin LFBGA package

1.2 Applications

LC1132 is ideal for power management and voice/audio subsystem of 2G, 3G, smart phones and other portable systems, such as Leadcore 3G smart phone platform LC1812.

1.3 General Description

LC1132 is a power management system chip including audio application optimized for 2G/3G handsets and smart phones. LC1132 contains 4 buck converters and 19 LDOs. Sophisticated controls are available for power up, battery charging and the RTC alarm. The battery charger in LC1132 supports lithium- ion (Li-ion) battery and provides pre-charge indication. The charger input voltage can be up to 15V and allows USB charging, too.

The LC1132 also provides an integrated audio subsystem that supports both analog and digital audio functions. The LC1132 includes a high quality stereo DAC, a mono DAC, a stereo ADC,a stereo headphone amplifier, which supports output cap-less (OCL) or AC-coupled (SE) modes of operation, a mono receiver amplifier, and a Class D loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices. The LC1132 features a bi-directional I2S interface and a bidirectional PCM interfaces for full range audio on either interface.

The LC1132 utilizes an I2C interface for control. The stereo DAC path features an SNR of 93 dB with a 24-bit 48 kHz input. The headphone amplifier delivers at least 33mW to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when CPVDD = 1.8V. The mono receiver amplifier delivers at least 55mWRMS to a 16Ω load with less than 1% distortion (THD+N) when A_VDD = 3.3V. The mono speaker amplifier delivers up to 800mW into an 8Ω load with less than 1% distortion when SPK_VDD = 4.2V.

The LC1132 employs advanced techniques to reduce power consumption, to reduce controller overhead, to speed development time, and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components.

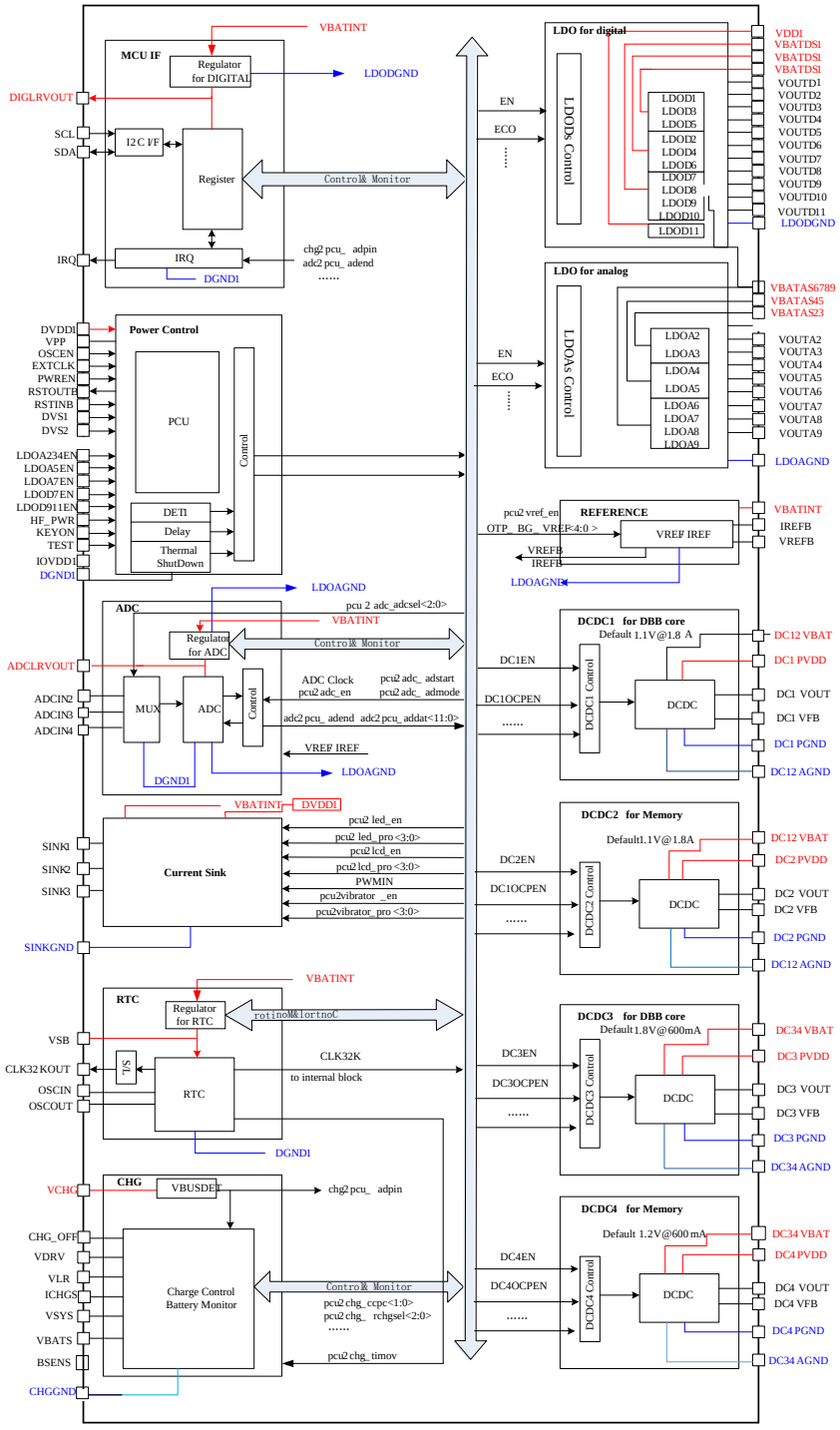
It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

LC1132 is available in a 147-pin LFBGA package. The operating temperature ranges from -25 to +85 ℃.

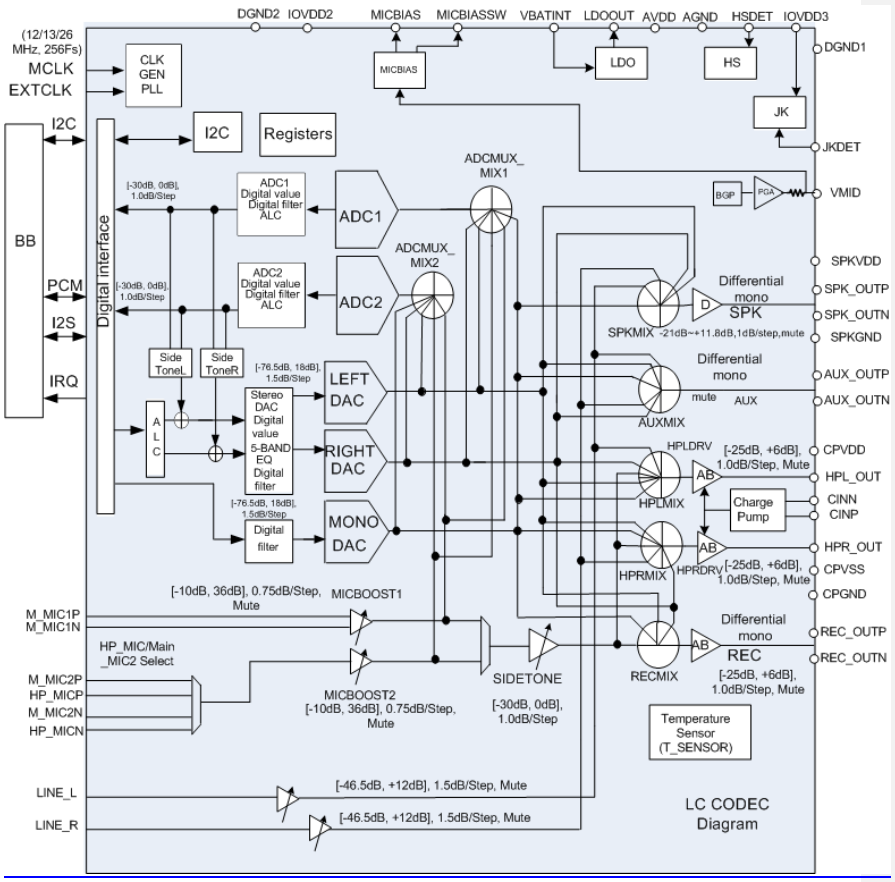
1.4 Ordering Information

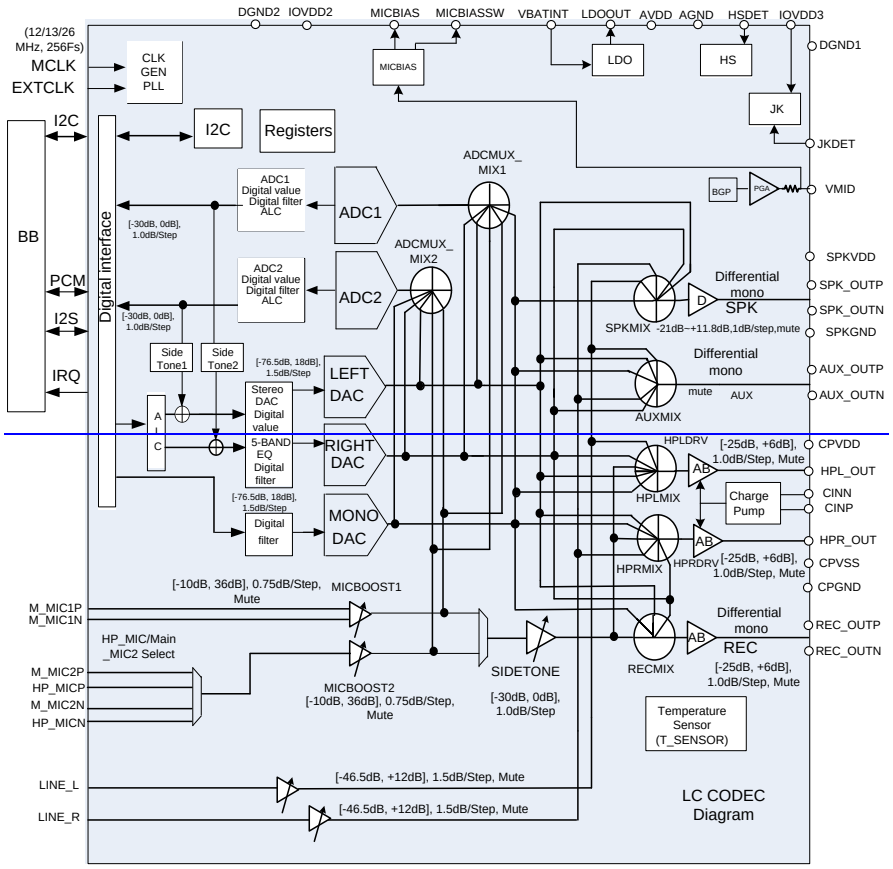
Order	Marking	Temp.range	Package
LC1132		-25 ~ +85°C	TBD

2 Block Diagram



PMU parts block diagram





Codec parts block diagram

3 Pin Information

3.1 Pin configuration（top view）

BGA	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DC2PGND	DC2PVDD	DC1VOUT	DC1VFB	DC1PGND	DC1PVDD	VBATS	ADCIN3	VOUTA3	VOUTA4	VOUTA7	VOUTA8	OSCOUT	A
B	DC2PGND	DC2PVDD	DC1VOUT	RSTINB	DC1PGND	DC1PVDD	CHGGND	BSENS	VOUTA2	VOUTA6	VBATA6789	VOUTA9	OSCIN	B
C	DC2VFB	RSTOUTB	PWREN	DVS1	OSCEN	LDOD7EN	ICHGS	VSYS	VBATA23	VBATA45	VOUTA5	VBATINT	VSB	C
D	DC2VOUT	DC2VOUT	DVS2							SINK3	DIGLRVOUT	HSDET	VREFB	D
E	IRQ	SCL	SDA		DC12VBAT	VLR	ADCLRVOUT	VDRV		CLK32KOUT	LDOOUT	IREFB	REC_OUTP	E
F	VOUTD10	LDOD911EN	MCLK		DC12AGND	ADCIN2	ADCIN4	IOVDD1		IOVDD3	VMID	AVDD	REC_OUTN	F
G	VOUTD9	VOUTD11	VDD1		VCHG	LDOA5EN	SINK1	SINK2		AGND	HF_PWR	HPR_OUT	HPL_OUT	G
H	VBATDS1	VOUTD8	VOUTD4		LDOA234EN	LDOA7EN	CHG_OFF	SINKGND		LDOAGND	KEYON	CPVSS	CINP	H
J	VOUTD3	VBATDS1	VOUTD5		DVDD1	VPP	I2SLRCK	I2SBICK		JKDET	AGND	CPGND	CINN	J
K	DC3VOUT	VBATDS1	VOUTD7							TEST	HP_MICN	SPKGND	CPVDD	K
L	DC3VFB	VOUTD1	VOUTD2	LDODGND	DC34AGND	EXTCLK	I2SSDTO	I2SSDTI	LINE_R	MICBIAS	HP_MICP	SPKGND	SPKVDD	L
M	DC3PGND	VOUTD6	DC4PGND	DC34VBAT	DGND1	DGND2	PCMSDTI	PCMLRCK	LINE_L	M_MIC2N	M_MIC1N	AUX_OUTP	SPK_OUTP	M
N	DC3PVDD	DC4VOUT	DC4VFB	DC4PVDD	IOVDD2	DVDD2	PCMSDTO	PCMBICK	MICBIASSW	M_MIC2P	M_MIC1P	AUX_OUTN	SPK_OUTN	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

3.2 Pin description

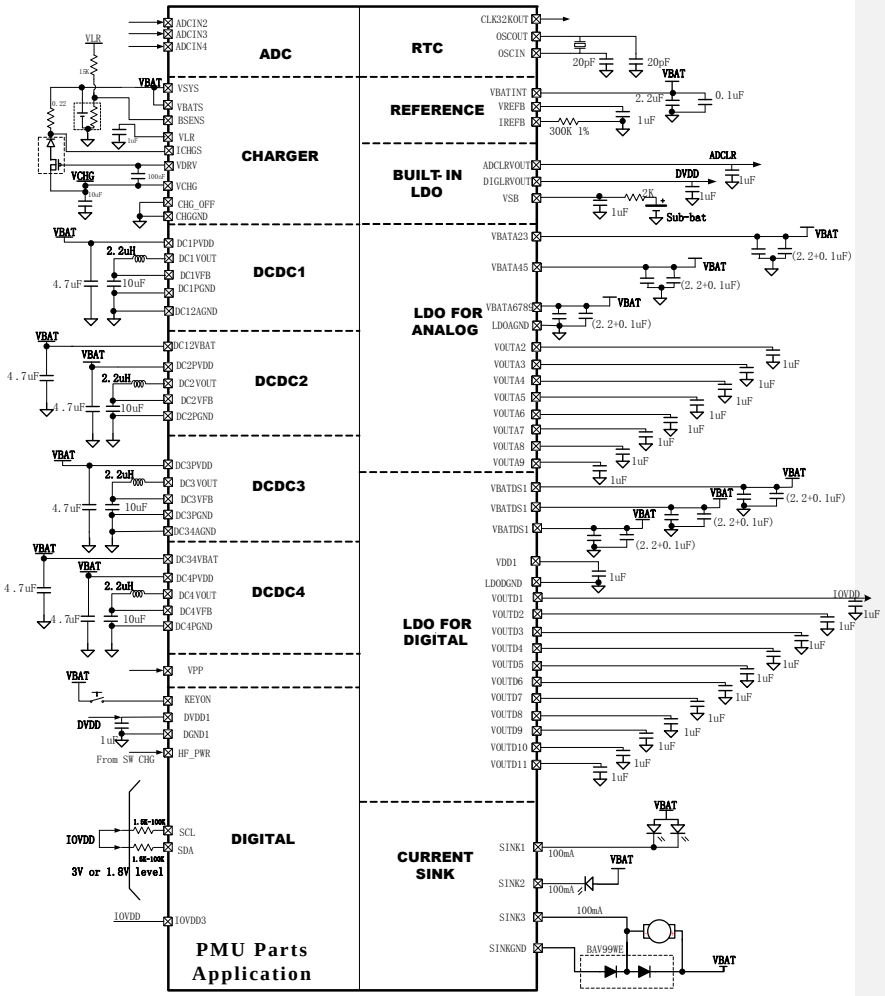
Interface	Ball#	Signal Name	A/D	IN/OUT	Description
ONOFF	**H11**	KEYON	Analog	IN	Power on key
	C2	RSTOUTB	Digital	OUT	Reset signal from PMU to DBB
	B4	RSTINB	Digital	IN	External reset input
	C3	PWREN	Digital	IN	Power-on status latch signal
	G11	HF_PWR	Analog	IN	Power on input by external SW charger
	C5	OSCEN	Digital	IN	Sleep mode enable
Control	**H5**	LDOA234EN	Digital	IN	External enable for LDOA2,LDOA3 and LDOA4
	G6	LDOA5EN	Digital	IN	External enable for LDOA5
	H6	LDOA7EN	Digital	IN	External enable for LDOA7
	C6	LDOD7EN	Digital	IN	External enable for LDOD7
	F2	LDOD911EN	Digital	IN	External enable for LDOD9 and LDOD11
	C4	DVS1	Digital	IN	Dynamic voltage scalling control for DCDC
	D3	DVS2	Digital	IN	Dynamic voltage scalling control for DCDC
PCM	**N8**	PCMBICK	Digital	INOUT	PCM Clock signal
	M8	PCMLRCK	Digital	INOUT	PCM Synchronous clock signal
	N7	PCMSDTO	Digital	OUT	PCM Serial data output
	M7	PCMSDTI	Digital	IN	PCM Serial data input
I2S	**J8**	I2SBICK	Digital	INOUT	I2S Clock Signal
	J7	I2SLRCK	Digital	INOUT	I2S Left/right channel select signal
	L7	I2SSDTO	Digital	OUT	I2S Serial data output signal
	L8	I2SSDTI	Digital	IN	I2S Serial data input signal
I2C	**E2**	SCL	Digital	IN	I2C Clock signal
	E3	SDA	Digital	INOUT	I2C Serial data signal
Clock	**F3**	MCLK	Digital	IN	External input 13MHz clock
	L6	EXTCLK	Digital	IN	External clock to CODEC
Interrupt	**E1**	IRQ	Digital	OUT	Interrupt to DBB
HOOK/JACK	**J10**	JKDET	Analog	IN	Headphone JACK remove/inert detector
	D12	HSDET	Analog	IN	Hook switch press detector
Main MIC, HP_MIC Inputs	**N11**	M_MIC1P	Analog	IN	Main Microphone1 positive input
	M11	M_MIC1N	Analog	IN	Main Microphone1 negative input

	L11	HP_MICP	Analog	IN	HP Microphone positive input
	K11	HP_MICN	Analog	IN	HP Microphone negative input
	N10	M_MIC2P	Analog	IN	Main Microphone2 positive input
	M10	M_MIC2N	Analog	IN	Main Microphone2 negative input
LINE	**M9**	LINE_L	Analog	IN	Left channel line in
	L9	LINE_R	Analog	IN	Right channel line in
SPEAKER	**M13**	SPK_OUTP	Analog	OUT	Speaker positive output
	N13	SPK_OUTN	Analog	OUT	Speaker negative output
RECEIVER	**E13**	REC_OUTP	Analog	OUT	Receiver positive output
	F13	REC_OUTN	Analog	OUT	Receiver negative output
HEADPHONE	**G13**	HPL_OUT	Analog	OUT	Left channel headphone output
	G12	HPR_OUT	Analog	OUT	Right channel headphone output
AUXOUT	**M12**	AUX_OUTP	Analog	OUT	Auxiliary positive output
	N12	AUX_OUTN	Analog	OUT	Auxiliary negative output
MIC BIAS	**L10**	MICBIAS	Analog	OUT	Microphone ultra clean supply1
	N9	MICBIASSW	Analog	OUT	Microphone ultra clean supply2
VMID	**F11**	VMID	Analog	OUT	Reference Voltage decoupling
Speaker Power	**L13**	SPKVDD	PWR		Speaker Driver supply (3.0-4.352V)
	K12,L12	SPKGND	GND		Speaker Driver ground
Analog Core Power	**F12**	AVDD	PWR		Analog Core Supply (2.8-3.6V)
	G10,J11	AGND	GND		Analog Core Ground
Codec Digital Core Power	**N6**	DVDD2	PWR		Digital Core, Supply 1.8V
	M6	DGND2	GND		Digital Core, Ground
IO Power	**F8**	IOVDD1	PWR		PMU IO Buffer Supply
	N5	IOVDD2	PWR		CODEC IO Buffer Supply
	F10	IOVDD3	PWR		CLK32K IO Buffer Supply
Charge Pump Power	**K13**	CPVDD	PWR		Charge Pump VDD (+1.8V)
	J12	CPGND	GND		Charge Pump GND (0V)
	H12	CPVSS	PWR		Charge Pump VSS (-1.7V)
	H13	CINP	Analog	INOUT	Charge Pump fly capacitor terminal
	J13	CINN	Analog	INOUT	Charge Pump fly capacitor terminal
Codec AVDD	**E11**	LDOOUT	Analog	OUT	AVDD Power Supply
AUXADC	**F6**	ADCIN2	Analog	IN	Adc input channel 2
	A8	ADCIN3	Analog	IN	Adc input channel 3
	F7	ADCIN4	Analog	IN	Adc input channel 4
DCDC	**A4**	DC1VFB	Analog	IN	DCDC1 feedback terminal
	A3,B3	DC1VOUT	Analog	OUT	DCDC1 switch output
	C1	DC2VFB	Analog	IN	DCDC2 feedback terminal
	D1,D2	DC2VOUT	Analog	OUT	DCDC2 switch output

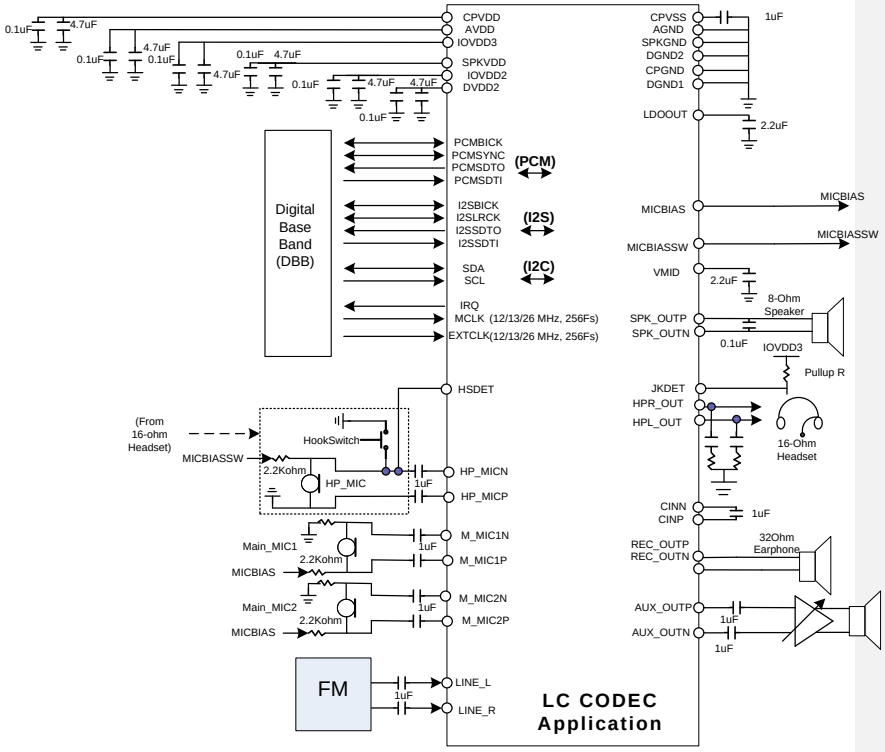
	L1	DC3VFB	Analog	IN	DCDC3 feedback terminal
	K1	DC3VOUT	Analog	OUT	DCDC3 switch output
	N3	DC4VFB	Analog	IN	DCDC4 feedback terminal
	N2	DC4VOUT	Analog	OUT	DCDC4 switch output
LDO	**L2**	VOUTD1	Analog	OUT	LDOD1 output
	L3	VOUTD2	Analog	OUT	LDOD2 output
	J1	VOUTD3	Analog	OUT	LDOD3 output
	H3	VOUTD4	Analog	OUT	LDOD4 output
	J3	VOUTD5	Analog	OUT	LDOD5 output
	M2	VOUTD6	Analog	OUT	LDOD6 output
	K3	VOUTD7	Analog	OUT	LDOD7 output
	H2	VOUTD8	Analog	OUT	LDOD8 output
	G1	VOUTD9	Analog	OUT	LDOD9 output
	F1	VOUTD10	Analog	OUT	LDOD10 output
	G2	VOUTD11	Analog	OUT	LDOD11 output
	D11	DIGLRVOUT	Analog	OUT	LDO output for PMU Digital Part
	E7	ADCLRVOUT	Analog	OUT	LDO output for PMU SAR ADC
	C13	VSB	Analog	OUT	LDO output for backup battery
	B9	VOUTA2	Analog	OUT	LDOA2 output
	A9	VOUTA3	Analog	OUT	LDOA3 output
	A10	VOUTA4	Analog	OUT	LDOA4 output
	C11	VOUTA5	Analog	OUT	LDOA5 output
	B10	VOUTA6	Analog	OUT	LDOA6 output
	A11	VOUTA7	Analog	OUT	LDOA7 output
	A12	VOUTA8	Analog	OUT	LDOA8 output
	B12	VOUTA9	Analog	OUT	LDOA9 output
Current Sink	**G7**	SINK1	Analog	IN	Current sink channel for LCD
	G8	SINK2	Analog	IN	Current sink channel for keyboard
	D10	SINK3	Analog	IN	Current sink channel for vibrator
RTC	**B13**	OSCIN	Analog	INOUT	Real Time Clock In terminal
	A13	OSCOUT	Analog	INOUT	Real Time Clock In terminal
	E10	CLK32KOUT	Analog	OUT	32KHz clock output
REFERENCE	**D13**	VREFB	Analog	OUT	Voltage reference output
	E12	IREFB	Analog	OUT	Current reference output connect 300KOhm resistor
TEST	**K10**	TEST	Analog	IN	Test input terminal
Analog Power	**E5**	DC12VBAT	PWR		DCDC1/DCDC2 analog supply
	M4	DC34VBAT	PWR		DCDC3/DCDC4 analog supply
	A6,B6	DC1PVDD	PWR		DCDC1 power supply
	A2,B2	DC2PVDD	PWR		DCDC2 power supply
	N1	DC3PVDD	PWR		DCDC3 power supply
	N4	DC4PVDD	PWR		DCDC4 power supply
	H1,J2,K2	VBATDS1	PWR		LDODs voltage supply

	C9	VBATA23	PWR		LDOA2/LDOA3 voltage supply
	C10	VBATA45	PWR		LDOA4/LDOA5 voltage supply
	B11	VBATA6789	PWR		LDOA6/LDOA7/LDOA8/LDOA 9 voltage supply
	G3	VDD1	PWR		LDOD11 voltage supply (1.8V)
	G5	VCHG	PWR		Adaptor input for charger(5V)
	C8	VSYS	PWR		Battery supply terminal for battery load
	A7	VBATS	Analog	IN	Battery voltage sampling terminal, connected with VSYS.
	C12	VBATINT	PWR		Voltage supply for internal clear analog blocks
Analog Ground	**F5**	DC12AGND	GND		DCDC1、DCDC2 analog ground
	L5	DC34AGND	GND		DCDC3、DCDC4 analog ground
	A5,B5	DC1PGND	GND		DCDC1 power ground
	A1,B1	DC2PGND	GND		DCDC2 power ground
	M1	DC3PGND	GND		DCDC3 power ground
	M3	DC4PGND	GND		DCDC4 power ground
	L4	LDODGND	GND		LDODs ground
	H10	LDOAGND	GND		LDOAs ground
	B7	CHGGND	GND		Charger ground
	H8	SINKGND	GND		Current sink ground
PMU Digital Power	**J6**	VPP	PWR		OTP programming supply(6.5V)
	J5	DVDD1	PWR		PMU digital parts supply(1.8V)
	M5	DGND1	GND		PMU digital parts ground
Charger control	**E8**	VDRV	Analog	OUT	External power PMOS gate driver
	B8	BSENS	Analog	IN	Battery thermal detection and battery absence detection, connected to NTC resistor built-in battery
	C7	ICHGS	Analog	IN	Charge current detection terminal
	E6	VLR	Analog	OUT	2.8V regulator output in adaptor domain
	H7	CHG_OFF	Analog	IN	Internal charger disable if using external SW charger. Floating or pull up to disable internal charger.

4 Typical Applications

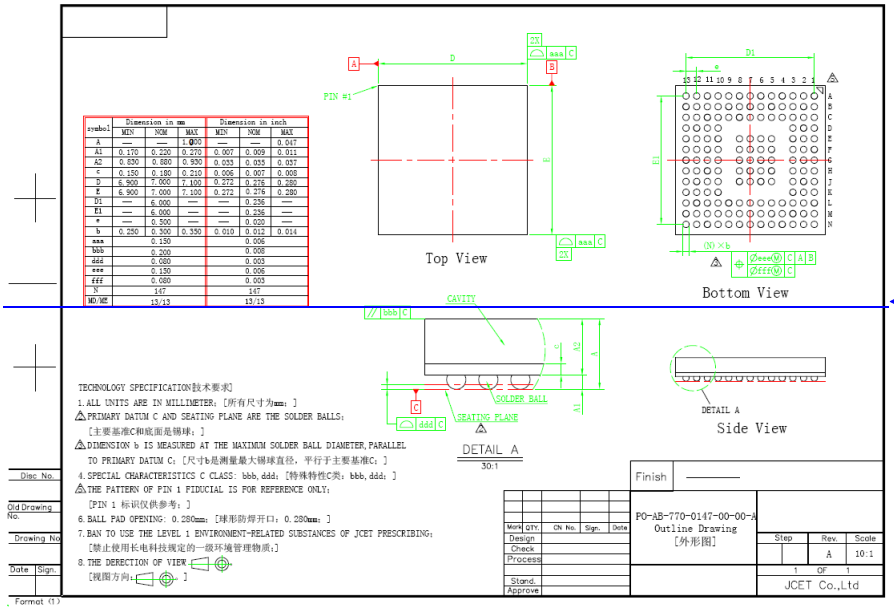


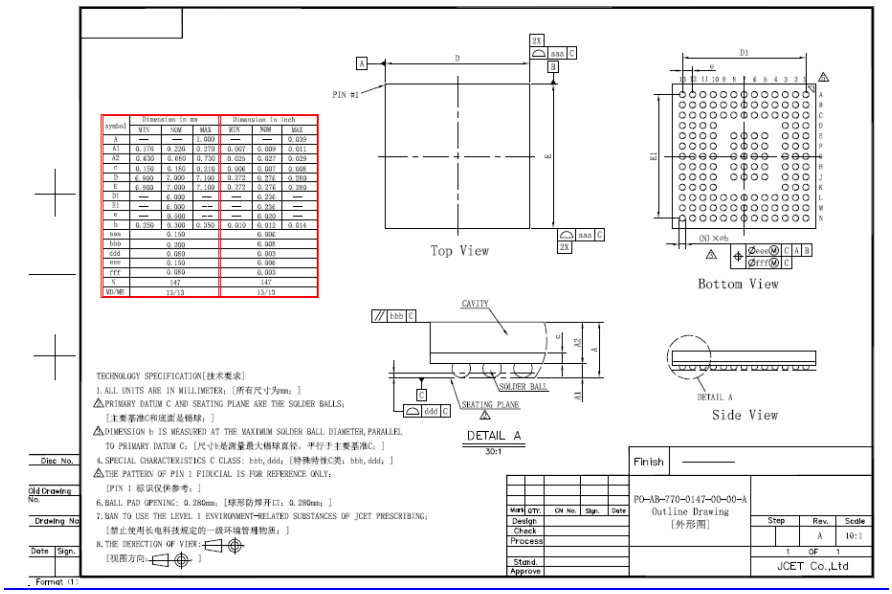
LC1132 PMU parts application



LC1132 Codec parts application

5 Package dimension





6 Absolute Maximum Ratings

Stresses beyond those listed under "absolute maximum ratings" ~~Table 3~~ may cause permanent damage

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to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Battery input Voltages			4.35	V
Charger input withstand			15	V
Operating Temperature Range	Ta	-25	85	℃
Storage Temperature	Tstg	-65	150	℃
ESD Susceptibility				
Human Body Model		2000		V
Machine Model		200		V

7 Recommended Operating Ratings

Temperature Range −25℃ to +85℃

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYPE	MAX	UNIT
Digital Voltages	DVDD1/2		1.62	1.8	1.92	V
IO Interface Digital Voltages	IOVDD1/2/3		2.7	3.0	3.3	V
			1.62	1.8	1.92	
Analog Voltages	AVDD		3.0	3.3	3.6	V
Speaker Supply Voltages	SPKVDD		3.0	3.7	4.35	V
Digital ground	DGND1/2			0		V
Analog ground	AGND,SPKGND			0		V
Different AGND and DGND			-0.3	0	+0.3	V
Charger Supply	VCHG	Adaptor voltage input pin	3.8	5	6	V
USB Supply	VUSB	USB voltage input pin		5		V
Battery Supply	VBAT	Battery voltage input pin	3.2		4.35	V
Digital Supply	VSB	Backup battery input pin	1.8		3.0	V
Operating Temperature	Ta		-25		85	℃
Logic Input Low Level	VIL				<0.4	V
Logic Input High	VIH				>0.7*IOVDD	V

Level						
Logic Output Low Level	VOL				<0.3*IOVDD	V

8 Thermal Performances

PARAMETER	Conditions	MIN	Typical	MAX	UNIT
Thermal resistance from junction to ambient	In free air		TBD		℃/W

9 Electrical Characteristics

9.1 General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Switch-off supply current					
VBAT < 2.5 V	RTC LDO OFF				μA
2.5 V < VBAT < 3.2 V					μA
3.2 V < VBAT					μA
Operation ground current					
Standby	Low-power mode		300		μA
Power key input					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			100		ms
Thermal shut-down					
PMIC shut-down threshold			165		degree
Interrupt threshold			125		degree

VBAT = 3.4 ~ 4.2V, noloads applied on all outputs, unless otherwise noted.

Typical values are at TA = 25 ℃.

		4	V
DC12VBAT	DCDC1	70	uA
DC34VBAT	DCDC3+ DCDC4	70	uA
VSYS	charger_VBAT+	21	uA

+VBATS	charger_POFF		
VBATA6789	LDOA8+LDOA9	28	uA
VBATDS1	LDOD1+IBIAS_LDOD	19	uA
VBATA45	IBIAS_LDOA	4	uA
VSB	RTC_OSC	2.5	uA
VBATINT	VREF+RTC_DVDD_SYSsys + IREF	45	uA
Total		259.5	uA

9.1.1 DC-DC/LDO General electrical specifications

Output	Loads	Input	Output	Default	Current Rating [mA]	Default on [Y/N]	Voltage Steps [mV]
Buck1	DBB Core(GPU)	VBAT	0.75-1.4	1.1	1800	Y	25
Buck2	DBB A7*4,A7*2 1.5GHz	VBAT	0.75-1.4	1.1	1800	Y	25
Buck3	Memory,Codec ,Sensor,RF	VBAT	1.05V,1.1V, 1.15V,1.2V 1.21V,1.22V, 1.23V,1.24V 1.25V,1.35V, 1.5V,1.6V 1.65V,1.7V, 1.75V,1.8V	1.8	600	Y	-
Buck4	LPDDR2,LPDDR	VBAT	0.9V,0.95V, 1.0V,1.05V 1.1V,1.15V, 1.2V,1.21V 1.22V,1.23V, 1.24V,1.25V 1.35V,1.5V, 1.7V,1.8V	1.2	600	Y	-
ALDO2	TG0 RF	VBAT	1.8/2.85	2.85	100	N	-
ALDO3	TG0 RF	VBAT	1.8/2.85	2.85	300	N	-
ALDO4	TG0 RF	VBAT	1.8/2.85	2.85	300	N	-
ALDO5	TG0 RF	VBAT	2.85	2.85	100	N	-
ALDO6	CAM'sanalog	VBAT	1.8-3.0	2.8	300	N	100
ALDO7		VBAT	1.8-3.0	1.8	200	N	100

ALDO8	DBB PLL_AVDD，LCD MIPI_AVDD	VBAT	2.5	2.5	100	Y	-
ALDO9	DBB Camera MIPI_AVDD	VBAT	2.5	2.5	100	Y	-
DLDO1	IO	VBAT	1.8/2.85/3.0	2.85	300	Y	-
DLDO2	CAM IO	VBAT	1.8/2.85/3.0	1.8	100	N	-
DLDO3	AF Motor	VBAT	1.8-3.0	2.85	200	N	-
DLDO4	USIM0	VBAT	1.8/3	1.8	100	N	-
DLDO5	USIM1	VBAT	1.8-3.0	1.8	200	N	-
DLDO6	USB OTG	VBAT	3.3	3.3	60	N	-
DLDO7	eMMC	VBAT	1.8-3.0	3	300	Y	100
DLDO8	SD Card	VBAT	1.8-3.0	3	300	N	-
DLDO9	CTP	VBAT	1.8-3.0	1.8	200	N	100
DLDO10		VBAT	1.8-3.0	1.8	200	N	100
DLDO11	CAM Core	Buck3	1.1-1.5	1.5	250	N	50
Sink1	Precharge indicator	VBAT			10-100mA	N	-

9.1.2 Voice/Audio Codec General electrical specifications

9.1.2.1 ANALOG INPUT INTERFACE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYPE	MAX	U
Stereo ADC Characteristics:						
Resolution				**16**		**Bi**
Sample rate				8kHz/11.025kHz/12kHz/ 16kHz/22.05kHz/ 24kHz/32kHz/44.1kHz/ 48kHz/96kHz		**kH**
SNR				**87**		**dB**
LINEL/LINER/MIC/ pins:						
Input Resistance	R_{IN}		28	42	56	
Input Capacitance	C_{IN}			5		
Full Scale Input Signal Level (ADC 0dB Gain)	V_{INFS}	Gain=0dB	1.68	1.98	2.28	V
Microphone input to ADC:						
Signal to Noise Ratio	SNR		80	87	-	
Total Harmonic	THD		-	-86	-80	

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Distortion						
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz	-	90	-	
Crosstalk	X_{TLAK}		-	75	-	
Line input to ADC:						
Signal to Noise Ratio	SNR		80	87	-	
Total Harmonic Distortion	THD		-	-86	-80	
Power Supply Rejection Ratio	PSRR		-	90	-	

Analog input electrical characteristics

9.1.2.2 ANALOG OUTPUT INTERFACE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYPE	MAX	UNIT
Stereo DAC Characteristics:						
Resolution				**24**		**Bits**
Sample rate				8kHz/11.025kHz /12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/96kHz		**kHz**
SNR				**95**		**dB**
AUXOUT Characteristics:						
Full-Scale output			1.78	1.98	2.18	Vpp
Signal to Noise Ratio	SNR		82	92	-	dB
Total Harmonic Distortion	THD	-3 dB output	-	-85	-74	dB
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz	-	95	-	dB
Load Resistance	R_O		10	-	-	KΩ
Load Capacitance	C_O		-	-	30	pF
Mono Receiver –Amp Output Characteristics:						
Output Power	P_O	At 3.3v, ,RL=16Ω, 1% THD	-	55	-	mW
Signal to Noise Ratio	SNR		82	92	-	dB
Total Harmonic Distortion	THD	P_O=15mW	-	-60	-	dB
PSRR	PSRR	217HZ		90		dB
Load Resistance	R_O		16	-	-	Ω
Load Capacitance	C_O		-	-	30	pF
Speaker –Amp Output Characteristics:						

Output Power	P_O	@4.2V into 8Ω load,1% THD，CLASS D	-	800	-	mW
Abs. max output power	P_{Omax}		-	1000	-	mW
Signal to Noise Ratio	SNR		80	90	-	dB
Total Harmonic Distortion	THD	P_O=200mW	-	-57	-	dB
PSRR	PSRR	217HZ		73		dB
Load Resistance	R_O		8	-	-	Ω
Load Capacitance	C_O				30	pF
Headphone-Amp Output Characteristics:						
Output Power	P_O	At 2.8v,RL=32Ω，1% THD	-	30	-	mW
Signal to Noise Ratio	SNR		80	90	-	dB
Total Harmonic Distortion	THD	P_O=20mW,RL=32Ω	-	-77	-	dB
PSRR	PSRR	217HZ		81		dB
Crosstalk	X_{TLAK}	P_O=30mW,RL=32Ω, f=1kHz Stereo analog input signal	-	75	-	dB
Load Resistance	R_O		32	-	-	Ω
Load Capacitance	C_O		-	-	30	pF

带格式表格

带格式表格

Analog output electrical characteristics

9.2 DC-DC Specification

DCDC1

Symbol	Parameter	conditon	Min	Typ	Max	Units
VBAT	Input Voltage Range		3.0	3.7	4.5	V
Vout	Output Voltage	3.0V≤VBAT≤4.5V		1.1		V
		Voltage Range		0.75-1.4V，25mV/step		
Iload	Load current	3.0V≤VBAT≤4.5V		1800		mA
Is	Quiescent current	3.0V≤VBAT≤4.5V IL=0mA，PWM/PFM		190		uA
		3.0V≤VBAT≤4.5V IL=0mA，LowPower Mode		70		uA
Ts	Soft-start time			100		us
$R_{DSON(P)}$	P channel FET on	VBAT =3.7V, IL=100mA		120		mohm

	resistance					
$R_{DSON(N)}$	N channel FET on resistance	VBAT =3.7V, IL=100mA		120		mohm
FOSC	Internal Oscillator Frequency	3.0V≤VBAT≤4.5V		1.2		MHz
Vrip	Ripple Voltage	VBAT=3.7V,Vout=1.1V,IL==1A,PWM		30		mV
		VBAT=3.7V,Vout=1.1V,IL==10mA,PFM		20		
		VBAT=3.7V,Vout=1.1V,IL==5mA,LowPower		15		
η	efficiency	VBAT=3.7V,IL=1.5A, Vout=1.1V, PWM mode		70		%
		VBAT=3.7V,IL=500mA, Vout=1.1V, PWM mode		86		
		VBAT=3.7V,IL=200mA, Vout=1.1V, PWM mode		88		
		VBAT=3.7V,IL=50mA, Vout=1.1V, PFM mode		84		
		VBAT=3.7V,IL=5mA, Vout=1.1V, LowPower mode		81		
		VBAT=3.7V,IL=1mA, Vout=1.1V, LowPower mode		71		
LNR	Line Regulation	VBAT =3~4.5V IL=1.8A		11		mV
		VBAT =3~4.5V IL=0.8A		13		
		VBAT=3~4.5V IL=10mA		16		
LDR	Load Regulation	IL=0.1A~1.8A,Vout=1.1V		12		mV
		IL=10mA~1.8A,Vout=1.1V		25		
Ilim	Limit Current			2.2		A
Tdisc	Fast Discharge Time			400		us

DCDC2

Symbol	Parameter	conditon	Min	Typ	Max	Units
VBAT	Input Voltage Range		3.0	3.7	4.5	V
Vout	Output Voltage	3.0V≤VBAT≤4.5V		1.1		V
		Voltage Range	0.75-1.4V，25mV/step			
Iload	Load current	3.0V≤VBAT≤4.5V		1800		mA
Is	Quiescent current	3.0V≤VBAT≤4.5V IL=0mA，PWM/PFM		170		uA
		3.0V≤VBAT≤4.5V IL=0mA，LowPower Mode		50		uA
Ts	Soft-start time			100		us
$R_{DSON(P)}$	P channel FET on	VBAT =3.7V, IL=100mA		120		mohm

	resistance					
$R_{DSON(N)}$	N channel FET on resistance	VBAT =3.7V, IL=100mA		120		mohm
FOSC	Internal Oscillator Frequency	3.0V≤VBAT≤4.5V		1.2		MHz
Vrip	Ripple Voltage	VBAT=3.7V,Vout=1.1V,IL==1A,PWM		30		mV
		VBAT=3.7V,Vout=1.1V,IL==10mA,PFM		20		
		VBAT=3.7V,Vout=1.1V,IL==5mA,LowPower		15		
η	efficiency	VBAT=3.7V,IL=1.5A, Vout=1.1V, PWM mode		70		%
		VBAT=3.7V,IL=500mA, Vout=1.1V, PWM mode		86		
		VBAT=3.7V,IL=200mA, Vout=1.1V, PWM mode		88		
		VBAT=3.7V,IL=50mA, Vout=1.1V, PFM mode		84		
		VBAT=3.7V,IL=5mA, Vout=1.1V, LowPower mode		82		
		VBAT=3.7V,IL=1mA, Vout=1.1V, LowPower mode		74		
LNR	Line Regulation	VBAT =3~4.5V IL=1.8A		11		mV
		VBAT =3~4.5V IL=0.8A		13		
		VBAT =3~4.5V IL=10mA		16		
LDR	Load Regulation	IL=0.1A~1.8A,Vout=1.1V		12		mV
		IL=10mA~1.8A,Vout=1.1V		25		
Ilim	Limit Current			2.2		A
Tdisc	Fast Discharge Time			400		us

DCDC3

Symbol	Parameter	conditon	Min	Typ	Max	Units
VBAT	Input Voltage Range		3.0	3.7	4.5	V
Vout	Output Voltage	3.0V≤VBAT≤4.5V ,Buck3		1.8		V
		Voltage range	1.05V/1.1V/1.15V/1.2V 1.21V/1.22V/1.23V/1.24V 1.25V/1.35V/1.5V/1.6V 1.65V/1.7V/1.75V/1.8V			
Iload	Load current	3.0V≤VBAT≤4.5V	600			mA
Is	Quiescent current	3.0V≤VBAT≤4.5V, Iavdd Iout=600mA，PWM Mode		160		uA
		3.0V≤VBAT≤4.5V, Iavdd Iout=0mA，LowPower Mode		34		
Ts	Soft-start time			100		us

$R_{DSON(P)}$	P channel FET on resistance	VBAT=3.7V, IL=100mA		140		mohm
$R_{DSON(N)}$	N channel FET on resistance	VBAT=3.7V, IL=100mA		110		mohm
FOSC	Internal Oscillator Frequency	3.0V≤VBAT≤4.5V		1.2		MHz
Vrip	Ripple Voltage	VBAT=3.7V,Vout=1.8V,Iload =600mA,PWM		18		mV
		VBAT=3.7V,Vout=1.8V,Iload =5mA,PFM		14		
		VBAT=3.7V,Vout=1.8V,Iload =1mA,LowPower		15		
η	efficiency	VBAT=3.7V,Iload=600mA, Vout=1.8V, PWM mode		88		%
		VBAT=3.7V,Iload=300mA, Vout=1.8V, PWM mode		93		
		VBAT=3.7V,Iload=5mA, Vout=1.2V, PFM mode		89		
		VBAT=3.7V,Iload=1mA, Vout=1.8V, LowPower mode		82		
LNR	Line Regulation	VBAT=3~4.5V		10		mV
LDR	Load Regulation	Iload=1mA ~600mA,Vout=1.2 V		12		mV
Ilim	Limit Current			1030		mA
Tdisc	Fast Discharge Time			200		us

DCDC4

Symbol	Parameter	conditon	Min	Typ	Max	Units
VBAT	Input Voltage Range		3.0	3.7	4.5	V
Vout	Output Voltage	3.0V≤VBAT≤4.5V ,Buck4		1.2		V
		Voltage range	0.9V/0.95V/1.0V/1.05V 1.1V/1.15V/1.2V/1.21V 1.22V/1.23V/1.24V/1.25V 1.35V/1.5V/1.7V/1.8V			
Iload	Load current	3.0V≤VBAT≤4.5V	600			mA
Is	Quiescent current	3.0V≤VBAT≤4.5V Iout=600mA，ForcePWM		150		uA
		3.0V≤VBAT≤4.5V Iout=0mA，LowPower Mode		31		uA
Ts	Soft-start time			100		us
$R_{DSON(P)}$	P channel FET on resistance	VBAT=3.7V, IL=100mA		140		mohm
$R_{DSON(N)}$	N channel FET on resistance	VBAT=3.7V, IL=100mA		110		mohm
FOSC	Internal Oscillator Frequency	3.0V≤VBAT≤4.5V		1.2		MHz
Vrip	Ripple Voltage	VBAT=3.7V,Vout=1.2V,Iload ==600mA,PWM		15		mV
		VBAT=3.7V,Vout=1.2V,Iload =5mA,PFM		15		
		VBAT=3.7V,Vout=1.2V,Iload =1mA,LowPower		15		
η	efficiency	VBAT=3.7V,Iload=600mA, Vout=1.2V, PWM mode		84		%
		VBAT=3.7V,Iload=300mA, Vout=1.2V, PWM mode		90		

		VBAT=3.7V,Iload=5mA, Vout=1.2V, PFM mode		84		
		VBAT=3.7V,Iload=1mA, Vout=1.2V, LowPower mode		79		
LNR	Line Regulation	VBAT=3.0~4.5V		7		mV
LDR	Load Regulation	Iload=1mA ~600mA,Vout=1.2 V		15		mV
Ilim	Limit Current			1030		mA
Tdisc	Fast Discharge Time			200		us

9.3 LDO Specification

9.3.1 LDO for Digital Target Electrical Characteristics

9.3.1.1 LDOD1 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8/2.85（default）/3.0		V
IOUT	Output Current	Normal mode		300		mA
		Eco mode		5		
Δ VOUT	Load Regulation@dc	10uA≤IOUT≤300mA	14@1.8 17@3.0	17@1.8 18@3.0	34.5@1.8 28@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤300mA Tstep=1us	8@1.8 12@3.0	14@1.8 23@3.0	23@1.8 68@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=150mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=150mA Tstep=1us	3@1.8 7@3.0	6.8@1.8 10@3.0	9.5@1.8 14@3.0	mV
DR	Dropout Voltage	Iout=300mA			184	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout= 150mA	f =1kHz	63@1.8 31@3.0	75@1.8 70@3.0	83@1.8 72@3.0	dB
		f=10kHZ	61@1.8 26@3.0	66@1.8 60@3.0	68@1.8 62@3.0	
		f =100kHz	48@1.8 13@3.0	50@1.8 44@3.0	54@1.8 50@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		74@1.8 127@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=300mA	95	110	130	us
Tf	Falling Time	Iout=0mA			0.217	ms
Iss	Supply Current	Normal mode: Iout=0mA		135	143	uA
		ECO mode		14		

		Iout=0uA				
		While turned off			13	nA
Io_lim	Output Current Limit	Vout=0	520		590	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.2 LDOD2 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8（default）/2.85/3		V
IOUT	Output Current	Normal mode		100		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	5.4@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V Iout =50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V Iout=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1kHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHZ	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		ECO mode Iout=0uA		14		
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA

Cout	Output Capacitor for stability			1		uF

9.3.1.3 LDOD3 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8~2.85(default)~3.0		V
IOUT	Output Current	Normal mode		200		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤200mA	11@1.8 12@3.0	11@1.8 12@3.0	21@1.8 27@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤200mA Tstep=1us	5@1.8 7@3.0	9@1.8 15@3.0	13@1.8 37@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=100mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=100mA Tstep=1us	1@1.8 3@3.0	2@1.8 5@3.0	5@1.8 9@3.0	mV
DR	Dropout Voltage	Iout=200mA			207	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=100mA	f=1kHz	66@1.8 33@3.0	78@1.8 73@3.0	90@1.8 74@3.0	dB
		f=10kHZ	66@1.8 30@3.0	73@1.8 67@3.0	76@1.8 72@3.0	
		f=100kHz	53@1.8 17@3.0	56@1.8 52@3.0	60@1.8 55@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		73@1.8 124@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=200mA	89	105	122	us
Tf	Falling Time	Iout=0mA			0.2	ms
Iss	Supply Current	Normal mode: Iout=0mA		125	135	uA
		ECO mode Iout=0uA		14		
		While turned off			31	nA
Io_lim	Output Current Limit	Vout=0	350		384	mA
Cout	Output Capacitor for			1		uF

	stability					

9.3.1.4 LDOD4 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V	1.746	1.8(default)	1.854	V
			2.91	3.0	3.09	
IOUT	Output Current	Normal mode		100		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1kHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHZ	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		ECO mode Iout=0uA		14		
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.5 LDOD5 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8(default)~3.0		V
IOUT	Output Current	Normal mode		200		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤200mA	11@1.8 12@3.0	11@1.8 12@3.0	21@1.8 27@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤200mA Tstep=1us	5@1.8 7@3.0	9@1.8 15@3.0	13@1.8 37@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=100mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=100mA Tstep=1us	1@1.8 3@3.0	2@1.8 5@3.0	5@1.8 9@3.0	mV
DR	Dropout Voltage	Iout=200mA			207	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=100mA	f=1KHz	66@1.8 33@3.0	78@1.8 73@3.0	82@1.8 74@3.0	dB
		f=10kHZ	66@1.8 30@3.0	73@1.8 67@3.0	76@1.8 72@3.0	
		f=100kHz	53@1.8 17@3.0	56@1.8 52@3.0	60@1.8 55@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		73@1.8 124@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=200mA	89	105	122	us
Tf	Falling Time	Iout=0mA			0.2	ms
Iss	Supply Current	Normal mode: Iout=0mA		125	135	uA
		ECO mode Iout=0uA		14		
		While turned off			31	nA
Io_lim	Output Current Limit	Vout=0	350		384	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.6 LDOD6 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, Ta=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.5	3.6	5.5	V
VOUTD6	Output Voltage	3.5V≤VBAT≤5.5V		3.3		V
IOUT	Output Current	Normal mode		60		mA
		Eco mode		5		
Vdrp	Dropout voltage				120	mV
△VOUT	Load Regulation@dc	10uA≤IOUT≤60mA	1.3	1.8	3.8	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤60mA Tstart=1us	17.7	26.7	34.9	mV
	Line Regulation@dc	3.5V≤VBAT≤5.5V IOUT=60mA			2.3	mV
	Vlinetrans Line Regulation@tran	3.5V≤VBAT≤5.5V IOUT=60mA Tstart=1us	5.5	11.4	17.5	mV
PSRR	Power supply restrain ratio Cout=1uF Iout=60mA	f=1kHz	33.4	55.2	93.7	dB
		f=10kHZ	31.7	52.9	77.2	
		f=100kHz	18.6	37	58.4	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		48.5		uV
Tr	Rising Time	Cout=1uf, Iout=60mA			130	us
Tf	Falling Time	Iout=0mA			283	Us
Iss	Supply Current	Normal mode: Iout=0mA		67		uA
		ECO mode: Iout=0uA		5.5		
		While turned off	<1		100	nA
Io_lim	Output Current Limit	Vout=0	~~62~~93		~~180~~138	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.7 LDOD7 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, Ta=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V

VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8~3.0(default)		V
IOUT	Output Current	Normal mode		300		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤300mA	14@1.8 17@3.0	17@1.8 18@3.0	34.5@1.8 28@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤300mA Tstep=1us	8@1.8 12@3.0	14@1.8 23@3.0	23@1.8 68@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=150mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=150mA Tstep=1us	3@1.8 7@3.0	3@1.8 10@3.0	9.5@1.8 14@3.0	mV
DR	Dropout Voltage	Iout=300mA			184	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=150mA	f=1kHz	63@1.8 31@3.0	75@1.8 70@3.0	83@1.8 72@3.0	dB
		f=10kHz	61@1.8 26@3.0	66@1.8 60@3.0	68@1.8 62@3.0	
		f=100kHz	48@1.8 13@3.0	50@1.8 44@3.0	54@1.8 50@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		74@1.8 127@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=300mA	95	110	130	us
Tf	Falling Time	Iout=0mA			0.217	ms
Iss	Supply Current	Normal mode: Iout=0mA		135	143	uA
		ECO mode Iout=0uA		14		
		While turned off			13	nA
Io_lim	Output Current Limit	Vout=0	520		590	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.8 LDOD8 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V

VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8~3.0(default)		V
IOUT	Output Current	Normal mode		300		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤300mA	14@1.8 17@3.0	17@1.8 18@3.0	34.5@1.8 28@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤300mA Tstep=1us	8@1.8 12@3.0	14@1.8 23@3.0	23@1.8 68@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=150mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=150mA Tstep=1us	3@1.8 7@3.0	3@1.8 10@3.0	9.5@1.8 14@3.0	mV
DR	Dropout Voltage	Iout=300mA			184	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=150mA	f=1kHz	63@1.8 31@3.0	75@1.8 70@3.0	83@1.8 72@3.0	dB
		f=10kHz	61@1.8 26@3.0	66@1.8 60@3.0	68@1.8 62@3.0	
		f=100KHz	48@1.8 13@3.0	50@1.8 44@3.0	54@1.8 50@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		74@1.8 127@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=300mA	95	110	130	us
Tf	Falling Time	Iout=0mA			0.217	ms
Iss	Supply Current	Normal mode: Iout=0mA		135	143	uA
		While turned off			13	nA
Io_lim	Output Current Limit	Vout=0	520		590	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.9 LDOD9 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8(default)~3.0		V
IOUT	Output Current	Normal mode		200		mA

		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤200mA	11@1.8 12@3.0	11@1.8 12@3.0	21@1.8 27@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤200mA Tstep=1us	5@1.8 7@3.0	9@1.8 15@3.0	13@1.8 37@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=100mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=100mA Tstep=1us	1@1.8 3@3.0	2@1.8 5@3.0	5@1.8 9@3.0	mV
DR	Dropout Voltage	Iout=200mA			207	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout= 100mA	f=1kHz	66@1.8 33@3.0	78@1.8 73@3.0	90@1.8 74@3.0	dB
		f=10kHZ	66@1.8 30@3.0	73@1.8 67@3.0	76@1.8 72@3.0	
		f=100KHz	53@1.8 17@3.0	56@1.8 52@3.0	60@1.8 55@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		73@1.8 124@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=200mA	89	105	122	us
Tf	Falling Time	Iout=0mA			0.2	ms
Iss	Supply Current	Normal mode: Iout=0mA		125	135	uA
		ECO mode Iout=0uA		14		
		While turned off			31	nA
Io_lim	Output Current Limit	Vout=0	350		384	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.10 LDOD10 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8(default)~3.0		V
IOUT	Output Current	Normal mode		200		mA

△ VOUT	Load Regulation@dc	10uA≤IOUT≤200mA	11@1.8 12@3.0	11@1.8 12@3.0	21@1.8 27@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤200mA Tstep=1us	5@1.8 7@3.0	9@1.8 15@3.0	13@1.8 37@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=100mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=100mA Tstep=1us	1@1.8 3@3.0	2@1.8 5@3.0	5@1.8 9@3.0	mV
DR	Dropout Voltage	Iout=200mA			207	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout= 100mA	f=1kHz	66@1.8 33@3.0	78@1.8 73@3.0	90@1.8 74@3.0	dB
		f=10kHz	66@1.8 30@3.0	73@1.8 67@3.0	76@1.8 72@3.0	
		F=100kHz	53@1.8 17@3.0	56@1.8 52@3.0	60@1.8 55@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		73@1.8 124@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=200mA	89	105	122	us
Tf	Falling Time	Iout=0mA			0.2	ms
Iss	Supply Current	Normal mode: Iout=0mA		125	135	uA
		While turned off			31	nA
Io_lim	Output Current Limit	Vout=0	350		384	mA
Cout	Output Capacitor for stability			1		uF

9.3.1.11 LDOD11 electrical characteristics

Operating Conditions (unless otherwise specified) VBAT=1.8V, Cout=1uF, T_A=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VDD1	Input Voltage			1.8		V
VOUT	Output Voltage of VOUT	1.7V≤VDD1≤1.9V		1.1~1.5(default)		V
IOUT	Output Current	Normal mode		250		mA
		Eco mode		5		
△	Load	10uA≤IOUT≤250mA	31@1.1	33@1.1	53@1.1	mV

VOUT	Regulation@dc		33@1.5	37@1.5	60@1.5	
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤250mA Tstep=1us	31@1.1 33@1.5	33@1.1 37@1.5	53@1.1 63@1.5	mV
	Line Regulation@dc	1.7V≤VDD1≤1.9V IOUT=250mA	0.05@1.1 2.2@1.5	0.2@1.1 2.8@1.5	0.6@1.1 6.8@1.5	mV
	Vlinetrans Line Regulation@tran	1.7V≤VDD1≤1.9V IOUT=250mA Tstep=1us	0.05@1.1 2.2@1.5	0.09@1.1 2.8@1.5	0.6@1.1 6.8@1.5	mV
DR	Dropout Voltage	Iout=250mA			164	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout= 125mA	f=1kHz	54@1.1 34@1.5		71@1.1 44@1.5	dB
		f=10kHz	51@1.1 30@1.5		52@1.1 41@1.5	
		f=100kHz	32@1.1 14@1.5		37@1.1 24@1.5	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		91		uV
Tr	Rising Time	Cout=1uf, Iout=250mA			88	us
Tf	Falling Time	Iout=0mA			90	us
Iss	Supply Current	Normal mode: Iout=0mA		58		uA
		ECO mode Iout=0mA		17		
		While turned off		24	5200	nA
Io_lim	Output Current Limit	Vout=0	275	417	588	mA
Cout	Output Capacitor for stability			1		uF
Switch mode	Rdson			591		moh

9.3.2 LDO for Analog Target Electrical Characterristic

9.3.2.1 LDOA2 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8/2.85(default)		V

IOUT	Output Current	Normal mode		100		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1kHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHZ	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.2 LDOA3 Electrical Characteristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8/2.85(default)		V
IOUT	Output Current	Normal mode		300		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤300mA	14@1.8 17@3.0	17@1.8 18@3.0	34.5@1.8 28@3.0	mV
	Vloadtrans	10uA≤IOUT≤300mA	8@1.8	14@1.8	23@1.8	mV

	Load Regulation@tran	Tstep=1us	12@3.0	23@3.0	68@3.0	
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=150mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=150mA Tstep=1us	3@1.8 7@3.0	3@1.8 10@3.0	9.5@1.8 14@3.0	mV
DR	Dropout Voltage	Iout=300mA			184	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout= 150mA	f=1KHz	63@1.8 31@3.0	75@1.8 70@3.0	83@1.8 72@3.0	dB
		f=10kHZ	61@1.8 26@3.0	66@1.8 60@3.0	68@1.8 62@3.0	
		f=100KHz	48@1.8 13@3.0	50@1.8 44@3.0	54@1.8 50@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		74@1.8 127@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=300mA	95	110	130	us
Tf	Falling Time	Iout=0mA			0.217	ms
Iss	Supply Current	Normal mode: Iout=0mA		135	143	uA
		While turned off			13	nA
Io_lim	Output Current Limit	Vout=0	520		590	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.3 LDOA4 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8/2.85(default)		V
IOUT	Output Current	Normal mode		300		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤300mA	14@1.8 17@3.0	17@1.8 18@3.0	34.5@1.8 28@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤300mA Tstep=1us	8@1.8 12@3.0	14@1.8 23@3.0	23@1.8 68@3.0	mV
	Line	3.2V≤VBAT≤4.5V			<1	mV

	Regulation@dc	IOUT=150mA				
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=150mA Tstep=1us	3@1.8 7@3.0	3@1.8 10@3.0	9.5@1.8 14@3.0	mV
DR	Dropout Voltage	Iout=300mA			184	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=150mA	f=1kHz	63@1.8 31@3.0	75@1.8 70@3.0	83@1.8 72@3.0	dB
		f=10kHZ	61@1.8 26@3.0	66@1.8 60@3.0	68@1.8 62@3.0	
		f=100kHz	48@1.8 13@3.0	50@1.8 44@3.0	54@1.8 50@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		74@1.8 127@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=300mA	95	110	130	us
Tf	Falling Time	Iout=0mA			0.217	ms
Iss	Supply Current	Normal mode: Iout=0mA		135	143	uA
		While turned off			13	nA
Io_lim	Output Current Limit	Vout=0	520		590	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.4 LDOA5 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		2.85		V
IOUT	Output Current	Normal mode		100		mA
△VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF	f=1kHz	63@1.8	86@1.8	92@1.8	dB

	Power supply restrain ratio Cout=1uF,Iout=50mA		39@3.0	80@3.0	88@3.0	
		f=10kHZ	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.5 LDOA6 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8~2.8(default)~3.0		V
IOUT	Output Current	Normal mode		300		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1kHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHZ	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100KHz	55@1.8	59@1.8	61@1.8	

			15@3.0	52@3.0	57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.6 LDOA7 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		1.8(default)~3.0		V
IOUT	Output Current	Normal mode		200		mA
△ VOUT	Load Regulation@dc	10uA≤IOUT≤200mA	11@1.8 12@3.0	11@1.8 12@3.0	21@1.8 27@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤200mA Tstep=1us	5@1.8 7@3.0	9@1.8 15@3.0	13@1.8 37@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=100mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=100mA Tstep=1us	1@1.8 3@3.0	2@1.8 5@3.0	5@1.8 9@3.0	mV
DR	Dropout Voltage	Iout=200mA			207	mV
PSRR	Power supply restrain ratio Cout=1uF,Iout=100mA	f=1KHz	66@1.8 33@3.0	78@1.8 73@3.0	82@1.8 74@3.0	dB
		f=10kHZ	66@1.8 30@3.0	73@1.8 67@3.0	76@1.8 72@3.0	
		f=100KHz	53@1.8 17@3.0	56@1.8 52@3.0	60@1.8 55@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		73@1.8 124@3.0		uV
Tr	Rising Time	Cout=1uf,	89	105	122	us

		Iout=200mA				
Tf	Falling Time	Iout=0mA			0.2	ms
Iss	Supply Current	Normal mode: Iout=0mA		125	135	uA
		While turned off			31	nA
Io_lim	Output Current Limit	Vout=0	350		384	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.7 LDOA8 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		2.5		V
IOUT	Output Current	Normal mode		100		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1kHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHz	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100KHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA

		ECO mode Iout=0uA		14		
		While turned off			33	nA
Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.2.8 LDOA9 Electrical Characterristic

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, T_A =25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.2	3.6	4.5	V
VOUT	Output Voltage of VOUT	3.2V≤VBAT≤4.5V		2.5		V
IOUT	Output Current	Normal mode		100		mA
		Eco mode		5		
△ VOUT	Load Regulation@dc	10uA≤IOUT≤100mA	6@1.8 6@3.0	6@1.8 6@3.0	7@1.8 9@3.0	mV
	Vloadtrans Load Regulation@tran	10uA≤IOUT≤100mA Tstep=1us	3@1.8 5@3.0	5@1.8 8@3.0	9@1.8 23@3.0	mV
	Line Regulation@dc	3.2V≤VBAT≤4.5V IOUT=50mA			<1	mV
	Vlinetrans Line Regulation@tran	3.2V≤VBAT≤4.5V IOUT=50mA Tstep=1us	1@1.8 3@3.0	2@1.8 4@3.0	4.2@1.8 6@3.0	mV
DR	Dropout Voltage	Iout=100mA			137	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=1uF,Iout=50mA	f=1KHz	63@1.8 39@3.0	86@1.8 80@3.0	92@1.8 88@3.0	dB
		f=10kHz	62@1.8 31@3.0	76@1.8 70@3.0	78@1.8 76@3.0	
		f=100kHz	55@1.8 15@3.0	59@1.8 52@3.0	61@1.8 57@3.0	
Noise	Output Noise voltage	RMS f=10Hz~100kHz		70@1.8 120@3.0		uV
Tr	Rising Time	Cout=1uf, Iout=100mA	100		130	us
Tf	Falling Time	Iout=0mA			0.24	ms
Iss	Supply Current	Normal mode: Iout=0mA	97	100	110	uA
		ECO mode Iout=0uA		14		
		While turned off			33	nA

Io_lim	Output Current Limit	Vout=0	170		187	mA
Cout	Output Capacitor for stability			1		uF

9.3.3 CODEC_LDO

Operating Conditions (unless otherwise specified) VBAT=3.8V VOUT=2.7V C_{LOAD}=2.2uF Ta=40℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Input Voltage		3.0	3.6	4.2	V
VOUT	Output Voltage	3.0V≤VBATINT≤4.2V	1.8~3.7(3.3default)			V
IOUT	Output Current			80		mA
△VOUT	Load Regulation	VBATINT=3.0V--4.2V IOUT = IMAX/2			0.18	mV
	Line Regulation	10uA<IOUT<80mA			40	mV
PSRR	LDO with VREF Power supply restrain ratio Cout=2.2uF,Iout=40mA	f=1kHz	75.6	79	83	dB
		f=10kHz	65	70	76	
Noise	Output Noise voltage	RMS f=20Hz~20kHz		161		uV
Tr	Rising Time	Cout=2.2uf, Iout=40mA		16.3	21.5	us
Tf	Falling Time	Iout=0mA		417	750	us
Iss	Supply Current	Iout=0mA		144		uA
		While turned off			33	nA
Cout	Output Capacitor for stability			2.2		uF

9.4 SAR ADC Specification

Parameter	Description	Min	Typ	Max	Units	Comment
ADCLRVOUT	2.8V analog power supply	2.772	2.8	2.828	V	
DVDD1	1.8V digital power supply	1.62	1.8	1.98	V	
TJ	Junction temperature	-40	60	125	℃	
FCLK	Clock frequency		541.667		KHz	
DCCLK	Clock duty cycle	40		60	%	
Tconv	Conversion time	12			period	
Offset	System offset			2	LSB	@ 0V input
VFS	Max analog input		2.8		V	

INL	INL	-1		1	LSB	
DNL	DNL	-1		1	LSB	
RIN	Input impedance	194			KΩ	
IAVDD_H	Average operating current		1	1.3	mA	
IPD_AVDD_H	Shutdown current		1		uA	
Resolution			12		bit	

9.5 Thermal shut down circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TSD_H	High over temperature threshold	3V<VBAT<4.5V		165		℃
TSD_L	Low over temperature threshold	3V<VBAT<4.5V		125		℃
Hysteresis_H		VBAT=3.6V		20		℃
Hysteresis_L		VBAT=3.6V		20		℃
Iss	Ground current	3V<VBAT<4.5V		9	27.5	uA
Isd	Shutdown current	3V<VBAT<4.5V			13	nA

9.6 Current Sink Specification

Sink1 for LCD Backlight					
Symbol	Parameters	Spec			Units
		Min	Typ	Max	
VBAT	Voltage tolerance at Sink1	3.2	3.6	4.5	V
Iout	Sink1 current range	10		100	mA
Iout Accuracy	Current accuracy at default current	-10		+10	%
Vdropout	Saturation voltage		0.2		V
fpwm	PWM Frequency	20.4			KHz
Iq	Quiescent current at 100mA		110		uA
Sink2 for Keyboard LED					
VBAT	Voltage tolerance at Sink2	3.2	3.6	4.5	V
Iout	Sink2 current range	10		100	mA
Iout Accuracy	Current accuracy at default current	-10		+10	%
Vdropout	Saturation voltage		0.2		V
Iq	Quiescent current at 100mA		110		uA
Sink3 for Vibrator					
VBAT	Voltage tolerance at Sink3	3.2	3.6	4.5	V
Iout	Sink3 current range	10		100	mA

Iout Accuracy	Current accuracy at default current	-10		+10	%
Vdropout	Saturation voltage		0.2		V
Iq	Quiescent current at 100mA		110		uA

9.7 VREF and IREF Target Electrical Characteristics

Operating Conditions (unless otherwise specified) VBAT=3.6V, Cout=1uF, Ta=25℃

Symbol	Parameter	Conditions	SPEC			Units
			Min	Typ	Max	
VBAT	Power supply voltage		3.0	3.6	4.5	V
BG_VREF1V5	The 1.5V Reference voltage	Bypass capacitor is 1uf		1.5		V
IREFB	The 2uA Reference current	Ouside resistor is 300kohm		2		uA
Iss	Quiescent current	Supply current		32		uA
		While turned off			25	nA
PSRR	The VREF1p5 power supply restrain ratio	F=dc	56	76	120	dB
		F=1khz	72	85	85	
		F=10khz		90		
		F=100khz		105		
EN	Output Noise voltage(RMS)	10Hz~100KHz Cout=1.0uf Vref=1. 5V		60		uV
Tr	Rising Time	The reference voltage reach 1.75V			9.14	ms
Vp	Power on voltage	The min Power supply voltage setup VBG1p75 to 1.75V			2.5	V
ΔVREF/VREFΔTa		-40℃≤Ta≤125℃		28		ppm/℃
Vopt	The voltage step of OTP Calibration precision			8		mV

9.8 RTC Specification

Symbol	Parameter	Condition	SPEC	Units

			Min	Typ	Max	
Vsb	Clock Operating Voltage		1.8	3		V
Ts	Oscillator Stable Start Time	Vsb=3V, CL=12.5pF		0.5		s
Fs	Output Frequency	Vsb=3V, CL=12.5pF		32.768		KHz
Is	Power Dissipation	Vsb=3V, CL=12.5pF		2.5		uA
Fp	Frequency Precision error	@all corner		<0.1%		

BAKBAT_LDO：

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSB	Output voltage	VBAT>3.3V		3 2.6 2.8 3.2		V
Vsw	Switch voltage of supply	VBAT fall (supply switch to sub-battery)		2.5		V
		VBAT rise (supply switch to main-battery)		2.7		
IOUT	Output Current	BAKBAT LDO active mode			5	mA
		Sub-battery mode			0	
ΔVOUT	Load Regulation	10uA≤IOUT≤5mA			20	mV
	Line Regulation	VOUT+0.4V≤VBAT≤4.5V, IOUT=5mA			10	
V_{DO}	Dropout Voltage	IOUT=5mA				mV
PSRR	Power Supply Rejection Ratio	@10kHz, IOUT=5mA		50		dB
		@1MHz, IOUT=5mA		40		
ISS	Quiescent Current	Normal mode, no load			4	uA
ISD	Shutdown Current	When VBAT<2.5V			0.1	uA
Cbyp	Bypass Capacitance			1		uF
Rex	Limitation resistor	If rechargeable coin-battery been used		2	5	KOhm

Digital_LDO：

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Input voltage		2		3	V
VOUT	Output voltage			1.8		V

△VOUT	Load Regulation	10uA≤IOUT≤2mA			20	mV
	Line Regulation	VOUT+0.2V≤VBAT≤3V, IOUT=2mA			10	
V_{DO}	Dropout Voltage	IOUT=2mA			100	mV
PSRR	Power Supply Rejection Ratio	@10kHz, IOUT=2mA		50		dB
		@1MHz, IOUT=2mA		30		
I_{SS}	Quiescent Current	Normal mode, no load			4(note)	uA
Cbyp	Bypass Capacitance		0.1	0.22	1	uF

9.9 Charger Specification

Li-Battery charger electrical characteristic

Operating Conditions (unless otherwise specified) VCHG=5V, Ta=25℃

Symbol	Parameter	Conditions	Spec			Units
			Min	Typ	Max	
VCHG	Adapter/USB effective voltage range			3.8~6		V
UVLO_VCHG1	Adapter/USB unter voltage value		-3%	3.495	+3%	V
UVLO_VCHG2	Adapter/USB under voltage value			4.207/4.352		V
OV_VCHG	Adapter/USB over voltage value		-3%	5.98	+3%	V
OV_VBAT	VBAT over voltage value		-3%	4.501	+3%	V
BATU3	PMU force shut down voltage		-2%	2.999	+2%	V
BATU33	battery under voltage value		-2%	3.52	+2%	V
			-2%	3.6	+2%	V
			-2%	3.65	+2%	V
			-2%	3.7	+2%	V
BATV32	the min startup voltage		-2%	3.201	+2%	V
Vterm	CV voltage	4.5V≤VCHG≤6V 1mA≤IOUT≤1A	-1%	4.208	+1%	V
			-1%	4.225	+1%	V
			-1%	4.25	+1%	V
			-1%	4.352	+1%	V
			-1%	4.375	+1%	V
			-1%	4.4	+1%	V
Vcv	CV cmp voltage	4.5V≤VCHG≤6V 1mA≤IOUT≤1A		4.131		V
				4.303		V
Vtrkl	Trickle voltage	3.8V≤VCHG≤6V，IOUT=100mA		3.001		V
Itrk	Trickle current	3.8V≤VCHG≤6V，VBAT≤3V	-2%	107	+2%	mA

Ichg	Charging current	3.8V≤VCHG≤6V，3V≤VOUT≤4.2V/4.35V	1140	1208	1260	mA
			1045	1108	1155	mA
			950	1008	1050	mA
			855	907	945	mA
			760	807	840	mA
			665	707	735	mA
			570	607	630	mA
			450	507	550	mA
			360	407	440	mA
			270	307	330	mA
			180	207	220	mA
			90	107	110	mA
Ieoc	Charging termination current	4.5V≤VCHG≤6V，4.125V≤VOUT≤4.2V 或 4.3V≤VOUT≤4.35V	45	46	55	mA
			90	100	110	mA
			135	150	165	mA
			180	205	220	mA
Vrec	Recharging voltage	4.5V≤VCHG≤6V，VOUT≤4.2V/4.35V	4.11	4.156/4.3	4.19	V
			4.059	4.10/4.25	4.141	V
			4.01	4.056/4.2	4.09	V
			3.96	4.00/4.15	4.04	V
			3.91	3.95/4.1	3.99	V
			3.86	3.9/4.05	3.94	V
			3.811	3.85/4	3.888	V
			3.762	3.807/3.95	3.838	V
RTIMOV	Charging Time			7	10	hour
BNTC	Battery exist voltage			2.498		V
	Battery under temprature voltage		-3	0	3	°C
	Battery over teprature voltage		42	45	48	°C
T125C	Thermal current limit temp：Die temp where current limit is reduced			125		°C
T165C	Charger shutdown temp：Die temp where			165		°C

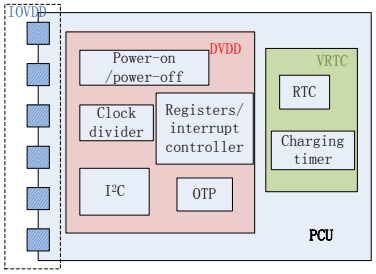
	charger is shutdown					
Ilkg	VBAT Leakage current	VCHG=0V,VBAT=3.6V VBATDETEN=0		5		uA
OVP_VCHG	Adapter/USB max voltage value			15		V

10 PMU Functional Descriptions

10.1 General Descriptions

10.2 Block diagram

The block diagram of PCU is shown below. Digital IOs are powered by IOVDD. Modules such as power-on/power-off control, I2C interface, registers and OTP are powered by DVDD. RTC and charging timer are powered by VRTC.

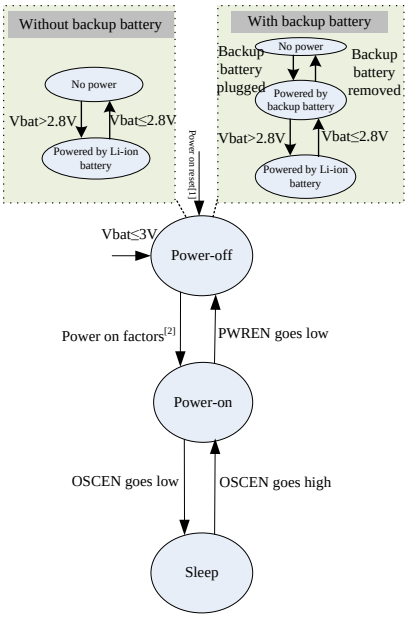


PCU block diagram

IOVDD and DVDD are both powered by Li-ion battery (or Ni-H battery) indirectly. VRTC can be regarded as an always-on supply, because it is powered by main battery when main battery is above 2.8V and by backup battery instead when main battery is below 2.8V.

10.3 Operation modes

In general, PMU has three operation modes： power-off、power-on and sleep. Power-on/power-off controller controls the transition of these modes according to specified trigger conditions, as shown below.



PMU operation modes transition

Notes：[1] power-on reset refers to reset when main battery voltage rises from below 2.6V to 2.6V

[2] power-on factors are described in following section.

The power state of RTC with and without back-up battery when PMU is powered off is shown in dashed block. The LDO for RTC can automatically switch between Li-ion and backup battery. In power-on state, if battery voltage falls below 3.3V, “battery undervoltage” interrupt will be asserted. If DBB doesn’t shut down PMU and battery voltage falls below 3V, PMU will be powered off directly.

All DCDCs and LDOs can be configured via I2C interface in power-on mode. In order to facilitate control, external pins are added for LDOA2, LDOA3, LDOA4, LDOA5, LDOA7, LDOD7, LDOD9 and LDOD11. These regulators except LDOD7 are controllerd by external pins by default, but they can also be configured via I2C interface if external pins are configured disabled.

带格式的：字体：Times New Roman，五号，字体颜色：自动设置

10.3.1 Power-on

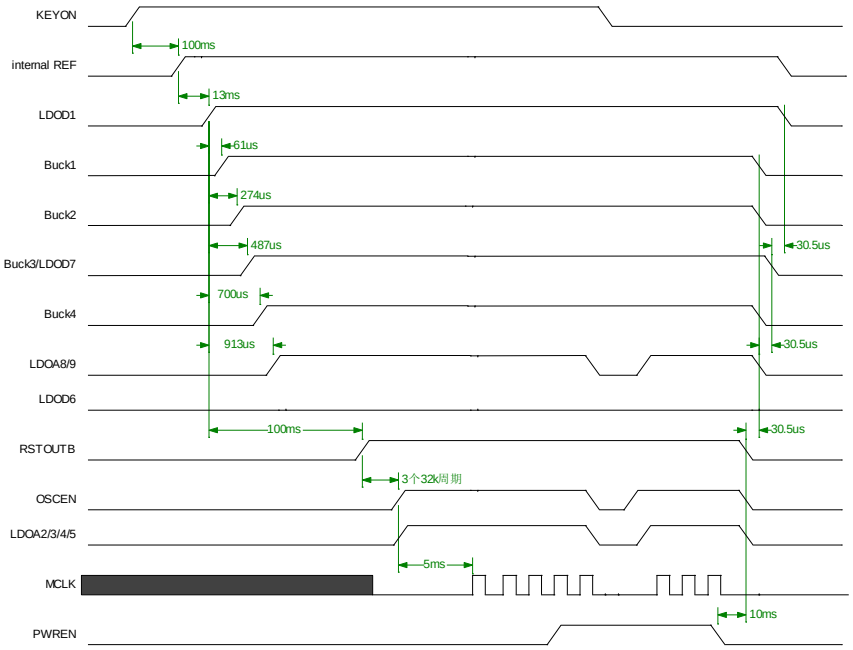
Power-on sequence can be triggered by one of four events: power-on key KEYON is pressed for 100ms or adaptor is plugged in or HF_PWR keeps high for at least 250ms or or RTC alarm occurs. The minimum power on voltage is 3.2V

We take power-on by KEYON as an example, so is it for other power-on events.

When power on key is pressed, or KEYON goes high, PMU begins power-on sequence. During power-on sequence，if power-on key is released or KEYON goes low before PWREN asserted, PMU will go to power-off state.

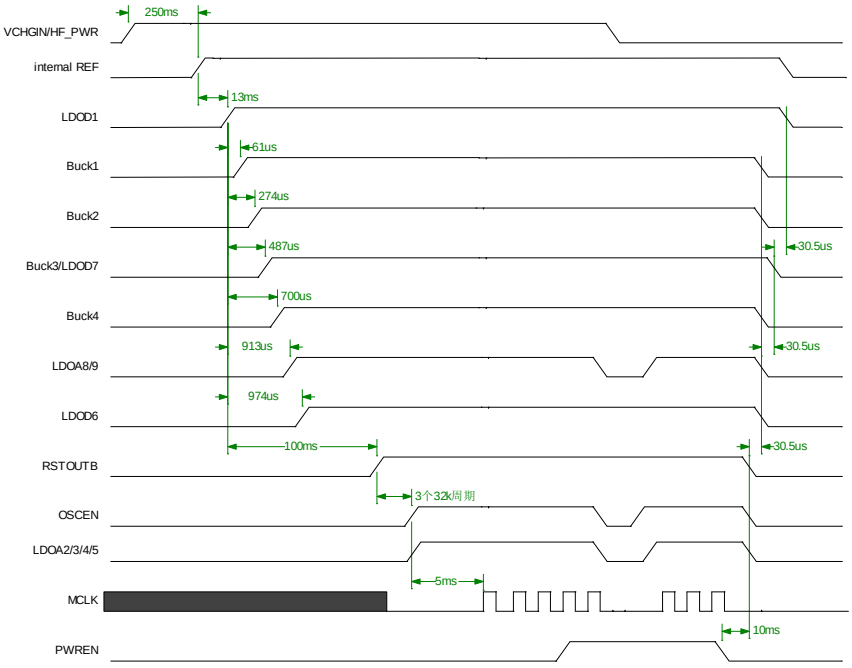
1. LDO for RTC is always on. After KEYON is pressed for 100ms, internal bandgap reference is turned on.
2. When reference bacomes stable after 13ms, battery voltage comparator is turned on and checks whether battery is above 3.2V after about 310us

3. If battery voltage is above 3.2V, LDOD1, DCDC1, DCDC2, DCDC3/LDOD7, DCDC4，and LDOA8/9/10 are turned on in sequence. The interval between DCDCs is 213μs and the interval between LDOs is 61μs. Whether LDOD6 that supplies power for USB is turned on depends on the status of adaptor. Whether LDOD7 that supplies power for eMMC is turned on is controlled by LDOD7EN.
4. PMU asserts RSTOUTB to reset DBB. RSTOUTB keeps low for 100ms since LDOD1 is turned on.
5. After RSTOUTB is released, OSCEN will go high. Wheter LDOA2/3/4/5 is turned on is controlled by external pins LDOxEN. In application, LDOxEN pin that controls LDO for 26MHz VCTCXO is usually connected to OSCEN.
6. Power-on sequence is completed when PWREN is asserted by DBB.
7. Power-on sequence triggered by KEYON is shown below.



Power-on sequence triggered by KEYON

Power-on sequence triggered by adaptor or HF_PWR is show below.



Power-on and power-off sequence triggered by adaptor

10.3.2 Deep sleep and wakeup

The flow that chip enters deep sleep from operation mode is:

1. DBB pulls OSCEN pin LOW when it enters sleep mode
2. DCDCx or LDOx is automatically shutdown if their "ALLOW_IN_SLP" bit is set to 0 while they keep their state before sleep if "ALLOW_IN_SLP" bit is set to 1. DCDCx and LDOx will enter into low power mode if automatic switch function of low power is enabled.
3. After VCTCXO is powered off, 26MHz clock is closed and system enters deep sleep state.

If DBB needs to return to operation mode, it will initiate wakeup flow.

1. DBB pulls OSCEN pin HIGH when it receives wakeup interrupts
2. DCDCx or LDOx automatically switch to the status before sleep; DCDCx and LDOx return to normal mode.
3. VCTCXO is powered on and outputs 26M clock. Then system wakes up.

This chip provides three low power management approaches:

1. **Dynamic Voltage Scaling(DVS)**
   - For DCDC1, DCDC3 and DCDC4, DBB can configure register DCxOVS0 and DCxOVS1 to set normal voltage DC1ONV and sleep voltage DC1SLPV. When OSCEN goes LOW, the voltage of DCDC1 will automatically switch to DC1SLPV.
   - For DCDC2, DBB can configure DC2_DVS_SEL bit of DCEN register. If DC2_DVS_SEL is set "00", the voltage of DCDC2 is determined by DC2OVS0; If DC2_DVS_SEL is set ~~to~~ "01", the voltage of DCDC2 can be controlled directly by DVS2 and DVS1 pins, as listed below.

DVS2	DVS1	output voltage
0	0	DC2OVS0
0	1	DC2OVS1
1	0	DC2OVS2
1	1	DC2OVS3

- The output voltage of other DCDC and LDOs can be configured via I2C bus.
-

2. Automatic shutdown in sleep

When DBB configures "ALLOW_IN_SLP" bit to 0, corresponding DCDCx or LDOx will be automatically shutdown when OSCEN goes LOW.

3. Automatic switch to low power mode in sleep
   - When LDOxECO is set to 1, LDOx will automatically switch to ECO mode when system enters into sleep
   - When DCx_LP_IN_SLP bit of register DCMODE is set to 1, DCDCx will automatically switch to low power mode; if DCx_LP_IN_SLP bit is set to 0, DCDCx will switch to PFM mode when its load is lighter than threshold.

10.3.3 Power-off

There are two kinds of power-off sequence: normal and abnormal.

Normal power-off contains software and hardware events. Software power-off event refers to the case that caused by PWREN. DBB enters into power-off stage upon receipt of conditions for trigger logoff. In power-off stage, the application must execute some saving operation to save information on related memory and pulls PWREN pin LOW. PMU starts power-off sequence when PWREN holds low for at least 20ms. Hardware power-off event refers to the case that caused by KEYON. If SHDN_EN.KEYON_SHDN_EN is enabled and KEYON is pressed for 10s (or 20s which is controlled by SHDN_EN.KEYON_SHDN_TIME), PMU will be powered off.

Abnormal power-off refers to the case caused when battery voltage is lower than 3V or chip temperature reaches 140℃ or LDOD1 undervoltage occurs. Abnomal power-off sequence is completed by hardware.

After PMU is powered on again, Software can read SHDN_STATUS register to get the event of last power-off sequence.

During power-off sequence, RSTOUTB is pulled LOW and regulators are disabled according to pre-defined timing, which is show in Fig. 2-4 and Fig. 2-5. After this, all regulators except some build-in LDOs are shutdown. Power-on/off controller remains active and is ready to initiate power-on sequence when power-on events are detected.

If backup battery is connected to VSB, RTC keeps counting for time and date even if main battery is removed in power-off state; If a capacitor is connected to VSB, RTC operates nomally when main battery voltage is above 2.8V and is supplied from capacitor when main battery voltage is lower than 2.8V.

10.4 Reset

PMU asserts reset signal on the following conditions:

- **Power-on sequence**

Reset in power-on sequence is shown in above section.

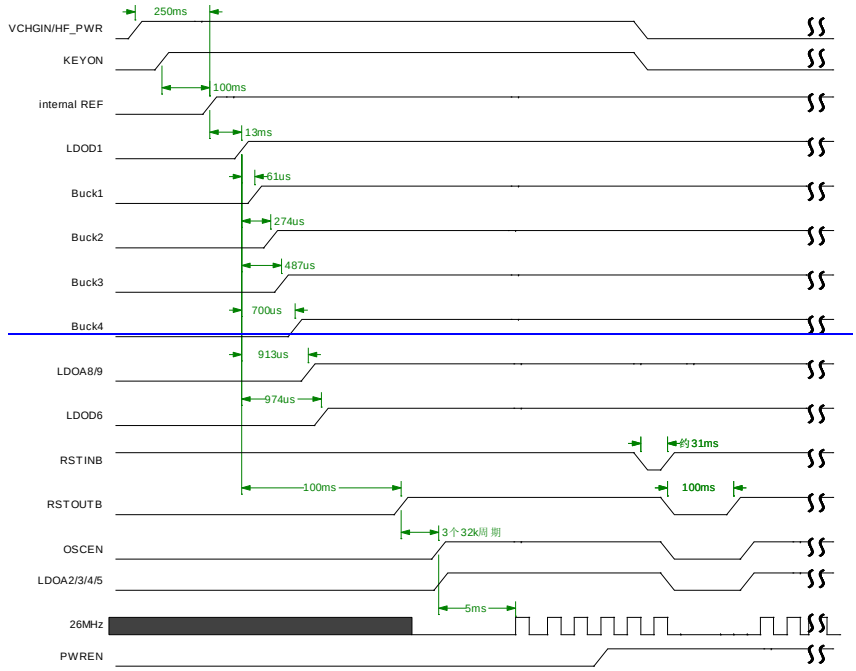
- **Input reset RSTINB keeps LOW for at least 31ms**

There are two different reset methods:

a. Cold reset (SHDN_EN.RSTINB_SHDN_EN=high): PMU will go to power-off state first and then initiate power-on event automatically. In this case, all regulators including default on power rails are disabled.

b. Hot reset(SHDN_EN.RSTINB_SHDN_EN=low):

In this case, PMU will pull RSTOUTB LOW and reset all registers except those in RTC. It will disable all power regulators except default on power rails such as LDOD1, DCDC1, DCDC2, DCDC4, DCDC3 and LDOA8/9/10. A power-on sequence then initiates automatically after RSTINB goes high..



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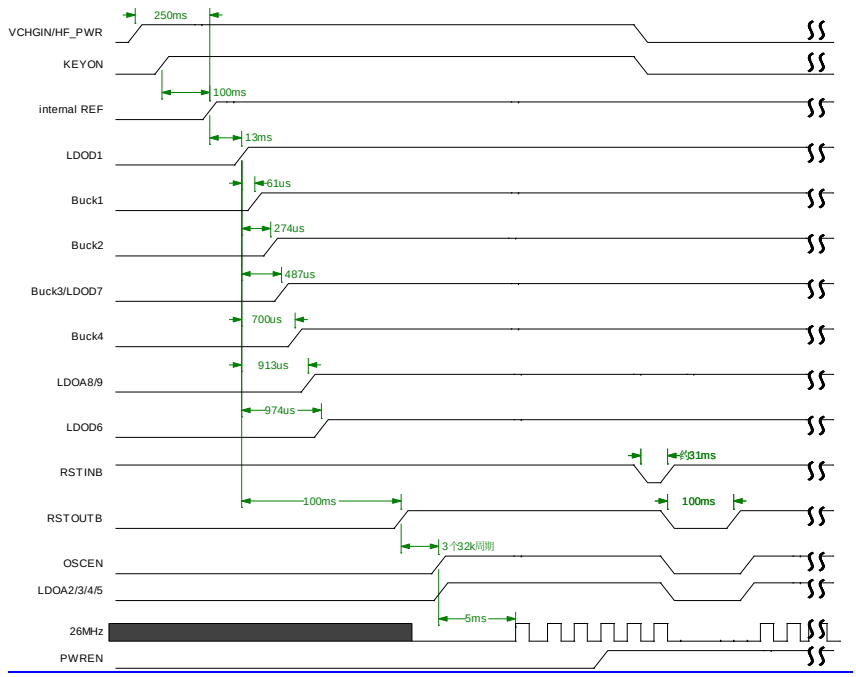

RSTINB hot reset timing

10.5 Interrupts

LC1132 provides plenty of interrupts for DBB, as listed below.

There are five combined interrupt sources, that is IRQST1, IRQST2, RTCIRQ, JKHSIRQ and CODECIRQ. Each combined interrupt has several individual interrupts. Software can read register IRQST first and then read individual interrupt status register to determin which interrupts occur.

Every interrupt has corresponding interrupt status, interrupt enable and interrupt mask. If specified interrupt condition occurs and it is alse enabled, interrupt status will be asserted. Interrupt mask control whether this interrupt is output to IRQ pin.

Interrupts generation and clear

Category	Name	Generation condition	Clearing
	CHGOV	Adaptor voltage is above 6V	Writing 1 to IRQST1.CHGOVIR bit
	CHGUV	Adaptor voltage is below 4.3V	Writing 1 to IRQST1.CHGUVIR bit
	RCHG	Battery voltage is below re-charge threshold (4V±150mV)	Writing 1 to IRQST1.RCHGIR bit

	BATOV	Battery voltage is above 4.5V	Writing 1 to IRQST1.BATOVIR bit
	BATUV	Battery voltage is below BATUV_TH	Writing 1 to IRQST1.BATUVIR bit
	BATOT	Battery temperature is hot or cold	Writing 1 to IRQST1.BATOTIR bit
IRQST2	TSD	Chip temperature reaches 110℃	Writing 1 to IRQST2.TSDIR BIT
	RTIM	Charging time reaches RTIM value	Writing 1 to IRQST2.RTIMIR bit
	CHGCP	Charging is completed	Writing 1 to IRQST1.CHGCPIR bit
	ADCCP	AD conversion is completed	Writing 1 to IRQST2.ADCCPIR bit
	KON	KEYON is pressed	Writing 1 to IRQST2.KONIR bit
	KOFF	KEYON is released	Writing 1 to IRQST2.KOFFIR bit
	ADPIN	Adaptor is plugged or HF_PWR pin transits from low to high	Writing 1 to IRQST2.ADPINIR bit
	ADPOUT	Adaptor is unplugged or HF_PWR pin transits from high to low	Writing 1 to IRQST2.ADPOUTIR
RTC	RTC	RTC constant cycle and alarm interrupts	Writing 1 to corresponding bit in RTC_INT_STATUS
Jack and hookswitch	JACKIN	Jack is inserted	Writing 1 to JKHSIRQ.JACKINIR
	JACKOUT	Jack is unplugged	Writing 1 to JKHSIRQ.JACKOUTIR
	HSUP	Hookswitch is pushed up	Writing 1 to JKHSIRQ.HSUPIR
	HSDN	Hookswitch is pushed down	Writing 1 to JKHSIRQ.HSDNIR
CODEC	CD_ALC	ClassD ALC interrupt	Writing 1 to R9.CD_ALC_CLR and then writing 0

	CD_DTS	ClassD over temperature	Writing 1 to R9.CD_DTS_CLR and then writing 0

The interrupts above are output via IRQ pin.

10.6 I²C interface

I2C interface uses two wires SCL and SDA for bi-directional communications between DBB and PMU. DBB acts as an I2C Master which generates Serial Clock Line (SCL), initiates and terminates data transfers. I2C interface of PMU acts as an I2C Slave which receives SCL and functions as slave-receiver and slave-transmitter. When 1.2MHz clock generated by internal oscillator is selected, only standard mode (100 KHz) is supported. When external input clock MCLK is selected, both Standard Mode and Fast Mode (400 KHz) are supported. ~~When external input clock CLK26M is selected, both Standard Mode and Fast Mode (400 KHz) are supported.~~

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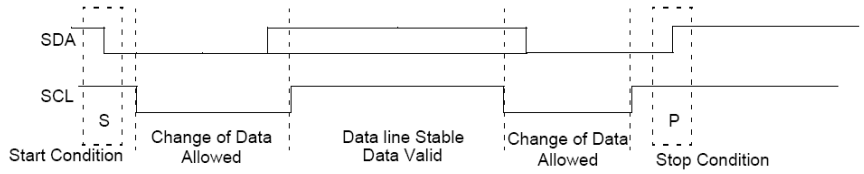
10.6.1 Basic data transactions

When the bus is idle, both SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start a transmission, it issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is high. When the master wants to terminate the transmission, it issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is high. Figure below shows the timing of the START and STOP conditions.

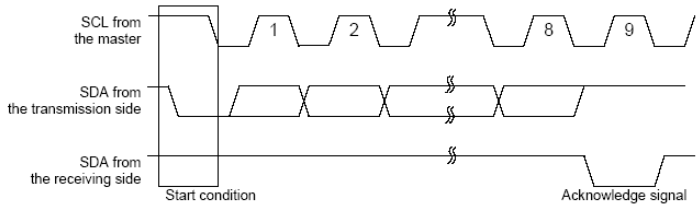


I²C START and STOP Condition

Each data transaction is composed of a START Condition, a number of byte transfers and a STOP condition. Every byte writtern to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

The Acknowledge cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer,.The transmitter releases the SDA line to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

If a master is the receiver, it must signal the end of data transmission to the slave-transmitter by not generating acknowledge signal on acknowledge clock pulse (9th clock). The slave transmitter must release SDA line to allow the master to generate a STOP condition.



I²C data transmission and acknowledge

10.6.2 I2C Slave address

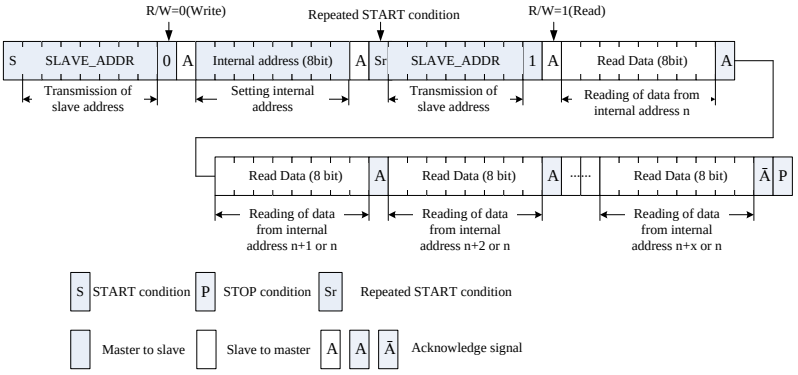
PMU supports 7-bit address format. The slave address of PMU is shown below.

A7	A6	A5	A4	A3	A2	A1
0	1	1	0	0	1	1

10.6.3 Data transmission read format

In order to read the internal register data:

- Master device generates a START condition
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0)
- Slave device sends acknowledge signal if the slave address is correct
- Master sends control register address (8 bits)
- Slave sends acknowledge signal
- Master device generates repeated START condition
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1)
- Slave sends acknowledge signal if the slave address is correct
- Slave sends data byte from addressed register
- If the master device sends acknowledge signal, the action of control register address has three choices: increased by one, fixed or only LSB increased, which is controlled by I2CCR. Then slave device sends data byte from addressed register
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates STOP condition.

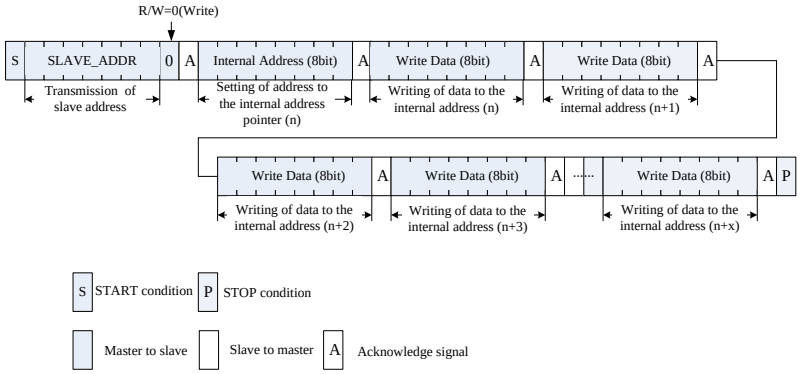


Read format

10.6.4 Data transmission write format

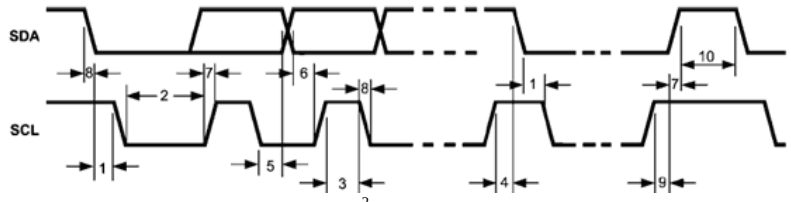
To write data to internal registers:

- Master device generates START condition
- Master device send slave address (7bits) and the data direction bit (r/w=0)
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8bits)
- Slave sends acknowledge signal
- Master sends data byte to be written to the addressed register
- Slave sends acknowledge signal
- If master will send further data bytes, the control register address will be increased by one after acknowledge signal
- Write cycle ends when master creates STOP condition



Write format

10.6.5 Timing Constraints



I²C Timing Diagram

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time(repeated)START Condition	0.6		us
2	Clock Low Time	1.3		us
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns

5	Data Hold Time (Output direction, delay generated by LC1132)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	300		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		us
C_B	Capacitive Load for Each Bus Line	10	200	pF

10.7 RTC

RTC operates with 32.768 KHz of external crystal and capacitor and is supplied either from RTCLDO when main battery is nomal or from backup battery when main battery voltage falls under 2.5V. RTC provides two alarm interrupts and sends interrupt to DBB via IRQ pin.

10.7.1 Time and date

RTC counts for second, minute, hour, day of month, day of week, month and year. The frequency of operation clock is 32.768 KHz, so one second contains 32768 clock cycles. Minute counter is increased by one every 60 seconds. Hour counter is increased by one every 60 minutes. Day of month counter enable signal is generated every 24 hours.

When day of month counter enable signal is valid, both day of week and day of month counters are increased by one. Day of week counts from 0 to 7, representing Sunday to Saturday. Valid value of day of month counter depends on month. There are 31 days in January, March, May, July, Auguest, October and December and 30 days in April, June, Septemper and November. February contains 29 days in leap year and 28 days in normal year. Month counter is increased by one at 00:00:00 on first day of a month. Month counter counts from 0 to 11, representing January to December. Year counter is increased by one every 12 months and counts from 0 to 99, representing 1980 to 2079.

10.7.2 RTC interrupt

RTC provides two types of interrupt: alarm interrupts and constant cycle interrupts.

Alarm interrupts contains alarm 1 and alarm 2. They are both second, minute, hour, day of month, month and year programmable. When RTC counters match the setting value, alarm interrupt will be generated.

Constant cycle interrupts contains:

- Second interrupt: asserted when second counter value changes
- Minute interrupt: asserted when minute counter value changes
- Hour interrupt: assted when hour counter value changes
- Day of month interrupt: asserted when day of month counter value changes

These interrupts are output through IRQ pin. Each interrupt has mask and enable bit. User can read interrupt status register to determine which interrupt occurs and clear it by writing 1.

- Interrupt enable

By writing to interrupt enable register RTC_INT_EN, user can control whether corresponding interrupt is enabled. DBB can enable multiple interrupts at one time.

- Interrupt clear

By writing 1 to corresponding bit of interrupt status register RTC_INT_STATUS, user can clear that interrupt.

- Interrupt generation

When interrupt is enabled and interrupt condition is satisfied, interrupt will be asserted.

- Interrupt mask

User can mask interrupt signal by setting interrupt mask register RTC_INT_MASK.

10.7.3 Clock calibration

RTC contains calibration function to calibrate 32.768 KHz clock. The software needs to calculate actual frequency of 32.768 KHz clock through other methods. Assuming that the actual frequency is f=fi+ff, where fi is integer section (Hz) and ff is fractional section. Setting RTC_SEC_CYC=fi , RTC_32K_ADJ= ff*3600 and then setting update register RTC_CALIB_UPDATE, clock calibration is accomplished.

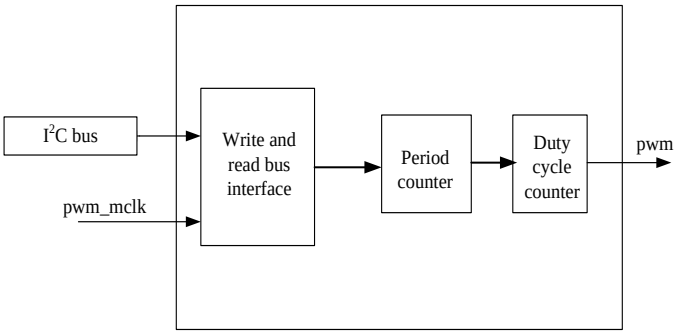
10.7.4 Power on alarm

If DBB shutdown PMU after it sets alarm interrupts, RTC continues to count. When programmed alarm time approaches, PMU will startup automatically. DBB can receive interrupt after PMU is powered on.

10.8 Buit-in PWM

This chip integrates a programmable PWM module for LCD backlight current sink control whose frequency and duty cycle can be adjusted.

10.8.1 Block diagram



The block diagram of PWM is shown above. The frequency of PWM pulse signal can be adjusted by setting the Period Configuration Register and the duty cycle of PWM pulse signal can be adjusted by setting the Duty Cycle Configuration Register.

The period counter starts counting from 0. When the count value adds up to the set value of Period Configuration Register, duty cycle counter will be added with 1 and period counter returns back to 0 and starts counting again. The duty cycle counter adds up from 0. When the value adds up to the set value of Duty Cycle Register, output pwm turns LOW and duty cycle counter continues to add. When the duty cycle counter counts to 49, the counter returns to 0 and start

counting again, while output pwm turns HIGH. Consequently a pulse signal is output whose frequency and duty cycle are adjustable.

10.8.2 Operation modes

By adjusting the values of Period Configuration Register and Duty Cycle Configuration Register, PWM can operate in three modes: fist is AM mode, where only duty cycleis adjusted with frequency unchanged; second is FM mode, where only frequency is adjusted with duty cycle unchanged; the third is AM&FM mode, where the duty cycle and frequency are adjusted simultaneously.

- **AM mode**

PWM only adjusts duty cycle of the clock in AM mode,that is, only adjusting the value of Duty Ratio Register. This is used to finely adjust the current of LCD current sink.

- **FM mode**

PWM only adjusts frequency of clock in FM mode,that is, only adjusting the value of the Period Configuration Register.

- **FM&AM mode**

PWM adjusts frequency and duty cycle of the clock simultaneously in FM&AM mode,that is, adjusting the value of Period Configuration Register and Duty Cycle Configuration Register at the same time.

10.8.3 Operation flow

PWM has three operating modes: AM, FM and FM&AM.

The following is a description of its software operation process with FM&AM mode as an example:

1. Set PWM_EN.PWM_EN bit to “0” to suspend the period couter and duty cycle counter
2. Write a new value to the Period Configuration Register and Duty Cycle Configuration Register.
3. Write “1” to PWM_UP.UPDATE bit to update the value of Period Register and Duty Cycle Register.
4. Set PWM_EN.PWM_EN bit to “1”， PWM operates with the new period and duty cycle value.

If you need to change the period and frequency, just repeat step 2 and 3.

For FM mode and AM mode, their software operation process is basically the same with that of FM&AM mode with ony one difference- only the Duty Cycle Configuration Register value needs to be set for AM mode and the Period Configuration Register value remains unchanged; only the Period Configuration Register value needs to be set for FM mode and the Duty Cycle Configuration Register value remains unchanged.

10.9 Test mode

The operation mode of PCU can be selected by external pin TEST. TEST pin is defined below.

TEST	MODE
0	function mode

1	test mode

Test mode contains three modes: normal scan mode , scan compression mode and fast power-on mode, which is controlled by pin DVS2 and DVS1.

DVS2	DVS1	MODE
0	X	fast power-on mode
1	0	Normal scan mode
1	1	Scan compression mode

In fast power-on mode, power on sequence is speed up and debounce function of KEYON and adaptor is masked. Reset time in power on sequence is reduced from 150ms to less than 1ms.
OTPMODE and OTPCMD registers can be used for OTP program in fast power-on mode, but they are invalid in other modes.

10.10 OTP test

OTP is one time programmable device which has two functions: controlling default settings and trimming analog modules. This chip adopts four 1x32-bits OTP Fuse macro. OTP can be programmed by adapting 6.5V power supply on VPP pin. Cells are initialized by ultraviolet light.
Before programming OTP, you need to determine the trimming values. If there are differences between test result and design spec but they are in the range of trimming, analog modules can be trimmed by OTP.
Trimming parameters can be determined in either function mode or test mode. After PMU is powered on, you can configure OTPSEL to 1 first and then write trimming parameters to TRIMx (x= 1,2,3,4) registers and test corresponding analog modules. If test results meet desgin requirements, the values of TRIMx are trimming values.
The meanings of TRIMx registers are defined below.

OTP Address	OTP bits	Equivalent Register	Trimming Parameters
0	0	TRIM0[0]	CHG_OTP_VREF[0]
	1	TRIM0[1]	CHG_OTP_VREF[1]
	2	TRIM0[2]	CHG_OTP_VREF[2]
	3	TRIM0[3]	CHG_OTP_VREF[3]
	4	TRIM0[4]	BG_OTP_VREF[0]
	5	TRIM0[5]	BG_OTP_VREF[1]
	6	TRIM0[6]	BG_OTP_VREF[2]
	7	TRIM0[7]	BG_OTP_VREF[3]
1	8	TRIM1[0]	CHG_OTP_VREF[4]
	9	TRIM1[1]	BG_OTP_VREF[4]
	10	TRIM1[2]	FREQ_OTP_SEL[0]
	11	TRIM1[3]	FREQ_OTP_SEL[1]
	12	TRIM1[4]	FREQ_OTP_SEL[2]

	13	TRIM1[5]	DC1_OTP_VOUT[0]
	14	TRIM1[6]	DC1_OTP_VOUT[1]
	15	TRIM1[7]	DC1_OTP_VOUT[2]
2	16	TRIM2[0]	DC2_OTP_VOUT[0]
	17	TRIM2[1]	DC2_OTP_VOUT[1]
	18	TRIM2[2]	DC2_OTP_VOUT[2]
	19	TRIM2[3]	DC3_OTP_VOUT[0]
	20	TRIM2[4]	DC3_OTP_VOUT[1]
	21	TRIM2[5]	DC3_OTP_VOUT[2]
	22	TRIM2[6]	
	23	TRIM2[7]	
3	24	TRIM3[0]	DC4_OTP_VOUT[0]
	25	TRIM3[1]	DC4_OTP_VOUT[1]
	26	TRIM3[2]	DC4_OTP_VOUT[2]
	27	TRIM3[3]	
	28	TRIM3[4]	LDOA2_OTP_VOUT[0]
	29	TRIM3[5]	LDOA2_OTP_VOUT[1]
	30	TRIM3[6]	LDOA3_OTP_VOUT[0]
	31	TRIM3[7]	LDOA3_OTP_VOUT[1]
4	32	TRIM4[0]	LDOA4_OTP_VOUT[0]
	33	TRIM4[1]	LDOA4_OTP_VOUT[1]
	34	TRIM4[2]	LDOA5_OTP_VOUT[0]
	35	TRIM4[3]	LDOA5_OTP_VOUT[1]
	36	TRIM4[4]	LDOA6_OTP_VOUT[0]
	37	TRIM4[5]	LDOA6_OTP_VOUT[1]
	38	TRIM4[6]	LDOA7_OTP_VOUT[0]
	39	TRIM4[7]	LDOA7_OTP_VOUT[1]
5	40	TRIM5[0]	LDOA8_OTP_VOUT[0]
	41	TRIM5[1]	LDOA8_OTP_VOUT[1]
	42	TRIM5[2]	LDOA9_OTP_VOUT[0]
	43	TRIM5[3]	LDOA9_OTP_VOUT[1]
	44	TRIM5[4]	LDOD1_OTP_VOUT[0]
	45	TRIM5[5]	LDOD1_OTP_VOUT[1]
	46	TRIM5[6]	LDOD2_OTP_VOUT[0]
	47	TRIM5[7]	LDOD2_OTP_VOUT[1]
6	48	TRIM6[0]	LDOD3_OTP_VOUT[0]
	49	TRIM6[1]	LDOD3_OTP_VOUT[1]
	50	TRIM6[2]	LDOD4_OTP_VOUT[0]
	51	TRIM6[3]	LDOD4_OTP_VOUT[1]
	52	TRIM6[4]	LDOD5_OTP_VOUT[0]
	53	TRIM6[5]	LDOD5_OTP_VOUT[1]

	54	TRIM6[6]	LDOD6_OTP_VOUT[0]
	55	TRIM6[7]	LDOD6_OTP_VOUT[1]
7	56	TRIM7[0]	LDOD7_OTP_VOUT[0]
	57	TRIM7[1]	LDOD7_OTP_VOUT[1]
	58	TRIM7[2]	LDOD8_OTP_VOUT[0]
	59	TRIM7[3]	LDOD8_OTP_VOUT[1]
	60	TRIM7[4]	LDOD9_OTP_VOUT[0]
	61	TRIM7[5]	LDOD9_OTP_VOUT[1]
	62	TRIM7[6]	LDOD10_OTP_VOUT[0]
	63	TRIM7[7]	LDOD10_OTP_VOUT[1]
8	64	TRIM8[0]	LDOD11_OTP_VOUT[0]
	65	TRIM8[1]	LDOD11_OTP_VOUT[1]
	66	TRIM8[2]	ADCLDO_OTP[0]
	67	TRIM8[3]	ADCLDO_OTP[1]
	68	TRIM8[4]	ADCLDO_OTP[2]
	69	TRIM8[5]	ADCLDO_OTP[3]
	70	TRIM8[6]	ADCLDO_OTP[4]
	71	TRIM8[7]	ADCLDO_OTP[5]
9	72	TRIM9[0]	LCD_OTP_TRIM[0]
	73	TRIM9[1]	LCD_OTP_TRIM[1]
	74	TRIM9[2]	LCD_OTP_TRIM[2]
	75	TRIM9[3]	LCD_OTP_TRIM[3]
	76	TRIM9[4]	KEYBOARD_LED_OTP_TRIM[0]
	77	TRIM9[5]	KEYBOARD_LED_OTP_TRIM[1]
	78	TRIM9[6]	KEYBOARD_LED_OTP_TRIM[2]
	79	TRIM9[7]	KEYBOARD_LED_OTP_TRIM[3]
10	80	TRIM10[0]	VIBRATOR_OTP_TRIM[0]
	81	TRIM10[1]	VIBRATOR_OTP_TRIM[1]
	82	TRIM10[2]	VIBRATOR_OTP_TRIM[2]
	83	TRIM10[3]	VIBRATOR_OTP_TRIM[3]
	84	TRIM10[4]	DC1_OTP_SLOPE[0]
	85	TRIM10[5]	DC1_OTP_SLOPE[1]
	86	TRIM10[6]	DC1_OTP_SLOPE[2]
	87	TRIM10[7]	DC2_OTP_SLOPE[0]
11	88	TRIM11[0]	DC2_OTP_SLOPE[1]
	89	TRIM11[1]	DC2_OTP_SLOPE[2]
	90	TRIM11[2]	DC3_OTP_SLOPE[0]
	91	TRIM11[3]	DC3_OTP_SLOPE[1]
	92	TRIM11[4]	DC3_OTP_SLOPE[2]
	93	TRIM11[5]	DC4_OTP_SLOPE[0]
	94	TRIM11[6]	DC4_OTP_SLOPE[1]

	95	TRIM11[7]	DC4_OTP_SLOPE[2]
12	96	TRIM12[0]	DC1_OTP_COMPRES[0]
	97	TRIM12[1]	DC1_OTP_COMPRES[1]
	98	TRIM12[2]	DC1_OTP_COMPRES[2]
	99	TRIM12[3]	DC1_OTP_COMPRES[3]
	100	TRIM12[4]	DC2_OTP_COMPRES[0]
	101	TRIM12[5]	DC2_OTP_COMPRES[1]
	102	TRIM12[6]	DC2_OTP_COMPRES[2]
	103	TRIM12[7]	DC2_OTP_COMPRES[3]
13	104	TRIM13[0]	DC3_OTP_COMPRES[0]
	105	TRIM13[1]	DC3_OTP_COMPRES[1]
	106	TRIM13[2]	DC3_OTP_COMPRES[2]
	107	TRIM13[3]	DC3_OTP_COMPRES[3]
	108	TRIM13[4]	DC4_OTP_COMPRES[0]
	109	TRIM13[5]	DC4_OTP_COMPRES[1]
	110	TRIM13[6]	DC4_OTP_COMPRES[2]
	111	TRIM13[7]	DC4_OTP_COMPRES[3]
14	112	TRIM14[0]	DC1OV_OTP[0]
	113	TRIM14[1]	DC1OV_OTP[1]
	114	TRIM14[2]	DC1OV_OTP[2]
	115	TRIM14[3]	DC2OV_OTP[0]
	116	TRIM14[4]	DC2OV_OTP[1]
	117	TRIM14[5]	DC2OV_OTP[2]
	118	TRIM14[6]	DC3OV_OTP[0]
	119	TRIM14[7]	DC3OV_OTP[1]
15	120	TRIM15[0]	DC3OV_OTP[2]
	121	TRIM15[1]	DC4OV_OTP[0]
	122	TRIM15[2]	DC4OV_OTP[1]
	123	TRIM15[3]	DC4OV_OTP[2]
	124	TRIM15[4]	LDOA234OV_OTP
	125	TRIM15[5]	LDOD1OV_OTP
	126	TRIM15[6]	
	127	TRIM15[7]	

OTP can be programmed only in test mode。Programming steps are shown below

1、 Write trimming values to TRIMx registers by I2C bus
2、 Configure OTPMODE=0x1
3、 Adjust the voltage of VPP from 3V to 6.5V
4、 Configure OTPCMD=0x4 to program byte 0 of OTP
5、 Wait at least 120us and then configure OTPCMD=0x5 to program byte 1 of OTP
6、 Wait at least 120us and then configure OTPCMD=0x6 to program byte 2 of OTP
7、 Wait at least 120us and then configure OTPCMD=0x7 to program byte 3 of OTP

8、 If not all bytes need to be programmed, select corresponding operation in steps 4-7

9、 Adjust voltage of VPP from 6.5V to 3V after program is finished

10、 Configure OTPMODE=0x0

After program, OTP can be read according to steps below to verify if program is successful.

1、 Configure OTPCMD=0x8 to update OTP data

2、 Read TRIMx registers via I2C bus to verify whether they are consistent with written values in program step.

10.11 DC-DC

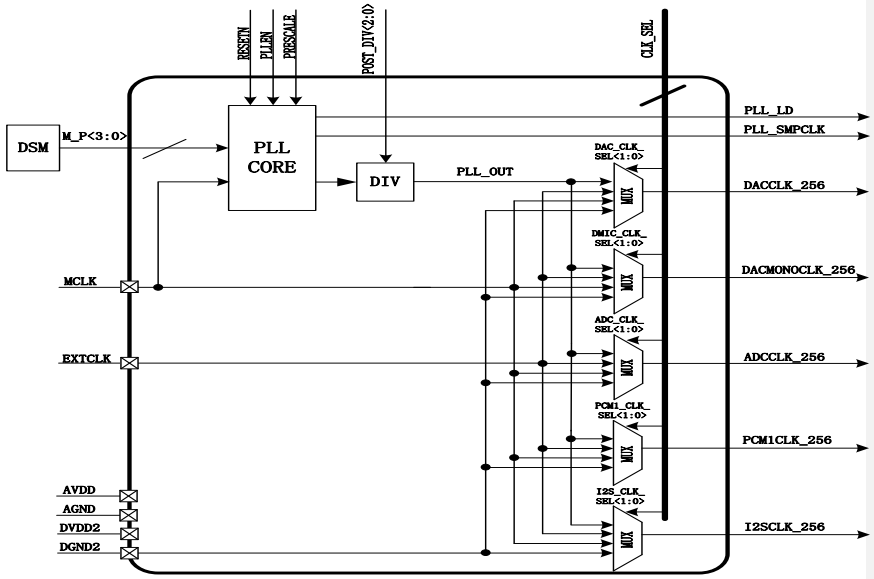
The LC1132 contains four high efficiency step down DCDC switching buck converters, capable of delivering a constant voltage from a single Li-Ion battery. Using a current mode architecture with synchronous rectification, the LC1132 has the ability to deliver up to 1.8A (Buck1, 2) and 600mA (Buck3, 4).

There are two modes of operation depending on the current required – PWM and PFM. PWM mode handles current loads of approximately 70mA or higher, delivering voltage precision of +/-3% with up to 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption and a longer battery life. User can force the buck converters to PWM mode by setting BUCKx_PWM_FORCE(x=1, 2, 3, 4) bit in Control Register. Besides PFM power saving feature, the buck-regulators inside the LC1132 also have low power operation mode, which has lower current consumption compare to PFM. The low power mode can be enabled when set DCx_LP_IN_SLP(x=1, 2, 3, 4) bit =1 in Control Register and OSCEN=0. However, the total load capability of bucks will be limited to 5mA when they operate at low power mode.

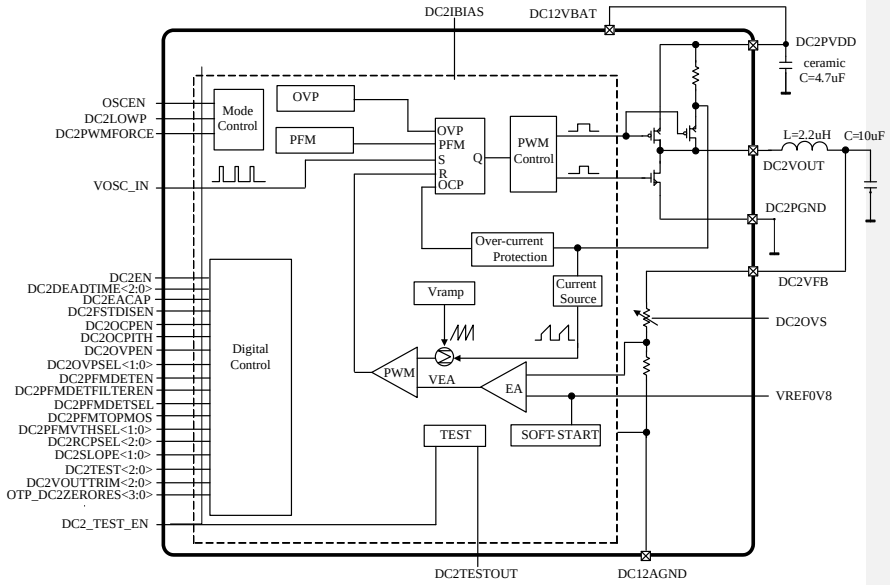
The Buck converters also have soft-start and over current protect.

Diagram of Buck converter is showed below.

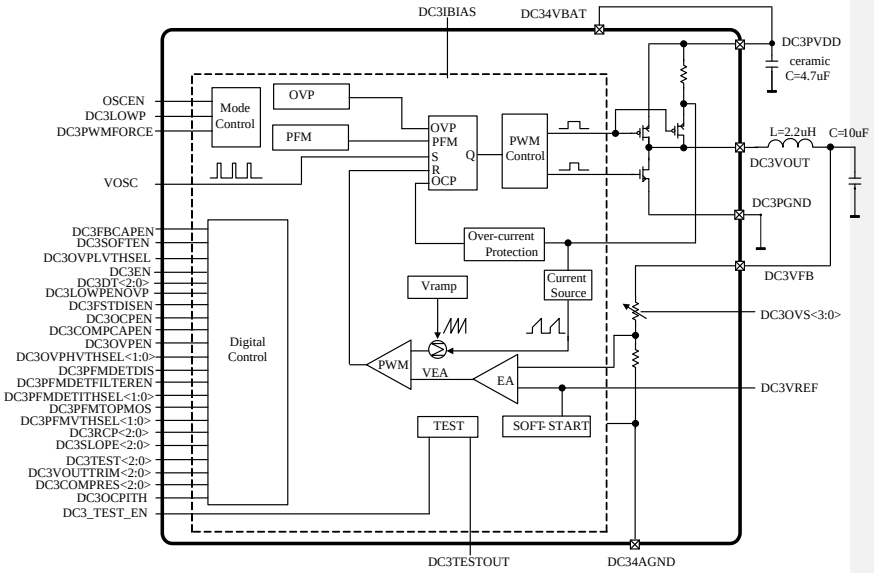
DC1



DC2



DC3/DC4



DCDC I/O list：

PADPINOUT	I/O	description
DC1PVDD	PWR	Power Supply
DC1PGND	GND	GND
DC1VFB	AO	Output Voltage
DC1VOUT	AO	DCDC Swtich pin ,Connect inductor
DC2PVDD	PWR	Power Supply
DC2PGND	GND	GND
DC2VFB	AO	Output Voltage
DC2VOUT	AO	DCDC Swtich pin ,Connect inductor
DC12VBAT	PWR	DCDC12 analog power
DC12AGND	PWR	DCDC12 analog gnd
DC3PVDD	PWR	Power Supply
DC3PGND	GND	GND
DC3VFB	AO	Output Voltage
DC3VOUT	AO	DCDC Swtich pin ,Connect inductor
DC4PVDD	PWR	Power Supply
DC4PGND	GND	GND
DC4VFB	AO	Output Voltage
DC4VOUT	AO	DCDC Swtich pin ,Connect inductor
DC34VBAT	PWR	DCDC34 analog power
DC34AGND	GND	DCDC34 analog gnd

DCDC internal list

DCDC1

PINOUT	I/O	description
DC1IBIAS	AI	DCDC1 current bias
VREF0V8	AI	DCDC1 reference voltage
VOSC_OUT	AO	DCDC1 oscillator output
DC1TESTOUT	DO	DCDC1 internal test point output
DC1EN	DI	DCDC1 enable signal 1: DCDC1 enable (default) 0: DCDC1 disable
DC1DEADTIME<2:0>	DI	DCDC1 non-overlapping time control 000: 0ns 001: 4ns (default) 010: 8ns 011: 12ns 100: 16ns 101: 20ns 110: 24ns 111: Reserved
DC1EACAP	DI	EA output high frequency capacitor select 1: EA cap connected 0: EA cap not connected (default)
DC1FSTDISEN	DI	DCDC1 fast discharge enable signal 1: Fast discharge enable (default) 0: Fast discharge disable
DC1OCPEN		DCDC1 over current protection control 1: OCP enable (default) 0: OCP disable
DC1OCPITH	DI	DCDC1 OCP threshold selection 1: 2.2A OCP (default) 0: 2A OCP
DC1OVPEN	DI	DCDC1 over voltage protection control 1: OVP enable (default) 0: OVP disable (not active in LP mode)
DC1OVPSEL<1:0>	DI	DCDC1 over voltage protection threshold select 00: Vout(1+40mV*Vout/0.7V) 01: Vout(1+30mV*Vout/0.7V) (default) 10: Vout(1+20mV*Vout/0.7V) 11: Reserved
DC1PFMDETEN	DI	DCDC1 load detection block for PFM or PWM 1: Enable 0: Disable (default)
DC1PFMDETFILTEREN	DI	DCDC1deglitch selection for load detection block 0: 1 clock circle

		1: 4 clock circle (default)
DC1PFMDETSEL	DI	DCDC1 load detection threshold selection 1:200mA to heavy load (50mA hysteresis) (default) 0: 150mA to heavy load (50mA hysteresis)
DC1PFMTOPMOS	DI	DCDC1 power PMOS control by PFMDET block 1: PFMDET block not control PMOS (default) 0: PFMDET block control PMOS
DC1PFMVTHSEL<1:0>	DI	DCDC1 PFM MODE threshold selection 00: 01: 10: 11:
DC1PWMFORCE	DI	DCDC1 PWM mode force 1: Force PWM mode (active with OSCEN=1) 0: PFM/PWM (default)
OSCEN	DI	DBB oscillator start signal 1: DBB normal mode 0: DBB sleep mode
DC1LOWP	DI	DCDC1 low power mode selection 1: LP mode (active with OSCEN=0) (default) 0: PFM/PWM
DC1RCPSEL<2:0>	DI	DCDC1 reverse current protection threshold 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV (default) 110: GND-SW=6mV 111: GND-SW=0mV
DC1SLOPE<1:0>	DI	DCDC1 slope compensation control 00: 1.5*slope 01: 1.25*slope 10: 1*slope (default) 11: 0.75*slope
DC1TEST<2:0>	DI	DCDC1 internal test point selection 000: No DCDC1 point for test 001: R 010: S 011: Q 100: OVP 101: PWM_MODE

		110: VOSCD 111: PGATE_D
DC1VOUTTRIM<2:0>	DI	DCDC1 output voltage trimming 000: +50mV 001: -50mV 010: -25mV 011: -10mV 100: +10mV 101: +25mV 110: +50mV 111: 0mV (default)
OTP_ DC1ZERORES<3:0>	DI	DCDC1 compensation net control 0000: Zero 53.6KHz, Fc=39K~78KHz 0001: Zero 40KHz, Fc=78K~157KHz 0010: Zero 26.8KHz, Fc=78K~157KHz 0011: Zero 20KHz, Fc=78K~157KHz 0100: Zero 40KHz, Fc=157K~314KHz 0101: Zero 20KHz, Fc=157K~314KHz 0110: Zero 13.4KHz, Fc=157K~314KHz 0111: Zero 10KHz, Fc=157K~314KHz 1000: Zero 30KHz, Fc=235K~470KHz 1001: Zero 15.2KHz, Fc=235K~470KHz 1010: Zero 10KHz, Fc=235K~470KHz 1011: Zero 6.7KHz, Fc=235K~470KHz 1100: Zero 6.7KHz, Fc=314K~628KHz 1101: Zero 26.8KHz, Fc=117K~235KHz 1110: Zero 17.9KHz, Fc=117K~235KHz 1111: Zero 13.4KHz, Fc=117K~235KHz (default)
OTP_DC1OSC <2:0>	DI	DC1 oscillator frequency adjust 000: 1.28MHz 001: 1.36MHz 010: 1.46MHz 011: 1.57MHz 100: 1.03MHz 101: 1.07MHz 110: 1.13MHz 111: 1.20MHz (default)
DC1_TEST_EN	DI	1: DC1 TEST enable 0:DC1 test disable

DCDC2

DC2IBIAS	AI	DCDC2 current bias
VREF0V8	AI	DCDC2 reference voltage
VOSC_IN	AO	DCDC1 oscillator for DCDC2

DC2TESTOUT	DO	DCDC2 internal test point output
DC2EN	DI	DCDC2 enable signal 1: DCDC2 enable (default) 0: DCDC2 disable
DC2DEADTIME<2:0>	DI	DCDC2 non-overlapping time control 000: 0ns 001: 4ns (default) 010: 8ns 011: 12ns 100: 16ns 101: 20ns 110: 24ns 111: Reserved
DC2EACAP	DI	EA output high frequency capacitor select 1: EA cap connected 0: EA cap not connected (default)
DC2FSTDISEN	DI	DCDC2 fast discharge enable signal 1: Fast discharge enable (default) 0: Fast discharge disable
DC2OCPEN		DCDC2 over current protection control 1: OCP enable (default) 0: OCP disable
DC2OCPITH	DI	DCDC2 OCP threshold selection 1: 2.2A OCP (default) 0: 2A OCP
DC2OVPEN	DI	DCDC2 over voltage protection control 1: OVP enable (default) 0: OVP disable (not active in LP mode)
DC2OVPSEL<1:0>	DI	DCDC2 over voltage protection threshold select 00: Vout(1+40mV*Vout/0.7V) 01: Vout(1+30mV*Vout/0.7V) (default) 10: Vout(1+20mV*Vout/0.7V) 11: Reserved
DC2PFMDETEN	DI	DCDC2 load detection block for PFM or PWM 1: Enable 0: Disable (default)
DC2PFMDETFILTEREN	DI	DCDC2 deglitch selection for load detection block 0: 1 clock circle 1: 4 clock circle (default)
DC2PFMDETSEL	DI	DCDC2 load detection threshold selection 1:200mA to heavy load (50mA hysteresis) (default)

		0: 150mA to heavy load (50mA hysteresis)
DC2PFMTOPMOS	DI	DCDC2 power PMOS control by PFMDET block 1: PFMDET block not control PMOS (default) 0: PFMDET block control PMOS
DC2PFMVTHSEL	DI	DCDC2 PFM MODE threshold selection 1: PFMDET block not control PMOS (default) 0: PFMDET block control PMOS
DC2PWMFORCE	DI	DCDC2 PWM mode force 1: Force PWM mode (active with OSCEN=1) 0: PFM/PWM (default)
OSCEN	DI	DBB oscillator start signal 1: DBB normal mode 0: DBB sleep mode
DC2LOWP	DI	DCDC2 low power mode selection 1: LP mode (active with OSCEN=0) (default) 0: PFM/PWM
DC2RCPSEL<2:0>	DI	DCDC2 reverse current protection threshold 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV (default) 110: GND-SW=6mV 111: GND-SW=0mV
DC2SLOPE<1:0>	DI	DCDC2 slope compensation control 00: 1.5*slope 01: 1.25*slope 10: 1*slope (default) 11: 0.75*slope
DC2TEST<2:0>	DI	DCDC2 internal test point selection 000: No DCDC1 point for test 001: R 010: S 011: Q 100: OVP 101: PWM_MODE 110: VOSCD 111: PGATE_D
DC2VOUTTRIM<2:0>	DI	DCDC2 output voltage trimming 000: +50mV 001: -50mV 010: -25mV

		011: -10mV 100: +10mV 101: +25mV 110: +50mV 111: 0mV (default)
OTP_ DC2ZERORES<3:0>	DI	DCDC1 compensation net control 0000: Zero 53.6KHz, Fc=39K~78KHz 0001: Zero 40KHz, Fc=78K~157KHz 0010: Zero 26.8KHz, Fc=78K~157KHz 0011: Zero 20KHz, Fc=78K~157KHz 0100: Zero 40KHz, Fc=157K~314KHz 0101: Zero 20KHz, Fc=157K~314KHz 0110: Zero 13.4KHz, Fc=157K~314KHz 0111: Zero 10KHz, Fc=157K~314KHz 1000: Zero 30KHz, Fc=235K~470KHz 1001: Zero 15.2KHz, Fc=235K~470KHz 1010: Zero 10KHz, Fc=235K~470KHz 1011: Zero 6.7KHz, Fc=235K~470KHz 1100: Zero 6.7KHz, Fc=314K~628KHz 1101: Zero 26.8KHz, Fc=117K~235KHz 1110: Zero 17.9KHz, Fc=117K~235KHz 1111: Zero 13.4KHz, Fc=117K~235KHz (default)
DC2_TEST_EN	DI	1: DC2TEST enable 0:DC2 test disable

DCDC3

PORT	I/O	description
DC3VREF	AI	Ref voltage
VOSC	AI	Oscillator from DCDC1
DC3IBIAS	AI	Current Bias
DC3TESTOUT	DO	Test signal
DC3EN	DI	1: DCDC3 enable(default) 0: DCDC3 disable
DC3OCPEN	DI	1: OCP enable 0: OCP disable(default)
DC3PWMFORCE	DI	1: FORCE PWM 0: PWM PFM auto control(default)
DC3PFMDETDIS	DI	1: PFMDET disable(default) 0: PFMDET enable
DC3LOWP	DI	1: Sleep in Lowp mode 0: Sleep in PFM mode(default)
OSCEN	DI	1: Normal Operating Mode 0: Sleep Mode
DC3OVS<3:0>	DI	Output Voltage Select 0000：1.05V 0001：1.1V 0010：1.15V 0011：1.2V

		0100：1.21V 0101：1.22V 0110：1.23V 0111：1.24V 1000：1.25V 1001：1.35V 1010：1.5V 1011：1.6V 1100：1.65V 1101：1.7V 1110：1.75V 1111：1.8V(default)
DC3SLOPE<2:0>OTP	DI	Slope Select 000：Mcap=6 001：Mcap=7 010：Mcap=8 011：Mcap=9 100：Mcap=2 101：Mcap=3 110：Mcap=4 111：Mcap=5 (default)
DC3RCP<2:0>	DI	RCP Select 000：GND-SW=42mV 001：GND-SW=36mV 010：GND-SW=30mV 011：GND-SW=24mV 100：GND-SW=18mV 101：GND-SW=12mV(default) 110：GND-SW=6mV 111： GND-SW=0mV
DC3OVPHVTHSEL<1:0>	DI	DC3 OVP High Vth Select 00：0.86 01：0.84 10：0.82 11：0.81 (default)
DC3OVPLVTHSEL	DI	DC3 OVP Low Vth Select 1: 0.81V 0: 0.805V(default)
DC3PFMVTHSEL<1:0>	DI	DC3 PFM Vth Select 00：0.3 (46mA) 01：0.4 (55mA) (default) 10：0.5 (77mA) 11：0.6 (114mA)
DC3PFMDETITHSEL<1:0>	DI	DC3 PFMDETVth Select Peak Current 11： ~~保留~~reserved 10：209mA 01：164mA(default) 00：119mA
DC3COMPRES<2:0>OTP	DI	Compensation Resistor Select 0000：350k 0001：750k 0010：150k

		0011: 550k 0100: 250k 0101:650 k 0110: 50k 0111: 450k 1000：300k 1001：700k 1010：100k 1011：500k 1100：200k 1101：600k 1110：0k 1111：400k(default)
DC3OVPEN	DI	1: OVP EN (default) 0: OVP Disable
DC3OCPITH	DI	DC3 OCP Ith Select 1:1270mA 0:1030mA(default)
DC3DT<2:0>	DI	DC3Deadtime select 000：0 001：4ns(default) 010：8ns 011：12ns 100：16ns 101：20ns 110：24ns 111：保留reserved
DC3FSTDISEN	DI	1：DC3FASTDIS enable(default) 0：DC3FASTDIS disable
DC3SOFTEN	DI	1：DC3Softstart enable (default) 0：DC3Softstart disable
DC3PFMTOPMOS	DI	1：PFMDET no control PMOS(default) 0：PFMDET control PMOS
DC3VOUTTRIM<2:0>OTP	DI	000：保留reserved 001：-50mV 010：-25mV 011: -10mV 100: +10mV 101: +25mV 110: +50mV 111: 0mV(default)
DC3FBCAPEN	DI	1：FBCAP enable(default) 0: FBCAP disable
DC3COMPCAPEN	DI	1：COMPCAP enable 0：COMPCAP disable(default)
DC3LOWPENOVP	DI	1：LOWP control OVP enable(default) 0: LOWP control OVP disable
DC3PFMDETFILTEREN	DI	1: DC3PFMDETFILTER enable(default) 0: DC3PFMDETFILTER disable
DC3TEST<2:0>	DI	000：保留reserved(default) 001：R 010：VOSC 011: PFM

		100: OVP 101: PFMDET 110: OCP 111: RCP
DC3_TEST_EN	DI	1: DC3TEST enable 0:DC3 test disable

DCDC4

PORT	I/O	description
DC4VREF	AI	Ref voltage
VOSC	AI	Oscillator from DCDC1
DC4IBIAS	AI	Current Bias
DC4TESTOUT	DO	Test signal
DC4EN	DI	1: DCDC3 enable(default) 0: DCDC3 disable
DC4OCPEN	DI	1: OCP enable 0: OCP disable(default)
DC4PWMFORCE	DI	1: FORCE PWM 0: PWM PFM auto control(default)
DC4PFMDETDIS	DI	1: PFMDET disable(default) 0: PFMDET enable
DC4LOWP	DI	1: Sleep in Lowp mode 0: Sleep in PFM mode(default)
OSCEN	DI	1: Normal Operating Mode 0: Sleep Mode
DC4OVS<3:0>	DI	Output Voltage Select 0000：0.9V 0001：0.95V 0010：1.0V 0011：1.05V 0100：1.1V 0101：1.15V 0110：1.2V(default) 0111：1.21V 1000：1.22V 1001：1.23V 1010：1.24V 1011：1.25V 1100：1.35V 1101：1.5V 1110：1.7V 1111：1.8V
DC4SLOPE<2:0>OTP	DI	Slope Select 000：Mcap=6 001：Mcap=7 010：Mcap=8 011：Mcap=9 100：Mcap=2 101：Mcap=3 110：Mcap=4

		111： Mcap=5 (default)
DC4RCP<2:0>	DI	RCP Select 000：GND-SW=42mV 001：GND-SW=36mV 010：GND-SW=30mV 011：GND-SW=24mV 100：GND-SW=18mV 101：GND-SW=12mV(default) 110：GND-SW=6mV 111： GND-SW=0mV
DC4OVPHVTHSEL<1:0>	DI	DC3 OVP High Vth Select 00：0.86 01：0.84 10：0.82 11：0.81 (default)
DC4OVPLVTHSEL	DI	DC3 OVP Low Vth Select 1: 0.81V 0: 0.805V(default)
DC4PFMVTHSEL<1:0>	DI	DC3 PFM Vth Select 00：0.2 01：0.3 （65mA） 10：0.4 (89mA) (default) 11：0.5 (111mA)
DC4PFMDETITHSEL<1:0>	DI	DC3 PFMDETVth Select Peak Current 11：~~保留~~reserved 10：231mA 01：183mA(default) 00：130mA
DC4COMPRES<2:0>OTP	DI	Compensation Resistor Select 0000：350k 0001：750k 0010：150k 0011: 550k 0100: 250k 0101:650 k 0110: 50k 0111: 450k 1000：300k 1001：700k 1010：100k 1011：500k 1100：200k 1101：600k 1110：0k 1111：400k(default)
DC4OVPEN	DI	1: OVP EN (default) 0: OVP Disable
DC4OCPITH	DI	DC3 OCP Ith Select 1:1270mA 0:1030mA(default)
DC4DT<2:0>	DI	DC3Deadtime select 000：0 001：4ns(default) 010：8ns

		011：12ns 100：16ns 101：20ns 110：24ns 111：保留reserved
DC4FSTDISEN	DI	1：DC3FASTDIS enable(default) 0：DC3FASTDIS disable
DC4SOFTEN	DI	1：DC3Softstart enable (default) 0：DC3Softstart disable
DC4PFMTOPMOS	DI	1：PFMDET no control PMOS(default) 0：PFMDET control PMOS
DC4VOUTTRIM<2:0>OTP	DI	000：保留reserved 001：-50mV 010：-25mV 011: -10mV 100: +10mV 101: +25mV 110: +50mV 111: 0mV(default)
DC4FBCAPEN	DI	1：FBCAP enable(default) 0: FBCAP disable
DC4COMPCAPEN	DI	1：COMPCAP enable 0：COMPCAP disable(default)
DC4LOWPENOVP	DI	1：LOWP control OVP enable(default) 0: LOWP control OVP disable
DC4PFMDETFILTEREN	DI	1:DC3PFMDETFILTER enable(default) 0: DC3PFMDETFILTER disable
DC4TEST<2:0>	DI	000：保留reserved(default) 001：R 010：VOSC 011: PFM 100: OVP 101: PFMDET 110: OCP 111: RCP
DC4_TEST_EN	DI	1: DC4TEST enable 0:DC4 test disable

10.12 Regulators for digital

10.12.1 General description

LC1132 have eleven Low Drop Output regulators for Digital, LDOD1 to LDOD11.

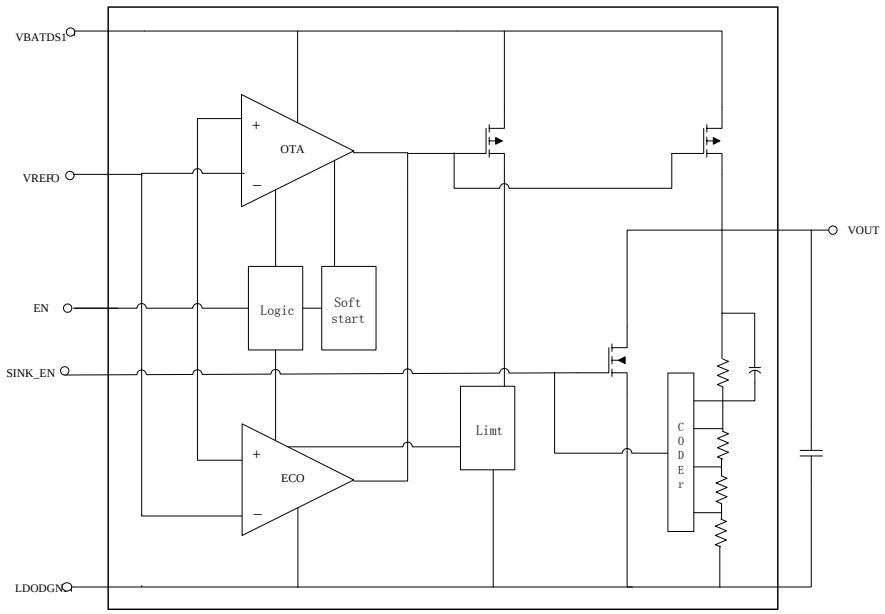
There are three regulators which output can drive 300mA current, and two regulators which maximal output current is 250mA, and three regulators which can give out 200mA output current.

The power supply of digital regulators is battery, except the 1.8V power supply of ~~LDOD10 and~~ LDOD11 is DCDC34.

Power on/off of each regulator can be controlled independently by setting data to each control bit through I2C-Bus.And Power on/off of LDOD7, LDOD9 and LDOD11 can be controlled independently by each external input pin.

For optimized phase compensation, bypass capacitor must be a ceramic type bigger than 1uf.
The regulators which output current capability more than 250mA are LDOD1, LDOD7, LDOD8, LDOD10 and LDOD11.
LDOD10 and LDOD11 have soft start function. LDOD6 startup when adapter is inserted.

10.12.2 LDO for Digital Block Diagram



10.12.3 LDO for Digital ~~Pin~~ PAD and ~~Port~~ PIN Description

External analog PAD Name	Type	Description
VBATDS1	I	Power supply for LDOD
LDODGND	I	GND for LDOD

带格式表格

Internal PIN Name	Type	Description
VOUT	O	Output of LDOD bapass capacitor is 1uf
EN	I	Enable control for LDOD
ECO	I	ECO mode control for LDOD1
LIM1_EN	I	Overcurrent protection control for LDOD
LIM2_EN	I	Shortcircuit protection control for LDOD
SOFT_EN	I	Softstart control for LDOD
SINK_EN	I	Discharge control for LDOD
OCP	O	Over current interrupt signal:

带格式表格

		OCP=1:overcurrent OCP=0:don't overcurrent
D<3:0>	I	1.8V-3.0V Programmable 4 signal bits
SEL	I	1.8V/3.0V selectable signal bit
OTP2.85	I	1.8V/3.0V selectable LDO's 2.85V OTP trimming bit
OTP<1:0>	I	±50mV 2 OTP trimming bits
VREF1.5	I	1.5V bias voltage
FB	P	Feedback of LDOD
V_	P	Negative port of OPA

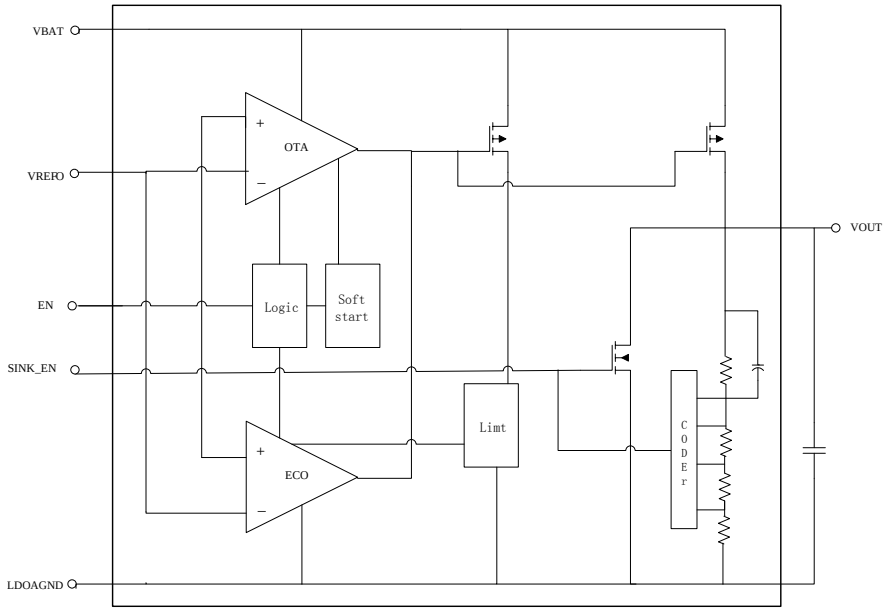
PIN Name	I/O	Description
VBAT	I	Power supply for LDOD
GND	I	GND for LDOD
VOUT	O	Output of LDOD bapass capacitor is 1uf
EN	I	Enable control for LDOD
ECO	I	ECO mode control for LDOD1
LIM1_EN	I	Overcurrent protection control for LDOD
LIM2_EN	I	Shortcircuit protection control for LDOD
SOFT_EN	I	Softstart control for LDOD
SINK_EN	I	Discharge control for LDOD
OCP	O	Overcurrent interrupt signal: OCP=1:overcurrent OCP=0:don't overcurrent
D<3:0>	I	1.8V-3.0V Programable 4 signal bits
SEL	I	1.8V/3.0V selectable signal bit
OTP2.85	I	1.8V/3.0V selectable LDO's 2.85V OTP trimming bit
OTP<1:0>	I	±50mV 2 OTP trimming bits
VREF1.5	I	1.5V bias voltage
FB	P	Feedback of LDOD
V_	P	Negative port of OPA

10.13 Regulators for analog

10.13.1 General description

LC1132 has eight Low Drop Output regulators for Analog, LDOA2 to LDOA9.
There are three regulators which output can drive 300mA current.
LDOA6 and LDOA7 are programmable.The power supply of analog regulators is battery.
Power on/off of each regulator can be controlled independently by setting data to each control bit through I2C-Bus.And Power on/off of LDOA2,LDOA3,LDOA4,LDOA5 and LDOA7 can be controlled independently by each external input pin.
For optimized phase compensation, bypass capacitor must be a ceramic type bigger than 1uf.

10.13.2 LDO for Analog Block Diagram



10.13.3 LDO for Analog ~~Pin~~ PAD and ~~Port~~ PIN Description

External analog PAD Name	Type	Description
VBAT	I	Power supply for LDOA（VBATA23，VBATA45，VBATA6789）
LDOAGND	I	GND for LDOA

Internal PIN Name	Type	Internal PIN Name
VOUT	O	Output of LDOA, bapass capacitor is 1uf
EN	I	Enable control for LDOA
ECO	I	ECO mode control for LDOA
LIM1_EN	I	Overcurrent protection control for LDOA
LIM2_EN	I	Shortcircuit protection control for LDOA
SOFT_EN	I	Softstart control for LDOA
SINK_EN	I	Discharge control for LDOA
OCP	O	Overcurrent interrupt signal: OCP=1:overcurrent OCP=0:don’t overcurrent
D<3:0>	I	1.8V-3.0V Programmable 4 signal bits

带格式表格

SEL	I	1.8V/3.0V selectable signal bit
OTP2.85	I	1.8V/3.0V selectable LDO's 2.85V OTP trimming bit
OTP<1:0>	I	±50mV 2 OTP trimming bits
VREF1.5	I	1.5V bias voltage
FB	P	Feedback of LDOA
V_	P	Negative port of OPA

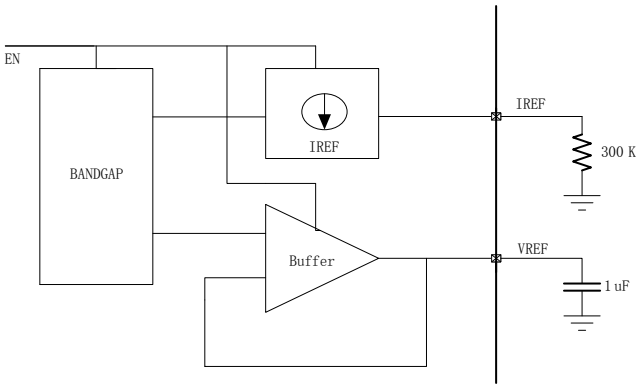
PIN Name	I/O	Description
VBAT	I	Power supply for LDOA（VBATA23，VBATA45，VBATA6789）
GND	I	GND for LDOA
VOUT	O	Output of LDOA, bapass capacitor is 1uf
EN	I	Enable control for LDOA
ECO	I	ECO mode control for LDOA
LIM1_EN	I	Overcurrent protection control for LDOA
LIM2_EN	I	Shortcircuit protection control for LDOA
SOFT_EN	I	Softstart control for LDOA
SINK_EN	I	Discharge control for LDOA
OCP	O	Overcurrent interrupt signal: OCP=1:overcurrent OCP=0:don't overcurrent
D<3:0>	I	1.8V 3.0V Programable 4 signal bits
SEL	I	1.8V/3.0V selectable signal bit
OTP2.85	I	1.8V/3.0V selectable LDO's 2.85V OTP trimming bit
OTP<1:0>	I	±50mV 2 OTP trimming bits
VREF1.5	I	1.5V bias voltage
FB	P	Feedback of LDOA
V_	P	Negative port of OPA

10.14 VREF/IREF Specification

10.14.1 General description

LC1132 reference circuit contains VREF and IREF circuits. The VREF circuit generates 1.5V bandgap reference voltage with 1uf outside bypass ceramic capacitor. The IREF circuit generates several 1uf reference current by 300kohm outside resistor. The 300kohm resistor's precision cannot exceed ±1%.

10.14.2 VREF and IREF Block Diagram



VREF and IREF Block Diagram

10.14.3 VREF and IREF PAD and PIN Description

I/O list of VREF and IREF block

External analog PAD Name	Type	Description
VREFB	AO	The 1.5V reference voltage with 1uf capacitor
IREFB	AIO	The 300Kohm resistor PAD

Internal PIN Name	Type	Description
AVDD	AIO	Power supply
AGND	AIO	GND
OTP_BG_VREF<4:0>	DI	The 1.5V bandgap voltage 5 bits OTP trimming signal
pcu2ibias_en	DI	The enable signal of ibias
pcu2vref_en	DI	The enable signal of vref
VBGOK	DO	The VBG1p5 get ready signal: 1: get ready 0:don’t OK
VBG1p5	AO	The 1.5V bandgap voltage

10.15 A/D Converter

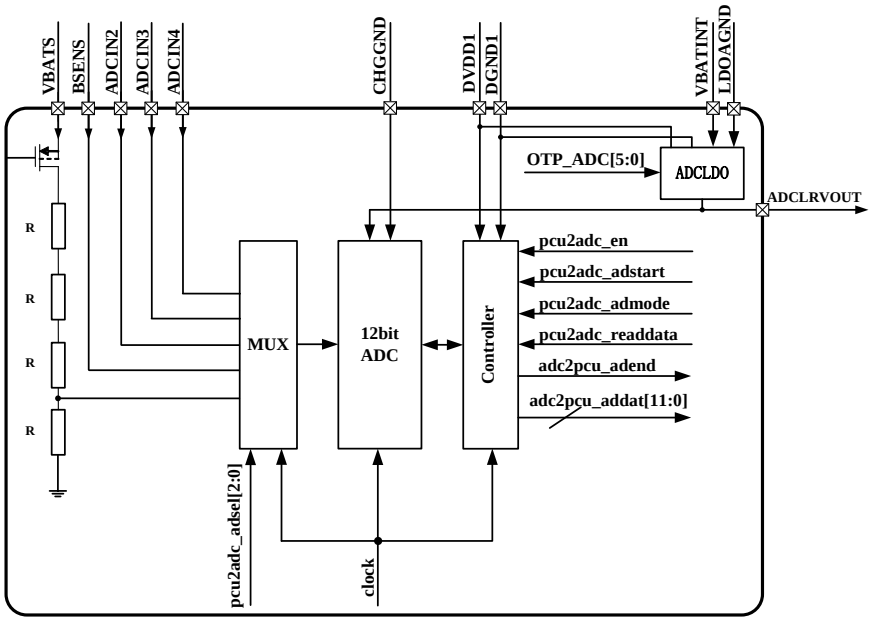
10.15.1 General Description

This ADC is a 12-bit charge redistribution successive approximation analog-to-digital converter (ADC) that operates under a single 2.8V power supply, ADCLRVOUT, which is generated by an internal ADCLDO. It operates under an internal-540KHz conversion clock which provided by the Digital Part. This converter contains 5 analog inputs: the first two are internal set for battery voltage-measurement and temperature-measurement,respectively, while the 3rd, 4th and 5th measure the signals imported by the pad ADCIN2, ADCIN3, and ADCIN4. These 5 channels can be selected by configuring a related register through I2C serial interface (NOTE: the battery voltage which is sensed by channel 1 is divided into 1/4 before it is sampled by the converter). This part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit, which can sample an analog input IN+ between 0 V to VREF with respect to a ground sense IN−. The reference voltage, VREF, 2.8V, is also supplied by the internal LDO, the same as ADCLRVOUT.

This converter is both available to be singly and continuously triggered. In single trigger mode, when the register which triggers the ADC is written through I2C serial interface, it begins to convert. After the conversion finish, the Digital Part informs the MCU by an interrupt, and then the conversion results can be read by the MCU. But in continuous trigger mode, when the MCU read the conversion results, it will also trigger the ADC to begin a new sample and conversion.

The input channel is selected by the register-pcu2adc_adsel[2:0], and the operating mode(single or continuous) is controlled by the register-pcu2adc_mode. They should be configured before the converter is enabled. What’s more, the converter shouldn’t be enabled before 12 more clocks from the output of internal LDO have already been stable.

10.15.2 Block Diagram



ADC Top Diagram

10.15.3 PAD Description

PAD Name	I/O	Description
VBATINT	I	ADC LDO analog power supply
LDOAGND	I	ADC LDO analog ground
ADCLRVOUT	O	ADC LDO output and ADC analog power supply and VREF
CHGGND	I	ADC analog ground
DVDD1	I	ADC and ADC LDO digital power supply
DGND1	I	ADC and ADC LDO digital ground
VBATS	I	battery voltage
BSENS	I	battery temperature indication voltage
ADCIN2	I	ADC external input
ADCIN3	I	ADC external input
ADCIN4	I	ADC external input

10.15.4Internal PIN Description

PIN Name	I/O	Description
clock	I	clock
pcu2adc_en	I	enable signal
pcu2adc_adstart	I	conversion start signal
pcu2adc_admode	I	mode select signal

pcu2adc_readdata	I	MCU read signal
pcu2adc_adsel[2:0]	I	3bits channel select signal
adc2pcu_adend	O	conversion finish signal
adc2pcu_addat[11:0]	O	12bits output data
OTP_ADC[5:0]	I	6bits OTP register for ADC LDO output voltage

10.15.5 Application information

5 channels for different measurements:

Channel 1 monitors the battery voltage:

$$V_{in1} = \frac{(0XXX)_{dec}}{4096} \times 2.8V \times 4$$

Channel 2 measures the battery temperature:

$$V_{in2} = \frac{(0XXX)_{dec}}{4096} \times 2.8V$$

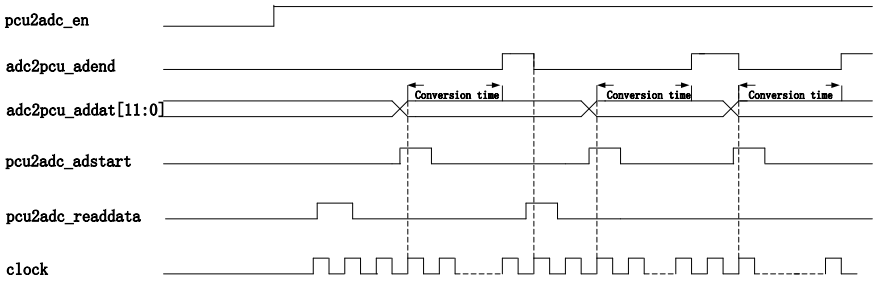
Channel 3 measures external input ADCIN[2:4], which can be used in Touch Screen measurement:

$$V_{in} = \frac{(0XXX)_{dec}}{4096} \times 2.8V$$

2 operating modes for different applications:

Single trigger mode:

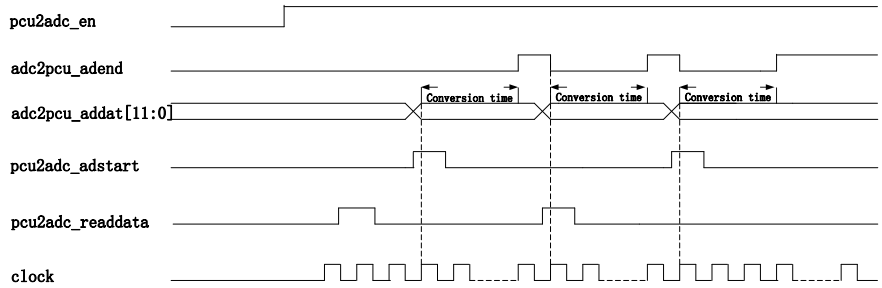
On the pcu2adc_adstart rising edge, the circuit begins to convert, where pcu2adc_adstart holds for 1 clock. When the conversion finishes, adc2pcu_adend turns to be high. But if pcu2adc_readdata is high, then adc2pcu_adend will be set to be low on the 1st clock rising edge, and ADC stop working.



Single trigger mode clock diagram

Continuous trigger mode:

On the pcu2adc_adstart rising edge, the circuit begins to convert, where pcu2adc_adstart holds for a clock. When the conversion finishes, adc2pcu_adend turns to be high. But if pcu2adc_readdata is high, then adc2pcu_adend will be set to be low on the first clock rising edge, and ADC begins a new conversion. And it can also begin a new conversion on the first clock rising edge after pcu2adc_ad start turns to be high.



Continuous trigger mode clock diagram

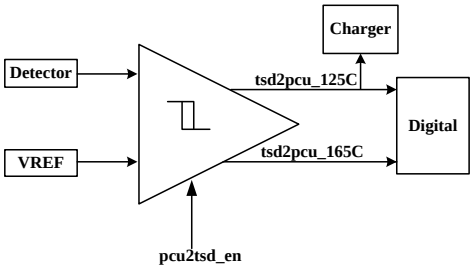
10.16 Thermal shut down circuit

A thermal shut down circuit is designed for over temperature protection in LC1132. This circuit detects the chip temperature so it is placed near to the big power dissipation device such as charger or DCDC. There are two threshold points: one for over temperature alarm to limit the charging current, and the other for shut down the whole chip.

Table1-1 IO list of TSD

IO Name	I/O Type	Description
pcu2tsd_en	Internal DI	Enable signal to TSD
tsd2pcu_125C	Internal DO	Chip temperature 125 degree alarm
tsd2pcu_165C	Internal DO	Chip temperature 165 degree alarm

10.16.1 Block Diagram



Thermal shut down block diagram

10.16.2 Function Description

There are two voltage references with different temperature coefficient. The over temperature threshold can be got using these two voltage compare. Two comparators are used to set two over temperature points, which comparator has hysteresis feature to avoid unstable decision. When temperature is higher than the lower point TSD_L, it will give an output signal to PCU and PMU charger block, to limit the charging current to a lower level. When temperature is higher than the higher point TSD_H, the output signal shut down the whole chip. This block can be enable or disabled by PCU control signal.

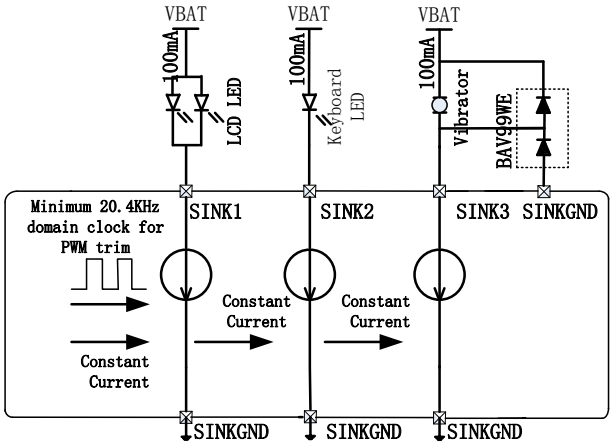
10.17 Current sink

10.17.1 General Description

The current sink used in LC1132 design for LED display application and vibrator, and it provides users with great flexibility and device performance. Users may adjust the output current from 10mA to 100mA with the help of logic circuits, which gives users flexibility in controlling the light intensity of LEDs and the vibration intensity of vibrator.

It can support the following feature:

- Output current invariant to load voltage change
- Constant output current range: 10~100mA
- 3.2~4.5V supply voltage
- Supports bi-directional current trimming
- PWM Dimming function (only for Sink1)



Current Sink schematic diagram

IO list of Current Sink

Interface	IO Name	I/O TYPE	Description
Current Sink	SINK1	AI	Current sink channel for LCD
	SINK2	AI	Current sink channel for keyboard
	SINK3	AI	Current sink channel for vibrator
	SINKGND	GND	Current sink ground

10.17.2 Current Sink Function Description

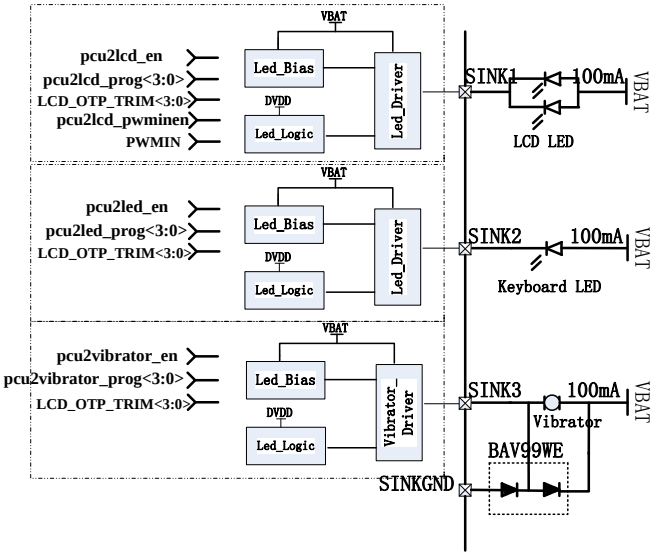


Diagram of Current Sink

The schematic diagram of current sink system is shown above. It consists of three blocks. The Sink1 is used to providing driving current for mobile phone LCD backlight; Sink2 can be used to provide driving current for mobile phone keyboard LED backlight; Sink3 is aimed to drive mobile phone vibrator circuit. Each block has the same structure. It consists of 3 blocks:

- Led bias circuit is Ultra-low power voltage reference circuit, and its quiescent current < 4uA
- Led logic circuit could change input signal from DVDD1 to VBAT domain, , with the help of the 11 level shifts.
- Led driver circuit, contains 4 individual constant-current output channels. Through the Led logic circuit, the output current can be adjusted and up to 100mA max .And with the help of the RC trimming circuits, the output current can be bi-directional trimmed, range from -23.2% to +37.8%.

Each sink needs to be supported constant current working mode. When sink is working, led logic circuits can convert the input signal from DVDD1 to VBAT domain, and then by the help of these converted signals, at sink output stage, 4 regulated current output channels can be set to provide current sinks for driving LEDs and vibrator.

In addition, Sink1 is compatible with true color PWM Dimming working mode. When the signal(pcu2lcd_pwminen) is enabled， the Sink1Sink1 could deal with the PWM signal. The minimum operating frequency of PWM signal is 20.4 KHz.

Sink1**Pin list of Current Sink**

PIN Name	I/O Type	Description
pcu2lcd_en	DI	Sink1 enable signal
pcu2lcd_pwminen	DI	PWM input enable signal
PWMIN	AI	PWM signal input

带格式的：字体：（默认）Times New Roman，五号，（中文）中文(中国)，（其他）英语(美国)

pcu2lcd_prog<3:0>	DI	Sink1 driving current selection 0001: 10mA 0010: 20mA 0100: 30mA 1000: 40mA 1001: 50mA 1010: 60mA 1100: 70mA 1101: 80mA 1110: 90mA 1111:100mA
LCD_OTP_TRIM<3:0>	DI	Sink1、Sink2 and Sink3 driving current trimming selection
BG_VERF1V5	AI	Sink1、Sink2 and Sink3 voltage bias signal
SINK1_IBIAS1U	AI	Sink1 current bias signal
SINK1	AO	Sink1 driving current output
pcu2led_en	DI	Sink2 enable signal
pcu2led_prog<3:0>	DI	Sink2 driving current selection 0001: 10mA 0010: 20mA 0100: 30mA 1000: 40mA 1001: 50mA 1010: 60mA 1100: 70mA 1101: 80mA 1110: 90mA 1111:100mA
SINK2_IBIAS1U	AI	Sink2 backlight module current bias signal
SINK2	AO	Sink2 backlight module driving current output
pcu2vibrator_en	DI	Sink3 enable signal
pcu2vibrator_prog<3:0>	DI	Sink3 driving current selection 0001: 10mA 0010: 20mA 0100: 30mA 1000: 40mA 1001: 50mA 1010: 60mA 1100: 70mA 1101: 80mA 1110: 90mA 1111:100mA
SINK3_IBIAS1U	AI	Sink3 current bias signal

SINK3	AO	Sink3 driving current output
VBATINT	PWR	Power supply for Analog part of Current sink
DVDD1	PWR	Power supply for digital part of Current sink

10.18 RTC & PMU digital parts supply

10.18.1 RTC OSC

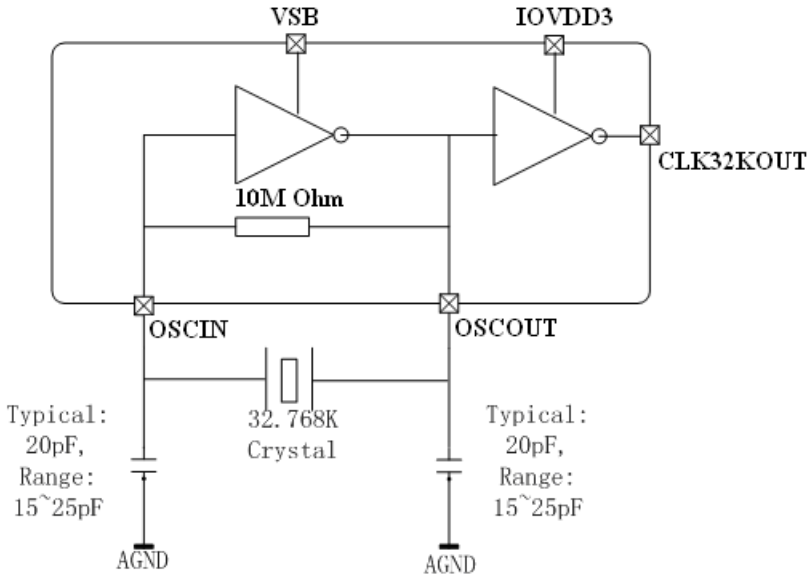
Real Time Clock module in LC1132 provides the second backup battery control circuit and 2-system of alarm function, which generate an interrupt on a set time. The accuracy of clock is dependant on the Clock Error Offset circuit. Real Time Clock operates with a frequency of 32.768 KHz, and it can output a digital clock with IOVDD3 domain to DBB.

It can support the following feature:

- Get power from main battery or backup battery (main battery removed)
- Clock and Calendar display
- Alarm clock function
- 32.768KHz clock output
- Support for 12-hour or 24-hour clock format selection
- High-accuracy clock error offset circuit function
- Interrupt function and RTC alarm clock interrupt for PMU power on factor

Table IO list of RTC OSC

IO Name	I/O Type	Description
VSB	PWR	Power supply for RTC
IOVDD3	PWR	RTC output clock buffer power
OSCIN	AI	One terminal of Crystal
OSCOUT	AO	One terminal of Crystal
CLK32KOUT	DO	RTC clock output



RTC OSC schematic diagram

10.18.2 Backup battery and PMU digital supply

The schematic diagram of backup battery system is shown below.

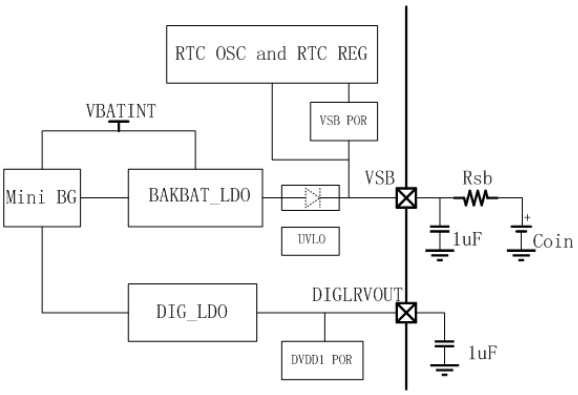


Diagram of backup battery system and DIGLDO

It including:

- Ultra-low power bandgap reference circuit, quiescent current < 2uA
- A regulator BAKBAT_LDO included for backup battery charging, with an output pin

named VSB connected to backup battery. This regulator has a programmed output voltage 2.6V, 2.8V, 3V (default) and 3.2V, with 5mA maximum drive ability. A built-in diode is designed for preventing current reversal, so the external diode is not needed.

- DIG_LDO provides supply for only PMU digital, with 1.8V output voltage and no more than 3uA quiescent ground current, maximum output capacity of 5mA.

RTC parts can get supply from main battery or backup battery. When the main battery exists and the battery voltage is bigger than 2.7V, the BAKBAT_LDO works as a backup battery charger, and supplies power for RTC parts. When the main battery is removed or the battery voltage drops less than 2.5V, the charging path for backup battery is cut off to prevent the reversed current to main battery, while the RTC parts get supply from backup battery.

A Linear regulator DIG_LDO is designed for PMU digital parts. Which is sharing mini bandgap reference with backup battery charger, the output voltage is 1.8V, 5mA driving ability, and a built-in POR circuit for digital parts power on reset.

Table IO list of RTC OSC

IO Name	I/O Type	Description
VSB	PWR	Supply for RTC parts
DIGLRVOUT	PWR	Supply for PMU digital parts
VBAT2V7	Internal AI	Battery deep discharge detect voltage
ISO_VBAT_VSB	Internal DO	Deep discharge or battery removed signal
BAKBAT_SEL<1:0>	Internal DI	Set output voltage of VSB 00: 3V, 01:2.8V, 10:2.6V, 11: 3.2V

10.19 Charger Specification

10.19.1 General description

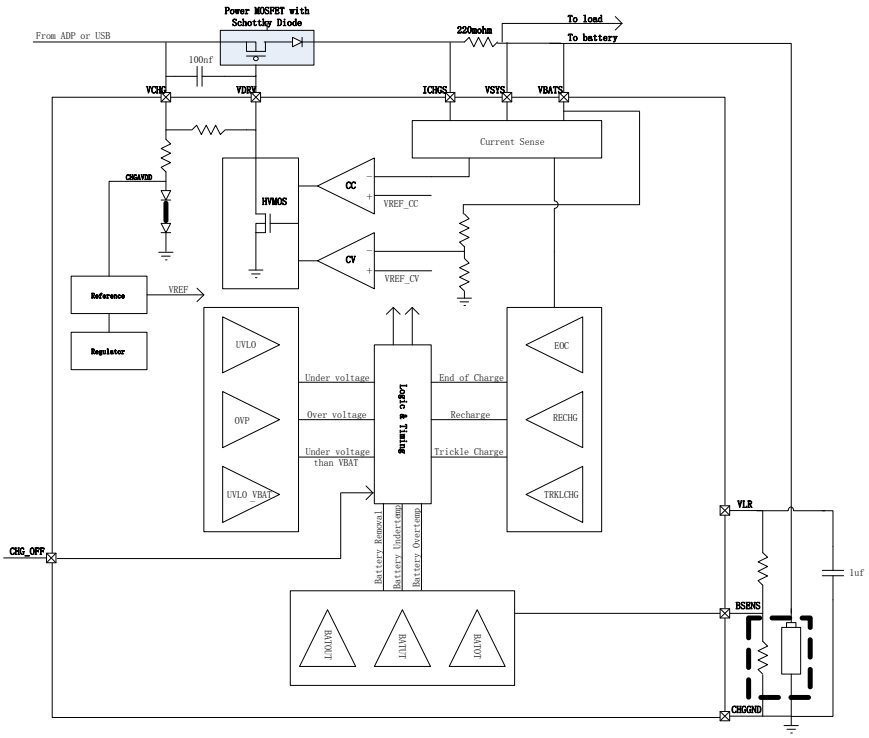
LC1132 supports AC-adapter charging and USB charging. The battery charge LOOP contains the Constant-voltage amplifier, Constant-current amplifier, Charge current sense circuit, Reference voltage source, Charge control circuit and several Protection circuits. The Charger control circuit contains Comparators for charge current monitor, Charge completion detecting circuit and Recharge detecting circuit. The Protection circuits include Comparators for charging voltage monitor, over voltage detecting circuit for battery voltage, Detecting circuits for battery presence and battery temperature.

Its main features are:

- Single input - AC adapter or USB

- CC/CV linear charging
- Selectable battery regulation voltage for 4.2V~4.4V
- Flexible charging cycle control
- Wide array of charging current from 100mA to 1.2A
- Selectable end of charge current from 50mA to 200mA
- Selectable recharge voltage
- Safety timer
- Power supply for no battery application
- Ni-H battery charge application

10.19.2 CHARGER Block Diagram

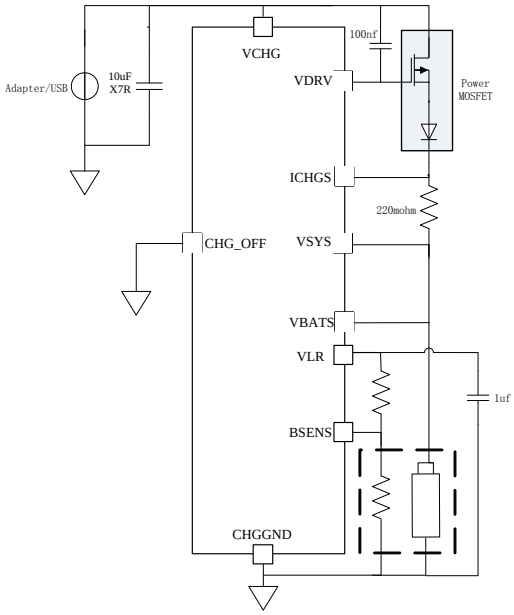


Charger block diagram

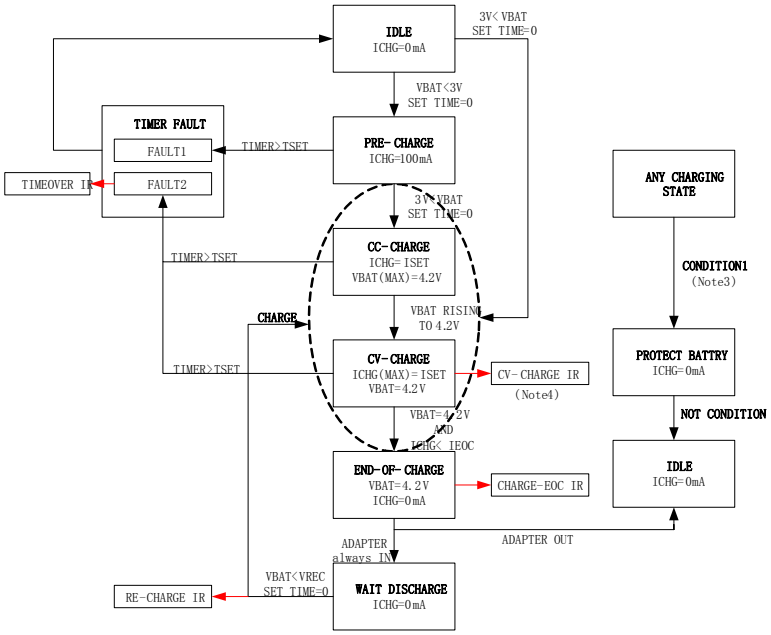
10.19.2.1 Baterry charge mode and function description

The register BATSEL is setted by I^2C to control the charge mode is Ni-H Battery or Li Battery. The default mode is Li battery charge mode and BATSEL=0.

10.19.2.2 Li Battery charge mode



Li Battery charge mode application diagram



Li Battery charge state diagram

IDEL state: charger initial prepare state.

PRE-CHARGE state: the battery voltage is smaller than 3V protection voltage, and the

trickle charge current is 100mA in this state.

CHARGE state: CHARGE state contains constant current charge, constant voltage and end of charge stage. The most charge current and most battery voltage are limited in CHARGE state.

When the battery voltage is smaller than 4.2V, charger works at constant current charge state. The charge current can be set from 100mA to 1.2A, default is 400mA..

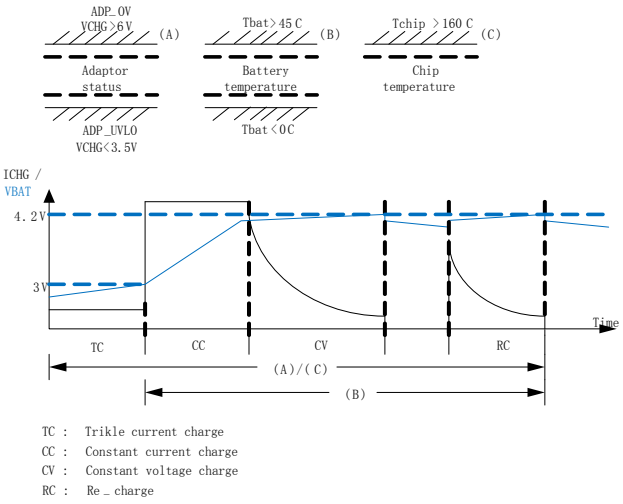
When the battery voltage raise to 4.2V, charge current began to decrease, and charger enter constant voltage charge state which state's battery voltage is limited. When charge current reduces to charge complete current, charger enters in end of charge state.

WAIT DISCHARGE state: when the charger complete charge state, charger come into WAIT DISCHARGE state. In this state battery began to discharge, and return to charge state when the battery voltage decreases to recharge voltage.

BATOUT OR BAD-BATTRY state: when battery voltage is smaller than 2V, battery is considered out of battery or battery is bad, and charger is estimated at BATOUT OR BAD-BATTRY state.

PROTECT BATTERY state: when the power supply voltage or battery voltage abnormal, the temperature of battery or chip abnormal, the charge process is shut down forcedly to protect battery, and change into PROTECT BATTERY state to wait.

TIMER FAULT state: when charging is overtime in trickle or fast charge state, the charge process comes into TIMER FAULT state to stop charge.



Li Battery charge process diagram

Note1: In Li battery charge mode, protection occurs at any condition as follows happened:

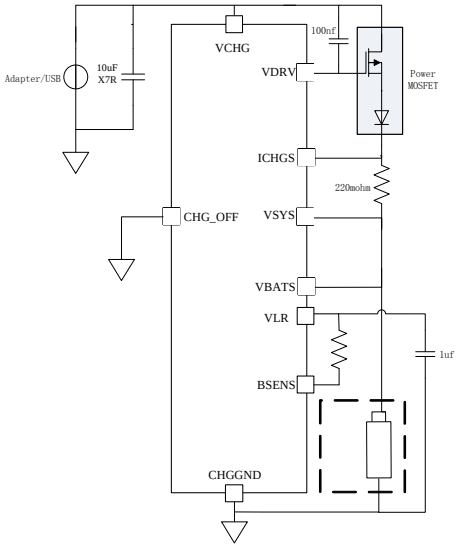
1) When adaptor or USB voltage is more than 6V, give out adaptor overvoltage interrupt.
2) When adaptor or USB voltage is smaller than 3.5V, give out adaptor under voltage interrupt.
3) When adaptor or USB voltage is smaller than battery voltage, give out adaptor under voltage interrupt.
4) When battery voltage is more than 4.5V, give out battery overvoltage interrupt
5) When battery temperature is smaller than 0 degree or more than 45 degree, give out battery temperature abnormal interrupt.

6) Chip temperature more than 160 degree.

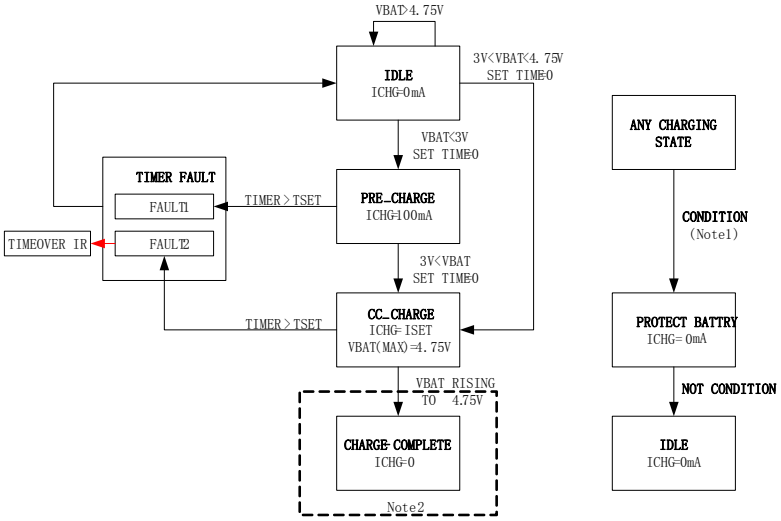
7) Charge time over 7 hours.

Note2: when the battery voltage is more than 4.13V/4.3V, give out CV interrupt but don't come into CV charge state.

10.19.2.3 Ni-H Battery charge mode



Ni-H Battery charge mode application diagram



Ni-H Battery charge state diagram

IDEL state: charger initial prepare state.

PRE-CHARGE state: the battery voltage is smaller than 3V protection voltage, and the small charge current is 100mA in this state.

CC CHARGE state: when the battery voltage is more than 3V, charger enter constant current charge state automatically. The charge current can be set from 100mA to 1.2A, default is 400mA..

CHARGE COMPLETE state: when the ADC within PMU detect battery voltage is raise to 4.75V in CC CHARGE state, charger turn into CHARGE COMPLETE state. Software control current setting register to decrease charge current, or set ACHGON register to shut down battery charger.

PROTECT BATTERY state: when the power supply voltage abnormal, or temperature of chip abnormal, the charge process is shut down forcedly to protect battery, and change into PROTECT BATTERY state to wait.

TIMER FAULT state: when the charge is overtime in trickle or fast charge state, come into TIMER FAULT state to stop charge.

Note3: In Ni-H battery charge mode, protection occurs at any condition as follows happened:

1) When adaptor or USB voltage is more than 6V, give out adaptor overvoltage interrupt.
2) When adaptor or USB voltage is smaller than 3.5V, give out adaptor under voltage interrupt.
3) When adaptor or USB voltage is smaller than battery voltage, give out adaptor under voltage interrupt.
4) Chip temperature more than 160 degree.
5) Charge time over 7 hours.

Note4: Ni-H Battery CHARGE COMPLETE state is estimated by the ADC within PMU, and must controlled by Software, can not shunt down by self.

10.19.3 CHARGER PAD and PIN Description

I/O list of charger block

External analog PAD Name	Type	Description
VCHG	AIO	Power supply for charger block
VDRV	AO	External power PMOS control
ICHGS	AIO	Input for detecting charging-current
VSYS	AIO	System output from charger
VBATS	AIO	Main battery connection(short to VSYS)
BSENS	AI/O	Input for detecting battery present and battery temperature
VLR	AO	2.8V reference voltage from charger with 1uf bypass capacitor
CHG_OFF	AI	Charger function disable when external charger used. 0：internal charger enable 1/floating：external charger used，internal charger function disable
CHGGND	AIO	Ground of charger block

Internal analog PIN Name	Type	Description

CHGAVDD	AIO	Power supply for analog block
VSB	AIO	Power supply for high voltage digital block
DVDD	AIO	Power supply for low voltage digital block
DGND	AIO	Ground of digital block
VREF_1V2	AI	1.2V Reference voltage form VBATS domain
CHG_IBIAS_BAT	AI	1uA Reference current from VBATS domain
VBAT_2V7	AO	2.7V battery voltage detection to VBATS domial
Internal digital PIN Name	Type	Description
CHG_OTP_VREF<0:4>	DI	CV voltage 5bits OTP trimming signal 00000：+15mV 00001：+30mV 00010：+45.5mV 00011：+61mV 00100：+77.5mV 00101：+94mV 00110：+110mV 00111：+127mV 01000：+145mV 01001：+163mV 01010：+181.5mV 01011：+200mV 01100：+219mV 01101：+238mV 01110：+258mV 01111：+278mV 10000：-194.5mV 10001：-183mV 10010：-171mV 10011：-159mV 10100：-147mV 10101：-135mV 10110：-122.5mV 10111：-110mV 11000：-97mV 11001：-84mV 11010：-70.5mV 11011：-57mV 11100：-43mV 11101：-29mV 11110：-14.5mV 11111：0（default）
pcu2chg_accsel<3:0>	DI	Adapter/USB charging current selection signal 0000：100mA 0001：200mA

		0010：300mA 0011：400mA (default) 0100：500mA 0101：600mA 0110：700mA 0111：800mA 1000：900mA 1001：1000mA 1010：1100mA 1011：1200mA others：600mA
pcu2chg_achgon	DI	Charger function enable signal 0: disable 1: enable (default)
pcu2chg_vbatdeten	DI	Battery voltage detection enable signal 0: disable 1: enable(default)
pcu2chg_batsel	DI	Battery type selection signal 0: Li-ion battery (default) 1: Ni-H battery
pcu2chg_cvsel	DI	Li-ion battery CV setting signal 0: 4.2V (default) 1: 4.35V
pcu2chg_cvadj<1:0>	DI	CV voltage adjust signal 00: 0V(default) 01: +25mV 10: +50mV 11：+50mV
pcu2chg_ntcen	DI	Battery temperature detection enable signal 0: disable (default) 1: enable
pcu2chg_eocen	DI	Charging auto end function enable signal 0: disable (default) 1: enable
pcu2chg_ccpc<1:0>	DI	Charging complete current selection signal 00：50mA (default) 01：100mA 10：150mA 11：200mA
pcu2chg_reccmpen	DI	Re-charging comparator enable signal 0: disable(default) 1: enable
pcu2chg_recstatus	DI	Recharging status signal 0:recharge end(default)

		1:recharge
pcu2chg_rchgsel<2:0>	DI	Recharge threshold selection signal 111：CV-400mV 3.8V@vbat=4.2V 110：CV-350mV 101：CV-300mV 100：CV-250mV 011：CV-200mV 010：CV-150mV (default) 001：CV-100mV 000：CV-50mV 4.15V@vbat=4.2V
pcu2chg_prot	DI	Charger abnormal status automatic protection signal 0：disable 1：enable (default)
Pcu2chg_rtimov	DI	Charging timeout signal 0：Charging(default) 1：Time out
pcu2chg_test<3:0>	DI	Internal test point selection 1111：work mode（default） Others：test mode
pcu2chg_hyssel	DI	EOCCMP and RECCMP hys voltage seletion signal 0：50mV(default） 1：70mV~90mV
pcu2chg_batuvth<1:0>	DI	Low battery voltage alarm threshold setting signal 00：3.52V(default) 01：3.6V 10：3.65V 11：3.7V
pcu2chg_eoccmpout_filter	DI	End of charge cmp out status after digital filter
pcu2chg_csens_ctrl	DI	End of charge current sense source contrl signal 0：VBAT current is the csens 1：VSYS current is the csens(default)
CHG_OT125C	DI	125 degree over temperature signal 0: don’t exceed 125 degree 1: exceed 125 degree
CHG_OT160C	DI	160 degree over temperature signal 0: don’t exceed 160 degree 1: exceed 160 degree
BAT_UVLO	DI	Low voltage detection of VBAT 1:battery under voltage 0:battery don’t under voltage
chg2pcu_adpin	DO	Adaptor/USB insert/removal status 0：adp<3.5V 1：adp>3.8V

chg2pcu_adpov	DO	Adaptor over voltage detection status 0：adp<6V-150mV 1：adp>6V
chg2pcu_adpuvcmp_out	DO	Adaptor under voltage detection status 0：ADP>VBAT+180mV 1：ADP<VBAT
chg2pcu_batout	DO	Battery present/removal status 0：present, 1：removal, CV mode
chg2pcu_batot	DO	Battery temperature abnormal alarm status 0：temp normal 1：bat temp abnormal
chg2pcu_batu3b	DO	Battery voltage below 3V status 0：vbat<3V 1：vbat>3V+150mV
chg2pcu_batv32	DO	Battery voltage over 3.2V status 0：vbat<3.2V-150mV 1：vbat>3.2V
chg2pcu_batu33b	DO	Under voltage alarm of battery status 0：vbat<3.4V 1：vbat>3.4V+150mV
chg2pcu_batv45	DO	Battery voltage above 4.5V status 0：vbat<4.5V-150mV 1：vbat>4.5V
chg2pcu_eoc	DO	End of charge status 0：chargeing 1：end of charge
chg2pcu_shdnb	DO	Abnormal shutdown charger signal 0:abnormal shutdown charger 1:enable charger
chg2pcu_trkl	DO	Trickle charge signal 0：vbat>3V 1：vbat<3V-150mV
chg2pcu_eoccmpout	DO	End of charge cmp out status 0：Ichg>Ichg_eoc+25mA 1：Ichg< Ichg_eoc,end of charge
chg2pcu_cvcmpout	DO	CV cmp out status 0：vbat<4.125V/4.3V-100mV 1：vbat>4.125V/4.3V
chg2pcu_rchgcmpout	DO	Recharge cmp out status 0：vbat>vbat_rec+50mV 1：vbat<vbat_rec,recharge

10.19.4 Charger block interrupt

1) adapter state interrupt:

CHGINIR: adaptor or USB insert interrupt

CHGOUTIR: adaptor or USB pull out interrupt

CHGOVIR: adaptor or USB voltage is over 6V interrupt

CHGUVLOIR: adaptor or USB voltage under VBATS voltage interrupt

2) Battery state interrupt:

BATOVIR: battery voltage over 4.5V interrupt (Li Battery charge mode available)

BATUVIR: battery voltage is under 3.52V interrupt

BATOTIR: battery temperature abnormal interrupt

3) charge state interrupt

CHGCPIR: charge complete interrupt (Li Battery charge mode available)

RCHGIR: recharge interrupt (Li Battery charge mode available)

CHGCVIR: battery voltage more than 4.13V/4.3V interrupt (Li Battery charge mode available)

RTIMIR: charger over time interrupt

10.19.5 Application diagram

Li Battery and Ni-H battery charge mode application diagram:

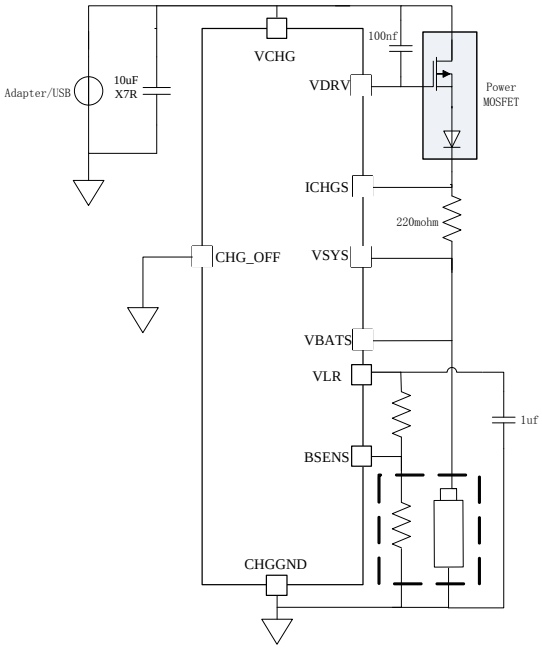
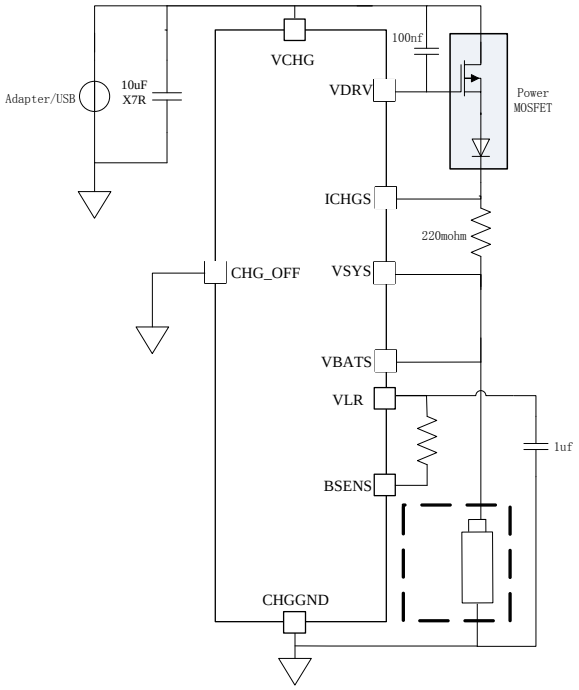


Diagram Li Battery charge mode application diagram



Ni-H Battery charge mode application diagram

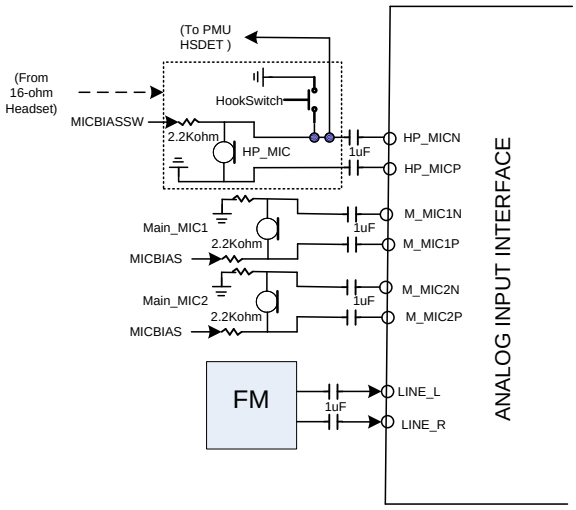
11 Codec Functional Description

11.1 Introduction

The codec part of LC1132 is a high performance audio subsystem that supports both analog and digital audio functions. This part includes a high quality stereo DAC, a mono DAC, a high quality stereo ADC, a stereo headphone amplifier that supports ground referenced output cap-less operation, a earpiece speaker amplifier, and a low EMI Class D loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices. The codec part of LC1132 features dual bi-directional I2S or PCM audio interfaces for full range audio and an I2C compatible interface for control. The stereo DAC path features an SNR of 96dB with 24-bit 48 kHz input. The headphone amplifier delivers 30mW (typ) to a 32Ω single-ended load with less than 1% distortion (THD+N). The earpiece speaker amplifier delivers 55mW (typ) to a 16Ω load with less than 1% distortion. The loudspeaker amplifier delivers up to 800mW into an 8Ω load with less than 1% distortion. The LC1132 employs advanced techniques to reduce power consumption, to reduce controller overhead, to speed development time, and to eliminate click and pop.

11.2 Analog Input Interface

Generation Description and function



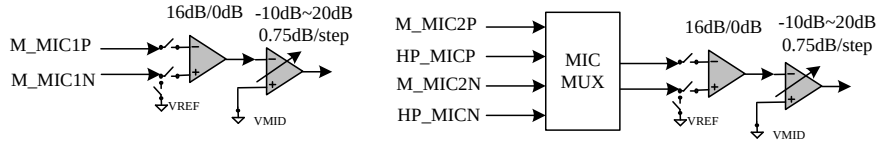
LC1132 have four pairs of analog input channel, Main Mic1, Main Mic2, Headphone Mic& Line input.

11.3 PGA

11.3.1 MIC PGA

11.3.1.1 Generation Description and function

MIC PGA includes MIC selection between HP MIC and Main MIC and MIC PGA (6-36dB). The MIC inputs are either single end or pseudo differential input.



A pseudo differential input is the preferential configuration where the positive terminal of the input PGA is connected to the MICP input pin by setting MICP2INP=1. And the MICP not connected to input PGA (when MICP2INP=0).

Alternatively a single ended microphone can be connected to the MICN input with MICN2INN set to 1. The non-inverting terminal of the input PGA should be connected internally to VREF by setting MICN2INN to 0.

In differential mode the larger signal should be input to MICP and the smaller (e.g. noisy ground connection) should be input to MICN.

The PGA gain is logarithmically adjustable from +6dB to 36dB in 0.75dB steps. The gain is independently adjustable on PGA channel. Setting MICZCEN, bit enables a zero-cross detector

which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting MICZCST

11.3.1.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
Reg24	7			
	6	MIC1_0_16_SEL	1	MIC1 1st PGA gain. 0: 0dB; 1: 16dB (Default) (Note:Total gain=1st PGA gain+2nd PGA gain)
	5:0	MIC1_PGA_LEVEL	000000	MIC1 2nd PGA gain 000000: -10db(Default) 000001: -9.25db 000010: -8.5db …0.75db/step 101000:20db 101001~111111: reserved (20db)
RegR40 Reg40	7			
	6	MIC2_0_16_SEL	1	MIC2 1st PGA gain. 0: 0dB; 1: 16dB (Default) (Note:Total gain=1st PGA gain+2nd PGA gain)
	5:0	MIC2_PGA_LEVEL	000000	MIC2 2nd PGA gain 000000: -10db(Default) 000001: -9.25db 000010: -8.5db …0.75db/step 101000:20db 101001~111111: reserved (20db)
RegR0	7			
	6	MIC2PGAZCEN	0	Main MIC2 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
	5	MIC2PGAMU	1	MainMIC2 PGA Mute signal 0: Un-Mute; 1:Mute
	4	MIC2PGAEN	0	MainMIC2 PGA Enable signal 1: MIC2PGA Enable; 0:MIC2PGA Power Down
	3			
	2	MIC1PGAZCEN	0	Main MIC1 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
	1	MIC1PGAMU	1	MainMIC1 PGA Mute signal 0: Un-Mute; 1:Mute
	0	MIC1PGAEN	0	MainMIC1 PGA Enable signal 1: MIC1PGA Enable; 0:MIC1PGA Power Down

RegR85	6	M_MIC1N2INN	1	Connect MIC1N to input PGA negative terminal.(Main Mic) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	5	M_MIC1P2INP	0	Connect input PGA amplifier positive terminal to MIC1P or VREF. (Main Mic) 0=input PGA amplifier positive terminal connected to VREF 1=input PGA amplifier positive terminal connected to MIC1P through variable resistor string
	4	HP_MICN2INN	1	Connect MICN to input PGA negative terminal.(HP Mic) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	3	HP_MICP2INP	0	Connect input PGA amplifier positive terminal to MICP or VREF. (HP Mic) 0=input PGA amplifier positive terminal connected to VREF 1=input PGA amplifier positive terminal connected to MICP through variable resistor string
RegR85	2	MIC2HPSEL	0	MainMIC2—HPMIC PGA select input signal 0: Select Main MIC2; 1: Select HP MIC
	1	M_MIC2N2INN	1	Connect MIC2N to input PGA negative terminal.(Main Mic) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	0	M_MIC2P2INP	0	Connect input PGA amplifier positive terminal to MIC2P or VREF. (Main Mic) 0=input PGA amplifier positive terminal connected to VREF 1=input PGA amplifier positive terminal connected to MIC2P through variable resistor string

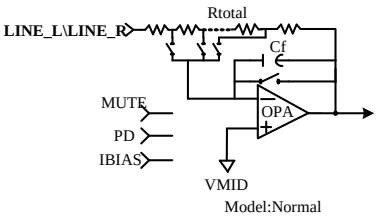
11.3.2 LINE PGA

11.3.2.1 Generation Description and function

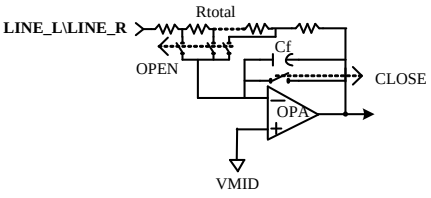
Every channel has 2 high impedances, low capacitance AC coupled Line inputs whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF to reduce any audible clicks that may otherwise be heard when changing inputs.

The PGA gain is logarithmically adjustable from +12dB to -46.5dB in 1.5dB steps. The gain is independently adjustable on each PGA channel. Setting LINLZCEN, LINRZCEN, bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting ZCST.

The inputs can also be muted in analog domain under soft control. If zero crossing is enabled it is necessary to enable zero cross timeout to un-mute the input PGAs. This is because their outputs will not cross zero when muted. Alternatively, zero crossing can be disabled before sending the un-mute command.



Model:Normal



Model:MUTE

11.3.2.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R1	2	LINREN	0	Line Right Enable signal: 1: Right Line PGA Enable; 0: Power Down
	1	LINLEN	0	Line Left Enable signal: 1: Left Line PGA Enable; 0: Power Down
~~Reg~~R2	7	LINLMU	1	Line Left PGA Mute signal: 0: Un-Mute; 1:Mute
	6	LINLZCEN	0	Line Left PGA ZeroCross Enable signal: 1: Enable; 0:Disable
	5:0	LINLVOL[5:0]	011111	Line Left PGA Volume Control 111111--101000: fix to 12dB 100111＝12dB; 100110＝10.5dB …… 011111＝0dB(Default) …… 000000＝-46.5dB
~~Reg~~R3	7	LINRMU	1	Line Right PGA Mute signal: 0: Un-Mute; 1:Mute

	6	LINRZCEN	0	Line Right PGA ZeroCross Enable signal 1: Enable; 0:Disable
~~Reg~~R3	5:0	LINRVOL[5:0]	011111	Line Right PGA Volume Control: 111111--101000: fix to 12dB 100111＝12dB; 100110＝10.5dB …… 011111＝0dB(Default) …… 000000＝-46.5dB

11.3.3 SIDE TONE PGA

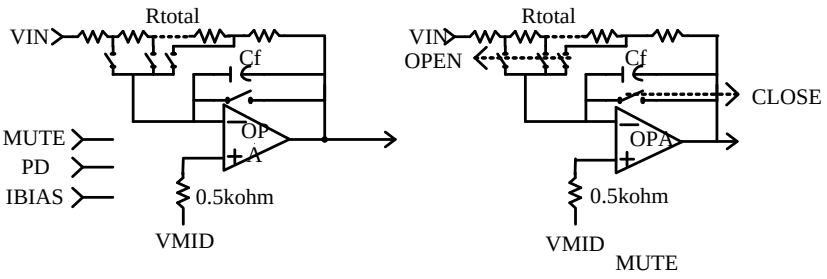
11.3.3.1 Generation Description and function

Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF to reduce any audible clicks that may otherwise be heard when changing inputs.

The PGA gain is logarithmically adjustable from 0~~+12~~dB to -30~~46.5~~dB in 1~~.~~ ~~5~~dB steps. The gain is independently adjustable on each PGA channel. Setting LPGAZCEN, RPGAZCEN, bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN.

The inputs can also be muted in analog domain under soft control. If zero crossing is enabled it is necessary to enable zero cross timeout to un-mute the input PGAs. This is because their outputs will not cross zero when muted. Alternatively, zero crossing can be disabled before sending the un-mute command.

One Channel work:



Note : Rtotal=80kohm;Cf =159fF

11.3.3.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
	7	SDMU	1	Side Tone PGA mute signal: 0: Un-Mute; 1：Mute
	6	SDEN	0	Side Tone PGA Enable signal: 1: Side Tone PGA Enable；0： Power Down
	5	SDZCEN	0	Side Tone PGA ZeroCross Enable signal 1: Enable；0：Disable
RegR4	4:0	SDVOL[4:0]	11110	Side Tone PGA Volume Control: 11111＝0dB; 11110＝0dB (Default) 11101=-1dB 11100=-2dB 11011=-3dB 11010=-4dB 11001=-5dB 11000=-6dB 10111=-7dB 10110=-8dB 10101=-9dB 10100=-10dB 10011=-11dB 10010=-12dB 10001=-13dB 10000=-14dB 01111=-15dB 01110=-16dB 01101=-17dB 01100=-18dB 01011=-19dB 01010=-20dB 01001=-21dB 01000=-22dB 00111=-23dB 00110=-24dB 00101=-25dB 00100=-26dB 00011=-27dB 00010=-28dB 00001=-29dB 00000=-30dB
RegR85	7	MICSTSEL	0	Sidetone select: 0: Select MIC1 1: Select MIC2 or HPMIC

11.4 ALC

11.4.1 Generation Description and Function

The LC1132 has an automatic PGA gain control circuit in ADC path and DAC path(ADC path ALC is explained in this part as an example, unless otherwise stated), which can function as an input peak limiter or as an automatic level control (ALC).

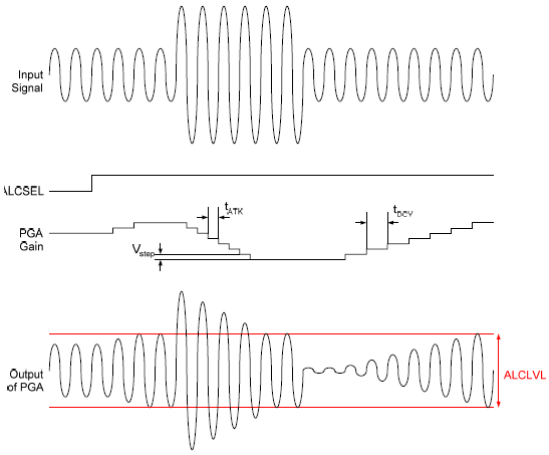
The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL). If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK. The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode.

The ALC function is enabled by settings the register ALCSEL. The ALC mode is determined by ALCMODE register.

11.4.2 Specification

11.4.2.1 Normal Mode

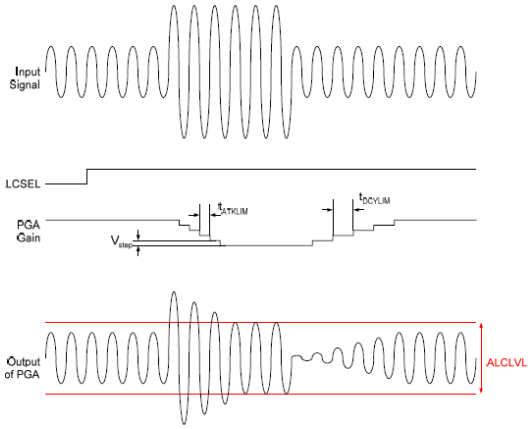
In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.



ALC Normal Mode

11.4.2.2 Limiter Mode

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at startup. If the ALC is switched into limiter mode from ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.



ALC Limiter Mode

11.4.2.3 Attack And Decay Times

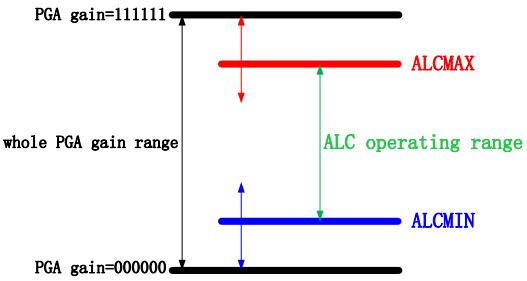
The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. The time constant in limiter mode is shorter than in ALC mode.

Note that, these times will vary depending on the sample rate. All the hold decay and attack time settings are referring to 48KHz's sampling rate, and the actual time used is the 'reference time*48KHz / Fs'.

11.4.2.4 Minimum And Maximum

The ALCMIN and ALCMAX register bits set the minimum/maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

In normal mode, ALCMAX sets the maximum boost which can be applied to the signal. In limiter mode, ALCMAX will normally have no effect (assuming the starting gain value is less than the maximum gain specified by ALCMAX) because the maximum gain is set at the starting gain level. ALCMIN sets the minimum gain value which can be applied to the signal.



ALC MAX and MIN Gain

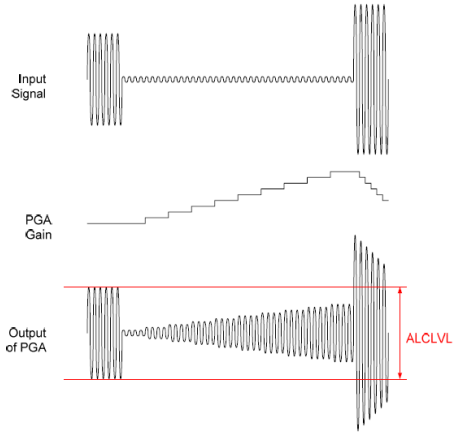
Note that if the ALC gain setting strays outside the ALC operating range, either by starting the ALC outside

of the range or changing the ALCMAX or ALCMIN settings during operation, the ALC will immediately adjust the gain to return to the ALC operating range. It is recommended that the ALC starting gain is set between the ALCMAX and ALCMIN limits.

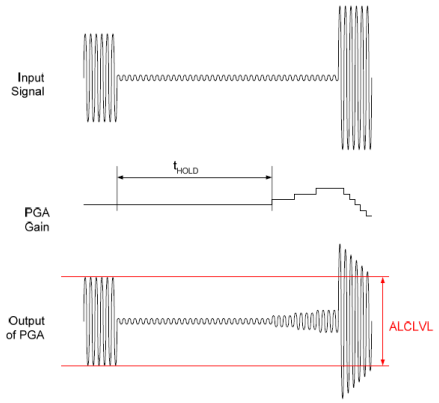
11.4.2.5 ALC Hold Time

In Normal mode, the ALC has an adjustable hold time which sets a time delay before the ALC begins its decay phase (gain increasing). The hold time is set by the ALCHLD register.

If the hold time is exceeded, this indicates that the signal has reached a new average level and the ALC will increase the gain to adjust for that new average level. If the signal goes above the threshold during the hold period, the hold phase is abandoned and the ALC returns to normal operation.



(a) without ALC HOLD



(b) with ALC HOLD

System Response with and without ALC HOLD Function

11.4.2.6 Peak Limiter

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ALCATK = 0000), until the signal level falls below 87.5% of full scale.

Note: If ALCATK = 0000, the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

11.4.2.7 Noise Gate

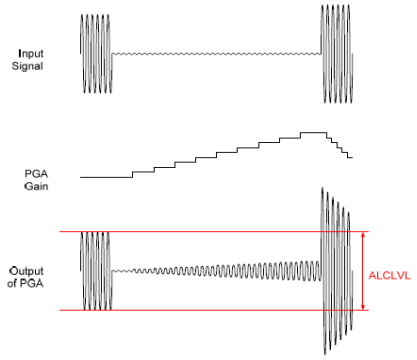
When the signal is very quiet and consists mainly of noise, the ALC function may cause ‘noise pumping’, i.e. loud hissing noise during silence periods. The LC1132 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dBFS] < NGTH [dBFS] + PGA gain [dB]

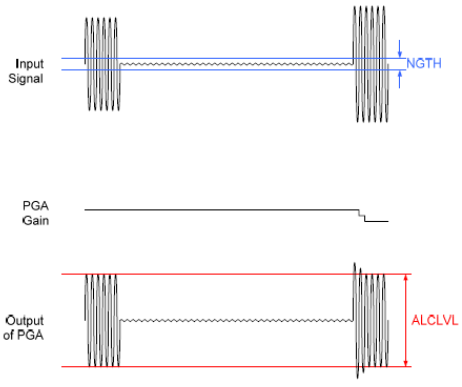
This is equivalent to:

Signal level at input pin [dBFS] < NGTH [dBFS]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet). The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 3dB steps. The diagrams below show the response of the system to the same signal with and without noise gate.



(a) Without NGTH



(b) With NGTH

System Response with and without NGTH Function

11.4.3 Register

<table>
<tr><th>REG. ADDR.</th><th>BIT</th><th>REG. NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>R17</td><td>7</td><td>ADC1_ERR</td><td>1</td><td>ADC1 ALC target error tolerance
0: +- 0.75dB; 1: +- 1.50dB.</td></tr>
<tr><td rowspan="6">R21</td><td>7</td><td>ADC1_ALC_DSEL</td><td>0</td><td>ADC ALC data selection
0: after comb filter; 1: after HPF filter</td></tr>
<tr><td>6</td><td>ADC1_ALCMODE</td><td>0</td><td>ALC mode selection
0: ALC mode(Normal Operation); 1: Limiter mode.</td></tr>
<tr><td>5</td><td>ADC1_ALCSEL</td><td>0</td><td>ALC function enable
0: disable; 1: enable.</td></tr>
<tr><td>4</td><td>ADC1_NG_EN</td><td>0</td><td>Noise Gate enable signal
0: disable; 1: enable.</td></tr>
<tr><td>3:0</td><td>ADC1_NG[3:0]</td><td>0111
(-60dB)</td><td>Noise gate threshold or noise floor level
<table>
<tr><td>1111</td><td>-84 dB</td></tr>
<tr><td>1110</td><td>-81 dB</td></tr>
<tr><td>1101</td><td>-78 dB</td></tr>
<tr><td>1100</td><td>-75 dB</td></tr>
<tr><td>1011</td><td>-72 dB</td></tr>
<tr><td>1010</td><td>-69 dB</td></tr>
<tr><td>1001</td><td>-66 dB</td></tr>
<tr><td>1000</td><td>-63 dB</td></tr>
<tr><td>0111</td><td>-60 dB</td></tr>
<tr><td>0110</td><td>-57 dB</td></tr>
<tr><td>0101</td><td>-54 dB</td></tr>
<tr><td>0100</td><td>-51 dB</td></tr>
<tr><td>0011</td><td>-48 dB</td></tr>
<tr><td>0010</td><td>-45 dB</td></tr>
<tr><td>0001</td><td>-42 dB</td></tr>
<tr><td>0000</td><td>-39 dB</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>R22</td><td>4:0</td><td>ADC_TARGET[4:0]</td><td>00011
(-6dB)</td><td>ALC target level<table>
<tr><td>11111</td><td>-48dB</td></tr>
<tr><td>11110</td><td>-46.5dB</td></tr>
<tr><td>11101</td><td>-45dB</td></tr>
<tr><td>11100</td><td>-43.5dB</td></tr>
<tr><td>11011</td><td>-42dB</td></tr>
<tr><td>11010</td><td>-40.5dB</td></tr>
<tr><td>11001</td><td>-39dB</td></tr>
<tr><td>11000</td><td>-37.5dB</td></tr>
<tr><td>10111</td><td>-36dB</td></tr>
<tr><td>10110</td><td>-34.5dB</td></tr>
<tr><td>10101</td><td>-33dB</td></tr>
<tr><td>10100</td><td>-31.5dB</td></tr>
<tr><td>10011</td><td>-30dB</td></tr>
<tr><td>10010</td><td>-28.5dB</td></tr>
<tr><td>10001</td><td>-27dB</td></tr>
<tr><td>10000</td><td>-25.5dB</td></tr>
<tr><td>01111</td><td>-24dB</td></tr>
<tr><td>01110</td><td>-22.5dB</td></tr>
<tr><td>01101</td><td>-21dB</td></tr>
<tr><td>01100</td><td>-19.5dB</td></tr>
<tr><td>01011</td><td>-18dB</td></tr>
<tr><td>01010</td><td>-16.5dB</td></tr>
<tr><td>01001</td><td>-15dB</td></tr>
<tr><td>01000</td><td>-13.5dB</td></tr>
<tr><td>00111</td><td>-12dB</td></tr>
<tr><td>00110</td><td>-10.5dB</td></tr>
<tr><td>00101</td><td>-9dB</td></tr>
<tr><td>00100</td><td>-7.5dB</td></tr>
<tr><td>00011</td><td>-6dB</td></tr>
<tr><td>00010</td><td>-4.5dB</td></tr>
<tr><td>00001</td><td>-3dB</td></tr>
<tr><td>00000</td><td>-1.5dB</td></tr>
</table></td></tr>
<tr><td>R23</td><td>7</td><td>ADC1MU</td><td>1</td><td>ADC1 mute signal
0: un-mute; 1: mute.</td></tr>
</table>

<table>
<tr><td></td><td>6:0</td><td>ADC1_DIG_VOL[6:0]</td><td>1100111
(0dB)</td><td>ADC digital gain
0000000: digital mute;
0000001: -76.50dB;
0000010: -75.75dB;
0000011: -75.00dB;
…0.75dB/step
1111110: 17.25dB;
1111111: 18.00dB.</td></tr>
<tr><td>R25</td><td>5:0</td><td>ADC1_ALCMAX[5:0]</td><td>101000</td><td>MAX PGA gain used in ALC model</td></tr>
<tr><td>R26</td><td>5:0</td><td>ADC1_ALCMIN[5:0]</td><td>000000</td><td>MIN PGA gain used in ALC model</td></tr>
<tr><td>R27</td><td>7:4</td><td>ADC1_ALCDCY[3:0]</td><td>0011</td><td>Decay (gain ramp-up) time (Fs=48kHz)
(ALCMODE ==0)(time doubles with every step)
<table>
<tr><td>1111</td><td>10.8s</td></tr>
<tr><td>1110</td><td>5.4s</td></tr>
<tr><td>1101</td><td>2.7s</td></tr>
<tr><td>1100</td><td>1.36s</td></tr>
<tr><td>1011</td><td>680.96ms</td></tr>
<tr><td>1010</td><td>340.48ms</td></tr>
<tr><td>1001</td><td>170.24ms</td></tr>
<tr><td>1000</td><td>85.12ms</td></tr>
<tr><td>0111</td><td>42.56ms</td></tr>
<tr><td>0110</td><td>21.28ms</td></tr>
<tr><td>0101</td><td>10.64ms</td></tr>
<tr><td>0100</td><td>5.32ms</td></tr>
<tr><td>0011</td><td>2.66ms</td></tr>
<tr><td>0010</td><td>1.33ms</td></tr>
<tr><td>0001</td><td>666us</td></tr>
<tr><td>0000</td><td>333us</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>0011</td><td>Decay (gain ramp-up) time (Fs=48kHz)
(ALCMODE ==1)(time doubles with every step)
<table><tr><td>1111</td><td>2.7s</td></tr><tr><td>1110</td><td>1.36s</td></tr><tr><td>1101</td><td>680.96ms</td></tr><tr><td>1100</td><td>340.48ms</td></tr><tr><td>1011</td><td>170.24ms</td></tr><tr><td>1010</td><td>85.12ms</td></tr><tr><td>1001</td><td>42.56ms</td></tr><tr><td>1000</td><td>21.28ms</td></tr><tr><td>0111</td><td>10.64ms</td></tr><tr><td>0110</td><td>5.32ms</td></tr><tr><td>0101</td><td>2.66ms</td></tr><tr><td>0100</td><td>1.33ms</td></tr><tr><td>0011</td><td>666us</td></tr><tr><td>0010</td><td>333us</td></tr><tr><td>0001</td><td>166.4us</td></tr><tr><td>0000</td><td>83.2us</td></tr></table></td></tr>
<tr><td></td><td>3:0</td><td>ADC1_ALCATK[3:0]</td><td>0010</td><td>ALC attack (gain ramp-down) time
(ALCMODE == 0)(time doubles with every step)
see ADC1_ALCDCY[3:0] (ALCMODE ==1)</td></tr>
<tr><td></td><td></td><td></td><td>0010</td><td>ALC attack (gain ramp-down) time
(ALCMODE == 1)(time doubles with every step)
<table><tr><td>1111</td><td>680ms</td></tr><tr><td>1110</td><td>340ms</td></tr><tr><td>1101</td><td>170ms</td></tr><tr><td>1100</td><td>85ms</td></tr><tr><td>1011</td><td>42.56ms</td></tr><tr><td>1010</td><td>21.28ms</td></tr><tr><td>1001</td><td>10.64ms</td></tr><tr><td>1000</td><td>5.32ms</td></tr><tr><td>0111</td><td>2.66ms</td></tr><tr><td>0110</td><td>1.33ms</td></tr><tr><td>0101</td><td>666us</td></tr><tr><td>0100</td><td>333us</td></tr><tr><td>0011</td><td>166.4us</td></tr><tr><td>0010</td><td>83.2us</td></tr><tr><td>0001</td><td>41.6us</td></tr><tr><td>0000</td><td>20.8us</td></tr></table></td></tr>
</table>

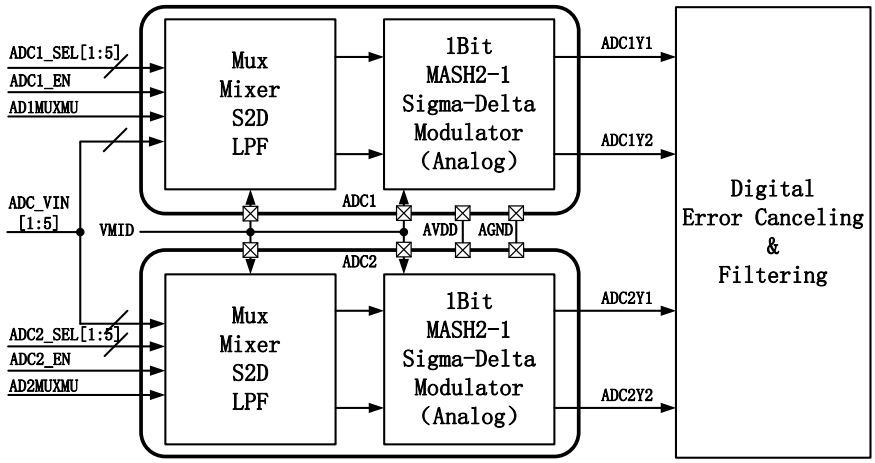
<table>
<tr><td>R28</td><td>3:0</td><td>ADC_ALCHLD[3:0]</td><td>0000
(0ms)</td><td>ALC hold time before gain is increased (Fs=48kHz)
(time doubles with every step)<table><tr><td>1111</td><td>43s</td></tr><tr><td>1110</td><td>21.76s</td></tr><tr><td>1101</td><td>10.88s</td></tr><tr><td>1100</td><td>5.44s</td></tr><tr><td>1011</td><td>2.72s</td></tr><tr><td>1010</td><td>1.36s</td></tr><tr><td>1001</td><td>0.68s</td></tr><tr><td>1000</td><td>0.34s</td></tr><tr><td>0111</td><td>0.17s</td></tr><tr><td>0110</td><td>85.28ms</td></tr><tr><td>0101</td><td>42.64ms</td></tr><tr><td>0100</td><td>21.32ms</td></tr><tr><td>0011</td><td>10.66ms</td></tr><tr><td>0010</td><td>5.33ms</td></tr><tr><td>0001</td><td>2.67ms</td></tr><tr><td>0000</td><td>0s</td></tr></table></td></tr>
<tr><td>R33</td><td>7</td><td>ADC2_ERR</td><td>1</td><td>ADC2 ALC target error tolerance
0: +- 0.75dB; 1: +- 1.50dB.</td></tr>
<tr><td rowspan="5">R37</td><td>7</td><td>ADC2_ALC_DSEL</td><td>0</td><td>ADC2 ALC data selection
0: after comb filter; 1: after HPF filter</td></tr>
<tr><td>6</td><td>ADC2_ALCMODE</td><td>0</td><td>ALC mode selection
0: ALC mode(Normal Operation); 1: Limiter mode.</td></tr>
<tr><td>5</td><td>ADC2_ALCSEL</td><td>0</td><td>ALC function enable
0: disable; 1: enable.</td></tr>
<tr><td>4</td><td>ADC2_NG_EN</td><td>0</td><td>Noise Gate enable signal
0: disable; 1: enable.</td></tr>
<tr><td>3:0</td><td>ADC2_NG[3:0]</td><td>0111
(-60dB)</td><td>Noise gate threshold or noise floor level
See ADC1_NG[3:0].</td></tr>
<tr><td>R38</td><td>4:0</td><td>ADC2_TARGET[4:0]</td><td>00011
(-6dB)</td><td>ALC target level
See ADC1_TARGET[4:0].</td></tr>
<tr><td rowspan="2">R39</td><td>7</td><td>ADC2MU</td><td>1</td><td>ADC2 mute signal
0: un-mute; 1: mute.</td></tr>
<tr><td>6:0</td><td>ADC2_DIG_VOL[6:0]</td><td>1100111
(0dB)</td><td>ADC digital gain
See ADC1_DIG_VOL[6:0].</td></tr>
<tr><td>R41</td><td>5:0</td><td>ADC2_ALCMAX[5:0]</td><td>101000</td><td>MAX PGA gain used in ALC model</td></tr>
<tr><td>R42</td><td>5:0</td><td>ADC2_ALCMIN[5:0]</td><td>000000</td><td>MIN PGA gain used in ALC model</td></tr>
<tr><td rowspan="2">R43</td><td>7:4</td><td>ADC2_ALCDCY[3:0]</td><td>0011</td><td>Decay (gain ramp-up) time, see ADC1_ALCDCY[3:0].</td></tr>
<tr><td>3:0</td><td>ADC2_ALCATK[3:0]</td><td>0010</td><td>Attack (gain ramp-down) time,
see ADC1_ALCATK[3:0].</td></tr>
<tr><td>R44</td><td>3:0</td><td>ADC2_ALCHLD[3:0]</td><td>0000</td><td>ALC hold time before gain is increased,
see ADC1_ALCHLD[3:0].</td></tr>
</table>

Note: Registers of DAC path ALC not listed here are similar to ADC1 (or ADC2). Please refer to the Codec Register Descriptions for details.

11.5 ADC

11.5.1 Generation Description and Function

The 2-channels 95dB ADC converts analog voltage into digital data stream. Each channel has 5 analog signal inputs at most. The single-end inputs enabled will be mixed, turned to differential voltage and filtered by a LPF. The full-scale input voltage is 1.0Vrms. The 1bit 128OSR sigma-delta modulator based on a MASH 3rd order structure converts the analog signal to digital data with quantization error, which will be canceled in digital part.



ADC Top Diagram

11.5.2 PAD Description

PAD NAME	I/O	DESCRIPTION
AVDD	I	CODEC analog power supply
AGND	I	CODEC analog ground
VMID	I	CODEC VREF

11.5.3 Register

REG. ADDR.	BIT	REG. NAME	DEFAULT	DESCRIPTION
R1	4	ADC2EN	0	ADC2 Enable signal 0: ADC disable; 1: ADC enable.
	3	ADC1EN	0	ADC1 Enable signal 0: ADC disable; 1: ADC enable.
R29	4	ADC1_RSTN	1	ADC1 soft reset signal 0: enable; 1: disable.
R45	4	ADC2_RSTN	1	ADC2 soft reset signal 0: enable; 1: disable.
R82	5	AD1IN5SEL	0	ADC1 select DAC MONO channel signal 0: unselect; 1: select.

	4	AD1IN4SEL	0	ADC1 select DAC L channel signal 0: unselect; 1: select.
	3	AD1IN3SEL	0	ADC1 select DAC R channel signal 0: unselect; 1: select.
	2	AD1IN2SEL	0	ADC1 select MainMIC2—HPMIC PGA OUT channel signal 0: unselect; 1: select.
	1	AD1IN1SEL	0	ADC1 select MainMIC1 PGA OUT signal 0: unselect; 1: select.
	0	AD1MUXMU	1	ADC1 MUX mute signal 0: MUX un-mute; 1: MUX mute.
R83	5	AD2IN5SEL	0	ADC2 select DAC MONO channel signal 0: unselect; 1: select.
	4	AD2IN4SEL	0	ADC2 select DAC L channel signal 0: unselect; 1: select.
	3	AD2IN3SEL	0	ADC2 select DAC R channel signal 0: unselect; 1: select.
	2	AD2IN2SEL	0	ADC2 select MainMIC2&HPMIC PGA OUT channel signal 0: unselect; 1: select.
	1	AD2IN1SEL	0	ADC2 select MainMIC1 PGA OUT signal 0: unselect; 1: select.
	0	AD2MUXMU	1	ADC2 MUX mute signal 0: MUX un-mute; 1: MUX mute.
R98	6:4	ICTR_ADC2	011	ADC2 Bias Current control signal (A) 000=3.5u; 001=4u; 010=4.5u;011=5u; 100=5.5u; 101=6u; 110=6.5u; 111=7u.
	2:0	ICTR_ADC1	011	ADC1 Bias Current control signal (A) 000=3.5u; 001=4u; 010=4.5u;011=5u; 100=5.5u; 101=6u; 110=6.5u; 111=7u.

11.6 ADC Decimation Filter

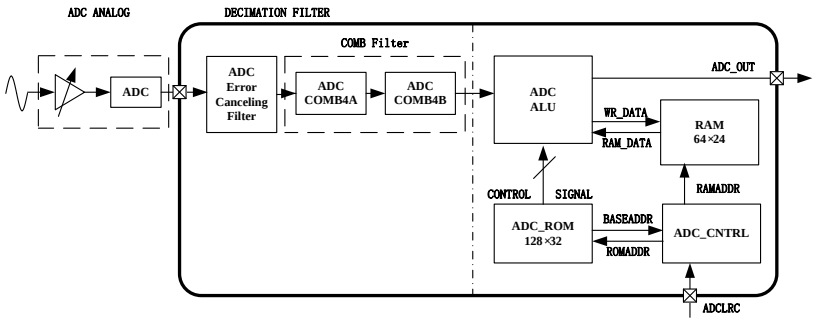
11.6.1 Generation Description and Function

Decimation filters are used for digital-signal processing (DSP) applications such as audio, music and video applications. There have been continuous efforts to improve the performance of digital decimation filters in terms of speed, hardware, and power dissipation.

The ADC decimation filter decreases the data rate of ADC output stream from oversampling rate to Nyquist rate. A low power and hardware efficient decimation filter is designed and implemented, which incorporates the poly-phase implementation of multi-stage multi-rate comb filter and half-band filters.

11.6.2 Specification

11.6.2.1 Decimation Filter Architecture

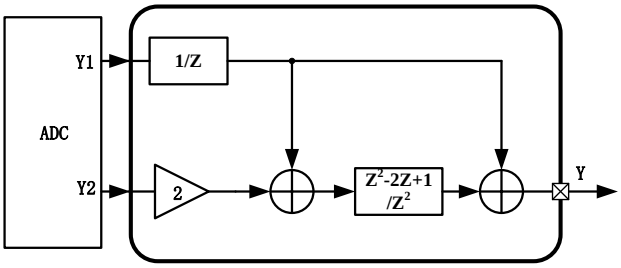


Decimation Filter Top Diagram

Generally, digital decimation filters are implemented by a cascade of either comb-FIR chain or FIR-comb chain. Multipliers represent most of the hardware used to implement a filter; as a result, multipliers contribute to most of the power dissipated in a filter. The comb filters do not require multipliers; therefore, they have been cascaded in the beginning of the comb-FIR chain. This reduces hardware and power consumption.

11.6.2.2 ADC Error Cancellation Filter

ADC error canceling filter is filter is a part of ADC sigma-delta modulator. According to the analog ADC structure, the block diagram is shown as below.



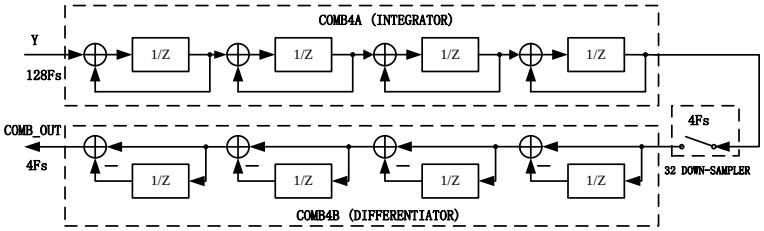
Error Canceling Filter Diagram

11.6.2.3 Comb Filter

The comb filter architecture is an efficient structure for the decimation filter due to its hardware efficiency and low power dissipation. Comb filters are described as:

$$H(z) = \left(\frac{1 - z^{-N}}{1 - z^{-1}}\right)^{K}$$

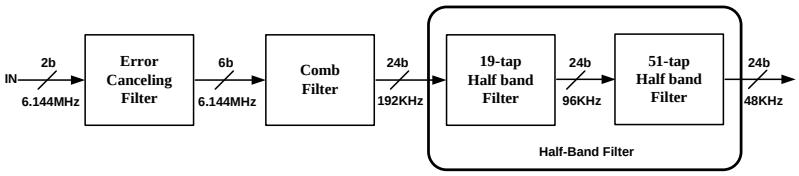
Where K represents the number of stages cascaded, and N represents the decimation factor. The equation can be further divided into an integrator represented by $1/ (1 - z^{-1})$, and a differentiator represented by $(1 - z^{-N})$. Comb filters have a drawback of poor stop band attenuation; therefore, a 4^{th} order comb filter has to be used. The implementation of a 4^{th} order comb filter, which consists of 4 integrators, a divide by 32 down-sampler and 4 differentiators is shown as following.



Comb Filter Diagram

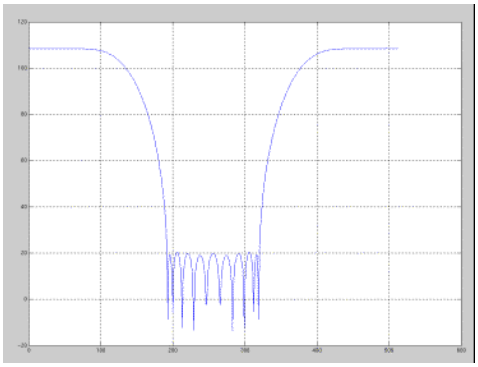
11.6.2.4 Half-Band Filter

After COMB filter, multi-rate multi-stage implementations of two half-band filters (19-tap and 51-tap) are used to improve the frequency response.

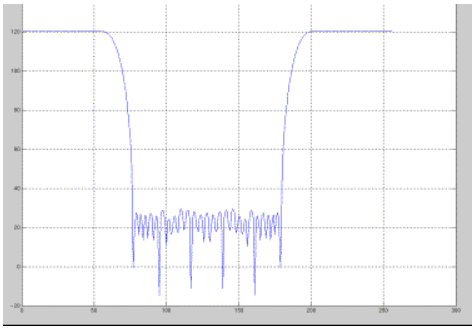


Half-Band Filter Diagram

In half-band filters, the number of taps is reduced considerably since the odd coefficients are zeros.



(a) 19-tap



(b) 51-tap

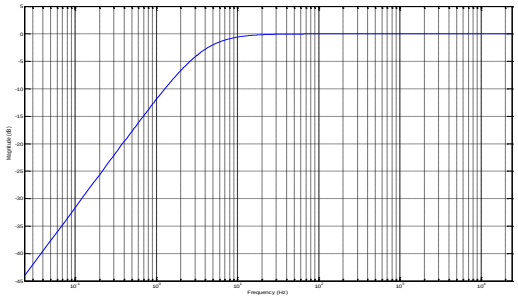
Half-Band Filter Frequency Response

11.7 ADC Path filter

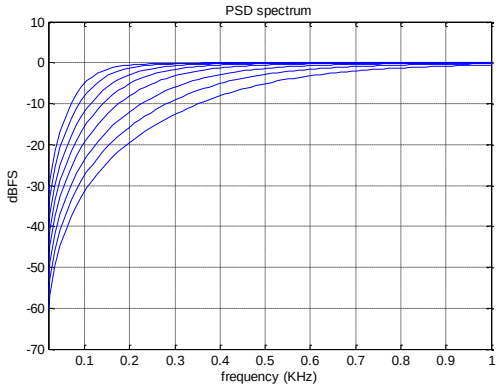
11.7.1 Generation Description and Function

11.7.1.1 HPF Filter

LC1132 has two selectable digital high-pass filters in the ADC filter path (1st HPF and 2nd HPF). Generally, 1st HPF is used in audio mode and 2nd HPF is used in application mode. In audio mode, the 1st HPF has a cut-off frequency around 3.7Hz (Fs= 48KHz). While in application mode, the 2nd HPF has a selectable cut-off frequency.



(a) 1st HPF

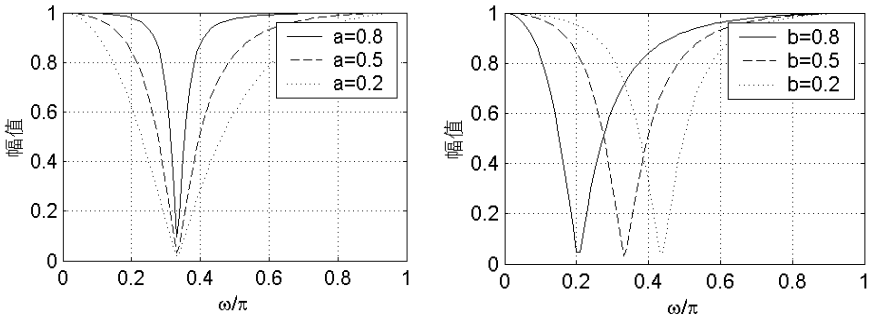


(b) 2nd HPF

HPF Frequency Response

11.7.1.2 Notch Filter

A programmable notch filter is also provided in LC1132, which has a variable centre frequency and bandwidth, programmed via two coefficients, a and b, which are represented by the register bits NFA0[13:0] and NFA1[13:0].



(a) b=0.5, a=0.8/0.5/0.2 (b) a=0.5, b=0.8/0.5/0.2

Notch Filter Frequency Response

11.7.2 Register

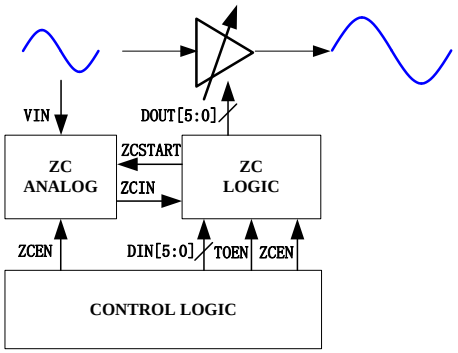
REG. ADDR.	BIT	REG. NAME	DEFAULT	DESCRIPTION
R17	6	ADC1_NFEN	0	ADC1 notch filter enable signal 1: enable 0:disable
	5:0	ADC1_NFA0[13:8]	00_0000	ADC1 notch filter A0 coefficient
R18	7:0	ADC1_NFA0[7:0]	0000_0000	
R19	7	ADC1_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0: disabled; 1: enabled Audio mode (1st order, fc = ~3.7Hz)
	6	ADC1_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0: disabled; 1: enabled Application mode (2nd order, fc = HPFCUT)
	5:0	ADC1_NFA1[13:8]	00_0000	ADC1 notch filter A1 coefficient
R20	7:0	ADC1_NFA1[7:0]	0000_0000	
R22	7:5	ADC1_HPFCUT[2:0]	000	Application mode cut-off frequency (Fs=48KHz) 000: 122Hz; 001: 153Hz; 010: 156Hz; 011: 245Hz; 100: 306Hz; 101: 392Hz; 110: 490Hz; 111: 612Hz.
R33	6	ADC2_NFEN	0	ADC2 notch filter enable signal 1: enable 0:disable
	5:0	ADC2_NFA0[13:8]	00_0000	ADC2 notch filter A0 coefficient
R34	7:0	ADC2_NFA0[7:0]	0000_0000	
R35	7	ADC2_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0: disabled; 1: enabled Audio mode (1st order, fc = ~3.7Hz)
	6	ADC2_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0: disabled; 1: enabled Application mode (2nd order, fc = HPFCUT)
	5:0	ADC2_NFA1[13:8]	00_0000	ADC2 notch filter A1 coefficient
R36	7:0	ADC2_NFA1[7:0]	0000_0000	

R38	7:5	ADC2_HPFCUT[2:0]	000	Application mode cut-off frequency (Fs=48KHz) 000: 122Hz; 001: 153Hz; 010: 156Hz; 011: 245Hz; 100: 306Hz; 101: 392Hz; 110: 490Hz; 111: 612Hz.

11.8 Volume and Filter Control

11.8.1 Zero-Crossing Block

The Zero-Crossing block is an assistant of analog zero crossing detector.



Zero-Crossing Block Diagram

When the CONTROL LOGIC is set to change the gain in analog part, DIN will be changed at first, and then ZC LOGIC will give out a ZCSTART signal to enable analog part ZC detector function. When the input analog signal crosses zero, a ZCIN signal will be passed to ZC LOGIC, which will change DOUT to be equal to DIN. If ZCIN doesn't appear for a long time (timeout time), a timeout signal will be generated in ZC LOGIC block, and the DOUT will be changed to DIN after timeout time reached.

11.8.2 Volume Control Characteristics

Symbol	Parameter	Conditions	Type	Units
VCRAUX	Stereo line in volume control range		-46.5~12	dB
VCRDAC_stereo	DAC volume control range		-76.5~18	dB
VCRADC	ADC volume control range		-76.5~18	dB
VCRMIC	MIC volume control range		-10~36	dB
SSAUX	Line in volume stepsize		1.5	dB
SSDAC_stereo	DAC volume stepsize		0.75	dB
SSADC	ADC volume stepsize		0.75	dB
SSMIC	MIC volume stepsize		0.75	dB
Gain_Speaker	Speaker output analog gain, 1dB/step	*1	-21~+11.8	dB
Gain_Headphone	Headphone left/right channel output analog gain, 1dB/step	*1	-25~+6	dB
Gain_Receiver	Receiver output analog gain, 1dB/step	*1	-25~+6	dB
Gain_Mic Boost	MIC PGA gain, 0.75dB/Step	*1	-10~ +36	dB
Gain_Line PGA	Line in PGA Gain, 1.5dB/Step	*1	-46.5/+12	dB

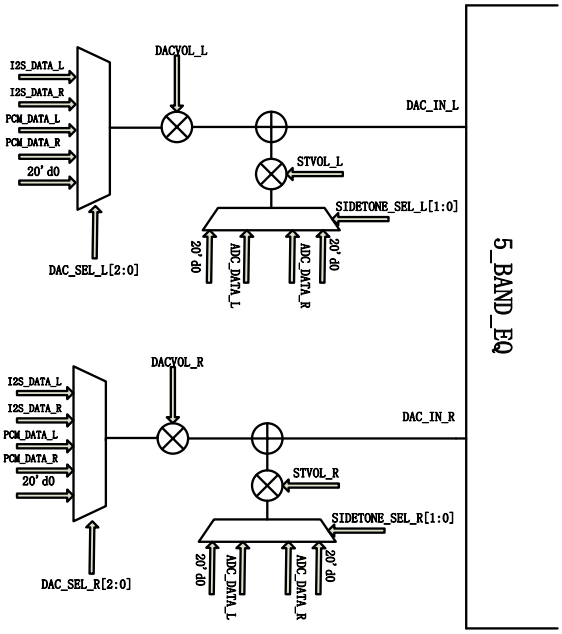
11.9 Digital SideTone and 5_band_EQ

11.9.1 Generation Description and function

The LC1132 has a digital side-tone and 5 band equalization filter functions.

11.9.2 Specification

11.9.2.1 Digital side-tone and gain control



11.9.2.2 Band Equalizer

A 5 band parametric equalizer is provided, which can be applied to ADC and DAC path (only used at DAC path in LC1132). The equalizer consists of five filters arranged in series as shown in Fig 1. This includes one low pass shelving filter (Band 1), one high pass shelving filter (Band 5) and three peaking filters for the center bands. Each filter has adjustable cut-off frequency (for shelving filters) or center frequency (for peaking filters), adjustable boost/cut between -15dB to +15dB in 1dB steps. The peaking filters have selectable bandwidth: 2/3 Octave or 4/3 Octave.

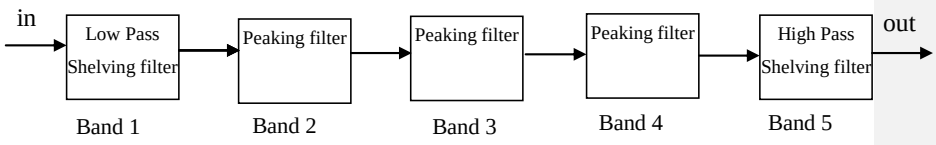


Fig 1.Structure of the 5 band equalizer

Shelving filters are implemented as first order IIR structures and peaking filters are implemented as second order IIR structures.

Fig 2 is an illustration of the magnitude response of a 5 band equalizer where the filter bands

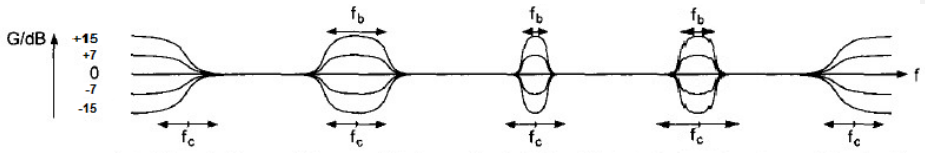


Fig 2.an illustration of the magnitude response of a 5 band equalizer where fc is the cut-off/center frequency, fb is the bandwidth and G is the Gain in dB

From Fig 3 to Fig 15 show the magnitude responses of each filter with a sampling frequency of 48kHz. Fig 3, 5, 8, 11 and 14 at the left show the responses of different cut-off/center frequencies with gain of ±15dB. Fig 4, 6, 9, 12 and 15 at the right show a sweep of the gain from -15dB to +15dB for the lowest cut-off/center frequency of each filter. Magnitude responses of peaking filters with different bandwidth are shown in Fig 7, 10 and 13 in different colours with gain of ±15dB.

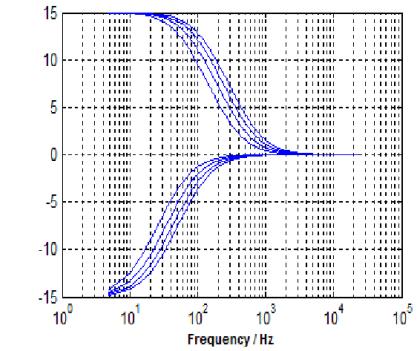


Fig 3 EQ Band 1 Cut-off Frequencies

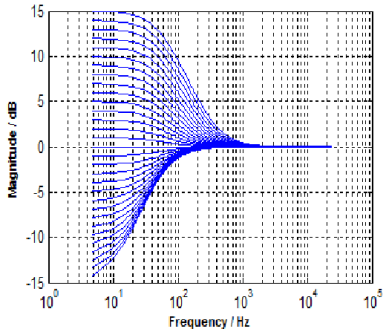
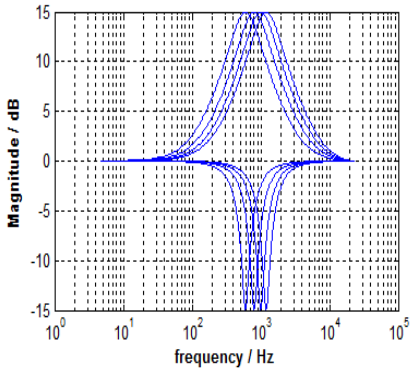


Fig 4 EQ Band 1 Gains for Lowest Cut-off



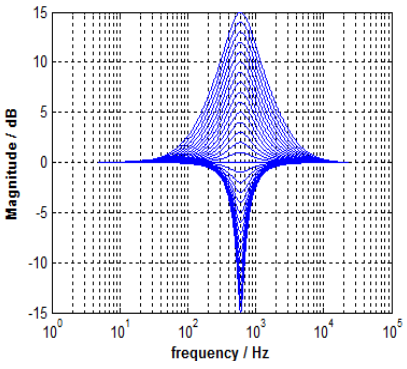


Fig 5 EQ Band 2 Center Frequencies

Fig 6 EQ Band 2 Gains for Lowest Center Frequency EQ2_Q=1

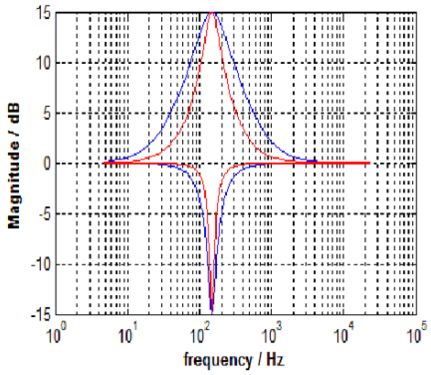


Fig 7 EQ Band 2 Bandwidth, EQ2_Q=1 (blue),EQ2_Q=0 (red)

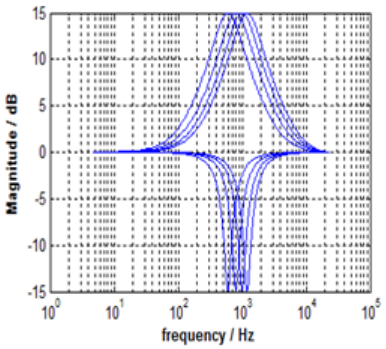


Fig 8 EQ Band 3 Center Frequencies, EQ3_Q=1

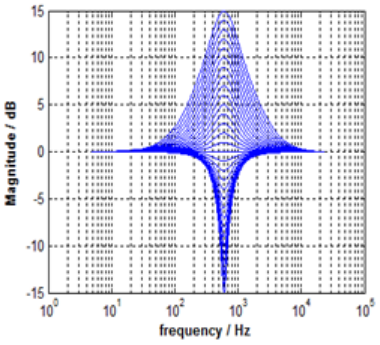


Fig 9 EQ Band 3 Gains for Lowest Center Frequency EQ3_Q=1

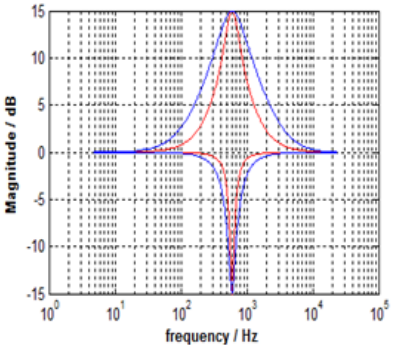


Fig 10 EQ Band 3 Bandwidth, EQ3_Q=1 (blue) EQ3_Q=0 (red)

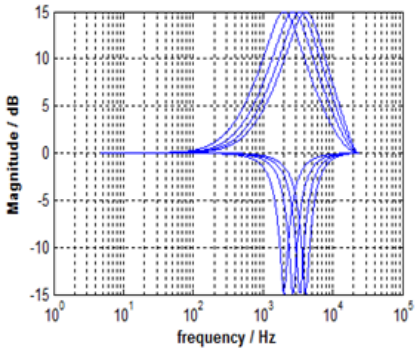


Fig 11 EQ Band 4 Center Frequencies, EQ4_Q=1

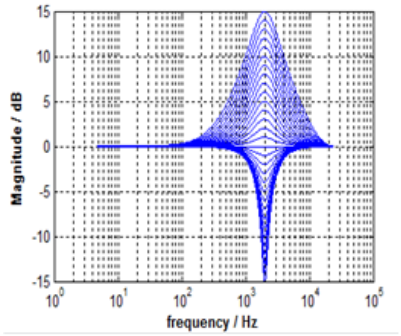


Fig 12 EQ Band 4 Gains for Lowest Center Frequency EQ4_Q=1

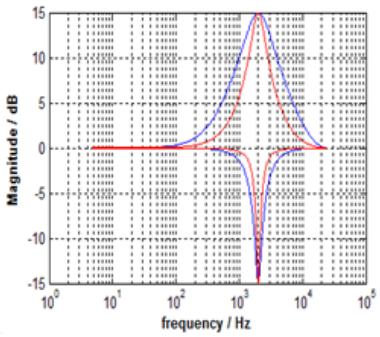


Fig 13 EQ Band 4 Bandwidth, EQ4_Q=1 (blue) EQ4_Q=0 (red)

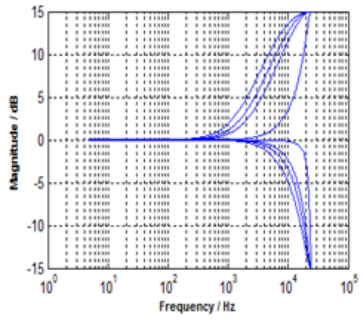


Fig 14 EQ Band 5 Cut-off Frequencies

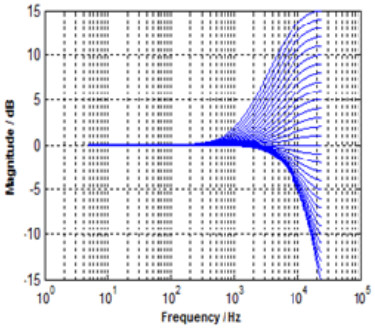


Fig 15 EQ Band 5 Gains for Lowest Cut-off Frequency

Fig 16 shows the result of having the gain set on five bands simultaneously. The blue traces show each band response with lowest cut-off/center frequencies and ±15dB gain. The pink traces show the aggregate responses of five bands with ±15dB and Eqx_Q = 0 for the peaking filters.

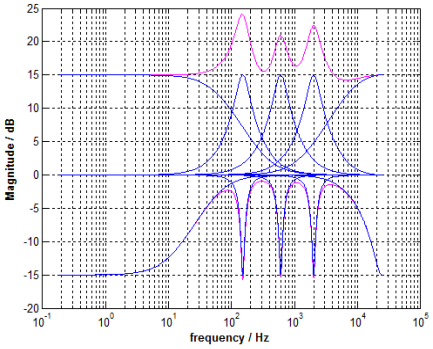


Fig16 5 band EQ

11.10 DAC interpolation filter

11.10.1 Generation Description and function

Interpolation filters are used for digital-signal processing (DSP) applications such as audio, music and video applications. There have been continuous efforts to improve the performance of digital interpolation filters in terms of speed, hardware, and power dissipation.

In our design, we propose to design and implement a low power and hardware efficient interpolation filter, which incorporates the poly-phase implementation of multi-stage multi-rate half-band filters.

11.10.2 Interpolation filter architecture

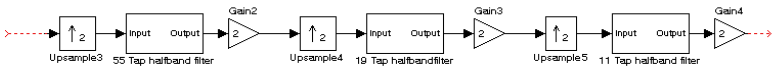
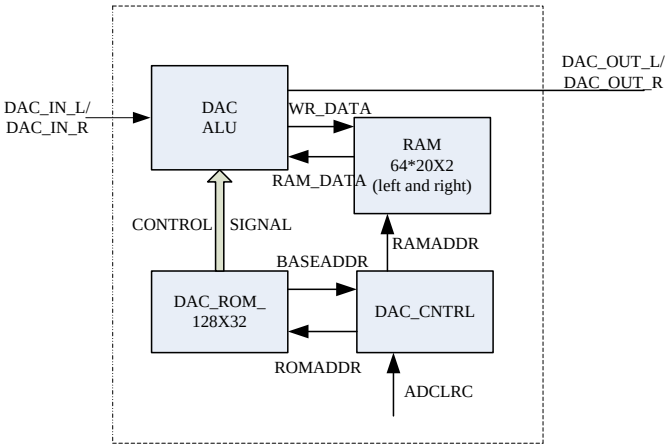


Fig 17Aggregate Magnitude Responses

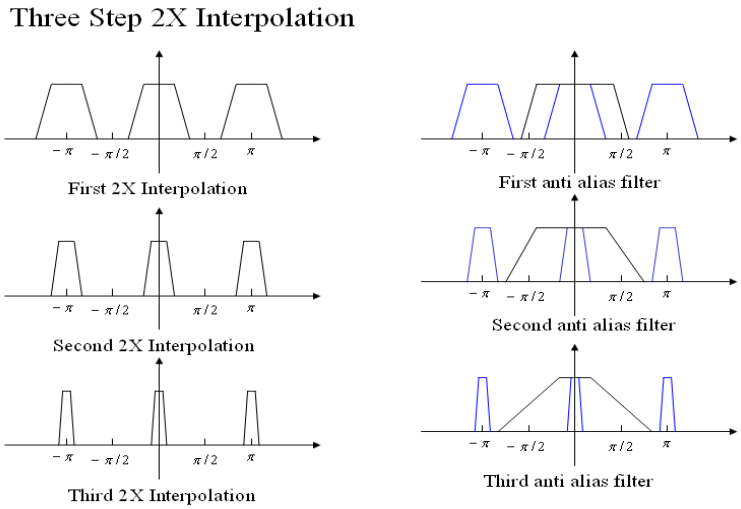
The digital interpolation filters are implemented by a cascade of three half-band filters. Multipliers represent most of the hardware used to implement a filter; as a result, multipliers contribute to most of the power dissipated in a filter. All the three filters share the same multipliers, thus reduces hardware and power consumption.

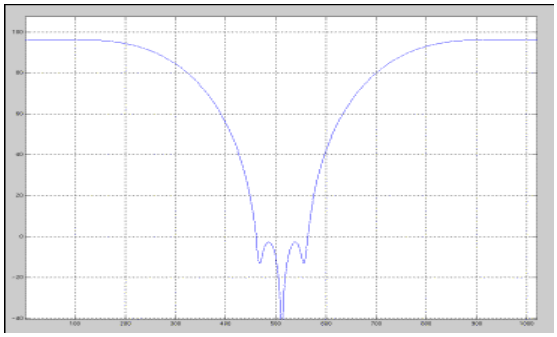


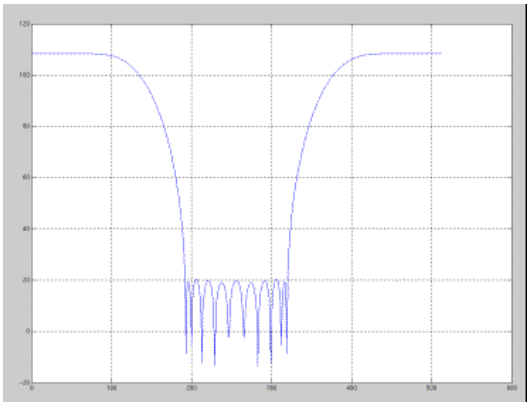
Half-Band Filter

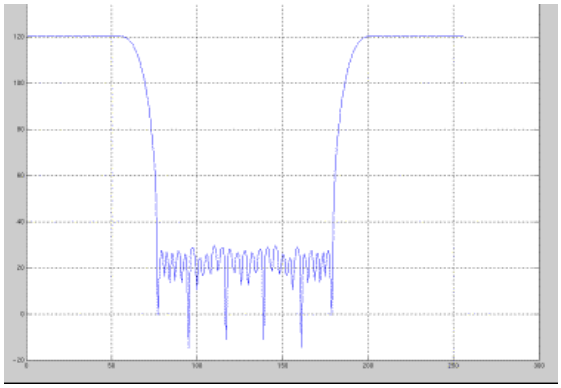
We have used multi-rate multi-stage implementations of three half-band filters to improve the frequency response. Three half-band filters (11-tap, 19-tap and 55-tap) are implemented in this design. In half-band filters, the number of taps is reduced considerably since the odd coefficients

are zeros, and in order to get low power and minimal hardware, the two HBF filter and later HPF share the same Arithmetic Logical Unit(ALU) as shown below, we will discuss it in detail later.





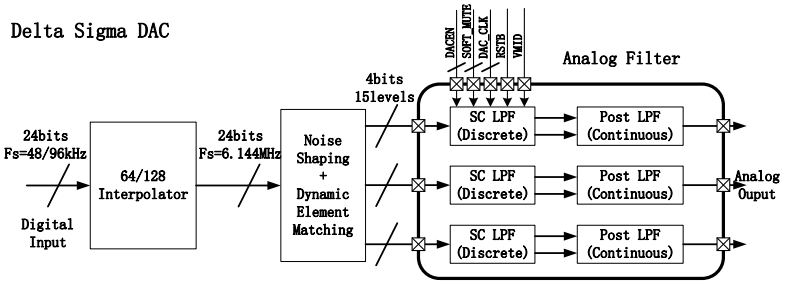




11.11 DAC

11.11.1 Generation Description and Function

The 3-channels 95dB audio stereo DAC converts digital data stream at 48kS/96kS digitally up-sampled at 6.144MHz, into an analog output voltage. Each channel is made of a differential low pass 1st order switched cap filter, clocked at 6.144MHz and a continuous time filter, turning the differential voltage to single-end. The full-scale output voltage is 1.0Vrms. The Delta sigma Modulator of DAC is 3rd order, 4-bits and 128/64 OSR.



DAC Top Diagram

11.11.2 PAD Description

PAD NAME	I/O	DESCRIPTION
AVDD	I	CODEC analog power supply
AGND	I	CODEC analog ground
AVDD_REF	I	CODEC analog reference power supply
AGND_REF	I	CODEC analog reference ground
DVDD2	I	CODEC digital ground
DGND2	I	CODEC digital ground
VMID	I	CODEC VREF

11.11.3 Register

REG. ADDR.	BIT	REG. NAME	DEFAULT	DESCRIPTION
R1	7	DACREN	0	DAC Right Enable signal 0: Rch DAC disable; 1: Rch DAC enable.
	6	DACLEN	0	DAC Left Enable signal 0: Lch DAC disable; 1: Lch DAC enable.
	5	DACMONOEN	0	DAC MONO Enable signal 0: mono DAC disable 1: mono DAC enable
R16	4:2	MONO_DAC_SEL [2:0]	111	mono DAC data selection 000: from I2S interface left channel data; 001: from I2S interface right channel data; 010: from PCM interface left channel data; 011: from PCM interface right channel data; 100: from ADC1 output data; 101: from ADC2 output data; 110/111: Reserved as Zero.
	1	MONODACMU	1	mono DAC mute (digital) 0: un-mute; 1: mute.
	0	MONOSOFTMUTE_EN	1	mono DAC soft mute function enable (analog) 0: disable; 1: enable.
R30	6:0	MONO_DAC_LEVEL[6:0]	1100111 (0dB)	mono DAC channel digital gain 0000000: digital mute; 0000001: -76.5dB; 0000010: -75.75dB; 0000011: -75dB; … 0.75dB/step 1111110: 17.25dB; 1111111: 18dB.
R32	4	MONO_DAC_RSTN	1	mono DAC soft reset signal 0: enable; 1: disable.
R46	7:5	DAC_SEL_L[2:0]	111	DAC left channel data selection 000: from I2S interface left channel data; 001: from I2S interface right channel data; 010: from PCM interface left channel data; 011: from PCM interface right channel data; 100/101/110/111: Reserved as Zero.
	4:2	DAC_SEL_R[2:0]	111	DAC right channel data selection 000: from I2S interface left channel data; 001: from I2S interface right channel data; 010: from PCM interface left channel data; 011: from PCM interface right channel data; 100/101/110/111: Reserved as Zero.
	1	LDACMU	1	DAC left channel mute signal (digital) 0: un-mute; 1: mute.

	0	RDACMU	1	DAC right channel mute signal (digital) 0: un-mute; 1: mute.
R47	7	SOFTMUTE_EN	1	DAC soft mute function enable signal (analog) 0: disable; 1: enable.
R49	6:0	DAC_LEVEL_L[6:0]	1100111 (0dB)	DAC left channel digital gain See MONO_DAC_LEVEL[6:0].
R50	6:0	DAC_LEVEL_R[6:0]	1100111 (0dB)	DAC right channel digital gain See MONO_DAC_LEVEL[6:0].
R71	4	DAC_RSTN	1	DAC soft reset signal 0: enable; 1: disable.
R84	7:5	ICTR_DAC[2:0]	011	DAC Bias Current control signal (A) 000=3.5u; 001=4u; 010=4.5u; 011=5u; 100=5.5u; 101=6u; 110=6.5u; 111=7u.

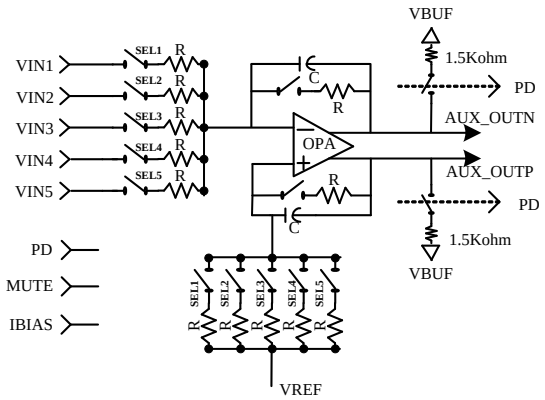
11.12 Output signal Path

11.13 MIXERS

11.13.1 AUX OUT MIXER

11.13.1.1 Generation Description and function

The Mixer can mix signals from LINLPGA, LINRPGA , Left DAC, right DAC and mono DAC source to AUX output. AUX out can drive line level load (10KOhm+50pF) with differential or single end output.



NOTE:R=50kohm;C=517fF

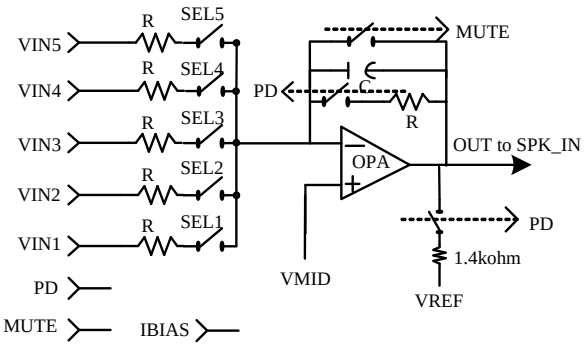
11.13.1.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R86	7			
	6	AUXMIXEN	0	AUX Mixer enable signal 1: Enable；0：Disable
	5	AUXMIXMU	1	AUX Mixer Mute signal: 0: Un-Mute; 1：Mute
	4	LINLSEL_AUX	0	AUX Select Left Line PGA control signal : 0:unselect; 1: Select
	3	LINRSEL_AUX	0	AUX Select Right Line PGA control signal : 0:unselect; 1: Select
	2	DACMONOSEL_AUX	0	AUX Select mono DAC control signal : 0:unselect 1:select
	1	DACLSEL_AUX	0	AUX Select Left DAC control signal: 0:unselect; 1: Select
	0	DACRSEL_AUX	0	AUX Select Right DAC control signal: 0:unselect; 1: Select

11.13.2 SPKMIX

11.13.2.1 Generation Description and function

The Mixer can mix signals from LINLPGA, LINRPGA , Left DAC, right DAC and mono DAC.



Note: When MUTE=1, SEL1, 2, 3, 4 ,5 are all off;
R=41kohm; C=159fF

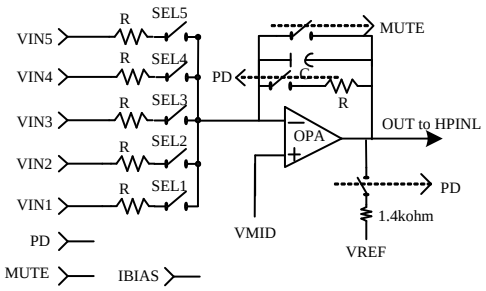
11.13.2.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
	6	SPKMIXEN	0	SPK Mixer Enable signal : 1: Enable；0：Disable
	5	SPKMIXMU	1	SPK Mixer Mute signal : 0: Un-Mute; 1:Mute
	4	LINLSEL_SPK	0	SPK Select Left Line PGA: 0:unselect; 1: Select
~~Reg~~R87	3	LINRSEL_SPK	0	SPK Select Right Line PGA: 0:unselect; 1: Select
	2	DACMONOSEL_SPK	0	SPK Select mono DAC: 0:unselect 1:select
	1	DACLSEL_SPK	0	SPK Select Left DAC: 0:unselect; 1: Select
	0	DACRSEL_SPK	0	SPK Select Right DAC: 0:unselect; 1: Select

11.13.3 HPLMIX

11.13.3.1 Generation Description and function

The Mixer can mix signals from LINLPGA, Left DAC, Right DAC, Sidetone PGA and mono DAC source.



Note: When MUTE=1, SEL1, 2, 3, 4, 5 are all off;
R=41kohm; C=159fF

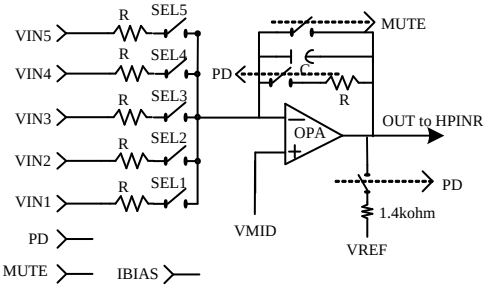
11.13.3.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R89	7			
	6	HPLMIXEN	0	HP L channel Mixer Enable : 1 : Enable 0 : Disable
	5	HPLMIXMU	1	HP L channel Mixer Mute. 0: Un-Mute; 1：Mute
	4	LINLSEL_HPL	0	HP L channel Select Left Line PGA: 0:unselect; 1: Select
	3	DACMONOSEL_HPL	0	HP L channel Select mono DAC: 0:unselect 1:select
	2	DACLSEL_HPL	0	HP L channel Select Left DAC: 0:unselect; 1: Select
	1	DACRSEL_HPL	0	HP L channel Select Right DAC: 0:unselect; 1: Select
	0	SDTSEL_HPL	0	HP L channel Select Side Tone: 0:unselect; 1: Select

11.13.4HPRMIX

11.13.4.1 Generation Description and function

The Mixer can mix signals from LINRPGA, SideTonePGA, left DAC and right DAC and mono DAC source.



Note: When MUTE=1, SEL1, 2, 3, 4, 5 are all off;
R=41kohm; C=159fF

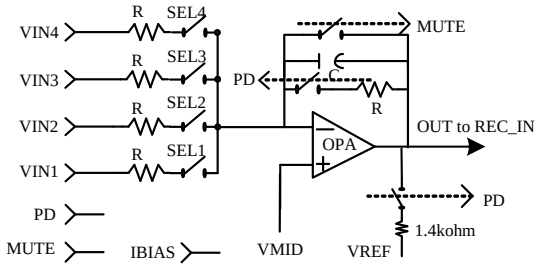
11.13.4.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
RegR90	7			
	6	HPRMIXEN	0	HP R channel Mixer Enable. 1: Enable；0：Disable
	5	HPRMIXMU	1	HP R Mixer Mute. 0: Un-Mute; 1：Mute
	4	LINRSEL_HPR	0	HP R Select Right Line PGA: 0:unselect; 1: Select
	3	DACMONOSEL_HPR	0	HP R Select mono DAC: 0:unselect 1:select
	2	DACLSEL_HPR	0	HP R Select Left DAC: 0:unselect; 1: Select
	1	DACRSEL_HPR	0	HP R Select Right DAC: 0:unselect; 1: Select
	0	SDTSEL_HPR		HP R Select Side Tone: 0:unselect; 1: Select

11.13.5 RECMIX

11.13.5.1 Generation Description and function

The Mixer can mix signals from Left DAC, SideTonePGA, Right DAC and mono DAC source.



Note: When MUTE=1, SEL1, 2, 3, 4 are all off.

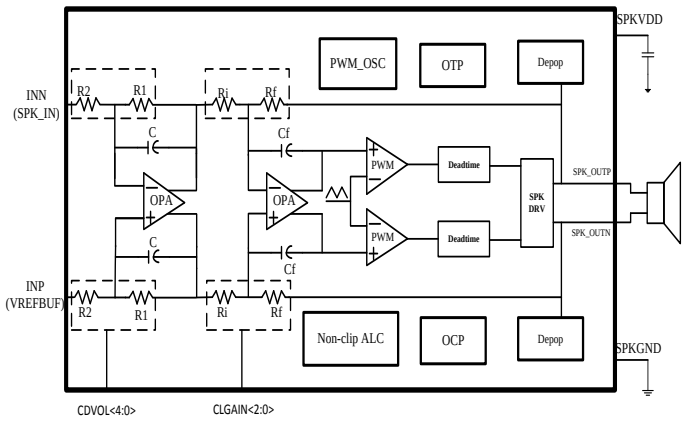
R=41kohm; C=159fF

11.13.5.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
RegR91	7	RECMIXEN	0	REC Mixer Enable. 1: Enable；0：Disable
	6	RECMIXMU	1	REC Mixer Mute. 0: Un-Mute; 1：Mute
	5	DACMONOSEL_REC	0	REC Select mono DAC: 0:unselect 1:select
	4	DACLSEL_REC	0	REC Select Left DAC: 0:unselect; 1: Select
	3	DACRSEL_REC	0	REC Select right DAC: 0:unselect; 1: Select
	2	SDTSEL_REC	0	REC Select Side Tone: 0:unselect; 1: Select
	1:0	SLOWCLK_SEL[1:0]	00	Slow Clock selection signal 00: 2^21 MCLK 01: 2^20MCLK 10：2^19 MCLK 11: 2^18MCLK

11.14 CLASSD

11.14.1 Generation Description and function



The Class-D is a mono high efficiency filter-free, analog in Class-D audio power amplifier (class-D amp). It can operate from 2.8V to 4.5V supply. When powered with 4.2V voltage, it can deliver up to 0.8W power into a 8Ω load with 1% THD.

The filter-free architecture allows the device to drive the speaker directly. High power efficiency is achieved due to digital output at the load.

High PSRR and differential architecture provide increased immunity to noise and RF rectification. The Class-D offers low THD+N, allowing it to produce high-quality sound reproduction.

The Class-D has an automatic peak limiter that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the Class D input remains constant. A digital peak detector monitors the Class D output, when clipping, it will sending a signal to the digital circuit which would decrease the PGA volume.

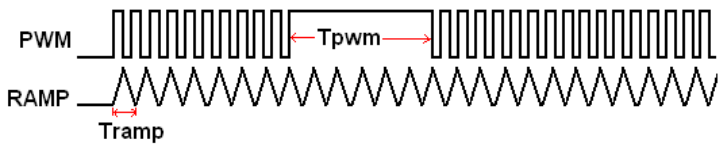
11.14.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R8	7	CD_MUTE	1	Class D Volume mute control. 0: unmute; 1: mute
	6	SPKZCEN	0	Class D PGA gain control zero-crossing enable 0: Disable; 1: Enable
	5			

	4:0	CDVOL[4:0]	10100	Volume gain control. 00000: -26dB 00001: -25dB 00010: -24dB 00011: -23dB 00100: -22dB 00101: -21dB 00110: -20dB 00111: -19dB 01000: -18dB 01001: -17dB 01010: -16dB 01011: -15dB 01100: -14dB 01101: -13dB 01110: -12dB 01111: -11dB 10000:-10dB 10001:-9dB 10010:-8dB 10011:-7dB 10100:-6dB(default) 10101:-5dB 10110:-4dB 10111:-3dB 11000:-2dB 11001:-1dB 11010:0dB 11011:1dB 11100:2dB 11101:3dB 11110:4dB 11111: 5dB
RegR9	1	CD_ALC_CLR	0	Class-D ALC flag clear
	0	CD_DTS_CLR	0	Class-D over temperature flag clear
RegR93	7	CD_CK_SEL	0	0: internal OSC; 1: no clock
	6	CD_ENB_TMNT	0	Time counter of CTRL_LOGIC enable control 0: Enable the time counter. 1: Disable the time counter
	5	CD_TSAT	0	Time counter Start Time control 0: Fast start(about 5ms); 1: Slow start(about 40ms)
	4	LOWPOWER	0	ClassD power consumption control 0: Normal work; 1: Low power mode
	3	PD_OCT	1	OCT detect （over current protect）start up control. 0: Start up; 1: Stop

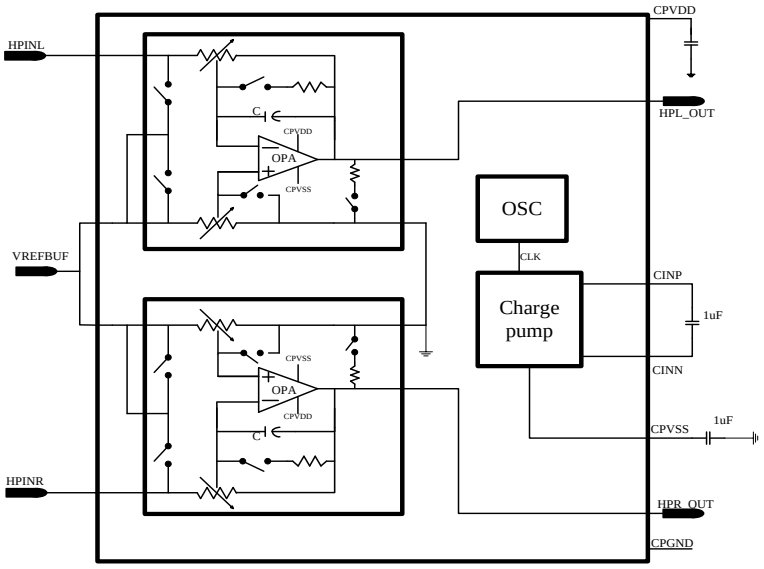
	2	PD3_CD	1	Function blocks of Class-D （other than op、PWM_osc、bias） power down control 0: Normal work. 1: Power-down
	1	PD2_CD	1	Function blocks Class-D（op、PWM_osc） power down control 0: Normal work. 1: Power-down
	0	PD_CD	1	Class-D（bias） power down control 0: Normal work. 1: Power-down
RegR94	7:6	CD_IBSRMP[1:0]	00	ClassD（Speaker）internal OSC_RAMP bias current select 00 :10U; 01: 9U; 10: 11U; 11: 10U
	5:3	CLGAIN[2:0]	000	Close-loop gain control 000 :6dB; 001: 6.90dB; 010: 6.60 dB; 011: 6.32 dB 100: 5.71 dB; 101: 5.44 dB; 110: 5.15 dB; 111: 4.91 dB
	2:1	CD_ALC[1:0]①	00	The trigger point of output signal clipping control 00: n=4; 01: n=2; 10: n=8; 11: n=16
	0	CD_ENB_ALC	0	Clipping ALC function enable control 0: normal work; 1: disable
RegR95	7:6	NOVSEL[1:0]	01	ClassD Dead Time Control 00:8ns; 01:9ns; 10:10.5ns; 11:13ns;
	5	TSSET	1	ClassD Temp-sensor threshold 0: 134C（protect）/115C（release）; 1: 112C（protect）/92C（release）;
	4			
	3	CD_ENB_GLITCH	0	Deglitch function enable control 0: Enable deglitch function; 1: Disable deglitch function
	2	CD_ENB_OCT	0	OCT(Over current protection) function enable control 0: Enable OCT function; 1: Disable OCT function
	1	CD_ENB_POP	0	De-pop function enable control 0: Enable De-pop function; 1: Disable De-pop function
	0	TS_EN	0	over temperature protect enable signal ; 0: Disable; 1: Enable
RegR97	3	CD_ALC_OUT		CLASSD ALC IRQ SIGNAL; 1: CD ALC IRQ;0:No IRQ;
	2	CD_DTS		CLASSD OVER TEMPERATURE FLAG SIGNAL; 0:normal; 1:OVER TEMP IRQ;

Note: When PWM is always high and Tpwm≥ n×Tramp, (n=2,4,8,16), the output signal is clipping, ALC block will generate a flag to digital part.



11.15 CLASSG

11.15.1 Generation Description and function



This block has a Class-G stereo headphone amplifiers with an integrated inverting charge pump power supply, the charge pump can supply up to 100mA of peak output current over a 1.6VDC to 1.8VDC supply voltage range. Class-G technology maximizes battery life by offering high performance efficiency.This block has an internal oscillator which can provide a 1MHz clock typically.Using charge-pump eliminates external DC-blocking capacitors.

11.15.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R6	7	HPMUTEL	1	HP left channel Mute control. 1: Mute. 0: Release mute.
	6	HPZCENL	0	HP left channel zero crossing enable. 1: Enable. 0: disable.
	5	HPENL	0	HP left channel Power down. 1: Power on. 0: Power down.

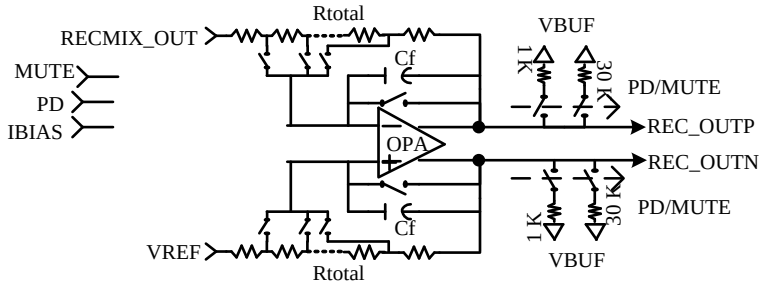
	4:0	HPVOLL[4:0]	11001	Left Channel Headphone Output Volume Control. 11111 = +6dB 11110 = +5dB 11101 = +4dB 11100 = +3dB 11011 = +2dB 11010 = +1dB 11001 = 0Db(default) 11000 = -1dB 10111 = -2dB 10110 = -3dB 10101 = -4dB 10100 = -5dB 10011 = -6dB 10010 = -7dB 10001 = -8dB 10000 = -9dB 01111 = -10dB 01110 = -11dB 01101 = -12dB 01100 = -13dB 01011 = -14dB 01010 = -15dB 01001 = -16dB 01000 = -17dB 00111 = -18dB 00110 = -19dB 00101 = -20dB 00100 = -21dB 00011 = -22dB 00010 = -23dB 00001 = -24dB 00000 = -25dB
~~Reg~~R7	7	HPMUTER	1	HP right channel Mute control. 1: Mute. 0: un mute.
	6	HPZCENR	0	HP right channel zero crossing enable.1: Enable. 0: disable
	5	HPENR	0	HP right channel Power down. 1: Power on. 0: Power down.
	4:0	HPVOLR[4:0]	11001	Right Channel Headphone Output Volume Control. 11111 = +6dB … 1dB steps down to 00000 = -25dB Same to the ‘HPVOLL[4:0]’
~~Reg~~R92	7:6	OSCIB_OPT[1:0]	11	ClassG internal OSC Current Control:00:3.75u；01:8.75u; 10:1.25u; 11:6.25uA

5:4	OSCF_SEL[1:0]	01	ClassG internal OSC Frequency: 00:2M; 01:1M; 10:4M; 11:0.5MHz
3	NVEN	0	Charge pump CPVSS Power down. 1: Power on. 0: Power down.
2	VREFEN_CG	0	CLASS G internal VREF Power down 1: Power up. 0: Power down.
1	OSC_EN	0	ClassG internal OSC Power Down: 1:Enable; 0: Power Down
0	CG_CK_SEL	0	0: from internal osc, 1: no clock

11.16 Receiver

11.16.1 Generation Description and function

This block has a differential output terminal to drive 16 ohm (+30pF) Earphone.
REC CalssAB has a gain control range of [-25dB +6dB] with 1dB/Step.



11.16.2 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
~~Reg~~R5	7	EPMUTE	1	REC Mute control. 1: Mute; 0:Unmute
	6	EPZCEN	0	REC zero crossing enable 1: Enable; 0:disable
	5	EPEN	0	REC Power down. 1: Power on; 0: Power down.
	4:0	EPVOL<4:0>	11001	REC Output Volume Control 11111=+6dB ……1dB steps 11001=0dB (Default) …… 000000=-25dB

11.17 MicBias and Jack/Hookswitch Detection

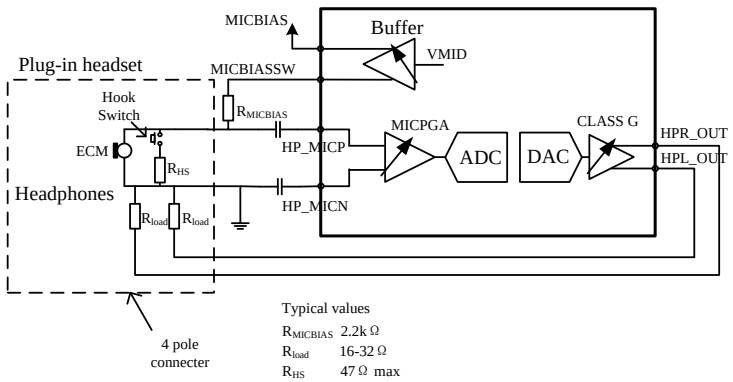
11.17.1 MicBias

11.17.1.1 Generation Description and function

The microphone bias circuit (micbias) provides a 2.625V bias voltage to a microphone connected to Main Mic, HP Mic input port. The circuit is able to supply an output current of more than 3mA. Since it's connected to the port inputs, it should not deteriorate audio performance when the ports are used as line inputs. Especially when the mic-boost is active the micbias output noise should be very low, because it will be amplified. Therefore the target for the output referred noise is set at an aggressive value of -110dBV.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYPE	MAX	UNIT
Microphone Bias						
Load Resistance			0.5	-	-	KΩ
Load Capacitance			-	-	30	pF
Bias Voltage	$V_{MICBIAS}$		2.47	2.624	2.81	V
Bias Current Source	$I_{MICBIAS}$		-	3	-	mA
Output Noise Voltage	Vn	1kHz to 20kHz	-	2.8	-	uV/√Hz

Headset Application Diagram:



11.17.1.2 Register

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION

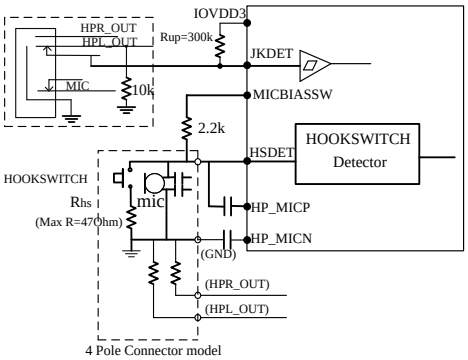
~~Reg~~R84	4:2	VMICSEL	101	VMID_SEL	VMID(V)	VMICSEL	VMICBIAS(V)
				111	1.39	000	2.45
				110	1.43	001	2.534
				101	1.49	010	2.623
				100	1.54	011	2.615
				011	1.60	100	2.614
				010	1.66	101	2.62(default)
				001	1.73	110	2.634
				000	1.80	111	2.656
	1	MICBEN	0	Micbias enable. 0: disable; 1: enable			
	0	MICBSWEN	0	Micbias switch ebable. 0:disable; 1:enable			

11.17.2 Jack/Hookswitch Detection

11.17.2.1 Generation Description and function

The LC1132 provide for detection of audio headset accessory insertion, extraction, and hookswitch events. The detector circuit is designed to operate with minimum power in standby mode. Accessory insertion and removal is detected using the JACKDET pin. The HSDET intended to interface to the external microphone~~-~~, monitor it's bias voltage and watch hookswitch events.

Hookswitch events cause the system to answer an incoming phone call or hang up on an active phone call.



11.17.2.2 Jack and Hookswitch Register

11.17.2.2.1 JKHSIRQST: Jack and Hookswitch interrupt status register

Address: 0x9A

Bits	Symbol	R/W	Function	Default
7	JKDETPOL	RW	**Jack detect polarity** 0: JACKDET high indicate Jack insertion.(Normal close)	0

			1: JACKDET low indicate Jack insertion (Normal Open)	
6	HSDETEN	RW	**Hookswitch detector enable** 0: disable 1: enable	0
5	HS_CMP	R	**Hookswitch comparator output status** 0: Hookswitch released 1: Hookswitch pressed	0
4	JACK_CMP	R	**Jack comparator output status** 0: Jack out 1: Jack in	0
3	HSUPIR	RW	**Hookswitch up interrupt status** Write 1 to clear this interrupt	0
2	HSDNIR	RW	**Hookswitch down interrupt status** Write 1 to clear this interrupt	0
1	JACKOUTIR	RW	**Jack out interrupt status** Write 1 to clear this interrupt	0
0	JACKINIR	RW	**Jack in interrupt status** Write 1 to clear this interrupt	0

11.17.2.2.2 JKHSMSK: Jack and Hookswitch interrupt enable register

Address: 0x9B

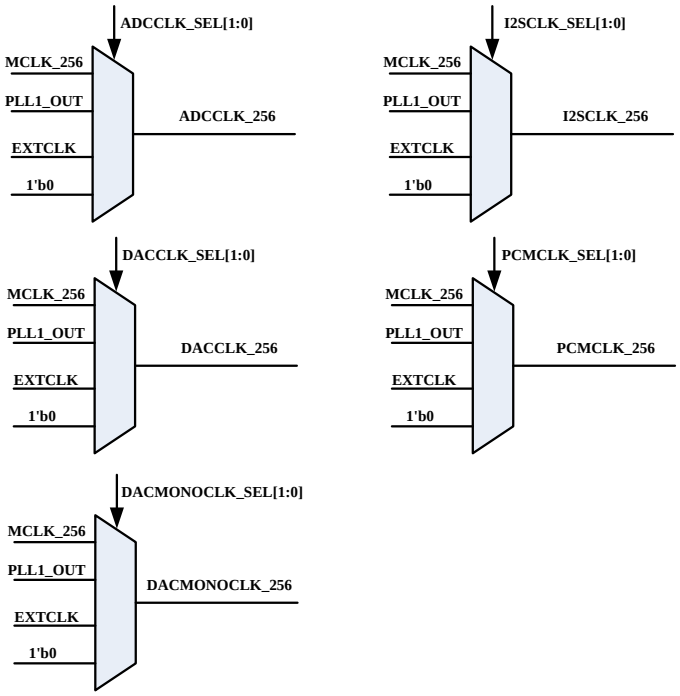
Bits	Symbol	R/W	Function	Default
7	HSUPIREN	RW	**Hookswitch up interrupt enable** 0: disable 1: enable	0
6	HSDNIREN	RW	**Hookswitch down interrupt enable** 0: disable 1: enable	0
5	JACKOUTIREN	RW	**Jack out interrupt enable** 0: disable 1: enable	0
4	JACKINIREN	RW	**Jack in interrupt enable** 0: disable 1: enable	0
3	HSUPIRMSK	RW	**Hookswitch up interrupt mask** 0: unmask 1: mask	0
2	HSDNIRMSK	RW	**Hookswitch down interrupt**	0

			mask 0: unmask 1: mask	
1	JACKOUTIRMSK	RW	**Jack out interrupt mask** 0: unmask 1: mask	0
0	JACKINIRMSK	RW	**Jack in interrupt mask** 0: unmask 1: mask	0

11.18 Digital Core Architecture

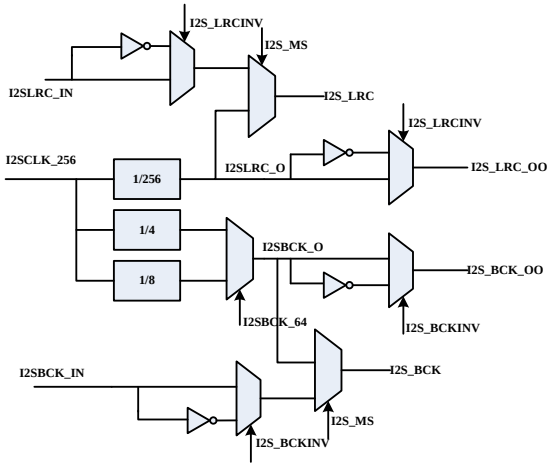
11.18.1 Digital Audio Interface Clock Selection and Configuration

11.18.1.1 256fs Clock Selection

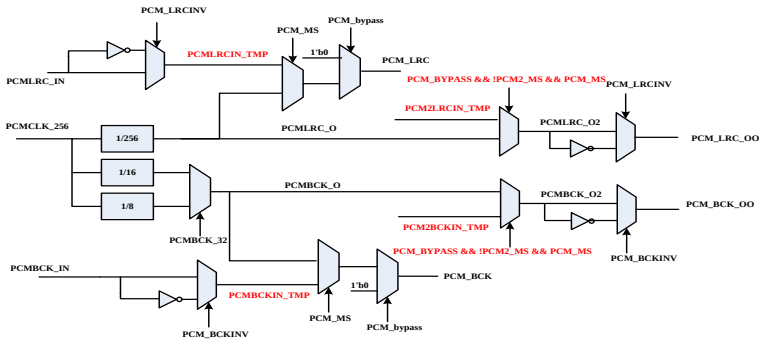


This part is moved to analog part for clock selection, it is just a reference here.

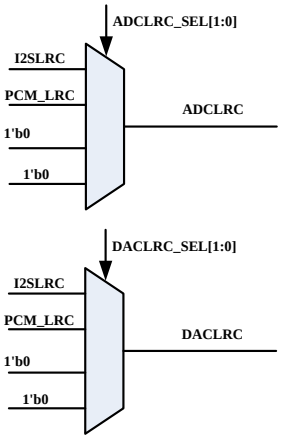
11.18.1.2 BCK and LRC Generation



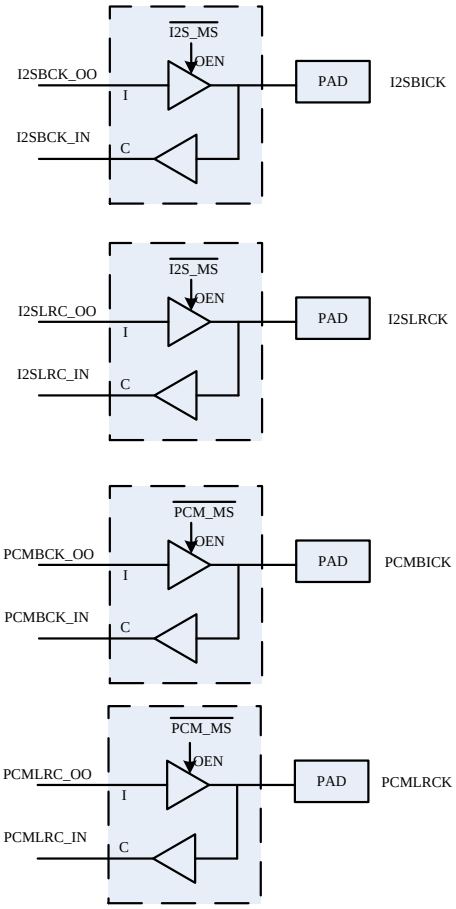
It is a block diagram of I2S part, PCM and BCK and LRC generation are similar.



11.18.1.3 ADCLRC DACLRC Selection



11.18.1.4 INOUT Digital Pad Connection



11.19 I2S interface

11.19.1 Generation Description and function

The LC1132 digital audio interface has four pins described as below:

Interface	Signal define	Type	IN/OUT	Description
I2S	I2SBICK	Digital	INOUT	I2S Bit Clock Signal
	I2SLRCK	Digital	INOUT	Left/right channel select signal
	I2SSDTO	Digital	OUT	Serial data output signal
	I2SSDTI	Digital	IN	Serial data input signal

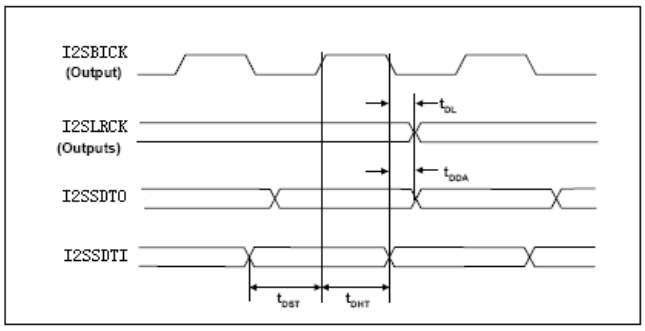
The LC1132 can be configured as either a master or slave mode device. As a master

(I2SMS = 1) device, the LC1132 generates I2SBICK and I2SLRCK and thus controls sequencing of the data transfer on I2SSDTI and I2SSDTO. In slave mode (I2SMS=0), the LC1132 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the I2SMS control bit.

11.19.2 Specification

11.19.2.1 I2S Audio Interface timing

11.19.2.1.1 Digital Audio Interface-Master Mode

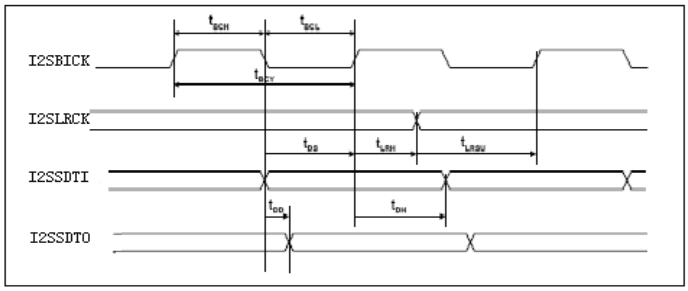


~~PARAMETER SYMBOL MIN TYP MAX UNIT~~

Audio Data Input Timing Information					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
I2SLRCK propagation delay from I2SBICK falling edge	t_{DL}	0		10	ns
I2SSDTO propagation delay from I2SBICK falling edge	t_{DDA}	0		10	ns
I2SSDTI setup time to I2SBICK rising edge	t_{DST}	10			ns
I2SSDTI hold time from I2SBICK rising edge	t_{DHT}	10			ns

带格式表格

11.19.2.1.2 Digital Audio Interface-slave Mode



~~PARAMETER~~	~~SYMBOL~~	~~MIN~~	~~TYP~~	~~MAX~~	
Audio Data Input Timing Information					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
I2SBICK cycle time	t_{BCY}	50			ns
I2SBICK pulse width high	t_{BCH}	20			ns
I2SBICK pulse width low	t_{BCL}	20			ns
I2SLRCK set-up time to I2SBICK rising edge	t_{LRSU}	10			ns
I2SLRCK hold time from I2SBICK rising edge	t_{LRH}	10			ns
I2SSDTI set-up time from I2SBICK rising edge	t_{DS}	10			ns
I2SSDTI hold time from I2SBICK rising edge	t_{DH}	10			ns
I2SSDTO propagation delay from I2SBICK falling edge	t_{DD}			10	ns

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带格式表格

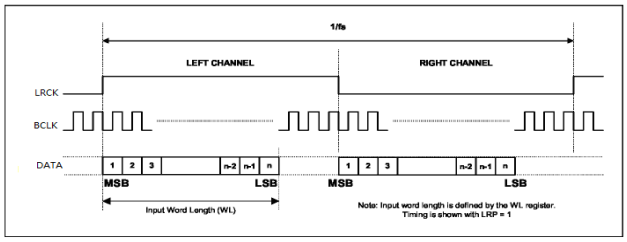
11.19.2.2 Digital Audio Interface Data Format

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP

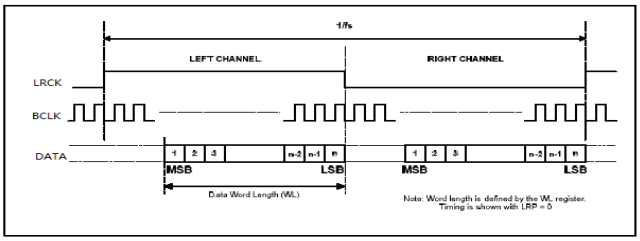
All Four of these modes are MSB first. They are described as below.
(BCLK = I2SBICK, LRCK=I2SLRCK, DATA including I2SSDTI and I2SSDTO in this section)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCK transition.



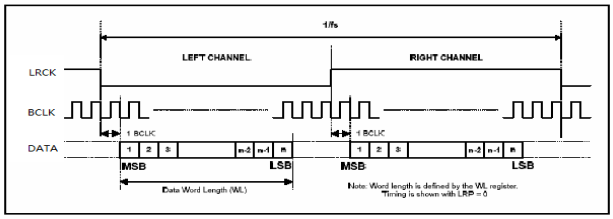
Left Justified Audio Interface (Assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCK transition.



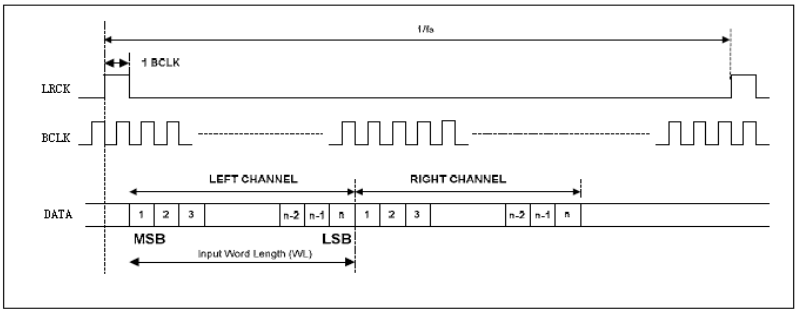
Right Justsified Audio Interface (Assuming n-bit word length)

In I^{2}S mode, the MSB is available on the second rising edge of BCLK following a LRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

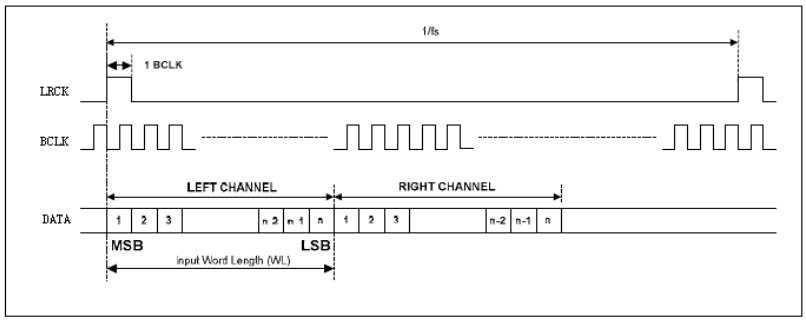


I^{2}S Audio Interface

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRCK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample. In device master mode, the LRCK output will resemble the frame pulse. In device slave mode, it is possible to use any length of frame pulse less than 1/fs.



DSP/PCM Mode Audio Interface (mode A, LRP=0)



DSP/PCM Mode Audio Interface (mode B, LRP=1)

11.19.2.3 Digital Audio Interface Control register

R10	7		0	Reserved
	6	I2S_RSTN	1	I2S soft reset, active low
	5:4	I2SCLK_SEL[1:0]	10	I2S 256fs clock selection 00: PLL out 01: EXTCLK 10: MCLK_IN 11: no clock
	3	I2S_LRCINV	0	I2SLRCK Invert 1: inverted 0: not inverted.
	2	I2S_BCKINV	0	I2SBICK Invert 1: inverted; 0: not inverted
	1	I2SBCK_64	1	BCLK frequency selection in master mode 0: 32Fs 1: 64Fs
	0	I2S_MS	0	Master / Slave Mode Control 1: Master Mode; 0: Slave Mode
R11	7		0	Reserved
	6		0	Reserved
	5	I2S_LOOPBACK	0	1: loop back I2S output DAT to input DAT 0: normal
	4	I2S_LRP	0	DSP mode selection 0: Mode A 1: Mode B
	3:2	I2S_WL[1:0]	10	Audio Data Word Length 11 = 32 bits; 10 = 24 bits 01 = 20 bits; 00 = 16 bits
	1:0	I2S_FORMAT[1:0]	10	Audio Data Format Select 11 = DSP/PCM; 10 = I2S Format 01 = Left justified; 00 = Right justified
R12	7:6	I2S_RSEL[1:0]	00	I2S output right channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output

5:4	I2S_LSEL[1:0]	00	I2S output Left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output
3	I2STXPOL	0	1: invert TX data 0: normal
2	I2SRXPOL	0	1: invert RX data 0: normal
1	I2STXLRSWAP	0	Swap Left and Right Channels data of I2S TX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)
0	I2SRXLRSWAP	0	Swap Left and Right Channels data of I2S RX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)

11.19.2.4 Digital Audio Interface I2SLRCK frequency

Interface Type	Symbol	Min	Type	Max	Units
I2S Interface :					
Reference Clock pin : I2SLRCK, I2SBICK, MCLKIN					
I2S Interface (Slave Mode):					
	Fs(I2SLRCK)	8	8kHz/11.025kHz/12kHz/16kHz/22.05kHz/ 24kHz/32kHz/44.1kHz/48kHz/96kHz	96	kHz
	Fs(I2SBICK)	256		6144	kHz
I2S Interface (Master Mode):					
	Fs(I2SLRCK)	8	8kHz/11.025kHz/12kHz/16kHz/22.05kHz/ 24kHz/32kHz/44.1kHz/48kHz/96kHz	96	kHz
	Fs(I2SBICK)		32Fs/64Fs		kHz
DATA Format					
	Format	I2S	Left justified	Right justified	DSP
Word length					
	length	16	16/20/24/32	32	bits

1. When LC1132 operates in master mode, I2SBICK and I2SLRCK are generated from MCLKIN, whose frequency is 256Fs (come from external or PLL output clock)
2. LC1132 Stereo DAC, mono DAC, ADC1 and ADC2, must operate at the same sample frequency which equal to I2SLRCK if they are connected to the I2S audio interface.

~~Note:~~
~~1. When LC1132 operates at master mode, I2SBICK and I2SLRCK is generated from MCLKIN, which frequency is 256Fs (come from external or PLL output clock)~~
~~2. LC1132 Stereo DAC, Mono ADC, Digital MIC must operate at the same sample frequency which equal to I2SLRCK if they are connected to the I2S audio interface.~~

11.20 PCM interface

11.20.1 Generation Description and function

PCM interface has four pins described as below:

Interface	Signal define	Type	IN/OUT	Description
PCM	PCMBICK	Digital	INOUT	PCM Bit Clock signal
	PCMSYNC	Digital	INOUT	Synchronous clock signal
	PCMSDTO	Digital	OUT	Serial data output
	PCMSDTI	Digital	IN	Serial data input

The LC1132 PCM interface can be configured as either a master or slave mode device. As a master (PCMMS = 1) device, the LC1132 generates PCMBICK and PCMLRCK and thus controls sequencing of the data transfer on PCMSDTI and PCMSDTO. In slave mode (PCMMS=0), the LC1132 responds with data to clocks it receives over the PCM interface. The mode can be selected by writing to the PCMMS control bit.

11.20.2 Specification

11.20.2.1 PCM Voice Interface Data Format

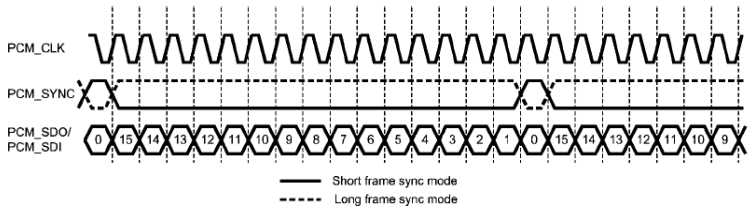
Two data formats are supported in the PCM interface:

- Short Frame Sync
- Long Frame Sync

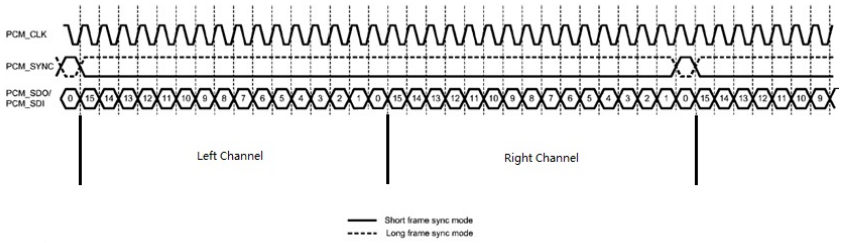
Both of the two modes are MSB first. They are described as below.
(PCM_CLK = PCMBICK, PCM_SYNC=PCMSYNC, PCM_SDO = PCMSDTO,
PCM_SDI = PCMSDTI in this section)

In Short frame sync mode, MSB is available on 2nd falling edge of PCM_CLK following a rising edge of PCM_SYNC. And In long frame sync mode, MSB is available on 2nd falling edge of PCM_CLK following a falling edge of PCM_SYNC. The PCM data length is always to be 16bit. There may be unused PCM_CLK cycles between the LSB of the current PCM data and the next sample.

LC1132 PCM interface can act as dual-channel interface if needed when PCM_CLK frequency is over 32Fs(where Fs is the frequency of PCM_SYNC). In dual channel mode, the left channel data is transferred same with mono mode, and the right channel data immediately follows left channel data. (As DSP/PCM mode described at I2S audio interface section)



PCM Serial Data Format (16 bit example)



PCM dual-channel mode (32 bit example)

11.20.2.2 PCM Interface Control register

R13	7	PCM_UALAW_INV	1	PCM UALAW inv 1: u-law all bits or A-law even bit inverted 0: not inverted
	6	PCM_DB	0	PCM interface in dual-channel mode 1: dual-channel 0: normal
	5:4	PCM_LSEL[1:0]	00	PCM output left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10 ,11: Zero output
	3:2	PCM_RSEL[1:0]	00	PCM output right channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10,11: Zero output
	1:0	PCM_Compand[1:0]	00	PCM Audio Data Format Select 00 = 16bit PCM; 01 = u-law (8bit u-law at PCM[15:7]) 10 = A-law (8bit A-law at PCM[15:7]) 11: reserved.
R15	7		0	reserved
	6	PCM_RSTN	1	PCM soft reset, active low
	5:4	PCMCLK_SEL[1:0]	10	PCM 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
	3	PCM_SYNCSEL	0	PCM sync format selection 1: long frame sync 0: short frame sync
	2	PCM_BCKINV	0	PCM BICK Invert 1: inverted; 0: not inverted
	1	PCMBCK_32	1	PCMBICK frequency selection in master mode 0: 16Fs 1: 32Fs

	0	PCM_MS	0	PCM Master / Slave Mode Control 1: Master Mode; 0: Slave Mode

11.20.2.3 PCM Interface PCMSYNC frequency

Interface Type	Symbol	Min	Type	Max	Units
Reference Clock pin : PCMSYNC, PCMBICK, PCMMCLKIN					
PCM Interface (Slave Mode):					
	Fs(PCMSYNC)	-	8/16	-	kHz
	Fs(PCMBICK)	128	-	4096	kHz
PCM Interface (Master Mode):					
	Fs(SYNC)	-	8/16	-	kHz
	Fs(BICK)		16 Fs /32 Fs		kHz
DATA Format					
	Format	Short frame sync	Long frame sync		
Compand					
	Format	16bit linear	8bit u-law	8bit A-law	

PCM interface electrical characteristics

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Note:

1:When LC1132 operates in master mode, PCMBICK and PCMSYNC are generated from MCLKIN, whose frequency is 256Fs (come from external or PLL output clock)

2: LC1132 Stereo DAC, Mono DAC, ADC1 and ADC2 must operate at the same sample frequency which equal to PCMSYNC if they are connected to the same PCM interface.

~~1: When LC1132 operates at master mode, PCMBICK and PCMSYNC is generated from PCMMCLKIN, which frequency is 256Fs (come from external or PLL output clock)~~

~~2:LC1132 Stereo DAC, Mono ADC, Digital MIC must operate at the same sample frequency which equal to PCMSYNC1 (or PCMSYNC2) if they are connected to the same PCM interface.~~

~~In BYPASS mode, at least one of the two LC1132 PCM interface need to operate at master mode. Both of them operate at slave mode is forbidden.~~

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11.20.2.4 u-Law and A-Law companding method

G.711 defines two main compression algorithms, the μ-law algorithm (used in North America & Japan) and A-law algorithm (used in Europe and the rest of the world). Both are logarithmic, but A-law was specifically designed to be simpler for a computer to process. The standard also defines a sequence of repeating code values which defines the power level of 0 dB.

The μ-law and A-law algorithms encode 14-bit and 13-bit signed linear PCM samples (in our codec, both are 16-bit for simply) to logarithmic 8-bit samples. Thus, the G.711 encoder will create a 64 kbit/s bit stream for a signal sampled at 8kHz.

G.711 μ-law tends to give more resolution to higher range signals while G.711 A-law provides

more quantization levels at lower signal levels. When using µ-law G.711 in networks where suppression of the all 0 character signal is required, the character signal corresponding to negative input values between decision values numbers 127 and 128 should be 00000010 and the value at the decoder output is -7519. The corresponding decoder output value number is 125.

A-law encoding thus takes a 13-bit signed linear audio sample as input and converts it to an 8 bit value as follows:

Linear input code	Compressed code
s0000000wxyza	s000wxyz
s0000001wxyza	s001wxyz
s000001wxyzab	s010wxyz
s00001wxyzabc	s011wxyz
s0001wxyzabcd	s100wxyz
s001wxyzabcde	s101wxyz
s01wxyzabcdef	s110wxyz
s1wxyzabcdefg	s111wxyz

Where s is the sign bit, and the ellipsis represents additional low-order bits that are not encoded. So for example, 1000'0000'1010'1111 maps to 1000'1010 (according to the first row of the table), and 0000'0001'1010'1111 maps to 0001'1010 (according to the second).

This can be seen as a floating point number with 4 bits of mantissa and 3 bits of exponent. In addition, the standard specifies that all resulting even bits are inverted before the octet is transmitted. This is to provide plenty of 0/1 transitions to facilitate the clock recovery process in the PCM receivers. Thus, a silent A-law encoded PCM channel has the 8 bit samples coded 0x55 instead of 0x00 in the octets (or 0xD5 if the sign bit happens to be set).

Note:

1. the ITU define bit 1 to have the value 128 and bit 8 to have the value 1.The more widely accepted convention has bit7=128 and bit 0=1.
2. when data is sent over E0 (G.703), MSB (sign bit) is sent first and LSB is sent last.

µ-Law

µ-law encoding takes a 14-bit signed linear audio sample as input, increases the magnitude by 32 (binary 100000), and converts it to an 8 bit value as follows:

Linear input code	Compressed code
s00000001wxyza	s000wxyz
s0000001wxyzab	s001wxyz
s000001wxyzabc	s010wxyz
s00001wxyzabcd	s011wxyz
s0001wxyzabcde	s100wxyz
s001wxyzabcdef	s101wxyz
s01wxyzabcdefg	s110wxyz
s1wxyzabcdefgh	s111wxyz

Where s is the sign bit, and the ellipsis represents additional low-order bits that are not encoded.

In addition, the standard specifies that all result bits are inverted before the octet is

transmitted. Thus, a silent μ-law encoded PCM channel has the 8 bit samples coded 0xFF instead of 0x00 in the octets. Also the "trick" of adding 32 means μ-law does not encode all 14-bit values, inputs must be within ±8159.

11.21 Clocking and Sample Rates（PLL）

11.21.1 Generation Description and Function

Generate all clocks for the CODEC.

Output Features:

1. 4 output modes: MCLK, PLL_OUT, EXTCLK and disabled.
2. 11.2896MHz /12.288MHz.
3. VCO covers 19MHz~283MHz.

Input Features:

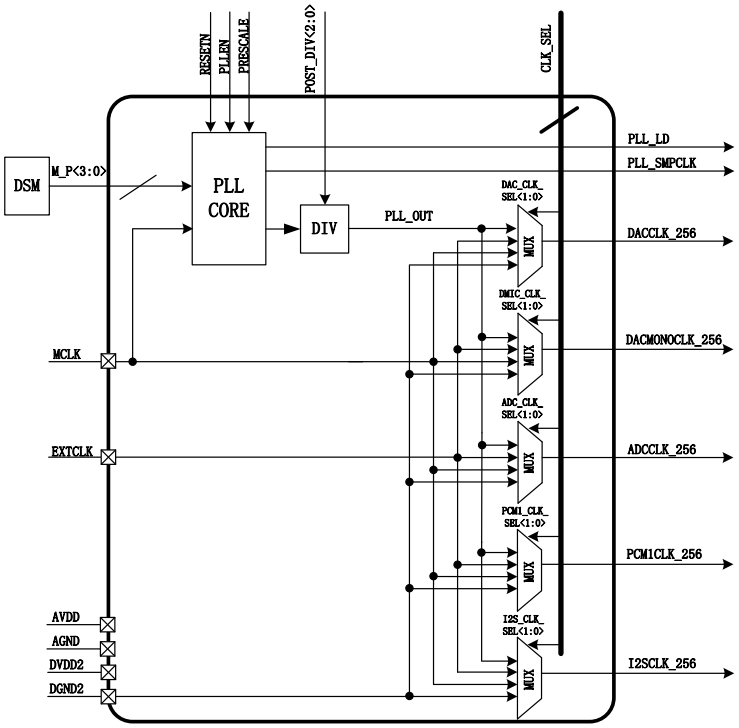
1. MCLK: 11.91MHz ~27MHz.
2. A power down input.
3. A reset input.

Frequency Plan:

The frequency synthesizer produces various clock outputs with different frequencies input. When the PLL_OUT is selected as the output clock, the PLL Core is enabled and the preset frequency can be changed by resending the registers PLL_INT [3:0] and PLL_FRA [23:0]. The M_P (divisor) generated by a Delta-Sigma Modulator (in the digital part) is not a fixed integer so that its 'average' value is fractional. The frequency of PLL_OUT is determined by the following equations:

$f_{PLL\_OUT} = (f_{MCLK} / PRESCALE) * M\_P / POSTDIV$

M_P = PLL_INT [3:0]+ PLL_FRA [23:0]/2^24



PLL Top Diagram

11.21.2 PAD Description

PAD NAME	I/O	DESCRIPTION
AVDD	I	CODEC analog power supply
AGND	I	CODEC analog ground
DVDD2	I	CODEC digital ground
DGND2	I	CODEC digital ground
MCLK	I	master clock input
EXTCLK	I	external clock input

11.21.3 Sample Rate Conversion

MCLK / PRESCALE =12MHz

Fs(KHz)	256Fs(MHz)	POST_DIV	fvco(MHz)	M_P	M_INT	M_FRA	PLL_INT[3:0]	PLL_FRA[23:0]
8	2.048	64(101)	131.072	10.92 2666 67	10	0.922667	1010	11101100001100111 1100001
11.025	2.8224	32(100)	90.3168	7.526	7	0.5264	0111	1000011011000010

				4				00100110
12	3.072	32(100)	98.304	8.192	8	0.192	1000	0011000100100110 11101001
16	4.096	32(100)	131.072	10.92 2666 67	10	0.922667	1010	11101100001100111 1100001
22.05	5.6448	16(011)	90.3168	7.526 4	7	0.5264	0111	1000011011000010 00100110
24	6.144	16(011)	98.304	8.192	8	0.192	1000	0011000100100110 11101001
32	8.192	16(011)	131.072	10.92 2666 67	10	0.922667	1010	11101100001100111 1100001
44.1	11.2896	8(010)	90.3168	7.526 4	7	0.5264	0111	1000011011000010 00100110
48	12.288	8(010)	98.304	8.192	8	0.192	1000	0011000100100110 11101001
96	24.576	4(001)	98.304	8.192	8	0.192	1000	0011000100100110 11101001

MCLK / PRESCALE =13MHz

Fs(KHz)	256Fs(MHz)	POST_DIV	fvco(MHz)	M_P	M_INT	M_FRA	PLL_INT[3:0]	PLL_FRA[23:0]
8	2.048	64(101)	131.072	10.08246154	10	0.082462	1010	000101010001110000110011
11.025	2.8224	32(100)	90.3168	6.947446154	6	0.947446	0110	111100101000101111010100
12	3.072	32(100)	98.304	7.561846154	7	0.561846	0111	100011111101010100100110
16	4.096	32(100)	131.072	10.08246154	10	0.082462	1010	000101010001110000110011
22.05	5.6448	16(011)	90.3168	6.947446154	6	0.947446	0110	111100101000101111010100
24	6.144	16(011)	98.304	7.561846154	7	0.561846	0111	100011111101010100100110
32	8.192	16(011)	131.072	10.08246154	10	0.082462	1010	000101010001110000110011
44.1	11.2896	8(010)	90.3168	6.947446154	6	0.947446	0110	111100101000101111010100

48	12.288	8(010)	98.304	7.561846154	7	0.561846	0111	10001111110101010100110
96	24.576	4(001)	98.304	7.561846154	7	0.561846	0111	10001111110101010100110

11.21.4 Register

<table>
<tr><th>REG. ADDR.</th><th>BIT</th><th>REG. NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>R10</td><td>5:4</td><td>I2SCLK_SEL[1:0]</td><td>10</td><td>I2S Clock output selection:<table><tr><td>CLK_SEL<1:0></td><td>OUTPUT</td></tr><tr><td>00</td><td>PLL output</td></tr><tr><td>01</td><td>EXTCLK input</td></tr><tr><td>10</td><td>MCLK input</td></tr><tr><td>11</td><td>no clock</td></tr></table></td></tr>
<tr><td>R15</td><td>5:4</td><td>PCMCLK_SEL[1:0]</td><td>10</td><td>PCM Clock output selection: see above.</td></tr>
<tr><td>R29</td><td>1:0</td><td>ADC1CLK_SEL[1:0]</td><td>10</td><td>ADC1 Clock output selection: see above.</td></tr>
<tr><td>R32</td><td>1:0</td><td>MONO_DACCLK_SEL[1:0]</td><td>10</td><td>MONO DAC Clock output selection: see above.</td></tr>
<tr><td>R45</td><td>1:0</td><td>ADC2CLK_SEL[1:0]</td><td>10</td><td>ADC2 Clock output selection: see above.</td></tr>
<tr><td>R71</td><td>1:0</td><td>DACCLK_SEL[1:0]</td><td>10</td><td>DAC Clock output selection: see above.</td></tr>
<tr><td>R76</td><td>3:0</td><td>PLL_INT_P[3:0]</td><td>0110</td><td>Integer part of PLL output/input frequency ratio
(Default Case: 12M input, 12.288M output)</td></tr>
<tr><td>R77</td><td>7:0</td><td>PLL_FRC_P[7:0]</td><td>11101001</td><td rowspan="3">Fractional part of PLL output/input frequency ratio
(Default Case: 12M input, 12.288M output)</td></tr>
<tr><td>R78</td><td>7:0</td><td>PLL_FRC_P[15:8]</td><td>00100110</td></tr>
<tr><td>R79</td><td>7:0</td><td>PLL_FRC_P[23:16]</td><td>00110001</td></tr>
<tr><td rowspan="3">R80</td><td>7:5</td><td>CP_P[2:0]</td><td>100</td><td>Charge pump current selection:<table><tr><td>CP_P1<2:0></td><td>I(uA)</td></tr><tr><td>000</td><td>20</td></tr><tr><td>001</td><td>25</td></tr><tr><td>010</td><td>30</td></tr><tr><td>011</td><td>35</td></tr><tr><td>100</td><td>40</td></tr><tr><td>101</td><td>45</td></tr><tr><td>110</td><td>50</td></tr><tr><td>111</td><td>55</td></tr></table></td></tr>
<tr><td>4</td><td>PLL_FRCEN_P</td><td>0</td><td>Fractional N function selection: 0: disable; 1: enable</td></tr>
<tr><td>3</td><td>RESETN_P</td><td>0</td><td>PLL reset signal: 0: enable; 1: disable.</td></tr>
</table>

<table>
<tr><td></td><td>2:0</td><td>POST_DIV1[2:0]</td><td>000</td><td>Post divider selection:<table><tr><td>POST_DIV<2:0></td><td>DIV</td></tr><tr><td>000</td><td>2</td></tr><tr><td>001</td><td>4</td></tr><tr><td>010</td><td>8</td></tr><tr><td>011</td><td>16</td></tr><tr><td>100</td><td>32</td></tr><tr><td>101</td><td>64</td></tr><tr><td>110</td><td>64</td></tr><tr><td>111</td><td>64</td></tr></table></td></tr>
<tr><td>R81</td><td>6</td><td>PRESCALE</td><td>0</td><td>Prescale division selection: 0: division=1; 1: division=2.</td></tr>
<tr><td></td><td>5</td><td>PLLEN</td><td>0</td><td>PLL enable signal: 0: disable; 1: enable.</td></tr>
<tr><td></td><td>4</td><td>TESTVCOB_P</td><td>1</td><td>VCO function test selection: 0: test enabled, Vctrl=VDD/2; 1: test disabled, normal work.</td></tr>
<tr><td></td><td>3:2</td><td>RLPF_P[1:0]</td><td>10</td><td>VCO V to I converter resister selection:<table><tr><td>RVI_P<1:0></td><td>resister(KΩ)</td></tr><tr><td>00</td><td>3</td></tr><tr><td>01</td><td>4</td></tr><tr><td>10</td><td>5</td></tr><tr><td>11</td><td>6</td></tr></table></td></tr>
<tr><td></td><td>1:0</td><td>RVI_P[1:0]</td><td>01</td><td>Low pass filter resister selection:<table><tr><td>RLPF_P<1:0></td><td>resister(KΩ)</td></tr><tr><td>00</td><td>4</td></tr><tr><td>01</td><td>5</td></tr><tr><td>10</td><td>6</td></tr><tr><td>11</td><td>8</td></tr></table></td></tr>
</table>

11.21.5 Application Information

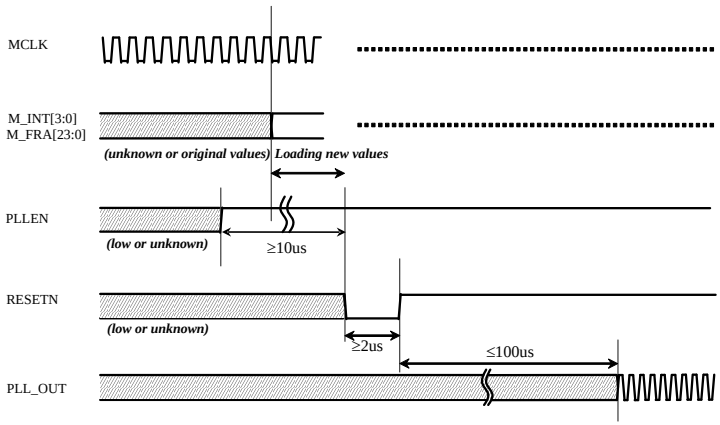
PLLEN low powers down the frequency synthesizer and RESETN low resets the phase-frequency detector, feedback divider, charge-pump, filter, and fractional-N generator. Following are the appropriate rules of using PLLEN and RESETN as well as loading the divisor values:

1. In order to have a proper initialization, after VDD and VSS are fully charged, PLLEN high for > 10 μs needs to precede RESETN low for > 2 μs;

2. PLLEN switching from low (or unknown) to high can either lead or lag the loading of the divisor values;

3. It takes no more than 100 μs to generate a stable output clock after RESETN switching from low to high;

4. A low (> 2 μs) of RESETN is also needed when the source clock resumes.

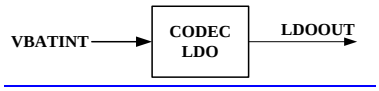


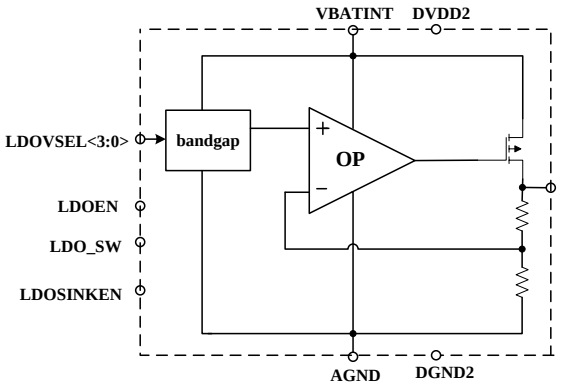
PLL Timing Diagram

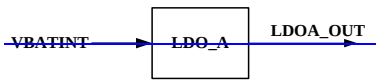
11.22 CODEC LDO

11.22.1 Generation Description and function

Generate Analog core power supply from VBATINT.







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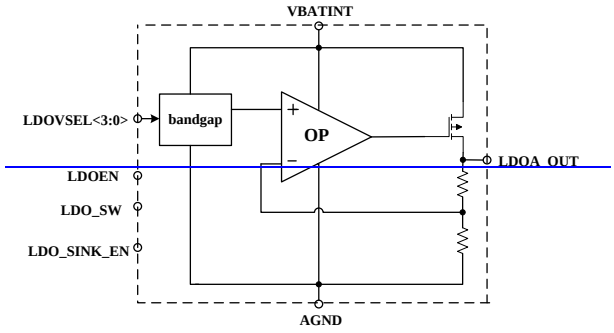
带格式的：两端对齐



11.22.2LDO for PADin and ~~Port~~ PIN Description

External analog PAD Name	Type	Description
VBATINT	I	Analog power supply for CODEC LDO
DVDD2	I	Digital power supply for CODEC LDO
AGND	I	Analog GND for CODEC LDO
DGND2	I	Digital GND for CODEC LDO

带格式表格

Internal PIN Name	Type	Description
LDOOUT	O	Output of CODEC LDO bapass capacitor is 2.2uf
LDOEN	I	Enable control for CODEC LDO
LDOSINKEN	I	Discharge control for CODEC LDO
LDOSEL<3:0>	I	1.8V-3.7V selectable signal bit
LDO_SW	I	Switch mode control for CODEC LDO

带格式表格

~~PIN Name~~	~~I/O~~	~~Description~~
~~VBATINT~~	~~I~~	~~Power supply for LDO_A~~
~~AGND~~	~~I~~	~~GND for LDO_A~~
~~LDOA_OUT~~	~~O~~	~~Output of LDO_A,~~ ~~bapass capacitor is 2.2uf~~
~~LDOEN~~	~~I~~	~~Enable control for LDOA~~
~~LDO_SINK_EN~~	~~I~~	~~Discharge control for LDOA~~
~~LDOSEL<3:0>~~	~~I~~	~~1.8V-3.7V selectable signal bit~~
~~LDO_SW~~	~~I~~	~~Switch mode control for LDOA~~

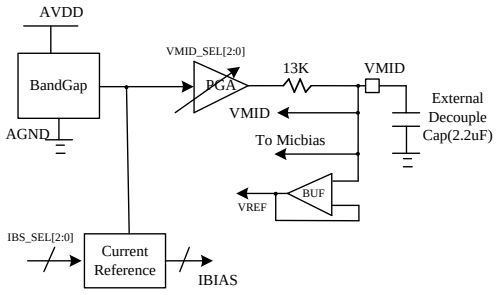
11.22.3 Register

Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
R88	4:1	LDOVSEL[3:0]	0100	Output Voltage Select: LDOVSEL<3:0> LDOA_OUT 0000 3.71 0001 3.61 0010 3.51 0011 3.41 0100 3.31(DEFAULT) 0101 3.21 0110 3.12 0111 3.0 1000 2.92 1001 2.82 1010 2.72 1111 1.82
	0	LDO_SW	0	0: LDO Normal work; 1: Switch mode
R87	7	LDOEN	0	1: LDO Enable; 0: LDO Disable
R98	3	LDOSINKEN	0	LDOEN=0,LDOSINKEN=1,Fast discharge

11.23 POP Suppression Control

11.24 Reference Voltages and MIC Bias

11.24.1 Generation Description and function



11.24.2 Register

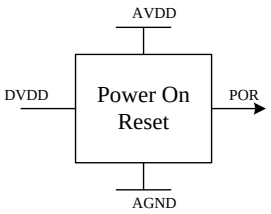
Reg. ADDR.	BIT	LABEL	DEFAULT	DESCRIPTION
Reg96	7	VBSPGAEN	0	Vref enable. 0 = disabled;1 = enabled

	6	IBSEN	0	Top Bias current enable signal. 0 = disabled;1 = enabled
	5	BGPEN	0	Vref output generator enable. 0 = disabled;1 = enabled
	4			
	3:1	IBS_SEL[2:0]	011	I-bias is default 5u and gradually increase from 3u to 7u. (000 to 111) 000 7.05uA; 001 6.27uA 010 5.64uA; 011 5.13uA(Default) 100 4.7uA; 101 4.34uA 110 4.03uA; 111 3.76uA
	0	VREFEN	0	VREF BUFFER Enable. 0 = disabled;1 = enabled
Reg88	7:5	VMID_SEL[2:0]	010	VMID Voltage Select signal: 000 1.804V; 001 1.73V 010 1.661V(Default); 011 1.598V 100 1.539V; 101 1.485V 110 1.434V; 111 1.387V

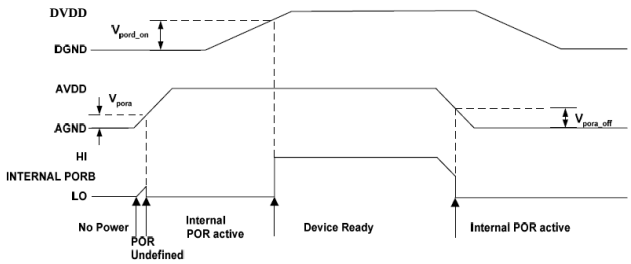
11.25 Thermal Shutdown

11.26 Power on Reset

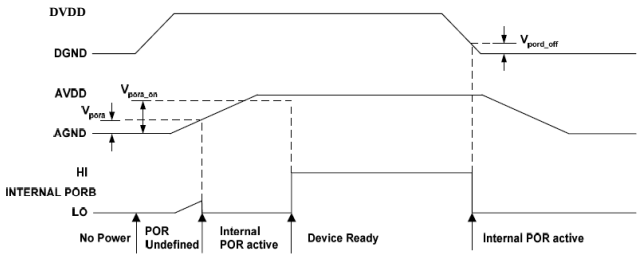
11.26.1 RESET



The following diagram is typical CODEC power up sequence where AVDD is powered before DVDD. After DVDD rises to Vpord_on, POR is set high. When power down, where AVDD falls first, POR is set low whenever AVDD is below Vpora_off.



When AVDD is powered after DVDD, after AVDD rises to Vpord_on, POR is set high. When power down, where DVDD falls first, POR is set low whenever DVDD is below Vpora_off.



SYMBOL	MIN	TYP	MAX	UNIT
Vopra		0.6		V
Vopra_on		1.65		V
Vopra_off		1.5		V
Voprd_on		0.92		V
Voprd_pff		0.9		V

11.26.2CLOCK

Clock Frequency						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYPE**	**MAX**	**UNIT**
Master clock frequency	MCLK		12	12, 13, 26, 256fs	26	MHz
Clock sourcing				Crystal /External clock		
Frequency voltage level		External clock	0.6* DVDD	DVDD		

Figure 25: Clock characteristics

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带格式表格
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带格式的：字体：小五
带格式的：字体：小五
带格式的：字体：小五
带格式的：字体：小五
带格式的：缩进：左侧： 0 厘米，悬挂缩进： 0.5 字符

12 Register

12.1 Register map

Block	Register	Description	Address	R/W	Default
DCDC	DCEN	DCDC enable register	0x00	RW	0x0F
	DC1OVS0	DCDC1 output voltage setting register 0	0x01	RW	0x0E
	DC1OVS1	DCDC1 output voltage setting register 1	0x02	RW	0x0E
	DC2OVS0	DCDC2 output voltage setting	0x03	RW	0x0E

		register 0			
	DC2OVS1	DCDC2 output voltage setting register 1	0x04	RW	0x0E
	DC2OVS2	DCDC2 output voltage setting register 2	0x05	RW	0x0E
	DC2OVS3	DCDC2 output voltage setting register 3	0x06	RW	0x0E
	DC3OVS0	DCDC3 output voltage setting register 0	0x07	RW	0x0F
	DC3OVS1	DCDC3 output voltage setting register 1	0x08	RW	0x0F
	DC4OVS0	DCDC4 output voltage setting register 0	0x09	RW	0x06
	DC4OVS1	DCDC4 output voltage setting register 1	0x0A	RW	0x06
	DCMODE	DCDC mode control register	0x0B	RW	0x00
LDOs for analog	LDOAEN	LDOA2-9 enable register	0x0C	RW	0x81
	LDOAONEN	LDOA external pin enable register	0x0E	RW	0x3E
	LDOAECO	LDOA8/9 ECO mode control register	0x0F	RW	0x00
	LDOAOVSEL	LDOA2/3/4 output voltage select register	0x10	RW	0x0E
	LDOA6OVS	LDOA6 output voltage setting register	0x11	RW	0x0A
	LDOA7OVS	LDOA7 output voltage setting register	0x12	RW	0x00
LDOs for digital	LDODEN1	LDOD1-8 enable register	0x13	RW	0x41
	LDODEN2	LDOD9-11 enable register	0x14	RW	0x00
	LDODONEN	LDOD external pin enable register	0x15	RW	0x06
	LDODECO1	LDOD1-8 ECO mode control register	0x16	RW	0x00
	LDODECO2	LDOD9-11 ECO mode control register	0x17	RW	0x00
	LDODOVSEL	LDOD output voltage select register	0x18	RW	0x01
	LDOD3OVS	LDOD3 output voltage setting register	0x19	RW	0x0A
	LDOD45ENOVS	LDOD4/5 enable and output voltage setting register	0x1A	RW	0x00
	LDOD7OVS	LDOD7 output voltage setting register	0x1B	RW	0x0C
	LDOD8OVS	LDOD8 output voltage setting	0x1C	RW	0x0C

		register			
	LDOD9OVS	LDOD9 output voltage setting register	0x1D	RW	0x00
	LDOD10OVS	LDOD10 output voltage setting register	0x1E	RW	0x00
	LDOD11OVS	LDOD11 output voltage setting register	0x1F	RW	0x08
OCP and UVP control	DCOCPEN	DCDC over-current protection enable register	0x20	RW	0x0F
	LDOAOCPEN	LDOA2-9 over-current protection control register	0x21	RW	0xFF
	LDODOCPEN1	LDOD1-8 over-current protection register	0x22	RW	0xFF
	LDODOCPEN2	LDOD9-11 over-current protection register	0x23	RW	0x07
Sleep mode	DC_SLEEP_MODE	DCDC sleep mode control register	0x24	RW	0x0F
	LDOA_SLEEP_MODE1	LDOA2-9 sleep mode control register	0x25	RW	0xFF
	LDOD_SLEEP_MODE1	LDOD1-8 sleep mode control register	0x26	RW	0xFF
	LDOD_SLEEP_MODE2	LDOD9-11 sleep mode control register	0x27	RW	0x07
LED current sink driver	SINKCR	current sink LED driver control register	0x28	RW	0x0
	LEDIOUT	LED driver output current setting register	0x29	RW	0x11
	VIBIOUT	vibrator direver output current setting register	0x2A	RW	0x01
	INDDIM	LCD current sink dimming register	0x2C	RW	0x08
reference current	IREF	reference current setting register	0x2D	RW	0x02
battery charger	CHGFILTER	charger status filter time register	0x2F	RW	0x00
	CHGCR	charger control register	0x30	RW	0x09
	CHGVSET	charger voltage setting register	0x31	RW	0x02
	CHGCSET	charger current setting register	0x32	RW	0x03
	CHGTSET	charger timer setting register	0x33	RW	0x58
	CHGSTATUS	charging status register	0x34	R	0x00
power status and control	PCST	power-related status register	0x35	R	0x04
	STARTUP_STAT	startup status register	0x36	R	0x00

	US				
	SHDN_STATUS	shutdown status register	0x37	R	0x00
	SHDN_ EN	shutdown enable register	0x2E	RW	0x5F
	BATUVCR	battery undervoltage interrupt control register	0x3F	RW	0x00
ADC	ADCLDOEN	LDO for ADC enable register	0x38	RW	0x0
	ADCCR	ADC control register	0x39	RW	0x0
	ADCCMD	ADC command register	0x3A	RW	0x0
	ADCEN	ADC enable register	0x3B	RW	0x0
	ADCDAT0	4 LSBs of A/D conversion data register	0x3C	RW	0x0
	ADCDAT1	8 MSBs of A/D conversion data register	0x3D	RW	0x0
	ADCFORMAT	A/D conversion data format register	0x3E	RW	0x0
I2C	I2CCR	I2C interface control register	0x40	RW	0x0
clock	CLKCR	clock control register	0x41	RW	0x0
interrupt	IRQST_FINAL	Final interrupt status	0x42	RW	0x0
	IRQST1	interrupt status register 1	0x43	RW	0x0
	IRQST2	interrupt status register 2	0x44	RW	0x0
	IRQEN1	interrupt enable register 1	0x45	RW	0x0
	IRQEN2	interrupt enable register 2	0x46	RW	0x0
	IRQMSK1	interrupt mask register 1	0x47	RW	0x0
	IRQMSK2	interrupt mask register 2	0x48	RW	0x0
DCDC and LDOs softstart control	DCSOFTEN	DCDC1-4 softstart enable register	0x49	RW	0x0F
	LDOASOFTEN	LDOA2-9 softstart enable register	0x4A	RW	0xFF
	LDODSOFTEN1	LDOD1-8 softstart enable register	0x4B	RW	0xFF
	LDODSOFTEN2	LDOD9-11 softstart enable register	0x4C	RW	0x07
DCDC and LDOs fast discharge control	DCFASTDISC	DCDC 1-4 fast discharge enable register	0x4D	RW	0x0F
	LDOAFASTDISC	LDOA2-9 fast discharge enable register	0x4E	RW	0xFF
	LDODFASTDISC 1	LDOD1-8 fast discharge enable register	0x4F	RW	0xFF
	LDODFASTDISC 2	LDOD9-11 fast discharge enable register	0x50	RW	0x07
thermal shutdown	TSHUT	thermal shutdown enable register	0x51	RW	0x01
test mode	TEST	charger test control register	0x52	RW	0x0F

	DC1PFMCTRL	DCDC1 PFM control register	0x53	RW	0x5A
	DC2PFMCTRL	DCDC2 PFM control register	0x54	RW	0x5A
	DC3PFMCTRL	DCDC3 PFM control register	0x55	RW	0x57
	DC4PFMCTRL	DCDC4 PFM control register	0x56	RW	0x5B
	DC1OVPOCP	DCDC1 OVP and OCP control register	0x57	RW	0x55
	DC2OVPOCP	DCDC2 OVP and OCP control register	0x58	RW	0x55
	DC3OVPOCP	DCDC3 OVP and OCP control register	0x59	RW	0xAD
	DC4OVPOCP	DCDC4 OVP and OCP control register	0x5A	RW	0xAD
	DC12DT	DCDC1 and DCDC2 dead time register	0x5B	RW	0x11
	DC34DT	DCDC3 and DCDC4 dead time register	0x5C	RW	0x11
	DC12RCP	DCDC1 and DCDC2 RCP register	0x5D	RW	0x55
	DC34RCP	DCDC3 and DCDC4 RCP register	0x5E	RW	0x55
version	VERSION	version number register	0x5F	R	0x20
RTC	RTC_SEC	RTC second counter register	0x60	RW	0x0
	RTC_MIN	RTC minute counter register	0x61	RW	0x0
	RTC_HOUR	RTC hour counter register	0x62	RW	0x0
	RTC_DAY	RTC day counter register	0x63	RW	0x0
	RTC_WEEK	RTC week counter register	0x64	RW	0x0
	RTC_MONTH	RTCmonth counter register	0x65	RW	0x0
	RTC_YEAR	RTC year counter register	0x66	RW	0x0
	RTC_TIME_UPDATE	RTC time update enable register	0x67	W	0x0
	RTC_32K_ADJL	8 LSBs of RTC clock adjust register	0x68	RW	0x0
	RTC_32K_ADJH	8 MSBs of RTC clock adjust register	0x69	RW	0x0
	RTC_SEC_CYCL	8 LSBs of RTC second cycle limit register	0x6A	RW	0xff
	RTC_SEC_CYCH	8 MSBs of RTC second cycle limit register	0x6B	RW	0x7f
	RTC_CALIB_UPDATE	RTC clock calibration upate register	0x6C	W	--
	RTC_AL1_SEC	second setting for RTC alarm interrupt1	0x6D	RW	0x0
	RTC_AL1_MIN	minute setting for RTC alarm interrupt1	0x6E	RW	0x0
	RTC_AL2_SEC	second setting for RTC alarm interrupt2	0x6F	RW	0x0
	RTC_AL2_MIN	minute setting for RTC alarm	0x70	RW	0x0

		interrupt 2			
	RTC_AL2_HOUR	hour setting for RTC alarm interrupt 2	0x71	RW	0x0
	RTC_AL2_DAY	day setting for RTC alarm interrupt 2	0x72	RW	0x0
	RTC_AL2_MONTH	month setting for RTC alarm interrupt 2	0x73	RW	0x0
	RTC_AL2_YEAR	year setting for RTC alarm interrupt 2	0x74	RW	0x0
	RTC_AL_UPDATE	RTC alarm time update register	0x75	W	--
	RTC_INT_EN	RTC interrupt enable register	0x76	RW	0x0
	RTC_INT_STATUS	RTC interrupt status register	0x77	RW	0x0
	RTC_INT_RAW	RTC raw interrupt status register	0x78	R	0x0
	RTC_CTRL	RTC control register	0x79	RW	0x3
	RTC_BK	RTC backup register	0x7A	RW	0x0
	RTC_INT_MASK	RTC interrupt mask register	0x7B	RW	0x0
	RTC_AL1_HOUR	hour setting for RTC alarm interrupt 1	0x7C	RW	0x0
	RTC_AL1_DAY	day setting for RTC alarm interrupt 1	0x7D	RW	0x0
	RTC_AL1_MONTH	month setting for RTC alarm interrupt 1	0x7E	RW	0x0
	RTC_AL1_YEAR	day setting for RTC alarm interrupt 1	0x7F	RW	0x0
PWM	PWM_EN	PWM enable register	0x80	RW	0x00
	PWM_UP	PWM update register	0x81	RW	0x00
	PWM_RESET	PWM reset register	0x82	RW	0x00
	PWM_P	PWM period setting register	0x83	RW	0xFF
	PWM_OCPY	PWM duty cycle setting register	0x84	RW	0x32
OTP control	OTPSEL0	OTP trimming enable register 0	0x86	RW	0x00
	OTPSEL1	OTP trimming enable register 1	0x87	RW	0x00
	OTPMODE	OTP mode register	0x88	RW	0x00
	OTPCMD	OTP command register	0x89	RW	0x00
	TRIM0	Byte0 of OTP trimming parameters setting register	0x8A	RW	0xFF
	TRIM1	Byte1 of OTP trimming parameters setting register	0x8B	RW	0xFF
	TRIM2	Byte2 of OTP trimming parameters setting register	0x8C	RW	0xFF
	TRIM3	Byte3 of OTP trimming parameters setting register	0x8D	RW	0xFF

	TRIM4	Byte4 of OTP trimming parameters setting register	0x8E	RW	0xFF
	TRIM5	Byte5 of OTP trimming parameters setting register	0x8F	RW	0xFF
	TRIM6	Byte6 of OTP trimming parameters setting register	0x90	RW	0xFF
	TRIM7	Byte7 of OTP trimming parameters setting register	0x91	RW	0xFF
	TRIM8	Byte8 of OTP trimming parameters setting register	0x92	RW	0xFF
	TRIM9	Byte9 of OTP trimming parameters setting register	0x93	RW	0xFF
	TRIM10	Byte10 of OTP trimming parameters setting register	0x94	RW	0xFF
	TRIM11	Byte11 of OTP trimming parameters setting register	0x95	RW	0xFF
	TRIM12	Byte12 of OTP trimming parameters setting register	0x96	RW	0xFF
	TRIM13	Byte13 of OTP trimming parameters setting register	0x97	RW	0xFF
	TRIM14	Byte14 of OTP trimming parameters setting register	0x98	RW	0xFF
	TRIM15	Byte15 of OTP trimming parameters setting register	0x99	RW	0xFF
Jack& Hook switch	JKHSIRQST	Jack and hookswitch interrupt status register	0x9A	RW	0x0
	JKHSIRQMSK	Jack and hookswitch interrupt mask register	0x9B	RW	0x0
CODEC	R0		0x9C	RW	0x22
	R1		0x9D	RW	0x00
	R2		0x9E	RW	0x9F
	R3		0x9F	RW	0x9F
	R4		0xA0	RW	0x9E
	R5		0xA1	RW	0x99
	R6		0xA2	RW	0x99
	R7		0xA3	RW	0x99
	R8		0xA4	RW	0xB4
	R9		0xA5	RW	0x00
	R10		0xA6	RW	0x62
	R11		0xA7	RW	0x0A
	R12		0xA8	RW	0x00
	R13		0xA9	RW	0x80
	R14		0xAA	RW	0x00

	R15		0xAB	RW	0x62
	R16		0xAC	RW	0x1F
	R17		0xAD	RW	0x80
	R18		0xAE	RW	0x00
	R19		0xAF	RW	0x00
	R20		0xB0	RW	0x00
	R21		0xB1	RW	0x07
	R22		0xB2	RW	0x03
	R23		0xB3	RW	0xE7
	R24		0xB4	RW	0x40
	R25		0xB5	RW	0x28
	R26		0xB6	RW	0x00
	R27		0xB7	RW	0x32
	R28		0xB8	RW	0x00
	R29		0xB9	RW	0x32
	R30		0xBA	RW	0x67
	R31		0xBB	RW	0x00
	R32		0xBC	RW	0x32
	R33		0xBD	RW	0x80
	R34		0xBE	RW	0x00
	R35		0xBF	RW	0x00
	R36		0xC0	RW	0x00
	R37		0xC1	RW	0x07
	R38		0xC2	RW	0x03
	R39		0xC3	RW	0xE7
	R40		0xC4	RW	0x40
	R41		0xC5	RW	0x28
	R42		0xC6	RW	0x00
	R43		0xC7	RW	0x32
	R44		0xC8	RW	0x00
	R45		0xC9	RW	0x32
	R46		0xCA	RW	0xFF
	R47		0xCB	RW	0x80
	R48		0xCC	RW	0x00
	R49		0xCD	RW	0x67
	R50		0xCE	RW	0x67
	R51		0xCF	RW	0x00
	R52		0xD0	RW	0x07
	R53		0xD1	RW	0x23
	R54		0xD2	RW	0x7F
	R55		0xD3	RW	0x00
	R56		0xD4	RW	0x7F
	R57		0xD5	RW	0x00

	R58		0xD6	RW	0x32
	R59		0xD7	RW	0x00
	R60		0xD8	RW	0x02
	R61		0xD9	RW	0x02
	R62		0xDA	RW	0x02
	R63		0xDB	RW	0x02
	R64		0xDC	RW	0x02
	R65		0xDD	RW	0x00
	R66		0xDE	RW	0x00
	R67		0xDF	RW	0x10
	R68		0xE0	RW	0x00
	R69		0xE1	RW	0x00
	R70		0xE2	RW	0x00
	R71		0xE3	RW	0x32
	R72		0xE4	RW	0x10
	R73		0xE5	RW	0x00
	R74		0xE6	RW	0x00
	R75		0xE7	RW	0x00
	R76		0xE8	RW	0x06
	R77		0xE9	RW	0xE9
	R78		0xEA	RW	0x26
	R79		0xEB	RW	0x31
	R80		0xEC	RW	0x80
	R81		0xED	RW	0x19
	R82		0xEE	RW	0x01
	R83		0xEF	RW	0x01
	R84		0xF0	RW	0x74
	R85		0xF1	RW	0x52
	R86		0xF2	RW	0x20
	R87		0xF3	RW	0x20
	R88		0xF4	RW	0x48
	R89		0xF5	RW	0x20
	R90		0xF6	RW	0x20
	R91		0xF7	RW	0x40
	R92		0xF8	RW	0xD0
	R93		0xF9	RW	0x0F
	R94		0xFA	RW	0x00
	R95		0xFB	RW	0x60
	R96		0xFC	RW	0x06
	R97		0xFD	R	0x00
	R98		0xFE	RW	0x3B
	R99		0xFF	RW	0x00

12.2 PMU Register descriptions

12.2.1 DCDC

12.2.1.1 DCEN: DCDC Enable Register

Address: 0x00

Bits	Symbol	R/W	Function	Default
7:6	--	--	**Reserved**	--
5:4	DC2_DVS_SEL	R/W	**DVS2 and DVS1 pins fuction select:** 00: DVS[2:1] pins disabled 01: DVS[2:1] controls the output voltage of DCDC2 for DVS application 10: DVS1 controls on and off of DCDC2 11: reserved	0
3	DC4EN	R/W	**DCDC4 enable control** 0: DCDC4 disabled 1: DCDC4 enabled	1
2	DC3EN	R/W	**DCDC3 enable control:** 0: DCDC3 disabled 1: DCDC3 enabled	1
1	DC2EN	R/W	**DCDC2 enable control:** 0: DCDC2 disabled 1: DCDC2 enabled	1
0	DC1EN	R/W	**DCDC1 enable control:** 0: DCDC1 disabled 1: DCDC1 enabled	1

12.2.1.2 DC1OVS0: DCDC1 Output Voltage Setting Register 0

Address: 0x01

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	--
4:0	DC1ONV	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V 01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V	01110

			01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V 10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V 10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	

12.2.1.3 DC1OVS1: DCDC1 Output Voltage Setting Register 1

Address: 0x02

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	--
4:0	DC1SLPV	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V 01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V 01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V 10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V	01110

			10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	

12.2.1.4 DC2OVS0: DCDC2 Output Voltage Setting Register0

Address: 0x03

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	--
4:0	DC2VOUT0	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V 01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V 01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V 10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V 10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	01110

12.2.1.5 DC2OVS1: DCDC2 Output Voltage Setting Register1

Address: 0x04

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	
4:0	DC2VOUT1	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V 01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V 01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V 10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V 10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	01110

12.2.1.6 DC2OVS2: DCDC2 Output Voltage Setting Register2

Address: 0x05

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	
4:0	DC2VOUT2	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V	01110

			01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V 01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V 10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V 10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	

12.2.1.7 DC2OVS3: DCDC2 Output Voltage Setting Register3

Address: 0x06

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	
4:0	DC2VOUT3	R/W	00000: 0.75V 00001: 0.775V 00010: 0.8V 00011: 0.825V 00100: 0.85V 00101: 0.875V 00110: 0.9V 00111: 0.925V 01000: 0.95V 01001: 0.975V 01010: 1.0V 01011: 1.025V 01100: 1.05V 01101: 1.075V 01110: 1.1V 01111: 1.125V 10000: 1.15V 10001: 1.175V	01110

			10010: 1.2V 10011: 1.225V 10100: 1.25V 10101: 1.275V 10110: 1.3V 10111: 1.325V 11000: 1.35V 11001: 1.375V 11010: 1.4V others: reserved	

12.2.1.8 DC3OVS0: DCDC3 Output Voltage Setting Register 0

Address: 0x07

Bits	Symbol	R/W	Function	Default
7:4	--	--	**Reserved**	--
3:0	DC3VOUT0	R/W	**DCDC3 output voltage setting in normal mode:** 0000:1.05 0001:1.1V 0010:1.15V 0011:1.2V 0100: 1.21V 0101: 1.22V 0110: 1.23V 0111: 1.24V 1000: 1.25V 1001: 1.35V 1010: 1.5V 1011: 1.6V 1100: 1.65V 1101: 1.7V 1110: 1.75V 1111: 1.8V	1111

12.2.1.9 DC3OVS1: DCDC3 Output Voltage Setting Register 1

Address: 0x08

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	DC3VOUT1	R/W	DCDC3 output voltage setting in sleep mode: 0000:1.05 0001:1.1V 0010:1.15V 0011:1.2V 0100: 1.21V 0101: 1.22V 0110: 1.23V 0111: 1.24V 1000: 1.25V 1001: 1.35V 1010: 1.5V 1011: 1.6V 1100: 1.65V 1101: 1.7V	1111

			1110: 1.75V 1111: 1.8V	

12.2.1.10 DC4OVS0: DCDC4 Output Voltage Setting Register

Address: 0x09

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	DC4VOUT0	R/W	DCDC4 output voltage setting in normal mode: 0000: 0.9V 0001: 0.95V 0010: 1.0V 0011: 1.05V 0100: 1.1V 0101: 1.15V 0110: 1.2V 0111: 1.21V 1000: 1.22V 1001: 1.23V 1010: 1.24V 1011: 1.25V 1100: 1.35V 1101: 1.5V 1110: 1.7V 1111: 1.8V	0110

12.2.1.11 DC4OVS1: DCDC4 Output Voltage Setting Register

Address: 0x0A

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	DC4VOUT1	R/W	DCDC4 output voltage setting in sleep mode: 0000: 0.9V 0001: 0.95V 0010: 1.0V 0011: 1.05V 0100: 1.1V 0101: 1.15V 0110: 1.2V 0111: 1.21V 1000: 1.22V 1001: 1.23V 1010: 1.24V 1011: 1.25V 1100: 1.35V 1101: 1.5V 1110: 1.7V 1111: 1.8V	0110

12.2.1.12 DCMODE: DC-DC Mode Control Register

Address: 0x0B

Bits	Symbol	R/W	Function	Default
7	DC4_LP_IN_SLP	R/W	**DCDC4 low power mode enable when system in Sleep mode** 0: DCDC4 switches to PFM mode when system in Sleep mode 1: DCDC4 enters low power mode when system in Sleep mode	0
6	DC3_LP_IN_SLP	R/W	**DCDC3 low power mode enable when system in Sleep mode**	0

			0: DCDC3 switches to PFM mode when system in Sleep mode 1: DCDC3 enters low power mode when system in Sleep mode	
5	DC2_LP_IN_SLP	R/W	**DCDC4 low power mode enable when system in Sleep mode** 0: DCDC2 switches to PFM mode when system in Sleep mode 1: DCDC2 enters low power mode when system in Sleep mode	0
4	DC1_LP_IN_SLP	R/W	**DCDC4 low power mode enable when system in Sleep mode** 0: DCDC1 switches to PFM mode when system in Sleep mode 1: DCDC1 enters low power mode when system in Sleep mode	0
3	DC4_PWM_FORCE	R/W	**DCDC4 forced PWM mode enable** 1: DCDC4 operates in forced PWM mode 0: DCDC4 chooses PWM/PFM mode automatically	0
2	DC3_PWM_FORCE	R/W	**DCDC3 forced PWM mode enable** 1: DCDC3 operates in forced PWM mode 0: DCDC3 chooses PWM/PFM mode automatically	0
1	DC2_PWM_FORCE	R/W	**DCDC2 forced PWM mode enable** 1: DCDC2 operates in forced PWM mode 0: DCDC2 chooses PWM/PFM mode automatically	0
0	DC1_PWM_FORCE	R/W	**DCDC1 forced PWM mode enable** 1: DCDC1 operates in forced PWM mode 0: DCDC1 chooses PWM/PFM mode automatically	0

12.2.2 LDO for Analog

12.2.2.1 LDOAEN: LDOA2-9 Enable Register

Address: 0x0C

Bits	Symbol	R/W	Function	Default
7	LDOA8EN	R/W	LDOA8 enable control: 0: LDOA8 disabled 1: LDOA8 enabled	1
6	LDOA7EN	R/W	LDOA7 enable control: 0: LDOA7 disabled 1: LDOA7 enabled	0
5	LDOA6EN	R/W	LDOA6 enable control 0: LDOA6 disabled 1: LDOA6 enabled	0
4	LDOA5EN	R/W	LDOA5 enable control 0: LDOA5 disabled 1: LDOA5 enabled	0
3	LDOA4EN	R/W	LDOA4 enable control 0: LDOA4 disabled 1: LDOA4 enabled	0
2	LDOA3EN	R/W	LDOA3 enable control: 0: LDOA3 disabled 1: LDOA3 enabled	0
1	LDOA2EN	R/W	LDOA2 enable control	0

			0: LDOA2 disabled 1: LDOA2 enabled	
0	LDOA9EN	R/W	LDOA9 enable control: 0: LDOA9 disabled 1: LDOA9 enabled	1

Note: LDOA2EN、LDOA3EN 、LDOA4EN、 LDOA5EN and LDOA7EN become valid only when corresponding bit in LDOAONEN are set to 0.

12.2.2.2 LDOAONEN: LDOA External Pin Enable Register

Address: 0x0E

Bits	Symbol	R/W	Function	Default
7:6	--	--	**Reserved**	--
5	LDOA7ONEN	R/W	**LDOA7 external pin enable** 0: disable(LDOA7 on/off controlled by LDOA7EN bit in LDOAEN) 1: enable(LDOA7 on/off controlled directly by LDOA7EN pin)	1
4	LDOA5ONEN	R/W	**LDOA5 external pin enable** 0: disable(LDOA5 on/off controlled by LDOA5EN bit in LDOAEN) 1: enable(LDOA5 on/off controlled directly by LDOA5EN pin)	1
3	LDOA4ONEN	R/W	**LDOA4 external pin enable** 1: enable(LDOA4 on/off controlled directly by LDOA234EN pin) 0: disable(LDOA4 on/off controlled by LDOA4EN bit in LDOAEN)	1
2	LDOA3ONEN	R/W	**LDOA3 external pin enable** 0: disable(LDOA3 on/off controlled by LDOA3EN bit in LDOAEN) 1: enable(LDOA3 on/off controlled directly by LDOA234EN pin)	1
1	LDOA2ONEN	R/W	**LDOA2 external pin enable** 0: disable(LDOA2 on/off controlled by LDOA2EN bit in LDOAEN) 1: enable(LDOA2 on/off controlled directly by LDOA234EN pin)	1
0	--	R/W	Reserved	--

12.2.2.3 LDOAECO: LDOA8/9/10 ECO Mode Control Register

Address: 0x0F

Bits	Symbol	R/W	Function	Default

7: 2	--	--	Reserved	--
1	LDOA9ECO	R/W	LDOA9 ECO mode switch enable 0: LDOA9 does not switch 1: LDOA9 switches to ECO mode automatically in sleep	0
0	LDOA8ECO	R/W	LDOA8 ECO mode switch enable 0: LDOA8 does not switch 1: LDOA8 switches to ECO mode automatically in sleep	0

12.2.2.4 LDOAOVSEL: LDOA2/3/4 Output Voltage Select Register

Address: 0x10

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3	LDOA4OV	R/W	LDOA4 output voltage selection 0: 1.8V 1: 2.85V	1
2	LDOA3OV	R/W	LDOA3 output voltage selection 0: 1.8V 1: 2.85V	1
1	LDOA2OV	R/W	LDOA2 output voltage selection 0: 1.8V 1: 2.85V	1
0	--	--	Reserved	--

12.2.2.5 LDOA6OVS: LDOA6 Output Voltage Setting Register

Address: 0x11

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	LDOA6OV	R/W	LDOA6 output voltage setting 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V	1010 (2.85V)

			1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	

12.2.2.6 LDOA7OVS: LDOA7 Output Voltage Setting Register

Address: 0x12

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	LDOA7OV	R/W	LDOA7 output voltage setting: 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	0000 (1.8V)

12.2.3 LDO for Digital

12.2.3.1 LDODEN1: LDOD1-8 Enable Register

Address: 0x13

Bits	Symbol	R/W	Function	Default
7	LDOD8EN	R/W	**LDOD8 enable control** 0: LDOD8 disabled 1: LDOD8 enabled	0
6	LDOD7EN	R/W	**LDOD7 enable control** 0: LDOD7 disabled 1: LDOD7 enabled	1
5	LDOD6EN	R/W	**LDOD6 enable control** 0: LDOD6 disabled 1: LDOD6 enabled	0

4:3	--	--	**Reserved**	--
2	LDOD3EN	R/W	**LDOD3 enable control** 0: LDOD3 disabled 1: LDOD3 enabled	0
1	LDOD2EN	R/W	**LDOD2 enable control** 0: LDOD2 disabled 1: LDOD2 enabled	0
0	LDOD1EN	R/W	**LDOD1 enable control** 0: LDOD1 disabled 1: LDOD1 enabled	1

Note: LDOD7EN becomes valid only when LDOD7ONEN bit in LDODONEN register is set to 0.

12.2.3.2 LDODEN2: LDOD9-11 Enable Register

Address: 0x14

Bits	Symbol	R/W	Function	Default
7:3	--	--	Reserved	--
3	LDOD11SW	RW	LDOD11 switch enable 0: disabled 1: enabled	0
2	LDOD11EN	R/W	LDOD11 enable control 0: LDOD11 disabled 1: LDOD11 enabled	0
1	LDOD10EN	R/W	LDOD10 enable control 0: LDOD10 disabled 1: LDOD10 enabled	0
0	LDOD9EN	R/W	LDOD9 enable control 0: LDOD9 disabled 1: LDOD9 enabled	0

Note: LDOD9EN and LDOD11EN become valid only when corresponding bit in LDODONEN are set to 0.

12.2.3.3 LDODONEN: LDOD External Pin Enable Register

Address: 0x15

Bits	Symbol	R/W	Function	Default
7: 3	--	--	Reserved	--
2	LDOD11ONEN	R/W	LDOD11 external pin enable 0: disable (LDOD11 on/off controlled by LDOD11EN bit in LDODEN2) 1: enable (LDOD11 on/off controlled directly by LDOD911EN pin)	1
1	LDOD9ONEN	R/W	LDOD9 external pin enable 0: disable (LDOD9 on/off controlled by LDOD9EN bit in LDODEN2) 1: enable (LDOD9 on/off controlled directly by LDOD911EN pin)	1

0	LDOD7ONEN	R/W	LDOD7 external pin enable 0: disable (LDOD7 on/off controlled by LDOD7EN bit in LDODEN1) 1: enable (LDOD7 on/off controlled directly by LDOD7EN pin)	0

12.2.3.4 LDODECO1: LDOD1-8 ECO Mode Control Register

Address: 0x16

Bits	Symbol	R/W	Function	Default
7	--	R/W	Reserved	--
6	LDOD7ECO	R/W	LDOD7 ECO mode switch enable 0: LDOD7 does not switch 1: LDOD7 switches to ECO mode automatically in sleep	0
5	LDOD6ECO	R/W	LDOD6 ECO mode switch enable 0: LDOD6 does not switch 1: LDOD6 switches to ECO mode automatically in sleep	0
4	LDOD5ECO	R/W	LDOD5 ECO mode switch enable 0: LDOD5 does not switch 1: LDOD5 switches to ECO mode automatically in sleep	0
3	LDOD4ECO	R/W	LDOD4 ECO mode switch enable 0: LDOD4 does not switch 1: LDOD4 switches to ECO mode automatically in sleep	0
2	LDOD3ECO	R/W	LDOD3 ECO mode switch enable 0: LDOD3 does not switch 1: LDOD3 switches to ECO mode automatically in sleep	0
1	LDOD2ECO	R/W	LDOD2 ECO mode switch enable 0: LDOD2 does not switch 1: LDOD2 switches to ECO mode automatically in sleep	0
0	LDOD1ECO	R/W	LDOD1 ECO mode switch enable 0: LDOD1 does not switch 1: LDOD1 switches to ECO mode automatically in sleep	0

12.2.3.5 LDODECO2: LDOD9-11 ECO Mode Control Register

Address: 0x17

Bits	Symbol	R/W	Function	Default

7: 3	--	RW	Reserved	--
2	LDOD11ECO	R/W	LDOD11 ECO mode switch enable 0: LDOD11 does not switch 1: LDOD11 switches to ECO mode automatically in sleep	0
1	--	--	Reserved	--
0	LDOD9ECO	R/W	LDOD9 ECO mode switch enable 0: LDOD9 does not switch 1: LDOD9 switches to ECO mode automatically in sleep	0

12.2.3.6 LDODOVSEL: LDOD Output Voltage Select Register

Address: 0x18

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:2	LDOD2OV	R/W	LDOD2 output voltage select 00: 1.8V 01: 2.85V 10: 3V 11: reserved	00
1:0	LDOD1OV	R/W	LDOD1 output voltage select 00: 1.8V 01: 2.85 10: 3V 11: reserved	01

12.2.3.7 LDOD3OVS: LDOD3 Output Voltage Setting Register

Address: 0x19

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	LDOD3OV	R/W	LDOD3 output voltage setting: 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V	1010 (2.85V)

			1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	

12.2.3.8 LDOD45ENOVS: LDOD4 and LDOD5 Enable and Output Voltage Setting Register

Address: 0x1A

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6:3	LDOD5OV	R/W	LDOD5 output voltage setting 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	0
2	LDOD5EN	R/W	LDOD5 enable 0: disable 1: enable	0
1	LDOD4OV	R/W	LDOD4 output voltage setting: 0: 1.8V 1: 3.0V	0
0	LDOD4EN	R/W	LDOD4 enable 0: disable 1: enable	0

12.2.3.9 LDOD7OVS: LDOD7 Output Voltage Setting Register

Address: 0x1B

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	LDOD7OV	R/W	LDOD7 output voltage setting 0000: 1.8V 0001: 1.9V 0010: 2.0V	1100 (3.0V)

			0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	

12.2.3.10 LDOD8OVS: LDOD8 Output Voltage Setting Register

Address: 0x1C

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	LDOD8OV	R/W	LDOD8 output voltage setting 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	1100 (3.0V)

12.2.3.11 LDOD9OVS: LDOD9 Output Voltage Setting Register

Address: 0x1D

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3:0	LDOD9OV	R/W	LDOD9 output voltage setting: 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V	0000 (1.8V)

			0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	

12.2.3.12 LDOD10OVS: LDOD10 Output Voltage Setting Register

Address: 0x1E

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	LDOD10OV	R/W	LDOD10 output voltage setting 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.85V 1011: 2.9V 1100: 3.0V 1101,1110,1111: reserved	0 (1.8V)

12.2.3.13 LDOD11OVS: LDOD11 Output Voltage Setting Register

Address: 0x1F

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	LDOD11OV	R/W	LDOD11 output voltage setting: 0000: 1.1V 0001: 1.15V 0010: 1.2V 0011: 1.25V 0100: 1.3V 0101: 1.35V 0110: 1.4V	1000 (1.5V)

			0111: 1.45V 1000: 1.5V others: reserved	

12.2.4 DCDC and LDOs OCP control

12.2.4.1 DCOCPEN: DCDC Overcurrent Protection Enable Register

Address: 0x20

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3	DC4OCPEN	R/W	DCDC4 overcurrent protection enable 0: disable 1: enable	1
2	DC3OCPEN	R/W	DCDC3 overcurrent protection enable 0: disable 1: enable	1
1	DC2OCPEN	R/W	DCDC2 overcurrent protection enable 0: disable 1: enable	1
0	DC1OCPEN	R/W	DCDC1 overcurrent protection enable 0: disable 1: enable	1

12.2.4.2 LDOAOCPEN: LDOA2-9 Over-current Protection Enable Register

Address: 0x21

Bits	Symbol	R/W	Function	Default
7	LDOA8OCPEN	R/W	LDOA8 over current protection enable 0: disable 1: enable	1
6	LDOA7OCPEN	R/W	LDOA7 over current protection enable 0: disable 1: enable	1
5	LDOA6OCPEN	R/W	LDOA6 over current protection enable 0: disable 1: enable	1
4	LDOA5OCPEN	R/W	LDOA5 over current protection enable 0: disable 1: enable	1
3	LDOA4OCPEN	R/W	LDOA4 over current protection enable 0: disable 1: enable	1

2	LDOA3OCPEN	R/W	LDOA3 over current protection enable 0: disable 1: enable	1
1	LDOA2OCPEN	R/W	LDOA2 over current protection enable 0: disable 1: enable	1
0	LDOA9OCPEN	R/W	LDOA9 over current protection enable 0: disable 1: enable	1

12.2.4.3 LDODOCPEN1: LDOD1-8 Over-Current Protection Enable Register

Address: 0x22

Bits	Symbol	R/W	Function	Default
7	LDOD8OCPEN	R/W	LDOD8 over current protection enable 0: disable 1: enable	1
6	LDOD7OCPEN	R/W	LDOD7 over current protection enable 0: disable 1: enable	1
5	LDOD6OCPEN	R/W	LDOD6 over current protection enable 0: disable 1: enable	1
4	LDOD5OCPEN	R/W	LDOD5 over current protection enable 0: disable 1: enable	1
3	LDOD4OCPEN	R/W	LDOD4 over current protection enable 0: disable 1: enable	1
2	LDOD3OCPEN	R/W	LDOD3 over current protection enable 0: disable 1: enable	1
1	LDOD2OCPEN	R/W	LDOD2 over current protection enable 0: disable 1: enable	1
0	LDOD1OCPEN	R/W	LDOD1 over current protection enable 0: disable 1: enable	1

12.2.4.4 LDODOCPEN2: LDOD9-11 Over-Current Protection Enable Register

Address: 0x23

Bits	Symbol	R/W	Function	Default
7:3	--	--	Reserved	--

2	LDOD11OCPEN	R/W	LDOD11 over current protection enable 0: disable 1: enable	1
1	LDOD10OCPEN	R/W	LDOD10 over current protection enable 0: disable 1: enable	1
0	LDOD9OCPEN	R/W	LDOD9 over current enable 0: disable 1: enable	1

12.2.5 Sleep mode

12.2.5.1 DC_SLEEP_MODE: DCDC Sleep Mode Register

Address: 0x24

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3	DC4_ALLOW_IN_SLP	R/W	Whether DCDC4 output is allowed in sleep 0: DCDC4 is disabled in sleep 1: DCDC4 output is allowed in sleep and keeps its previous state	1
2	DC3_ALLOW_IN_SLP	R/W	Whether DCDC3 output is allowed in sleep 0: DCDC3 is disabled in sleep 1: DCDC3 output is allowed in sleep and keeps its previous state	1
1	DC2_ALLOW_IN_SLP	R/W	Whether DCDC2 output is allowed in sleep 0: DCDC2 is disabled in sleep 1: DCDC2 output is allowed in sleep and keeps its previous state	1
0	DC1_ALLOW_IN_SLP	R/W	Whether DCDC1 output is allowed in sleep 0: DCDC1 is disabled in sleep 1: DCDC1 output is allowed in sleep and keeps its previous state	1

12.2.5.2 LDOA_SLEEP_MODE: LDOA2-9 Sleep Mode Setting Register

Address: 0x25

Bits	Symbol	R/W	Function	Default
7	LDOA8_ALLOW_IN_SLP	R/W	Whether LDOA8 output is allowed in sleep 0: LDOA8 is disabled in sleep 1: LDOA8 output is allowed in sleep and keeps its previous state	1
6	LDOA7_ALLOW_IN_SLP	R/W	Whether LDOA7 output is allowed in sleep 0: LDOA7 is disabled in sleep	1

			1: LDOA7 output is allowed in sleep and keeps its previous state	
5	LDOA6_ALLOW_IN_SLP	R/W	Whether LDOA6 output is allowed in sleep 0: LDOA6 is disabled in sleep 1: LDOA6 output is allowed in sleep and keeps its previous state	1
4	LDOA5_ALLOW_IN_SLP	R/W	Whether LDOA5 output is allowed in sleep 0: LDOA5 is disabled in sleep 1: LDOA5 output is allowed in sleep and keeps its previous state	1
3	LDOA4_ALLOW_IN_SLP	R/W	Whether LDOA4 output is allowed in sleep 0: LDOA4 is disabled in sleep 1: LDOA4 output is allowed in sleep and keeps its previous state	1
2	LDOA3_ALLOW_IN_SLP	R/W	Whether LDOA3 output is allowed in sleep 0: LDOA3 is disabled in sleep 1: LDOA3 output is allowed in sleep and keeps its previous state	1
1	LDOA2_ALLOW_IN_SLP	R/W	Whether LDOA2 output is allowed in sleep 0: LDOA2 is disabled in sleep 1: LDOA2 output is allowed in sleep and keeps its previous state	1
0	LDOA9_ALLOW_IN_SLP	R/W	Whether LDOA9 output is allowed in sleep 0: LDOA9 is disabled in sleep 1: LDOA9 output is allowed in sleep and keeps its previous state	1

12.2.5.3 LDOD_SLEEP_MODE1: LDOD1-8 Sleep Mode Register

Address: 0x26

Bits	Symbol	R/W	Function	Default
7	LDOD8_ALLOW_IN_SLP	R/W	Whether LDOD8 output is allowed in sleep 0: LDOD8 is disabled in sleep 1: LDOD8 output is allowed in sleep and keeps its previous state	1
6	LDOD7_ALLOW_IN_SLP	R/W	Whether LDOD7 output is allowed in sleep 0: LDOD8 is disabled in sleep 1: LDOD8 output is allowed in sleep and keeps its previous state	1
5	LDOD6_ALLOW_IN_SLP	R/W	Whether LDOD6 output is allowed in sleep 0: LDOD6 is disabled in sleep 1: LDOD6 output is allowed in sleep and keeps its previous state	1
4	LDOD5_ALLOW_I	R/W	Whether LDOD5 output is allowed in sleep	1

	N_SLP		0: LDOD5 is disabled in sleep 1: LDOD5 output is allowed in sleep and keeps its previous state	
3	LDOD4_ALLOW_IN_SLP	R/W	Whether LDOD4 output is allowed in sleep 0: LDOD4 is disabled in sleep 1: LDOD4 output is allowed in sleep and keeps its previous state	1
2	LDOD3_ALLOW_IN_SLP	R/W	Whether LDOD3 output is allowed in sleep 0: LDOD3 is disabled in sleep 1: LDOD3 output is allowed in sleep and keeps its previous state	1
1	LDOD2_ALLOW_IN_SLP	R/W	Whether LDOD2 output is allowed in sleep 0: LDOD2 is disabled in sleep 1: LDOD2 output is allowed in sleep and keeps its previous state	1
0	LDOD1_ALLOW_IN_SLP	R/W	Whether LDOD1 output is allowed in sleep 0: LDOD1 is disabled in sleep 1: LDOD1 output is allowed in sleep and keeps its previous state	1

12.2.5.4 LDOD_SLEEP_MODE2: LDOD9-11 Sleep Mode Register

Address: 0x27

Bits	Symbol	R/W	Function	Default
7: 3	--	--	~~保留~~ reserved	--
2	LDOD11_ALLOW_IN_SLP	R/W	Whether LDOD11 output is allowed in sleep 0: LDOD11 is disabled in sleep 1: LDOD11 output is allowed in sleep and keeps its previous state	1
1	LDOD10_ALLOW_IN_SLP	R/W	Whether LDOD10 output is allowed in sleep 0: LDOD10 is disabled in sleep 1: LDOD10 output is allowed in sleep and keeps its previous state	1
0	LDOD9_ALLOW_IN_SLP	R/W	Whether LDOD9 output is allowed in sleep 0: LDOD9 is disabled in sleep 1: LDOD9 output is allowed in sleep and keeps its previous state	1

12.2.6 LED Current Sinks

12.2.6.1 SINKCR: Current Sinks Control Register

Address: 0x28

Bits	Symbol	R/W	Function	Default
7: 4	—	—	~~保留~~ reserved	—

3	LCDPWMEN	RW	Current sink for LCD backlight PWM enable control: 0: disable 1: enable	0
2	VIBRATOREN	R/W	Current sink for vibrator enable control 0: disable 1: enable	0
1	LCDEN	R/W	Current sink for LCD backlight enable control 0: disable 1: enable	0
0	KEYEN	R/W	Current sink for keyboard backlight enable control 0: disable 1: enable	0

12.2.6.2 LEDIOUT: LED Driver Output Current Setting Register

Address: 0x29

Bits	Symbol	R/W	Function	Default
7: 4	LCDIOUT	RW	output current setting of current sink for LCD backlight: 0001: 10mA 0010: 20mA 0100: 30mA 1000: 40mA 1001: 50mA 1010: 60mA 1100: 70mA 1101: 80mA 1110: 90mA 1111: 100mA others: reserved	0001
3: 0	KEYIOUT	R/W	output current setting of current sink for keyboard backlight: 0001: 10mA 0010: 20mA 0100: 30mA 1000: 40mA 1001: 50mA 1010: 60mA 1100: 70mA 1101: 80mA 1110: 90mA 1111: 100mA others: reserved	0001

12.2.6.3 VIBIOUT: Vibrator driver Output Current Setting Register

Address: 0x2A

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	VIBIOUT	RW	output current setting of current sink for vibrator: 0001: 10mA 0010: 20mA 0100: 30mA 1000 : 40mA 1001 : 50mA 1010 : 60mA 1100 : 70mA 1101 : 80mA 1110: 90mA 1111: 100mA others: reserved	0001

12.2.6.4 INDDIM: LCD current sink Dimming Register

Address: 0x2C

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3:2	DIMEN	R/W	Current sink for LCD backlight function selection: 00: used for LCD backlight 01: used as indicator light 10: used for charging status 11: reserved	10
1: 0	FDIM	R/W	Dimming frequency of indicator light 00: 2Hz 01: 4Hz 10: 8Hz 11: 16Hz	00

12.2.7 Reference current

12.2.7.1 IREF: Reference current setting register

Address: 0x2D

Bits	Symbol	R/W	Function	Default
7:2	--	--	Reserved	0
1:0	SPEED	RW	Backup battery voltage selection : 00: 0.5uA 01: 0.75uA	10

			10: 1uA 11: 1.25uA	

12.2.8 Battery charger

12.2.8.1 CHGFILTER: Charging Filter Time Register

Address: 0x2F

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	0
6:4	EOC_TIME	RW	End of charge filter time 000: 250ms 001: 1min 010: 5mins 011: 10mins 100: 15mins 101: 20mins 110: 25mins 111: 30mins	000
3	--	--	Reserved	--
2:0	RCHG_TIME	RW	Recharge filter time 000 : 250ms 001 : 1min 010 : 2mins 011 : 3mins 100 : 4mins 101 : 5mins 110 : 6mins 111 : 7mins	000

12.2.8.2 CHGCR: Charging Control Register

Address: 0x30

Bits	Symbol	R/W	Function	Default
7	FORCEOCEN	R/W	Forced charging end enable 0: EOC is controlled automatically by hardware 1: EOC is controlled automatically by FORCEOC bit	0
6	FORCEOC	R/W	Forced charging end 0: EOC is forced low by software 1: EOC is forced high by software	0
5	EOCEN	R/W	Charging automatic end function enable 0: disable 1: enable	0
4	NTCEN	R/W	Battery temperature detection enable 0: disable	0

			1: enable	
3	CHGPROT	R/W	charger automatic protection enable: 0: disable 1: enable	1
2	CSENSE	R/W	End of charge current sense source control 0：VBAT current is the csens 1：VSYS current is the csens	1
1	BATSEL	R/W	battery type select: 0: Li-ion battery 1: Ni-H battery	0
0	ACHGON	R/W	Adapter/USB charging enable 0: disable 1: enable	1

12.2.8.3 CHGVSET: Charging Voltage Setting Register

Address: 0x31

Bits	Symbol	R/W	Function	Default
7	—	—	Reserved	—
6:5	CVADJ	R/W	CV voltage adjustment 00: 0V 01: +25mV 10: +50mV 11:+75mV	00
4	CVSEL	R/W	CV charging voltage select: 0: 4.2V 1: 4.35V	0
3	VHYSSEL	R/W	EOCCMP and RECCMP hys voltage seletion 0：50mV 1：70mV~90mV	0
2:0	RCHGSEL	R/W	Setting recharge voltage 111: reserved 110: CV-350mV 101: CV-300mV 100: CV-250mV 011: CV-200mV 010: CV-150mV 001: CV-100mV 000: CV-50mV	010

12.2.8.4 CHGCSET: Charging Current Setting Register

Address: 0x32

Bits	Symbol	R/W	Function	Default

7: 6	--	-	Reserved	--
5: 4	CCPC	R/W	Setting end-of-charge current: 00: 50mA 01: 100mA 10: 150mA 11: 200mA	00
3: 0	ACCSEL	R/W	Setting Adapter/USB CC current: 0000: 100mA 0001: 200mA 0010: 300mA 0011: 400mA 0100: 500mA 0101: 600mA 0110: 700mA 0111: 800mA 1000: 900mA 1001: 1000mA 1010: 1100mA 1011: 1200mA others: reserved	0011

12.2.8.5 CHGTSET: Charging Timer Setting Register

Address: 0x33

Bits	Symbol	R/W	Function	Default
7	—	—	Reserved	—
6: 4	RTIM	R/W	Setting charging timer 000: 3 hours 001: 4 hours 010: 5 hours 011: 6 hours 100: 7 hours 101: 8 hours others: reserved	101
3	RTIMCLRB	W	Clearing charging timer 0: clear charging timer 1: operate charging timer	1
2: 1	—	—	Reserved	—
0	RTIMSTP	R/W	Stopping Charging timer 0: operate charging timer 1: stop charging timer	0

12.2.8.6 CHGSTATUS: Charging Status Register

Address: 0x34

Bits	Symbol	R/W	Function	Default
7	RTIMOV	R	Charging timeout status: 0: normal 1: timeout	0
6	--	--	Reserved	--
5	ADPUV	R	Adapter under voltage 0: inactive 1: active	--
4	ADPOV	R	Adapter/USB over voltage 0: inactive 1: active	0
3	BATOT	R	Battery temperature abnomal (hot or cold) 0: inactive 1: active	0
2	RECSTATUS	R	recharging status 0: initial charging or not charging 1: recharging	0
1	CHGSHDN	R	charging abnomal status 0: charging abnomal 1: charging normal	1
0	CHGCP	R	Charging completion 0: inactive 1: active	0

12.2.9 Power status and control

12.2.9.1 PCST: Power-related Status Register

Address: 0x35

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	HFPWR	R	HF_PWR pin status: 0: HF_PWR low 1: HF_PWR high	0
5	KONMON	R	KEYON pin status 0: KEYON is released 1: KEYON is pressed	0
4	BATV45	R	Battery voltage over 4.5V detection 0: VBAT<4.5V（battery normal） 1: VBAT≥4.5V（battery overvoltage）	0
3	VBATV32	R	Battery voltage over 3.2V detection 1: VBAT>3.2V 0: VBAT≤3.2V	1

2	VBATV33	R	Battery voltage over UVTH detection 0: VBAT<UVTH 1: VBAT≥UVTH	1
1	BATOUT	R	Battery present/removal status 0: battery is present 1: battery is removed	0
0	ADPIN	R	Adapter/USB plugged status: 0: unplugged 1: plugged	0

12.2.9.2 STARTUP_STATUS: Start-up Status Register

Address: 0x36

Bits	Symbol	R/W	Function	Default
7: 6	--	--	Reserved	--
5	RSTINB_STARTUP	R	Startup event: 1: Startup is caused by RSTINB	0
4	ALARM2_STARTUP	R	Startup event: 1: startup is caused by RTC alarm2	0
3	ALARM1_STARTUP	R	Startup event: 1: startup is caused by RTC alarm1	0
2	ADPIN_STARTUP	R	Startup event: 1: startup is caused by charger input connection	0
1	HF_PWR_STARTUP	R	Startup event: 1: startup is caused by HF_PWR	0
0	KEYON_STARTUP	R	Startup event: 1: startup is caused by KEYON button	0

12.2.9.3 SHDN_STATUS: Shut-down Status Register

Address: 0x37

Bits	Symbol	R/W	Function	Default
7: 6	--	--	Reserved	--
5	RSTINB_SHDN	R	Shutdown event: 1: Shutdown is caused by RSTINB	0
4	KEYON_SHDN	R	Shutdown event: 1: Shutdown is caused by pressing KEYON for 10s	0
3	--	--	Reserved	--
2	BATUV_SHDN	R	Shutdown event: 1: Shutdown is caused by battery voltage under 2.9V	0
1	TSD_SHDN	R	Shutdown event: 1: Shutdown is caused by high temperature of the chip	0
0	PWREN_SHDN	R	Shutdown event:	0

			1: Shutdown is caused by PWREN pulled low	

12.2.9.4 SHDN_EN: Shutdown Enable Register

Address: 0x2E

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	RSTINB_SHDN_EN	R/W	Shutdown by RSTINB enable 0: disable 1: enable	1
5	KEYON_SHDN_TIME	R/W	Debounce time of KEYON in order to shutdown 0: 10s 1:20s	0
4	KEYON_SHDN_EN	R/W	Shutdown by KEYON enable: 0: disable 1: enable	1
3	--	--	Reserved	--
2	BATUV_SHDN_EN	R/W	Shutdown by BATUV enable: 0: disable 1: enable	1
1	TSD_SHDN_EN	R/W	Shutdown by TSD enable: 0: disable 1: enable	1
0	PWREN_SHDN_EN	R/W	Shutdown by PWREN enable: 0: disable 1: enable	1

12.2.9.5 BATUVCR: Battery Undervoltage Interrupt Control Register

Address: 0x3F

Bits	Symbol	R/W	Function	Default
7: 5	--	--	--	--
4	TRMOD	R/W	**Transmission mode enable** 0: normal mode 1: transmission mode: used for high power transmission to avoid false battery undervoltage interrupt due to momentary voltage drop.	1'b0
3: 2	--	--	**Reserved**	--
1: 0	BATUV_TH	R/W	Threshold voltage setting for battery undervoltage interrupt 00: 3.4V 01: 3.6V 10: 3.65V 11: 3.7V	00

12.2.10 ADC

12.2.10.1 ADCLDOEN: LDO for ADC Enable Register

Address: 0x38

Bits	Symbol	R/W	Function	Default
7: 6	—	—	Reserved	—
0	LDOADCEN	R/W	LDO for ADC enable: 0: disable 1: enable	0

12.2.10.2 ADCCR: A/D Converter Control Register

Address: 0x39

Bits	Symbol	R/W	Function	Default
7: 5	—	—	Reserved	—
4	ADMODE	R/W	Setting conversion mode 0: single conversion mode 1: continuous conversion mode	0
3	—	—	Reserved	—
2: 0	ADSEL	R/W	Selecting ADC channel 000: battery voltage 001: battery temperature 010: ADCIN2~~1~~ 011: ADCIN3~~2~~ 100: ADCIN4~~3~~ others: reserved	00

12.2.10.3 ADCCMD: A/D Converter Command Register

Address: 0x3A

Bits	Symbol	R/W	Function	Default
7: 5	—	—	Reserved	—
4	ADEND	R	End of conversion 1: AD conversion is completed. This bit is cleared by reading the conversion data.	0
3: 1	—	—	Reserved	—
0	ADSTART	W	Start of AD conversion command 1: Start AD conversion This bit is automatically cleared after conversion starts.	0

12.2.10.4 ADCEN: ADC Enable Register

Address: 0x3B

Bits	Symbol	R/W	Function	Default
7: 6	—	—	Reserved	—
0	ADCEN	R/W	ADC enable 0: ADC is disabled and goes into low power state 1: ADC is enabled and operates normally	0

12.2.10.5 ADCDAT0: 4 LSBs of A/D Conversion Data Register

Address: 0x3C

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3: 0	ADDATL	R	4 LSBs of AD conversion data	0

12.2.10.6 ADCDAT1: 8 MSBs of A/D Conversion Data Register

Address: 0x3D

Bits	Symbol	R/W	Function	Default
7: 0	ADDATH	R	8 MSBs of AD conversion data	—

12.2.10.7 ADCFORMAT: A/D Conversion Data Format Register

Address: 0x3E

Bits	Symbol	R/W	Function	Default
7: 1	--	--	Reserved	--
0	ADFORMAT	R/W	format of AD conversion data 0: 12-bit 1: 10-bit	0

12.2.11RTC

12.2.11.1 RTC_SEC: RTC Second Counter Register

Read this register to get current value of second counter. Write this register to set second counter.

Address: 0x60

Bits	Symbol	R/W	Function	Default
7: 6	--	--	Reseved	--
5:0	SEC	RW	Second counter value （0—59）	0

12.2.11.2 RTC_MIN: RTC Minute Counter Register

Read this register to get current value of minute counter. Write this register to set minute counter.

Address: 0x61

Bits	Symbol	R/W	Function	Default

7: 6	--	--	Reserved	--
5:0	MIN	RW	Minute counter value（0－59）	0

12.2.11.3 RTC_HOUR: RTC Hour Counter Register

Read this register to get current value of hour counter. Write this register to set hour counter.

Address: 0x62

Bits	Symbol	R/W	Function	Default
7: 5	--	--	Reserved	--
4:0	HOUR	RW	Hour counter value（0－23）	0

12.2.11.4 RTC_DAY: RTC Day of a Month Counter Register

Read this register to get current value of day counter. Write this register to set day counter.

Address: 0x63

Bits	Symbol	R/W	Function	Default
7:5	--	--	Reserved	--
4:0	DAY	RW	Day counter value（0－30，represent 1st to 31st of a month respectively） Note: there are 31 days in Jan, Mar, May, July, Aug, Oct and Dec； there are 30 days in Apr, June and Nov there are 29 days in Feb in leap year and 28 days in normal year	0x0

12.2.11.5 RTC_WEEK: RTC Current Day of a Week Counter Register

Read this register to get current value of week counter. Write this register to set week counter

Address: 0x64

Bits	Symbol	R/W	Function	Default
7: 3	--	--	Reserved	--
2:0	WEEK	RW	Current week counter value: 000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday	0

12.2.11.6 RTC_MONTH: RTC Month Counter Register

Read this register to get current value of month counter. Write this register to set month counter

Address: 0x65

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3:0	MONTH	RW	Current month counter value（0－11 represents Jan to Dec）	0x0

12.2.11.7 RTC_YEAR: RTC Year Counter Register

Address: 0x66

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6:0	YEAR	RW	Current year counter value（0－99） Note: 7'd0-7'd99 represents 1980 to 2079 or 2000 to 2099	0x0

12.2.11.8 RTC_TIME_UPDATE: RTC Time Update Enable Register

Address: 0x67

Bits	Symbol	R/W	Function	Default
7: 0	TIME_UPDATE	W	Time and date settings are updated to 32K clock domain only when specified value (0x1a) is written to this register	--

12.2.11.9 RTC_32K_ADJL: 8 LSBS of RTC Clock Adjust Register

Address: 0x68

Bits	Symbol	R/W	Function	Default
7:0	ADJL	RW	8 LSBs of adjust value for 32KHz clock	0x00

12.2.11.10 RTC_32K_ADJH: 8 MSBS of RTC Clock Adjust Register

Address: 0x69

Bits	Symbol	R/W	Function	Default
7: 4	--	--	Reserved	--
3:0	ADJH	RW	4 MSBs of adjust value for 32KHz clock	0x0

12.2.11.11 RTC_SEC_CYCL: 8 LSBS of RTC Second Cycle Limit Register

Address: 0x6A

Bits	Symbol	R/W	Function	Default

7:0	CYCL	RW	CYCL refers to the LSB of 32KHz clock cycles required by counting one second. For example，when 32KHz clock frequency is 32768HZ, 32768 clock cycles are required to count one second. When counter lcock frequency is not equal to 32768Hz, CYC value can be set as the frequency of actual clock. Moreover, setting CYC as a smaller value during debugging can reduce the wating time. 0x0000: 1 second means 1 clk32k clock cycles… 0x7fff: 1 second means 32768 clk32k clock cycles	0xff

12.2.11.12 RTC_SEC_CYCH: 8 MSBS of RTC Second Cycle Limit Register

Address: 0x6B

Bits	Symbol	R/W	Function	Default
7:0	CYCH	RW	CYCH refers to the MSB of 32KHz clock cycles required by counting one second. For example，when 32KHz clock frequency is 32768HZ, 32768 clock cycles are required to count one second. When counter lcock frequency is not equal to 32768Hz, CYC value can be set as the frequency of actual clock. Moreover, setting CYC as a smaller value during debugging can reduce the wating time. 0x0000: 1 second means 1 clk32k clock cycles… 0x7fff: 1 second means 32768 clk32k clock cycles	0x7F

12.2.11.13 RTC_CALIB_UPDATE: RTC Clock Calibration Update Register

Address: 0x6C

Bits	Symbol	R/W	Function	Default
7:0	CALIB_UPDATE	W	Calibration settings are updated to 32K clock domain only when specified value（0x2a）is written to this register.	--

12.2.11.14 RTC_AL1_SEC: Second Setting for Alarm Interrupt 1

Address: 0x6D

Bits	Symbol	R/W	Function	Default
7:6	--	--	Reseved	--
5:0	AL1_SEC	RW	Setting second couter value for alarm interrupt1	0x0

12.2.11.15 RTC_AL1_MIN: Minute Setting for Alarm Interrupt 1

Address: 0x6E

Bits	Symbol	R/W	Function	Default

7:6	--	--	Reserved	--
5:0	AL1_MIN	RW	Setting minute counter value for alarm interrupt1	0x0

12.2.11.16 RTC_AL1_HOUR: Hour Setting for Alarm Interrupt 1

Address: 0x7C

Bits	Symbol	R/W	Function	Default
7:5	--	--	Reseved	--
4:0	AL1_HOUR	RW	Setting hour counter value for alarm interrupt1	0x0

12.2.11.17 RTC_AL1_DAY: Day Setting for Alarm Interrupt 1

Address: 0x7D

Bits	Symbol	R/W	Function	Default
7:5	--	--	Reseved	--
4:0	AL1_DAY	RW	Setting day counter value for alarm interrupt1	0x0

12.2.11.18 RTC_AL1_MONTH: Month Setting for Alarm Interrupt 1

Address: 0x7E

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reseved	--
3:0	AL1_MONTH	RW	Setting month counter value for alarm interrupt1	0x0

12.2.11.19 RTC_AL1_YEAR: Year Setting for Alarm Interrupt 1

Address: 0x7F

Bits	Symbol	R/W	Function	Default
7	--	--	**Reseved**	--
6:0	AL1_YEAR	RW	Setting year counter value for alarm interrupt1	0x0

12.2.11.20 RTC_AL2_SEC: Second Setting for Alarm Interrupt 2

Address: 0x6F

Bits	Symbol	R/W	Function	Default
7:6	--	--	**Reseved**	--
5:0	AL2_SEC	RW	**Setting second couter value for alarm interrupt2**	0x0

12.2.11.21 RTC_AL2_MIN: Minute Setting for Alarm Interrupt 2

Address: 0x70

Bits	Symbol	R/W	Function	Default
7:6	--	--	**Reseved**	--
5:0	AL2_MIN	RW	Setting minute counter value for alarm interrupt2	0x0

12.2.11.22 RTC_AL2_HOUR: Hour Setting for Alarm Interrupt 2

Address: 0x71

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reseved**	--
4:0	AL2_HOUR	RW	Setting hour counter value for alarm interrupt2	0x0

12.2.11.23 RTC_AL2_DAY: Day Setting for Alarm Interrupt 2

Address: 0x72

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reseved**	--
4:0	AL2_DAY	RW	Setting day counter value for alarm interrupt2	0x0

12.2.11.24 RTC_AL2_MONTH: Month Setting for Alarm Interrupt 2

Address: 0x73

Bits	Symbol	R/W	Function	Default
7:4	--	--	**Reseved**	--
3:0	AL2_MONTH	RW	Setting month counter value for alarm interrupt2	0x0

12.2.11.25 RTC_AL2_YEAR: Year Setting for Alarm Interrupt 2

Address: 0x74

Bits	Symbol	R/W	Function	Default
7	--	--	**Reseved**	--
6:0	AL2_YEAR	RW	Setting year counter value for alarm interrupt2	0x0

12.2.11.26 RTC_AL_UPDATE: RTC Alarm Time Update Register

Address: 0x75

Bits	Symbol	R/W	Function	Default
7: 0	AL_UPDATE	W	Alarm interrupts time settings are updated to 32K clock domain only when specified value(0x3a) is written into this register	--

12.2.11.27 RTC_INT_EN: RTC Interrupt Enable Register

Address: 0x76

Bits	Symbol	R/W	Function	Default
7:6	--	--	Reseved	--
5	AL1_EN	RW	Alarm interrupt 1 enable	0x0

			0: diable 1: enable	
4	AL2_EN	RW	Alarm interrupt 2 enable 0: disable 1: enable	0x0
3	SEC_EN	RW	Second interrupt enable: set whether to enable second interrupt 0: disable 1: enable	0x0
2	MIN_EN	RW	Minute interrupt enable: set whether to enable minute interrupt 0: disable 1: enable	0
1	HOUR_EN	RW	Hour interrupt enable: set whether to enable hour interrupt 0: diable 1: enable	0
0	DAY_EN	RW	Day interrupt enable: Set whether to enable day interrupt 0: disable 1: enable	0

12.2.11.28 RTC_INT_STATUS: RTC Interrupt Status Register

Address: 0x77

Bits	Symbol	R/W	Function	Default
7:6	--	--	Reseved	--
5	AL1IS	RW	Interrupt status: this bit is enabled raw status of alarm interrupt 1 and can be cleared by writing 1. 0: interrupt is inactive 1: interrupt is active	0x0
4	AL2IS	RW	Interrupt status: this bit is enabled raw status of alarm interrupt 2 and can be cleared by writing 1. 0: interrupt is inactive 1: interrupt is active	
3	SECIS	RW	Interrupt status: this bit is enabled raw status of second interrupt and can be cleared by writing 1. 0: interrupt is inactive 1: interrupt is active	0
2	MINIS	RW	Interrupt status: this bit is enabled raw status of minute interrupt and can be cleared by writing 1. 0: interrupt is inactive 1: interrupt is active	
1	HOURIS	RW	Interrupt status: this bit is enabled raw status of hour interrupt and can be cleared by writing 1.	0x0

			0: interrupt is inactive 1: interrupt is active	
0	DAYIS	RW	Interrupt status: this bit is enabled raw status of day interrupt and can be cleared by writing 1. 0: interrupt is inactive 1: interrupt is active	0x0

12.2.11.29 RTC_INT_RAW: RTC Raw Interrupt Status Register

Address: 0x78

Bits	Symbol	R/W	Function	Default
7:6	--	--	Reseved	--
5	AL1_RAW	R	Interrupt status: this bit is raw status of alarm interrupt 1 0: interrupt is inactive 1: interrupt is active	0x0
4	AL2_RAW	R	Interrupt status: this bit is raw status of alarm interrupt 2 0: interrupt is inactive 1: interrupt is active	
3	SEC_RAW	R	Interrupt status: this bit is raw status of second interrupt 0: interrupt is inactive 1: interrupt is active	0
2	MIN_RAW	R	Interrupt status: this bit is raw status of minute interrupt 0: interrupt is inactive 1: interrupt is active	0
1	HOUR_RAW	R	Interrupt status: this bit is raw status of hour interrupt 0: interrupt is inactive 1: interrupt is active	0x0
0	DAY_RAW	R	Interrupt status: this bit is raw status of day interrupt 0: interrupt is inactive 1: interrupt is active	0x0

12.2.11.30 RTC_CTRL: RTC Control Register

Address: 0x79

Bits	Symbol	R/W	Function	Default
7:5	--	--	Reseved	--
3:2	BAKBAT_VSEL	RW	Backup battery voltage selection : 00: 3.0V 01: 2.8V 10: 2.6V 11: 3.2V	0
1	RTC_RESET_FLAG	RW	RTC reset flag: 0: RTC is not reset since this bit is cleared 1: RTC has been reset	0x1

0	CNT_EN	RW	Counter enable: Control whether to enable counter 0: counter disabled 1: counter enabled	0x1

12.2.11.31 RTC_BK: RTC Backup Register

Address: 0x7A

Bits	Symbol	R/W	Function	Default
7:0	DATA	RW	**backup register**	0x0

12.2.11.32 RTC_MASK: RTC Interrupt Mask Register

Address: 0x7B

Bits	Symbol	R/W	Function	Default
7:0	INT_MASK	RW	**interrupts mask:** 0: interrupts unmasked 1: interrupts masked	0x0

12.2.12 I2C

12.2.12.1 I2CCR: I2C Interface Control Register

Address: 0x40

Bits	Symbol	R/W	Function	Default
7:2	--	--	**Reserved**	--
1: 0	INCR	R/W	**Address pointer control at continuous read operation:** 00: address pointer automatically increases 01: address pointer is fixed 10: only LSB of address pointer increases 11: reserved	0

12.2.13 Clock

12.2.13.1 CLKCR: Clock Control Register

Address: 0x41

Bits	Symbol	R/W	Function	Default
7:2	--	--	**Reserved**	--
1	CLKDIVEN	R/W	**MCLK~~CLK26M~~ clock division enable:** 0: MCLK~~CLK26M~~ not divided 1: MCLK~~CLK26M~~ divided by 6	0
0	CLKSEL	R/W	**Clock select:** 0: 1.2MHz clock generated by internal oscillator 1: clock input from MCLK~~CLK26M~~ pin	0

12.2.14 Interrupt status

12.2.14.1 IRQST_FINAL: Final Interrupt Status Register

Address: 0x43

Bits	Symbol	R/W	Function	Default
7:5	--	--	**Reserved**	--
4	CODECIRQ	R	**CODEC interrupt status** 0: no interrupt in CODEC 1: at least one interrupt asserted in CODEC	0
3	JKHSIRQ	R	**Jack and hookswitch interrupt status** 0: no interrupt in JKHSIRQST 1: at least one interrupt asserted in JKHSIRQST	0
2	IRQ2	R	**IRQ2 interrupt status** 0: no interrupt in IRQST2 1: at least one interrupt asserted in IRQST2	0
1	IRQ1	R	**IRQ1 interrupt status** 0: no interrupt in IRQST1 1: at least one interrupt asserted in IRQST1	0
0	RTCIRQ	R	**RTC interrupt status** 0: no interrupt in RTC 1: at least one interrupt asserted in RTC	0

12.2.14.2 IRQST1: Interrupt Status Register 1

Address: 0x43

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	CHGOVIR	R/W	Charger overvoltage interrupt status 0: no interrupt 1: interrupt asserted	0
5	CHGUVIR	R/W	Charger undervoltage interrupt status 0: no interrupt 1: interrupt asserted	0
4	RCHGIR	R/W	Charger re-charging interrupt status 0: no interrupt 1: interrupt asserted	0
3	CHGCVIR	R/W	CC to CV transition interrupt status 0: no interrupt 1: interrupt asserted	0
2	BATOVIR	R/W	Battery overvoltage interrupt status 0: no interrupt 1: interrupt asserted	0
1	BATUVIR	R/W	Battery undervoltage interrupt status 0: no interrupt	0

			1: interrupt asserted	
0	BATOTIR	R/W	Battery temperature abnormal interrupt status 0: no interrupt 1: interrupt asserted	0

12.2.14.3 IRQST2: Interrupt Status Register 2

Address: 0x44

Bits	Symbol	R/W	Function	Default
7	TSDIR	R/W	Thermal shutdown interrupt status 0: no interrupt 1: interrupt asserted	0
6	RTIMIR	R/W	Charging timeout interrupt status 0: no interrupt 1: interrupt asserted	0
5	CHGCPIR	R/W	Charging completion interrupt status 0: no interrupt 1: interrupt asserted	0
4	ADCCPIR	R/W	AD conversion completion interrupt status 0: no interrupt 1: interrupt asserted	0
3	KONIR	R/W	KEYON pressed interrupt status 0: no interrupt 1: interrupt asserted	0
2	KOFFIR	R/W	KEYON released interrupt status 0: no interrupt 1: interrupt asserted	0
1	ADPINIR	RW	Adaptor plugged interrupt status 0: no interrupt 1: interrupt asserted	0
0	ADPOUTIR	RW	Adaptor unplugged interrupt status 0: no interrupt 1: interrupt asserted	0

12.2.15 Interrupt enable

12.2.15.1 IRQEN1: Interrupt Enable Register 1

Address: 0x45

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	CHGOVIREN	R/W	Charger overvoltage interrupt enable 0: disable 1: enable	0
5	CHGUVIREN	R/W	Charger undervoltage interrupt enable 0: disable	0

			1: enable	
4	RCHGIREN	R/W	Charger re-charging interrupt enable 0: disable 1: enable	0
3	CHGCVIREN	R/W	CC to CV transition interrupt enable 0: disable 1: enable	0
2	BATOVIREN	R/W	Battery overvoltage interrupt enable 0: disable 1: enable	0
1	BATUVIREN	R/W	Battery undervoltage interrupt enable 0: disable 1: enable	0
0	BATOTIREN	R/W	Battery temperature abnormal interrupt enable 0: disable 1: enable	0

12.2.15.2 IRQEN2: Interrupt Enable Register 2

Address: 0x46

Bits	Symbol	R/W	Function	Default
7	TSDIREN	R/W	Thermal shutdown interrupt enable 0: disable 1: enable	0
6	RTIMIREN	R/W	Charging timeout interrupt enable 0: disable 1: enable	0
5	CHGCPIREN	R/W	Charging completion interrupt enable 0: disable 1: enable	0
4	ADCCPIREN	R/W	AD conversion completion interrupt enable 0: disable 1: enable	0
3	KONIREN	R/W	KEYON pressed interrupt enable 0: disable 1: enable	0
2	KOFFIREN	R/W	KEYON released interrupt enable 0: disable 1: enable	0
1	ADPINIREN	R/W	Adaptor plugged interrupt enable 0: disable 1: enable	0
0	ADPOUTIREN	R/W	Adaptor unplugged interrupt enable 0: disable	0

			1: enable	

12.2.16 Interrupt mask

12.2.16.1 IRQMSK1: Interrupt Mask Register 1

Address: 0x47

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	CHGOVIRMSK	R/W	Charger overvoltage interrupt mask 0: unmask 1: mask	0
5	CHGUVIRMSK	R/W	Charger undervoltage interrupt mask 0: unmask 1: mask	0
4	RCHGIRMSK	R/W	Charger re-charging interrupt mask 0: unmask 1: mask	0
3	CHGCVIRMSK	R/W	CC to CV transition interrupt mask 0: unmask 1: mask	0
2	BATOVIRMSK	R/W	Battery overvoltage interrupt mask 0: unmask 1: mask	0
1	BATUVIRMSK	R/W	Battery undervoltage interrupt mask 0: unmask 1: mask	0
0	BATOTIRMSK	R/W	Battery temperature abnormal interrupt mask 0: unmask 1: mask	0

12.2.16.2 IRQMSK2: Interrupt Mask Register 2

Address: 0x48

Bits	Symbol	R/W	Function	Default
7	TSDIRMSK	R/W	Thermal shutdown interrupt mask 0: unmask 1: mask	0
6	RTIMIRMSK	R/W	Charging timeout interrupt mask 0: unmask 1: mask	0
5	CHGCPIRMSK	R/W	Charging completion interrupt mask 0: unmask 1: mask	0
4	ADCCPIRMSK	R/W	AD conversion completion interrupt mask	0

			0: unmask 1: mask	
3	KONIRMSK	R/W	KEYON pressed interrupt mask 0: unmask 1: mask	0
2	KOFFIRMSK	R/W	KEYON released interrupt mask 0: unmask 1: mask	0
1	ADPINIRMSK	R	Adaptor plugged interrupt mask 0: unmask 1: mask	0
0	ADPOUTIRMSK	R	Adaptor unplugged interrupt mask 0: unmask 1: mask	0

12.2.17 DCDC and LDOs softstart control

12.2.17.1 DCSOFTEN: DCDC Softstart Enable Register

Address: 0x49

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3	DC4SOFTEN	R/W	DCDC4 softstart enable 0: disable 1: enable	1
2	DC3SOFTEN	R/W	DCDC3 softstart enable 0: disable 1: enable	1
1	DC2SOFTEN	R/W	DCDC2 softstart enable 0: disable 1: enable	1
0	DC1SOFTEN	R/W	DCDC1 softstart enable 0: disable 1: enable	1

12.2.17.2 LDOASOFTEN: LDOA2-9 Softstart Enable Register

Address: 0x4A

Bits	Symbol	R/W	Function	Default
7	LDOA9SOFTEN	R/W	LDOA9 softstart enable 0: disable 1: enable	1
6	LDOA8SOFTEN	R/W	LDOA8 softstart enable 0: disable	1

			1: enable	
5	LDOA7SOFTEN	R/W	LDOA7 softstart enable 0: disable 1: enable	1
4	LDOA6SOFTEN	R/W	LDOA6 softstart enable 0: disable 1: enable	1
3	LDOA5SOFTEN	R/W	LDOA5 softstart enable 0: disable 1: enable	1
2	LDOA4SOFTEN	R/W	LDOA4 softstart enable 0: disable 1: enable	1
1	LDOA3SOFTEN	R/W	LDOA3 softstart enable 0: disable 1: enable	1
0	LDOA2SOFTEN	R/W	LDOA2 softstart enable 0: disable 1: enable	1

12.2.17.3 LDODSOFTEN1: LDOD1-8 Softstart Enable Register

Address: 0x4B

Bits	Symbol	R/W	Function	Default
7	LDOD8SOFTEN	R/W	LDOD8 softstart enable 0: disable 1: enable	1
6	LDOD7SOFTEN	R/W	LDOD7 softstart enable 0: disable 1: enable	1
5	LDOD6SOFTEN	R/W	LDOD6 softstart enable 0: disable 1: enable	1
4	LDOD5SOFTEN	R/W	LDOD5 softstart enable 0: disable 1: enable	1
3	LDOD4SOFTEN	R/W	LDOD4 softstart enable 0: disable 1: enable	1
2	LDOD3SOFTEN	R/W	LDOD3 softstart enable 0: disable 1: enable	1
1	LDOD2SOFTEN	R/W	LDOD2 softstart enable 0: disable	1

			1: enable	
0	LDOD1SOFTEN	R/W	LDOD1 softstart enable 0: disable 1: enable	1

12.2.17.4 LDODSOFTEN2: LDOD9-11 Softstart Enable Register

Address: 0x4C

Bits	Symbol	R/W	Function	Default
7:3	--	--	Reserved	--
2	LDOD11SOFTEN	R/W	LDOD11 softstart enable 0: disable 1: enable	1
1	LDOD10SOFTEN	R/W	LDOD10 softstart enable 0: disable 1: enable	1
0	LDOD9SOFTEN	R/W	LDOD9 softstart enable 0: disable 1: enable	1

12.2.18 DCDC and LDOs fast discharge control

12.2.18.1 DCFASTDISC: DCDC Fast Discharge Enable Register

Address: 0x4D

Bits	Symbol	R/W	Function	Default
7:4	--	--	Reserved	--
3	DC4_FST_DISC	R/W	DCDC4 fast discharge enable 0: disable 1: enable	1
2	DC3_FST_DISC	R/W	DCDC3 fast discharge enable 0: disable 1: enable	1
1	DC2_FST_DISC	R/W	DCDC2 fast discharge enable 0: disable 1: enable	1
0	DC1_FST_DISC	R/W	DCDC1 fast discharge enable 0: disable 1: enable	1

12.2.18.2 LDOAFASTDISC: LDOA2-9 Fast Discharge Enable Register

Address: 0x4E

Bits	Symbol	R/W	Function	Default
7	LDOA9SINKEN	R/W	LDOA9 fast discharge enable	1

			0: disable 1: enable	
6	LDOA8SINKEN	R/W	LDOA8 fast discharge enable 0: disable 1: enable	1
5	LDOA7SINKEN	R/W	LDOA7 fast discharge enable 0: disable 1: enable	1
4	LDOA6SINKEN	R/W	LDOA6 fast discharge enable 0: disable 1: enable	1
3	LDOA5SINKEN	R/W	LDOA5 fast discharge enable 0: disable 1: enable	1
2	LDOA4SINKEN	R/W	LDOA4 fast discharge enable 0: disable 1: enable	1
1	LDOA2SINKEN	R/W	LDOA3 fast discharge enable 1: enable 0: disable	1
0	LDOA2SINKEN	R/W	LDOA2 fast discharge enable 0: disable 1: enable	1

12.2.18.3 LDODFASTDISC1: LDOD1-8 Fast Discharge Enable Register

Address: 0x4F

Bits	Symbol	R/W	Function	Default
7	LDOD8SINKEN	R/W	LDOD8 fast discharge enable 0: disable 1: enable	1
6	LDOD7SINKEN	R/W	LDOD7 fast discharge enable 0: disable 1: enable	1
5	LDOD6SINKEN	R/W	LDOD6 fast discharge enable 0: disable 1: enable	1
4	LDOD5SINKEN	R/W	LDOD5 fast discharge enable 0: disable 1: enable	1
3	LDOD4SINKEN	R/W	LDOD4 fast discharge enable 0: disable 1: enable	1
2	LDOD3SINKEN	R/W	LDOD3 fast discharge enable	1

			0: disable 1: enable	
1	LDOD2SINKEN	R/W	LDOD2 fast discharge enable 0: disable 1: enable	1
0	LDOD1SINKEN	R/W	LDOD1 fast discharge enable 0: disable 1: enable	1

12.2.18.4 LDODFASTDISC2: LDOD9-11 Softstart Enable Register

Address: 0x50

Bits	Symbol	R/W	Function	Default
7:3	--	--	Reserved	--
2	LDOD11SINKEN	R/W	LDOD11 fast discharge enable 0: disable 1: enable	1
1	LDOD10SINKEN	R/W	LDOD10 softstart enable 0: disable 1: enable	1
0	LDOD9SINKEN	R/W	LDOD9 softstart enable 0: disable 1: enable	1

12.2.19 Thermal shutdown

12.2.19.1 TSHUT: Thermal Shutdown Control Register

Address: 0x51

Bits	Symbol	R/W	Function	Default
7:1	--	--	**Reserved**	--
0	TSDEN	R/W	**Thermal shutdown protection enable** 0: disable 1: enable	1

12.2.20 PWM module

12.2.20.1 PWM_EN: PWM Enable Register

Address: 0x80

Bits	Symbol	R/W	Function	Default
7:6	--	--	**Reserved**	--
0	PWM_EN	R/W	**PWM enable control bit.** **Controls PWM internal counter and operation status** 0: PWM disabled	0

			1: PWM enabled	

12.2.20.2 PWM_UP: PWM Update Register

Address: 0x81

Bits	Symbol	R/W	Function	Default
7:1	--	--	**Reserved**	--
0	UPDATE	R/W	**PWM parameters update bit.** If writing 1 to this bit, the new value of period and duty cycle configurations are updated when PWM is diabled or a whole PWM wave is output, then this bit will be cleared to 0; it is invalid if writing 0 to this bit.	0

12.2.20.3 PWM_RESET: PWM Reset Register

Address: 0x82

Bits	Symbol	R/W	Function	Default
7:1	--	--	**Reserved**	--
0	RESET	R/W	**PWM module reset.** **Controls PWM reset operation** 0: PWM operates nomally 1: PWM is reset	0

12.2.20.4 PWM_P: PWM Period Setting Register

When the counter value matches PERIOD, the counter will restart another cycle. By the following equation:

PWMO (Hz) = PWMCLK (Hz) / （(PERIOD + 1)*50）

PWM signal frequency can be caculated, where

50: stands for the couting cycle is duty cycle counter, which is fixed to 50

PERIOD: bit 7 to 0 of PWM_P register

PWMCLK: PWM main clock, pwm_mclk， default 1.2MHZ。

PWMO: PWM output frequency

Address: 0x83

Bits	Symbol	R/W	Function	Default
7: 0	PERIOD	R/W	**PERIOD controls the period of period counter.** When period counter value reaches PWRIOD, it will return to 0, and restart counting.	0xFF

12.2.20.5 PWM_OCPY: PWM Duty Cycle Setting Register

PWM _OCPY controls the duty cycle of PWM. For the counter period of PWM duty cycle counter is 50, the value of PWM_OCPY should not beyond 49, or PWM signal with the duty cycle equal to 1 will be output.

Address: 0x84

Bits	Symbol	R/W	Function	Default
7: 6	--	--	~~保留~~ reserved	--
5: 0	OCPY_RATIO	R/W	**OCPY_RATIO controls the duty cycle of PWM signal.** When duty cycle counter equals PWM_OCPY, PWM outputs low level; when counter returns back to 0 from 49, PWM outputs high level. Duty cycle of PWM output can be adjusted by setting OCPY_RATIO.	0x32

12.2.21 Test mode

12.2.21.1 TEST: DCDC and Charger Test Control Register

Address: 0x52

Bits	Symbol	R/W	Function	Default
7	--	--	**Reserved**	--
6:4	DCTEST	R/W	**DCDC test point selection** 000: no test point selected 001-111: DCDCx internal test point selected	000
3:0	CHGTEST	R/W	**charger test control** 0000-1110: select test point in charger 1111: test disabled	1111

12.2.21.2 DC1PFMCTRL: DCDC1 PFM Control Register

Address: 0x53

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	
6	DC1_PFMDET_FILTER_EN	R/W	DCDC1 deglitch selection for load detection block 0: 1 clock cycles 1: 4 clock cycle	1
5	--	--	Reserved	--
4	DC1_PFMDET_SEL	R/W	DCDC1 load detection threshold selection 0: 220mA to heavy load(50mA hysteresis) 1: 270mA to heavy load(50mA hysteresis)	1
3:2	DC1_PFMVTH_SEL	R/W	DCDC1 PFM threshold voltage selection 00: 0.2V 01: 0.3V 10: 0.4V 11: 0.5V	10
1	DC1_PFMTOPMOS	R/W	DCDC1 PMOS controlled by PFMDET 0: PFM_DET controls PMOS 1: PFM_DET does not control PMOS	1

0	DC1_PFMDET_EN	R/W	DCDC1 load detection block for PFM or PWM enable 0: disable 1: enable	0

12.2.21.3 DC2PFMCTRL: DCDC2 PFM Control Register

Address: 0x54

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	
6	DC2_PFMDET_FILTER_EN	R/W	DCDC1 deglitch selection for load detection block 0: 1 clock cycles 1: 4 clock cycle	1
5	--	--	Reserved	--
4	DC2_PFMDET_SEL	R/W	DCDC2 load detection threshold selection 0: 220mA to heavy load(50mA hysteresis) 1: 270mA to heavy load(50mA hysteresis)	1
3:2	DC2_PFMVTH_SEL	R/W	DCDC2 PFM threshold voltage selection 00: 0.2V 01: 0.3V 10: 0.4V 11: 0.5V	10
1	DC2_PFMTOPMOS	R/W	DCDC2 PMOS controlled by PFM_DET 0: PFM_DET controls PMOS 1: PFM_DET does not control PMOS	1
0	DC2_PFMDET_EN	R/W	DCDC2 load detection block for PFM or PWM enable 0: disable 1: enable	0

12.2.21.4 DC3PFMCTRL: DCDC3 PFM Control Register

Address: 0x55

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	DC3_PFMDET_FILTER_EN	R/W	DCDC3 PFM_DET filter enable 0: disable 1: enable	1
5:4	DC3_PFMDET_ITH_SEL	R/W	DCDC3 PFM_DET threshold current selection	01

			00: 119mA 01: 164mA 10: 209mA 11: reserved	
3:2	DC3_PFMVTH_SEL	R/W	DCDC3 PFM threshold voltage selection 00: 0.3V 01: 0.4V 10: 0.5V 11: 0.6V	01
1	DC3_PFMTOPMOS	R/W	DCDC3 PMOS controlled by PFM_DET 0: PFM_DET controls PMOS 1: PFM_DET does not control PMOS	1
0	DC3_PFMDET_DIS	R/W	DCDC3 PFM_DET disable 0: disable 1: enable	1

12.2.21.5 DC4PFMCTRL: DCDC4 PFM Control Register

Address: 0x56

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	
6	DC4_PFMDET_FILTER_EN	R/W	DCDC4 PFM_DET filter enable 0: disable 1: enable	1
5:4	DC4_PFMDET_ITH_SEL	R/W	DCDC4 PFM_DET threshold current selection 00: 130mA 01: 183mA 10: 231mA 11: reserved	01
3:2	DC4_PFMVTH_SEL	R/W	DCDC4 PFM threshold voltage selection 00: 0.2V 01: 0.3V 10: 0.4V 11: 0.5V	10
1	DC4_PFMTOPMOS	R/W	DCDC4 PMOS controlled by PFM_DET 0: PFM_DET controls PMOS 1: PFM_DET does not control PMOS	1
0	DC1_PFMDET_DIS	R/W	DCDC1 PFM_DET disable 0: disable 1: enable	1

12.2.21.6 DC1OVPOCP: DCDC1 OVP and OCP Control Register

Address: 0x57

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	DC1_FBCAP_EN	R/W	DCDC1 FBCAP enable 0: disable 1: enable	1
5	DC1_EACAP	R/W	DCDC1 EA output high frequency capacitor select 0: EA capacitor not connected 1: EA capacitor connected	0
4	DC1_OCP_ITH	R/W	DCDC1 OCP threshold current selection 0: 2A 1: 2.2A	1
3:2	DC1_OVP_SEL	R/W	DCDC1 OVP threshold voltage selection 00: Vout(1+40mV*Vout/0.7V) 01: Vout(1+30mV*Vout/0.7V) 10: Vout(1+20mV*Vout/0.7V) 11: Reserved	01
1	--	--	Reserved	--
0	DC1_OVP_EN	R/W	DCDC1 OVP enable 0: disable 1: enable	1

12.2.21.7 DC2OVPOCP: DCDC2 OVP and OCP Control Register

Address: 0x58

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	DC2_FBCAP_EN	R/W	DCDC2 FBCAP enable 0: disable 1: enable	1
5	DC2_EACAP	R/W	DCDC2 EA output high frequency capacitor select 0: EA capacitor not connected 1: EA capacitor connected	0
4	DC2_OCP_ITH	R/W	DCDC2 OCP threshold current selection 0: 2A 1: 2.2A	1
3:2	DC2_OVP_SEL	R/W	DCDC2 OVP threshold voltage selection 00: Vout(1+40mV*Vout/0.7V) 01: Vout(1+30mV*Vout/0.7V) 10: Vout(1+20mV*Vout/0.7V) 11: Reserved	01
1	--	--	Reserved	--
0	DC2_OVP_EN	R/W	DCDC2 OVP enable 0: disable 1: enable	1

12.2.21.8 DC3OVPOCP: DCDC3 OVP and OCP Control Register

Address: 0x59

Bits	Symbol	R/W	Function	Default
7	DC3_FBCAP_EN	R/W	DCDC3 FBCAP enable 0: disable 1: enable	1
6	DC3_COMPCAP_EN	R/W	DCDC3 COMPCAP enable 0: disable 1: enable	0
5	DC3_LOWP_EN_OVP	R/W	DCDC3 LOWP controlling OVP enable: 0: disable 1: enable	1
4	DC3_OCP_ITH	R/W	DCDC3 OCP threshold current selection 1: 1270mA 0: 1030mA	0
3:2	DC3_OVP_HVTH_SEL	R/W	DCDC3 OVP high threshold voltage selection 00: 0.86V 01: 0.84V 10: 0.82V 11: 0.81V	11
1	DC3_OVP_LVTH_SEL	R/W	DCDC3 OVP low threshold voltage selection 0: 0.805V 1: 0.81V	0
0	DC3_OVP_EN	R/W	DCDC3 OVP enable 0: disable 1: enable	1

12.2.21.9 DC4OVPOCP: DCDC4 OVP and OCP Control Register

Address: 0x5A

Bits	Symbol	R/W	Function	Default
7	DC4_FBCAP_EN	R/W	DCDC4 FBCAP enable 0: disable 1: enable	1
6	DC4_COMPCAP_EN	R/W	DCDC4 COMPCAP enable 0: disable 1: enable	0
5	DC4_LOWP_EN_OVP	R/W	DCDC4 LOWP controlling OVP enable: 0: disable 1: enable	1
4	DC4_OCP_ITH	R/W	DCDC4 OCP threshold current selection 1: 1150mA 0: 950mA	0
3:2	DC4_OVP_HVTH_SEL	R/W	DCDC4 OVP high threshold voltage selection 00: 0.86V 01: 0.84V	11

			10: 0.82V 11: 0.81V	
1	DC4_OVP_LVTH_SEL	R/W	DCDC4 OVP low threshold voltage selection 0: 0.805V 1: 0.81V	0
0	DC4_OVP_EN	R/W	DCDC4 OVP enable 0: disable 1: enable	1

12.2.21.10 DC12DT: DCDC1 and DCDC2 Dead Time Control Register

Address: 0x5B

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6:4	DC2DT	R/W	DCDC2 dead time 000: 0ns 001: 4ns 010: 8ns 011: 12ns 100: 16ns 101: 20ns 110: 24ns 111: Reserved	001
3	--	--	Reserved	
2:0	DC1DT	R/W	DCDC1 dead time 000: 0ns 001: 4ns 010: 8ns 011: 12ns 100: 16ns 101: 20ns 110: 24ns 111: Reserved	001

12.2.21.11 DC34DT: DCDC3 and DCDC4 Dead Time Control Register

Address: 0x5C

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6:4	DC4DT	R/W	DCDC4 dead time	001
3	--	--	Reserved	
2:0	DC3DT	R/W	DCDC3 dead time	001

12.2.21.12 DC12RCP: DCDC1 and DCDC2 RCP Control Register

Address: 0x5D

Bits	Symbol	R/W	Function	Default
7	DC2TESTEN	--	DCDC2 test pin output enable 0: disable 1: enable	0
6:4	DC2RCP	R/W	DCDC2 RCP threshold 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV 110: GND-SW=6mV 111: GND-SW=0mV	101
3	DC1TESTEN	--	DCDC1 test pin output enable 0: disable 1: enable	0
2:0	DC1RCP	R/W	DCDC1 RCP threshold 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV 110: GND-SW=6mV 111: GND-SW=0mV	101

12.2.21.13 DC34RCP: DCDC3 and DCDC4 RCP Control Register

Address: 0x5E

Bits	Symbol	R/W	Function	Default
7	DC4TESTEN	--	DCDC4 test pin output enable 0: disable 1: enable	0
6:4	DC4RCP	R/W	DCDC4 RCP selection 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV 110: GND-SW=6mV 111: GND-SW=0mV	101
3	DC3TESTEN	--	DCDC3 test pin output enable	0

			0: disable 1: enable	
2:0	DC3RCP	R/W	DCDC3 RCP selection 000: GND-SW=42mV 001: GND-SW=36mV 010: GND-SW=30mV 011: GND-SW=24mV 100: GND-SW=18mV 101: GND-SW=12mV 110: GND-SW=6mV 111: GND-SW=0mV	101

12.2.22 OTP control

12.2.22.1 OTPSEL0: OTP Trimming Enable Register0

Address: 0x86

Bits	Symbol	R/W	Function	Default
7	FREQ_OTP_SEL	R/W	0: trimming oscillator frequency of DCDC by OTP 1: trimming oscillator frequency of DCDC by TRIMx register	0
6	DC4_OTP_SEL	R/W	0: trimming DCDC4 by OTP 1: trimming DCDC4 by TRIMx register	0
5	DC3_OTP_SEL	R/W	0: trimming DCDC3 by OTP 1: trimming DCDC3 by TRIMx register	0
4	DC2_OTP_SEL	R/W	0: trimming DCDC2 by OTP 1: trimming DCDC2 by TRIMx register	0
3	DC1_OTP_SEL	R/W	0: trimming DCDC1 by OTP 1: trimming DCDC1 by TRIMx register	0
2	ADC_OTP_SEL	R/W	0: trimming ADC by OTP 1: trimming ADC by TRIMx register	0
1	CHG_OTP_SEL	R/W	0: trimming bandgap in charger by OTP 1: trimming bandgap in charger by TRIMx register	0
0	BG_OTP_SEL	R/W	0: trimming bandgap reference by OTP 1: trimming bandgap reference by TRIMx register	0

12.2.22.2 OTPSEL1: OTP Trimming Enable Register1

Address: 0x87

Bits	Symbol	R/W	Function	Default
7:5	--	R/W	Reserved	--
4	VIBRATOR_OTP_SEL	R/W	0: trimming current sink for vibrator by OTP 1: trimming current sink for vibrator by TRIMx register	0
3	KEYBOARD_LED_OTP_SEL	R/W	0: trimming current sink for keyboard backlight LED by OTP	0

			1: trimming current sink for keyboard backlight LED by TRIMx register	
2	LCD_OTP_SEL	R/W	0: trimming current sink for LCD by OTP 1: trimming current sink for LCD by TRIMx register	0
1	LDOD_OTP_SEL	R/W	0: trimming bandgap in charger by OTP 1: trimming bandgap in charger by TRIMx register	0
0	LDOA_OTP_SEL	R/W	0: trimming LDOA output voltage by OTP 1: trimming LDOA output voltage by TRIMx register	0

12.2.22.3 OTPMODE: OTP Mode Register

Address: 0x88

Bits	Symbol	R/W	Function	Default
2: 1	OTPPTM	R/W	**OTP test mode** 00: user mode 01: reserved 10: margin-2 read mode which setups a critical read condition to filter out “weak retention” bits during CP2 sort in testing flow 11: margin-1 read mode which provides a critical read condition to filter out “weak programmed bits” during CP1 sort in testing flow	0x0
0	OTPPROG	R/W	**OTP programe mode enable** 0: read or standby mode 1: programe mode	0

12.2.22.4 OTPCMD: OTP Command Register

Address: 0x89

Bits	Symbol	R/W	Function	Default
7	--	--	Reserved	--
6	OTPMGRD	W	**OTP margin read operation command** Writing 1 to this bit to margin read OTP data. This bit is cleared automatically. This command is only used for margin-1 and margin-2 read mode	0
5	OTPRD	W	**OTP read operation command** Writing 1 to this bit to read OTP data. This bit is cleared automatically	0
4	OTPWR	W	**OTP write operation command** Writing 1 to this bit to write data from TRIMx registers to OTP. This bit is cleared automatically.	0
3: 0	OTPPA	R/W	**OTP write address**	0

12.2.22.5 TRIM0: Byte0 of Trimming Parameters Setting Register

Address: 0x8A

Bits	Symbol	R/W	Function	Default
7:0	TRIM0	R/W	**Byte0 of trimming parameters, equivalent to OTP[7:0]**	0xFF

12.2.22.6 TRIM1: Byte1 of Trimming Parameters Setting Register

Address: 0x8B

Bits	Symbol	R/W	Function	Default
7:0	TRIM1	R/W	**Byte1 of trimming parameters, equivalent to OTP[15:8]**	0xff

12.2.22.7 TRIM2: Byte2 of Trimming Parameters Setting Register

Address: 0x8C

Bits	Symbol	R/W	Function	Default
7:0	TRIM2	R/W	**Byte2 of trimming parameters, equivalent to OTP[23:16]**	0xFF

12.2.22.8 TRIM3: Third byte of Trimming Parameters Setting Register

Address: 0x8D

Bits	Symbol	R/W	Function	Default
7:0	TRIM3	R/W	**Byte3 of trimming parameters for analog blocks, equivalent to OTP[31:24]**	0xFF

12.2.22.9 TRIM4: Byte4 of Trimming Parameters Setting Register

Address: 0x8E

Bits	Symbol	R/W	Function	Default
7:0	TRIM4	R/W	**Byte4 of trimming parameters, equivalent to OTP [39:32]**	0xFF

12.2.22.10 TRIM5: Byte5 of Trimming Parameters Setting Register

Address: 0x8F

Bits	Symbol	R/W	Function	Default
7:0	TRIM5	R/W	**Byte5 of trimming parameters, equivalent to OTP [47:40]**	0xFF

12.2.22.11 TRIM6: Byte6 of Trimming Parameters Setting Register

Address: 0x90

Bits	Symbol	R/W	Function	Default
7:0	TRIM6	R/W	**Byte6 of trimming parameters, equivalent**	0xFF

			to OTP [55:48]	

12.2.22.12 TRIM7: Byte7 of Trimming Parameters Setting Register

Address: 0x91

Bits	Symbol	R/W	Function	Default
7:0	TRIM7	R/W	**Byte7 of trimming parameters, equivalent to OTP [63:56]**	0xFF

12.2.22.13 TRIM8: Byte8 of Trimming Parameters Setting Register

Address: 0x92

Bits	Symbol	R/W	Function	Default
7:0	TRIM8	R/W	**Byte8 of trimming parameters, equivalent to OTP [71:64]**	0xFF

12.2.22.14 TRIM9: Byte9 of Trimming Parameters Setting Register

Address: 0x93

Bits	Symbol	R/W	Function	Default
7:0	TRIM9	R/W	**Byte9 of trimming parameters, equivalent to OTP [79:72]**	0xFF

12.2.22.15 TRIM10: Byte10 of Trimming Parameters Setting Register

Address: 0x94

Bits	Symbol	R/W	Function	Default
7:0	TRIM10	R/W	**Byte10 of trimming parameters, equivalent to OTP [87:80]**	0xFF

12.2.22.16 TRIM11: Byte11 of Trimming Parameters Setting Register

Address: 0x95

Bits	Symbol	R/W	Function	Default
7:0	TRIM11	R/W	**Byte11 of trimming parameters, equivalent to OTP [95:88]**	0xFF

12.2.22.17 TRIM12: Byte12 of Trimming Parameters Setting Register

Address: 0x96

Bits	Symbol	R/W	Function	Default
7:0	TRIM12	R/W	**Byte12 of trimming parameters, equivalent to OTP [103:96]**	0xFF

12.2.22.18 TRIM13: Byte13 of Trimming Parameters Setting Register

Address: 0x97

Bits	Symbol	R/W	Function	Default
7:0	TRIM13	R/W	**Byte13 of trimming parameters, equivalent to OTP [111:104]**	0xFF

12.2.22.19 TRIM14: Byte14 of Trimming Parameters Setting Register

Address: 0x98

Bits	Symbol	R/W	Function	Default
7:0	TRIM14	R/W	**Byte14 of trimming parameters, equivalent to OTP [119:112]**	0xFF

12.2.22.20 TRIM15: Byte15 of Trimming Parameters Setting Register

Address: 0x99

Bits	Symbol	R/W	Function	Default
7:0	TRIM15	R/W	**Byte15 of trimming parameters, equivalent to OTP [127:120]**	0xFF

12.2.23 Jack and Hookswitch

12.2.23.1 JKHSIRQST: Jack and Hookswitch interrupt status register

Address: 0x9A

Bits	Symbol	R/W	Function	Default
7	JKDETPOL	RW	Jack detect polarity 0: JACKDET high indicate Jack insertion.(Normal close) 1: JACKDET low indicate Jack insertion (Normal Open)	0
6	HSDETEN	RW	Hookswitch detector enable 0: disable 1: enable	0
5	HS_CMP	R	Hookswitch comparator output status 0: Hookswitch released 1: Hookswitch pressed	0
4	JACK_CMP	R	Jack comparator output status 0: Jack out 1: Jack in	0
3	HSUPIR	RW	Hookswitch up interrupt status Write 1 to clear this interrupt	0
2	HSDNIR	RW	Hookswitch down interrupt status Write 1 to clear this interrupt	0

1	JACKOUTIR	RW	Jack out interrupt status Write 1 to clear this interrupt	0
0	JACKINIR	RW	Jack in interrupt status Write 1 to clear this interrupt	0

12.2.23.2 JKHSMSK: Jack and Hookswitch interrupt enable register

Address: 0x9B

Bits	Symbol	R/W	Function	Default
7	HSUPIREN	RW	Hookswitch up interrupt enable 0: disable 1: enable	0
6	HSDNIREN	RW	Hookswitch down interrupt enable 0: disable 1: enable	0
5	JACKOUTIREN	RW	Jack out interrupt enable 0: disable 1: enable	0
4	JACKINIREN	RW	Jack in interrupt enable 0: disable 1: enable	0
3	HSUPIRMSK	RW	Hookswitch up interrupt mask 0: unmask 1: mask	0
2	HSDNIRMSK	RW	Hookswitch down interrupt mask 0: unmask 1: mask	0
1	JACKOUTIRMSK	RW	Jack out interrupt mask 0: unmask 1: mask	0
0	JACKINIRMSK	RW	Jack in interrupt mask 0: unmask 1: mask	0

12.2.24 Version

12.2.24.1 VERSION: Version Number Register

Address: 0x5F

Bits	Symbol	R/W	Function	Default
7:0	VERSION	R	Version number register, representing chip version LC1132 V2.0	0x20

12.3 Codec register descriptions

带格式表格

Address	Reg.Name	BIT	Register bit Name	DEFAULT	DESCRIPTION
0x9C	R0	7			
		6	MIC2PGAZCEN	0	MainMIC2 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
		5	MIC2PGAMU	1	MainMIC2 PGA Mute signal 0: Un-Mute; 1：Mute
		4	MIC2PGAEN	0	MainMIC2 PGA Enable signal 1: MIC2PGA Enable；0：MIC2PGA Power Down
		3			
		2	MIC1PGAZCEN	0	MainMIC1 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
		1	MIC1PGAMU	1	MainMIC1 PGA Mute signal 0: Un-Mute; 1：Mute
		0	MIC1PGAEN	0	MainMIC1 PGA Enable signal 1: MIC1PGA Enable；0：MIC1PGA Power Down
0x9D	R1	7	DACREN	0	DAC Right Enable signal 0: Rch DAC disable; 1: Rch DAC enable.
		6	DACLEN	0	DAC Left Enable signal 0: Lch DAC disable; 1: Lch DAC enable.
		5	DACMONOEN	0	DAC MONO Enable signal 0: mono DAC disable 1: mono DAC enable
		4	ADC2EN	0	ADC2 Enable signal 0: ADC2 disable; 1: ADC2 enable.
		3	ADC1EN	0	ADC1 Enable signal 0: ADC1 disable; 1: ADC1 enable.
		2	LINREN	0	Line Right Enable signal 1: Right Line PGA Enable；0： Power Down
		1	LINLEN	0	Line Left Enable signal 1: Left Line PGA Enable；0： Power Down
		0	SLOWCLK_EN	0	Slow clock enable signal 1: enable 0: disable
0x9E	R2	7	LINLMU	1	Line Left PGA Mute signal 0: Un-Mute; 1：Mute
		6	LINLZCEN	0	Line Left PGA ZeroCross Enable signal 1: Enable；0：Disable
		5:0	LINLVOL[5:0]	011111	Line Left PGA Volume Control:

111111--101000	fix to 12dB		
100111	12dB	010011	-18 dB
100110	10.5 dB	010010	-19.5 dB
100101	9 dB	010001	-21 dB

						100100	7.5 dB	010000	-22.5 dB
						100011	6 dB	001111	-24 dB
						100010	4.5 dB	001110	-25.5 dB
						100001	3 dB	001101	-27 dB
						100000	1.5 dB	001100	-28.5 dB
						011111	0dB dB	001011	-30 dB
						011110	-1.5 dB	001010	-31.5 dB
						011101	-3 dB	001001	-33 dB
						011100	-4.5 dB	001000	-34.5 dB
						011011	-6 dB	000111	-36 dB
						011010	-7.5 dB	000110	-37.5 dB
						011001	-9 dB	000101	-39 dB
						011000	-10.5 dB	000100	-40.5 dB
						010111	-12 dB	000011	-42 dB
						010110	-13.5 dB	000010	-43.5 dB
						010101	-15 dB	000001	-45 dB
						010100	-16.5 dB	000000	-46.5 dB
0x9F	R		7	LINRMU	1	Line Right PGA Mute signal: 0: Un-Mute; 1：Mute			
			6	LINRZCEN	0	Line Right PGA ZeroCross Enable signal 1: Enable; 0:Disable			
			5:0	LINRVOL[5:0]	011111	Line Right PGA Volume Control:			
						111111--101000	fix to 12dB		
						100111	12dB	010011	-18 dB
						100110	10.5 dB	010010	-19.5 dB
						100101	9 dB	010001	-21 dB
						100100	7.5 dB	010000	-22.5 dB
						100011	6 dB	001111	-24 dB
						100010	4.5 dB	001110	-25.5 dB
						100001	3 dB	001101	-27 dB
						100000	1.5 dB	001100	-28.5 dB
						011111	0dB dB	001011	-30 dB
						011110	-1.5 dB	001010	-31.5 dB
						011101	-3 dB	001001	-33 dB
						011100	-4.5 dB	001000	-34.5 dB
						011011	-6 dB	000111	-36 dB
						011010	-7.5 dB	000110	-37.5 dB
						011001	-9 dB	000101	-39 dB
						011000	-10.5 dB	000100	-40.5 dB
						010111	-12 dB	000011	-42 dB
						010110	-13.5 dB	000010	-43.5 dB
						010101	-15 dB	000001	-45 dB

						010100	-16.5 dB	000000	-46.5 dB
0xA0	R4		7	SDMU	1	Side Tone PGA mute signal: 0: Un-Mute; 1：Mute			
			6	SDEN	0	Side Tone PGA Enable signal: 1: Side Tone PGA Enable；0： Power Down			
			5	SDZCEN	0	Side Tone PGA ZeroCross Enable signal 1: Enable；0：Disable			
			4:0	SDVOL[4:0]	11110	Side Tone PGA Volume Control:			
						11111	0dB	01111	-15dB
						11110	0dB	01110	-16dB
						11101	-1dB	01101	-17dB
						11100	-2dB	01100	-18dB
						11011	-3dB	01011	-19dB
						11010	-4dB	01010	-20dB
						11001	-5dB	01001	-21dB
						11000	-6dB	01000	-22dB
						10111	-7dB	00111	-23dB
						10110	-8dB	00110	-24dB
						10101	-9dB	00101	-25dB
						10100	-10dB	00100	-26dB
						10011	-11dB	00011	-27dB
						10010	-12dB	00010	-28dB
						10001	-13dB	00001	-29dB
						10000	-14dB	00000	-30dB
0xA1	R5		7	EPMUTE	1	REC Mute control. 1: Mute. 0:unmute			
			6	EPZCEN	0	REC zero crossing enable 1: Enable. 0:disable			
			5	EPEN	0	REC Power down. 1: Power on. 0: Power down.			
			4:0	EPVOL[4:0]	11001	REC Output Volume Control.			
						11111	6dB	01111	-10dB
						11110	5dB	01110	-11dB
						11101	4dB	01101	-12dB
						11100	3dB	01100	-13dB
						11011	2dB	01011	-14dB
						11010	1dB	01010	-15dB
						11001	0dB	01001	-16dB
						11000	-1dB	01000	-17dB
						10111	-2dB	00111	-18dB
						10110	-3dB	00110	-19dB
						10101	-4dB	00101	-20dB

						10100	-5dB	00100	-21dB	
						10011	-6dB	00011	-22dB	
						10010	-7dB	00010	-23dB	
						10001	-8dB	00001	-24dB	
						10000	-9dB	00000	-25dB	
0xA2	R6		7	HPMUTEL	1	HP left channel Mute control. 1: Mute. 0: unmute.				
			6	HPZCENL	0	HP left channel zero crossing enable. 1: Enable. 0: disable.				
			5	HPENL	0	HP left channel Power down. 1: Power on. 0: Power down.				
			4:0	HPVOLL[4:0]	11001	Left Channel Headphone Output Volume Control.				
						11111	6dB	01111	-10dB	
						11110	5dB	01110	-11dB	
						11101	4dB	01101	-12dB	
						11100	3dB	01100	-13dB	
						11011	2dB	01011	-14dB	
						11010	1dB	01010	-15dB	
						11001	0dB	01001	-16dB	
						11000	-1dB	01000	-17dB	
						10111	-2dB	00111	-18dB	
						10110	-3dB	00110	-19dB	
						10101	-4dB	00101	-20dB	
						10100	-5dB	00100	-21dB	
						10011	-6dB	00011	-22dB	
						10010	-7dB	00010	-23dB	
						10001	-8dB	00001	-24dB	
						10000	-9dB	00000	-25dB	
0xA3	R7		7	HPMUTER	1	HP right channel Mute control. 1: Mute. 0: unmute.				
			6	HPZCENR	0	HP right channel zero crossing enable. 1: Enable. 0: disable				
			5	HPENR	0	HP right channel Power down. 1: Power on. 0: Power down.				
			4:0	HPVOLR[4:0]	11001	Right Channel Headphone Output Volume Control.				
						11111	6dB	01111	-10dB	
						11110	5dB	01110	-11dB	
						11101	4dB	01101	-12dB	
						11100	3dB	01100	-13dB	
						11011	2dB	01011	-14dB	
						11010	1dB	01010	-15dB	
						11001	0dB	01001	-16dB	
						11000	-1dB	01000	-17dB	

						10111	-2dB	00111	-18dB	
						10110	-3dB	00110	-19dB	
						10101	-4dB	00101	-20dB	
						10100	-5dB	00100	-21dB	
						10011	-6dB	00011	-22dB	
						10010	-7dB	00010	-23dB	
						10001	-8dB	00001	-24dB	
						10000	-9dB	00000	-25dB	
0xA4	R8		7	CD_MUTE	1	Class D Volume mute control. 0: unmute; 1: mute				
			6	SPKZCEN	0	Class D PGA gain control zero-crossing enable 0: Disable; 1: Enable				
			5	TOEN	1	Zero-crossing timeout enable 1: enable 0: disable				
			4:0	CDVOL[4:0]	10100	Class D Volume gain control.				
						11111	5dB	01111	-11dB	
						11110	4dB	01110	-12dB	
						11101	3dB	01101	-13dB	
						11100	2dB	01100	-14dB	
						11011	1dB	01011	-15dB	
						11010	0dB	01010	-16dB	
						11001	-1dB	01001	-17dB	
						11000	-2dB	01000	-18dB	
						10111	-3dB	00111	-19dB	
						10110	-4dB	00110	-20dB	
						10101	-5dB	00101	-21dB	
						10100	-6dB	00100	-22dB	
						10011	-7dB	00011	-23dB	
						10010	-8dB	00010	-24dB	
						10001	-9dB	00001	-25dB	
						10000	-10dB	00000	-26dB	
0xA5	R9		7:2			Reserved				
			1	CD_ALC_CLR	0	Class-D ALC flag clear Writing “1” to clear CD_ALC_FLAG				
			0	CD_DTS_CLR	0	Class-D over temperature flag clear Writing “1” to clear CD_DTS_FLAG				
0xA6	R10		7		0	Reserved				
			6	I2S_RSTN	1	I2S soft reset, active low				
			5:4	I2SCLK_SEL[1:0]	10	I2S 256fs clock selection 00: PLL out 01: EXTCLK 10: MCLK_IN 11: no clock				
			3	I2S_LRCINV	0	I2SLRCK Invert				

					1: inverted 0: not inverted.
		2	I2S_BCKINV	0	I2SBICK Invert 1: inverted; 0: not inverted
		1	I2SBCK_64	1	BCLK frequency selection in master mode 0: 32Fs 1: 64Fs
		0	I2S_MS	0	Master / Slave Mode Control 1: Master Mode; 0: Slave Mode
0xA7	R11	7		0	Reserved
		6		0	Reserved
		5	I2S_LOOPBACK	0	1: loop back I2S output DAT to input DAT 0: normal
		4	I2S_LRP	0	DSP mode selection 0: Mode A 1: Mode B
		3:2	I2S_WL[1:0]	10	Audio Data Word Length 11 = 32 bits; 10 = 24 bits 01 = 20 bits; 00 = 16 bits
		1:0	I2S_FORMAT[1:0]	10	Audio Data Format Select 11 = DSP/PCM; 10 = I2S Format 01 = Left justified; 00 = Right justified
0xA8	R12	7:6	I2S_RSEL[1:0]	00	I2S output right channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output
		5:4	I2S_LSEL[1:0]	00	I2S output Left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output
		3	I2STXPOL	0	1: invert TX data 0: normal
		2	I2SRXPOL	0	1: invert RX data 0: normal
		1	I2STXLRSWAP	0	Swap Left and Right Channels data of I2S TX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)
		0	I2SRXLRSWAP	0	Swap Left and Right Channels data of I2S RX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)
0xA9	R13	7	PCM_UALAW_INV	1	PCM UALAW inv 1: u-law all bits or A-law even bit inverted 0: not inverted
		6	PCM_DB	0	PCM interface in dual-channel mode 1: dual-channel 0: normal
		5:4	PCM_LSEL[1:0]	00	PCM output left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10 ,11: Zero output
		3:2	PCM_RSEL[1:0]	00	PCM output right channel data selection

					00: ADC1 decimation output 01: ADC2 decimation output 10,11: Zero output
		1:0	PCM_Compand[1:0]	00	PCM Audio Data Format Select 00 = 16bit PCM; 01 = u-law (8bit u-law at PCM[15:7]) 10 = A-law (8bit A-law at PCM[15:7]) 11: reserved.
0xAB	R15	7		0	reserved
		6	PCM_RSTN	1	PCM soft reset, active low
		5:4	PCMCLK_SEL[1:0]	10	PCM 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
		3	PCM_SYNCSEL	0	PCM sync format selection 1: long frame sync 0: short frame sync
		2	PCM_BCKINV	0	PCM BICK Invert 1: inverted; 0: not inverted
		1	PCMBCK_32	1	PCMBICK frequency selection in master mode 0: 16Fs 1: 32Fs
		0	PCM_MS	0	PCM Master / Slave Mode Control 1: Master Mode; 0: Slave Mode
0xAC	R16	7:5			reserved
		4:2	MONO_DAC_SEL [2:0]	111	mono DAC data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: from ADC1 output data 101: from ADC2 output data 110: 111: Reserved as Zero
		1	MONODACMU	1	mono DAC mute 1: mute 0: unmute
		0	MONOSOFTMUTE_EN	1	mono DAC soft mute fuction enable 1: enable 0: disable
0xAD	R17	7	ADC1_ERR	1	ADC1 ALC target error tolerance 1: +- 1.5db 0: +- 0.75db
		6	ADC1_NFEN	0	ADC1 notch filter enable signal 1: enable 0: disable
		5:0	ADC1_NFA0[13:8]	00_0000	ADC1 notch filter A0 coefficient MSBs
0xAE	R18	7:0	ADC1_NFA0[7:0]	0000_0000	ADC1 notch filter A0 coefficient LSBs
0xAF	R19	7	ADC1_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz)

					0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)
		6	ADC1_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1= enabled Application mode (2nd order, fc = HPFCUT)
		5:0	ADC1_NFA1[13:8]	00_0000	ADC1 notch filter A1 coefficient MSBs
0xB0	R20	7:0	ADC1_NFA1[7:0]	0000_0000	ADC1 notch filter A1 coefficient LSBs
0xB1	R21	7	ADC1_ALC_DSEL	0	ADC1 ALC data selection 0: after comb filter 1: after HPF filter
		6	ADC1_ALCMODE	0	ADC1 ALC mode selection 0： ALC mode(Normal Operation) 1: Limiter mode
		5	ADC1_ALCSEL	0	ADC1 ALC function enable 1: Enable 0: Disable
		4	ADC1_NG_EN	0	ADC1 Noise Gate enable signal 1: Enable 0: Disable
		3:0	ADC1_NG[3:0]	0111	ADC1 noise floor level

1111	-84dB	0111	-60 dB
1110	-81 dB	0110	-57 dB
1101	-78 dB	0101	-54 dB
1100	-75 dB	0100	-51 dB
1011	-72 dB	0011	-48 dB
1010	-69 dB	0010	-45 dB
1001	-66 dB	0001	-42 dB
1000	-63 dB	0000	-39 dB

0xB2	R22	7:5	ADC1_HPFCUT [2:0]	000	Application mode cut-off frequency.(Fs=48KHz) 000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz
		4:0	ADC1_TARGET [4:0]	00011	ADC1 ALC target level

11111	-48dB	01111	-24dB
11110	-46.5dB	01110	-22.5dB
11101	-45dB	01101	-21dB
11100	-43.5dB	01100	-19.5dB
11011	-42dB	01011	-18dB
11010	-40.5dB	01010	-16.5dB
11001	-39dB	01001	-15dB
11000	-37.5dB	01000	-13.5dB
10111	-36dB	00111	-12dB
10110	-34.5dB	00110	-10.5dB
10101	-33dB	00101	-9dB
10100	-31.5dB	00100	-7.5dB
10011	-30dB	00011	-6dB

					10010	-28.5dB	00010	-4.5dB	
					10001	-27dB	00001	-3dB	
					10000	-25.5dB	00000	-1.5dB	
0xB3	R23	7	ADC1MU	1	ADC1 mute signal 1: mute 0: un-mute				
		6:0	ADC1_DIG_VOL [6:0]	1100111 (default 0dB)	ADC1 digital gain				
					1111111	18dB	0111111	-30dB	
					1111110	17.25dB	0111110	-30.75dB	
					1111101	16.5dB	0111101	-31.5dB	
					1111100	15.75dB	0111100	-32.25dB	
					1111011	15dB	0111011	-33dB	
					1111010	14.25dB	0111010	-33.75dB	
					1111001	13.5dB	0111001	-34.5dB	
					1111000	12.75dB	0111000	-35.25dB	
					1110111	12dB	0110111	-36dB	
					1110110	11.25dB	0110110	-36.75dB	
					1110101	10.5dB	0110101	-37.5dB	
					1110100	9.75dB	0110100	-38.25dB	
					1110011	9dB	0110011	-39dB	
					1110010	8.25dB	0110010	-39.75dB	
					1110001	7.5dB	0110001	-40.5dB	
					1110000	6.75dB	0110000	-41.25dB	
					1101111	6dB	0101111	-42dB	
					1101110	5.25dB	0101110	-42.75dB	
					1101101	4.5dB	0101101	-43.5dB	
					1101100	3.75dB	0101100	-44.25dB	
					1101011	3dB	0101011	-45dB	
					1101010	2.25dB	0101010	-45.75dB	
					1101001	1.5dB	0101001	-46.5dB	
					1101000	0.75dB	0101000	-47.25dB	
					1100111	0dB	0100111	-48dB	
					1100110	-0.75dB	0100110	-48.75dB	
					1100101	-1.5dB	0100101	-49.5dB	
					1100100	-2.25dB	0100100	-50.25dB	
					1100011	-3dB	0100011	-51dB	
					1100010	-3.75dB	0100010	-51.75dB	
					1100001	-4.5dB	0100001	-52.5dB	
					1100000	-5.25dB	0100000	-53.25dB	
					1011111	-6dB	0011111	-54dB	
					1011110	-6.75dB	0011110	-54.75dB	
					1011101	-7.5dB	0011101	-55.5dB	
					1011100	-8.25dB	0011100	-56.25dB	
					1011011	-9dB	0011011	-57dB	

					1011010	-9.75dB	0011010	-57.75dB
					1011001	-10.5dB	0011001	-58.5dB
					1011000	-11.25dB	0011000	-59.25dB
					1010111	-12dB	0010111	-60dB
					1010110	-12.75dB	0010110	-60.75dB
					1010101	-13.5dB	0010101	-61.5dB
					1010100	-14.25dB	0010100	-62.25dB
					1010011	-15dB	0010011	-63dB
					1010010	-15.75dB	0010010	-63.75dB
					1010001	-16.5dB	0010001	-64.5dB
					1010000	-17.25dB	0010000	-65.25dB
					1001111	-18dB	0001111	-66dB
					1001110	-18.75dB	0001110	-66.75dB
					1001101	-19.5dB	0001101	-67.5dB
					1001100	-20.25dB	0001100	-68.25dB
					1001011	-21dB	0001011	-69dB
					1001010	-21.75dB	0001010	-69.75dB
					1001001	-22.5dB	0001001	-70.5dB
					1001000	-23.25dB	0001000	-71.25dB
					1000111	-24dB	0000111	-72dB
					1000110	-24.75dB	0000110	-72.75dB
					1000101	-25.5dB	0000101	-73.5dB
					1000100	-26.25dB	0000100	-74.25dB
					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute
0xB4	R24	7						
		6	MIC1_0_16_SEL	1	MIC1 1st PGA gain 0: 0dB; 1: 16dB (Default) （Note： total gain=1st PGA gain + 2nd PGA gain）			
		5:0	MIC1_PGA_LEVEL	000000 （6dB）	MIC1 2nd PGA gain			
					111111--101001	fix to 20dB		
					101000	20 dB		
					100111	19.25 dB	010011	4.25 dB
					100110	18.5 dB	010010	3.5 dB
					100101	17.75 dB	010001	2.75 dB
					100100	17 dB	010000	2 dB
					100011	16.25 dB	001111	1.25 dB
					100010	15.5 dB	001110	0.5 dB
					100001	14.75 dB	001101	-0.25 dB
					100000	14 dB	001100	-1 dB

					011111	13.25 dB	001011	-1.75 dB
					011110	12.5 dB	001010	-2.5 dB
					011101	11.75 dB	001001	-3.25 dB
					011100	11 dB	001000	-4 dB
					011011	10.25 dB	000111	-4.75 dB
					011010	9.5 dB	000110	-5.5 dB
					011001	8.75 dB	000101	-6.25 dB
					011000	8 dB	000100	-7 dB
					010111	7.25 dB	000011	-7.75 dB
					010110	6.5 dB	000010	-8.5 dB
					010101	5.75 dB	000001	-9.25 dB
					010100	5 dB	000000	-10 dB
0xB5	R25	7			Reserved			
		6			Reserved			
		5:0	ADC1_ALCMAX	101000	max PGA gain used in ADC1 ALC model Description similar with MIC1_PGA_LEVEL			
0xB6	R26	7						
		6						
		5:0	ADC1_ALCMIN	000000	min PGA gain used in ADC1 ALC model Description similar with MIC1_PGA_LEVEL			
0xB7	R27	7:4	ADC1_ALCDCY	0011	ADC1 decay time(Fs=48KHz) When ADC1_ALCMODE=0			
					1111	10.92s	0111	42.67ms
					1110	5.46s	0110	21.33ms
					1101	2.73s	0101	10.67ms
					1100	1.37s	0100	5.33ms
					1011	682.67ms	0011	2.67ms
					1010	341.33ms	0010	1.33ms
					1001	170.67ms	0001	666.7μs
					1000	85.33ms	0000	333.3μs
					When ADC1_ALCMODE =1			
					1111	2.73s	0111	10.67ms
					1110	1.37s	0110	5.33ms
					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs
					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.7μs
					1000	21.33ms	0000	83.3μs
		3:0	ADC1_ALCATK	0010	ADC1 attack time (Fs=48kHz)			

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>When ADC1_ALCMODE =0<table><tr><td>1111</td><td>2.73s</td><td>0111</td><td>10.67ms</td></tr><tr><td>1110</td><td>1.37s</td><td>0110</td><td>5.33ms</td></tr><tr><td>1101</td><td>682.67ms</td><td>0101</td><td>2.67ms</td></tr><tr><td>1100</td><td>341.33ms</td><td>0100</td><td>1.33ms</td></tr><tr><td>1011</td><td>170.67ms</td><td>0011</td><td>666.7µs</td></tr><tr><td>1010</td><td>85.33ms</td><td>0010</td><td>333.3µs</td></tr><tr><td>1001</td><td>42.67ms</td><td>0001</td><td>166.6µs</td></tr><tr><td>1000</td><td>21.33ms</td><td>0000</td><td>83.3µs</td></tr></table>When ADC1_ALCMODE =1<table><tr><td>1111</td><td>682.67ms</td><td>0111</td><td>2.67ms</td></tr><tr><td>1110</td><td>341.33ms</td><td>0110</td><td>1.33ms</td></tr><tr><td>1101</td><td>170.67ms</td><td>0101</td><td>666.7µs</td></tr><tr><td>1100</td><td>85.33ms</td><td>0100</td><td>333.3µs</td></tr><tr><td>1011</td><td>42.67ms</td><td>0011</td><td>166.6µs</td></tr><tr><td>1010</td><td>21.33ms</td><td>0010</td><td>83.3µs</td></tr><tr><td>1001</td><td>10.67ms</td><td>0001</td><td>41.7µs</td></tr><tr><td>1000</td><td>5.33ms</td><td>0000</td><td>20.8µs</td></tr></table></td></tr>
<tr><td>0xB8</td><td>R28</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>3:0</td><td>ADC1_ALCHLD</td><td>0000</td><td>ADC1 hold time (Fs=48kHz)<table><tr><td>1111</td><td>43.69s</td><td>0111</td><td>170.67ms</td></tr><tr><td>1110</td><td>21.85s</td><td>0110</td><td>85.33ms</td></tr><tr><td>1101</td><td>10.92s</td><td>0101</td><td>42.67ms</td></tr><tr><td>1100</td><td>5.46s</td><td>0100</td><td>21.33ms</td></tr><tr><td>1011</td><td>2.73s</td><td>0011</td><td>10.67ms</td></tr><tr><td>1010</td><td>1.37s</td><td>0010</td><td>5.33ms</td></tr><tr><td>1001</td><td>682.67ms</td><td>0001</td><td>2.67ms</td></tr><tr><td>1000</td><td>341.33ms</td><td>0000</td><td>2.67ms</td></tr></table></td></tr>
<tr><td>0xB9</td><td>R29</td><td>7</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>6</td><td>ADC1LPEN</td><td>0</td><td>ADC1 low power enable
1: ADC1 clocks are turned off automatically when ADC1 is disabled
0: ADC1 clocks are not turned off automatically</td></tr>
<tr><td></td><td></td><td>5</td><td>ADC1OSR128</td><td>1</td><td>ADC1 over-sampling rate
0: 64X 1: 128X</td></tr>
<tr><td></td><td></td><td>4</td><td>ADC1_RSTN</td><td>1</td><td>ADC1 soft reset signal, active low</td></tr>
<tr><td></td><td></td><td>3:2</td><td>ADC1LRC_SEL[1:0]</td><td>00</td><td>ADC1 LRC selection
00: from I2S LRCK 01: from PCM SYNC
10,11: no LRCK</td></tr>
<tr><td></td><td></td><td>1:0</td><td>ADC1CLK_SEL[1:0]</td><td>10</td><td>ADC1 256fs clock selection</td></tr>
</table>

					00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
0xBA	R30	7			Reserved
		6:0	MONO_DAC_LEVEL[6:0]	1100111 (default 0db)	mono DAC channel digital gain

1111111	18dB	0111111	-30dB
1111110	17.25dB	0111110	-30.75dB
1111101	16.5dB	0111101	-31.5dB
1111100	15.75dB	0111100	-32.25dB
1111011	15dB	0111011	-33dB
1111010	14.25dB	0111010	-33.75dB
1111001	13.5dB	0111001	-34.5dB
1111000	12.75dB	0111000	-35.25dB
1110111	12dB	0110111	-36dB
1110110	11.25dB	0110110	-36.75dB
1110101	10.5dB	0110101	-37.5dB
1110100	9.75dB	0110100	-38.25dB
1110011	9dB	0110011	-39dB
1110010	8.25dB	0110010	-39.75dB
1110001	7.5dB	0110001	-40.5dB
1110000	6.75dB	0110000	-41.25dB
1101111	6dB	0101111	-42dB
1101110	5.25dB	0101110	-42.75dB
1101101	4.5dB	0101101	-43.5dB
1101100	3.75dB	0101100	-44.25dB
1101011	3dB	0101011	-45dB
1101010	2.25dB	0101010	-45.75dB
1101001	1.5dB	0101001	-46.5dB
1101000	0.75dB	0101000	-47.25dB
1100111	0dB	0100111	-48dB
1100110	-0.75dB	0100110	-48.75dB
1100101	-1.5dB	0100101	-49.5dB
1100100	-2.25dB	0100100	-50.25dB
1100011	-3dB	0100011	-51dB
1100010	-3.75dB	0100010	-51.75dB
1100001	-4.5dB	0100001	-52.5dB
1100000	-5.25dB	0100000	-53.25dB
1011111	-6dB	0011111	-54dB
1011110	-6.75dB	0011110	-54.75dB
1011101	-7.5dB	0011101	-55.5dB
1011100	-8.25dB	0011100	-56.25dB
1011011	-9dB	0011011	-57dB
1011010	-9.75dB	0011010	-57.75dB
1011001	-10.5dB	0011001	-58.5dB

						1011000	-11.25dB	0011000	-59.25dB
						1010111	-12dB	0010111	-60dB
						1010110	-12.75dB	0010110	-60.75dB
						1010101	-13.5dB	0010101	-61.5dB
						1010100	-14.25dB	0010100	-62.25dB
						1010011	-15dB	0010011	-63dB
						1010010	-15.75dB	0010010	-63.75dB
						1010001	-16.5dB	0010001	-64.5dB
						1010000	-17.25dB	0010000	-65.25dB
						1001111	-18dB	0001111	-66dB
						1001110	-18.75dB	0001110	-66.75dB
						1001101	-19.5dB	0001101	-67.5dB
						1001100	-20.25dB	0001100	-68.25dB
						1001011	-21dB	0001011	-69dB
						1001010	-21.75dB	0001010	-69.75dB
						1001001	-22.5dB	0001001	-70.5dB
						1001000	-23.25dB	0001000	-71.25dB
						1000111	-24dB	0000111	-72dB
						1000110	-24.75dB	0000110	-72.75dB
						1000101	-25.5dB	0000101	-73.5dB
						1000100	-26.25dB	0000100	-74.25dB
						1000011	-27dB	0000011	-75dB
						1000010	-27.75dB	0000010	-75.75dB
						1000001	-28.5dB	0000001	-76.5dB
						1000000	-29.25dB	0000000	digital mute

0xBB	R31	7			Reserved
		6			
		5			
		4			
		3			
		2:0			
0xBC	R32	7			Reserved
		6	MONO_DACLPEN	0	mono DAC low power enable 0: disable 1: enable
		5	MONO_DACOSR128	1	mono DAC over-sampling rate 0: 64X 1: 128X
		4	MONO_DAC_RSTN	1	mono DAC soft reset signal, active low
		3:2	MONO_DACLRC_SEL[1:0]	00	DAC LRC selection 00: from I2S LRCK 01: from PCM SYNC 10: 11: no LRCK
		1:0	MONO_DACCLK_SEL[1:0]	10	DAC 256fs clock selection 00: PLL1 out 01: EXTCLK

					10: MCLK_IN 11: no clock
0xBD	R33	7	ADC2_ERR	1	ADC2 ALC target error tolerance 1: +- 1.5db 0: +- 0.75db
		6	ADC2_NFEN	0	ADC2 notch filter enable signal 1: enable 0:disable
		5:0	ADC2_NFA0[13:8]	00_0000	ADC2 notch filter A0 coefficient MSBs
0xBE	R34	7:0	ADC2_NFA0[7:0]	0000_0000	ADC2 notch filter A0 coefficient LSBs
0xBF	R35	7	ADC2_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)
		6	ADC2_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1= enabled Application mode (2nd order, fc = HPFCUT)
		5:0	ADC2_NFA1[13:8]	00_0000	ADC2 notch filter A1 coefficient MSBs
0xC0	R36	7:0	ADC2_NFA1[7:0]	0000_0000	ADC2 notch filter A1 coefficient LSBs
0xC1	R37	7	ADC2_ALC_DSEL	0	ADC2 ALC data selection 0: after comb filter 1: after HPF filter
		6	ADC2_ALCMODE	0	ADC2 ALC mode selection 0：ALC mode(Normal Operation) 1: Limiter mode
		5	ADC2_ALCSEL	0	ADC2 ALC function enable 1: Enable 0: Disable
		4	ADC2_NG_EN	0	ADC2 Noise Gate enable signal 1: Enable 0: Disable
		3:0	ADC2_NG[3:0]	0111	ADC2 noise floor level 1111 -84dB 0111 -60 dB 1110 -81 dB 0110 -57 dB 1101 -78 dB 0101 -54 dB 1100 -75 dB 0100 -51 dB 1011 -72 dB 0011 -48 dB 1010 -69 dB 0010 -45 dB 1001 -66 dB 0001 -42 dB 1000 -63 dB 0000 -39 dB
0xC2	R38	7:5	ADC2_HPFCUT [2:0]	000	Application mode cut-off frequency.(Fs=48KHz) 000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz
		4:0	ADC2_TARGET [4:0]	00011	ADC2 ALC target level 11111 -48dB 01111 -24dB 11110 -46.5dB 01110 -22.5dB 11101 -45dB 01101 -21dB

					11100	-43.5dB	01100	-19.5dB	
					11011	-42dB	01011	-18dB	
					11010	-40.5dB	01010	-16.5dB	
					11001	-39dB	01001	-15dB	
					11000	-37.5dB	01000	-13.5dB	
					10111	-36dB	00111	-12dB	
					10110	-34.5dB	00110	-10.5dB	
					10101	-33dB	00101	-9dB	
					10100	-31.5dB	00100	-7.5dB	
					10011	-30dB	00011	-6dB	
					10010	-28.5dB	00010	-4.5dB	
					10001	-27dB	00001	-3dB	
					10000	-25.5dB	00000	-1.5dB	
0xC3	R39	7	ADC2MU	1	ADC2 mute signal 1: mute 0: un-mute				
		6:0	ADC2_DIG_VOL [6:0]	1100111 (default 0db)	ADC2 digital gain				
					1111111	18dB	0111111	-30dB	
					1111110	17.25dB	0111110	-30.75dB	
					1111101	16.5dB	0111101	-31.5dB	
					1111100	15.75dB	0111100	-32.25dB	
					1111011	15dB	0111011	-33dB	
					1111010	14.25dB	0111010	-33.75dB	
					1111001	13.5dB	0111001	-34.5dB	
					1111000	12.75dB	0111000	-35.25dB	
					1110111	12dB	0110111	-36dB	
					1110110	11.25dB	0110110	-36.75dB	
					1110101	10.5dB	0110101	-37.5dB	
					1110100	9.75dB	0110100	-38.25dB	
					1110011	9dB	0110011	-39dB	
					1110010	8.25dB	0110010	-39.75dB	
					1110001	7.5dB	0110001	-40.5dB	
					1110000	6.75dB	0110000	-41.25dB	
					1101111	6dB	0101111	-42dB	
					1101110	5.25dB	0101110	-42.75dB	
					1101101	4.5dB	0101101	-43.5dB	
					1101100	3.75dB	0101100	-44.25dB	
					1101011	3dB	0101011	-45dB	
					1101010	2.25dB	0101010	-45.75dB	
					1101001	1.5dB	0101001	-46.5dB	
					1101000	0.75dB	0101000	-47.25dB	
					1100111	0dB	0100111	-48dB	
					1100110	-0.75dB	0100110	-48.75dB	
					1100101	-1.5dB	0100101	-49.5dB	

					1100100	-2.25dB	0100100	-50.25dB
					1100011	-3dB	0100011	-51dB
					1100010	-3.75dB	0100010	-51.75dB
					1100001	-4.5dB	0100001	-52.5dB
					1100000	-5.25dB	0100000	-53.25dB
					1011111	-6dB	0011111	-54dB
					1011110	-6.75dB	0011110	-54.75dB
					1011101	-7.5dB	0011101	-55.5dB
					1011100	-8.25dB	0011100	-56.25dB
					1011011	-9dB	0011011	-57dB
					1011010	-9.75dB	0011010	-57.75dB
					1011001	-10.5dB	0011001	-58.5dB
					1011000	-11.25dB	0011000	-59.25dB
					1010111	-12dB	0010111	-60dB
					1010110	-12.75dB	0010110	-60.75dB
					1010101	-13.5dB	0010101	-61.5dB
					1010100	-14.25dB	0010100	-62.25dB
					1010011	-15dB	0010011	-63dB
					1010010	-15.75dB	0010010	-63.75dB
					1010001	-16.5dB	0010001	-64.5dB
					1010000	-17.25dB	0010000	-65.25dB
					1001111	-18dB	0001111	-66dB
					1001110	-18.75dB	0001110	-66.75dB
					1001101	-19.5dB	0001101	-67.5dB
					1001100	-20.25dB	0001100	-68.25dB
					1001011	-21dB	0001011	-69dB
					1001010	-21.75dB	0001010	-69.75dB
					1001001	-22.5dB	0001001	-70.5dB
					1001000	-23.25dB	0001000	-71.25dB
					1000111	-24dB	0000111	-72dB
					1000110	-24.75dB	0000110	-72.75dB
					1000101	-25.5dB	0000101	-73.5dB
					1000100	-26.25dB	0000100	-74.25dB
					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute
0xC4	R40	7						
		6	MIC2_0_16_SEL	1	MIC2 1st PGA gain 0: 0dB; 1: 16dB (Default) （Note：total gain=1st PGA gain + 2nd PGA gain）			
		5:0	MIC2_PGA_LEVEL	000000（6db）	MIC2 2nd PGA gain			
					111111--101001	fix to 20dB		

					101000	20 dB		
					100111	19.25 dB	010011	4.25 dB
					100110	18.5 dB	010010	3.5 dB
					100101	17.75 dB	010001	2.75 dB
					100100	17 dB	010000	2 dB
					100011	16.25 dB	001111	1.25 dB
					100010	15.5 dB	001110	0.5 dB
					100001	14.75 dB	001101	-0.25 dB
					100000	14 dB	001100	-1 dB
					011111	13.25 dB	001011	-1.75 dB
					011110	12.5 dB	001010	-2.5 dB
					011101	11.75 dB	001001	-3.25 dB
					011100	11 dB	001000	-4 dB
					011011	10.25 dB	000111	-4.75 dB
					011010	9.5 dB	000110	-5.5 dB
					011001	8.75 dB	000101	-6.25 dB
					011000	8 dB	000100	-7 dB
					010111	7.25 dB	000011	-7.75 dB
					010110	6.5 dB	000010	-8.5 dB
					010101	5.75 dB	000001	-9.25 dB
					010100	5 dB	000000	-10 dB
0xC5	R41	7						
		6						
		5:0	ADC2_ALCMAX	101000	max PGA gain used in ADC2 ALC model Descritption similar with MIC2_PGA_LEVEL			
0xC6	R42	7						
		6						
		5:0	ADC2_ALCMIN	000000	min PGA gain used in ADC2 ALC model Descritption similar with MIC2_PGA_LEVEL			
0xC7	R43	7:4	ADC2_ALCDCY	0011	ADC2 decay time(Fs=48KHz) When ADC2_ALCMODE=0			
					1111	10.92s	0111	42.67ms
					1110	5.46s	0110	21.33ms
					1101	2.73s	0101	10.67ms
					1100	1.37s	0100	5.33ms
					1011	682.67ms	0011	2.67ms
					1010	341.33ms	0010	1.33ms
					1001	170.67ms	0001	666.7μs
					1000	85.33ms	0000	333.3μs
					When ADC2_ALCMODE =1			
					1111	2.73s	0111	10.67ms

					1110	1.37s	0110	5.33ms
					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs
					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.7μs
					1000	21.33ms	0000	83.3μs
		3:0	ADC2_ALCATK	0010	ADC2 attack time(Fs=48kHz) When ADC2_ALCMODE =0			
					1111	2.73s	0111	10.67ms
					1110	1.37s	0110	5.33ms
					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs
					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.6μs
					1000	21.33ms	0000	83.3μs
					When ADC2_ALCMODE =1			
					1111	682.67ms	0111	2.67ms
					1110	341.33ms	0110	1.33ms
					1101	170.67ms	0101	666.7μs
					1100	85.33ms	0100	333.3μs
					1011	42.67ms	0011	166.6μs
					1010	21.33ms	0010	83.3μs
					1001	10.67ms	0001	41.7μs
					1000	5.33ms	0000	20.8μs
0xC8	R44							
		3:0	ADC2_ALCHLD	0000	ADC2 hold time(Fs=48kHz)			
					1111	43.69s	0111	170.67ms
					1110	21.85s	0110	85.33ms
					1101	10.92s	0101	42.67ms
					1100	5.46s	0100	21.33ms
					1011	2.73s	0011	10.67ms
					1010	1.37s	0010	5.33ms
					1001	682.67ms	0001	2.67ms
					1000	341.33ms	0000	2.67ms
0xC9	R45	7						
		6	ADC2LPEN	0	ADC2 low power enable 1: ADC2 clocks are turned off automatically when ADC2 is disabled 0: ADC2 clocks are not turned off automatically			

		5	ADC2OSR128	1	ADC2 over-sampling rate 0: 64X 1: 128X
		4	ADC2_RSTN	1	ADC2 soft reset signal, active low
		3:2	ADC2LRC_SEL[1:0]	00	ADC2 LRC selection 00: from I2S LRCK 01: from PCM SYNC 10,11: no LRCK
		1:0	ADC2CLK_SEL[1:0]	10	ADC2 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
0xCA	R46	7:5	DAC_SEL_L[2:0]	111	DAC left channel data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: 101: 110: 111: Reserved as Zero
		4:2	DAC_SEL_R[2:0]	111	DAC right channel data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: 101: 110: 111: Reserved as Zero
		1	LDACMU	1	DAC left channel mute signal 1: mute 0: un-mute
		0	RDACMU	1	DAC right channel mute signal 1: mute 0: un-mute
0xCB	R47	7	SOFTMUTE_EN	1	DAC soft mute function enable signal 1: enable 0: disable
		6:5	ST_SEL_L[1:0]	00	DAC left channel side-tone data selection 00: ADC1 output 01: ADC2 output 10, 11: Reserved
		4:0	STVOL_L[4:0]	00000	DAC left channel side-tone gain

11111	0dB	01111	-16 dB
11110	-1 dB	01110	-17 dB
11101	-2 dB	01101	-18 dB
11100	-3 dB	01100	-19 dB
11011	-4 dB	01011	-20 dB
11010	-5 dB	01010	-21 dB
11001	-6 dB	01001	-22 dB
11000	-7 dB	01000	-23 dB
10111	-8 dB	00111	-24 dB
10110	-9 dB	00110	-25 dB
10101	-10 dB	00101	-26 dB

					10100	-11 dB	00100	-27 dB
					10011	-12 dB	00011	-28 dB
					10010	-13 dB	00010	-29 dB
					10001	-14 dB	00001	-30 dB
					10000	-15 dB	00000	mute
0xCC	R48	7		0	Reserved			
		6:5	ST_SEL_R[1:0]	00	DAC right channel side-tone data selection 00: ADC1 output 01: ADC2 output 10: 11: Reserved			
		4:0	STVOL_R[4:0]	00000	DAC right channel side-tone gain			
					11111	0dB	01111	-16 dB
					11110	-1 dB	01110	-17 dB
					11101	-2 dB	01101	-18 dB
					11100	-3 dB	01100	-19 dB
					11011	-4 dB	01011	-20 dB
					11010	-5 dB	01010	-21 dB
					11001	-6 dB	01001	-22 dB
					11000	-7 dB	01000	-23 dB
					10111	-8 dB	00111	-24 dB
					10110	-9 dB	00110	-25 dB
					10101	-10 dB	00101	-26 dB
					10100	-11 dB	00100	-27 dB
					10011	-12 dB	00011	-28 dB
					10010	-13 dB	00010	-29 dB
					10001	-14 dB	00001	-30 dB
					10000	-15 dB	00000	mute
0xCD	R49	7		0	Reserved			
		6:0	DAC_LEVEL_L [6:0]	1100111 (default 0dB)	DAC left channel digital gain			
					1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB

						1110010	8.25dB	0110010	-39.75dB
						1110001	7.5dB	0110001	-40.5dB
						1110000	6.75dB	0110000	-41.25dB
						1101111	6dB	0101111	-42dB
						1101110	5.25dB	0101110	-42.75dB
						1101101	4.5dB	0101101	-43.5dB
						1101100	3.75dB	0101100	-44.25dB
						1101011	3dB	0101011	-45dB
						1101010	2.25dB	0101010	-45.75dB
						1101001	1.5dB	0101001	-46.5dB
						1101000	0.75dB	0101000	-47.25dB
						1100111	0dB	0100111	-48dB
						1100110	-0.75dB	0100110	-48.75dB
						1100101	-1.5dB	0100101	-49.5dB
						1100100	-2.25dB	0100100	-50.25dB
						1100011	-3dB	0100011	-51dB
						1100010	-3.75dB	0100010	-51.75dB
						1100001	-4.5dB	0100001	-52.5dB
						1100000	-5.25dB	0100000	-53.25dB
						1011111	-6dB	0011111	-54dB
						1011110	-6.75dB	0011110	-54.75dB
						1011101	-7.5dB	0011101	-55.5dB
						1011100	-8.25dB	0011100	-56.25dB
						1011011	-9dB	0011011	-57dB
						1011010	-9.75dB	0011010	-57.75dB
						1011001	-10.5dB	0011001	-58.5dB
						1011000	-11.25dB	0011000	-59.25dB
						1010111	-12dB	0010111	-60dB
						1010110	-12.75dB	0010110	-60.75dB
						1010101	-13.5dB	0010101	-61.5dB
						1010100	-14.25dB	0010100	-62.25dB
						1010011	-15dB	0010011	-63dB
						1010010	-15.75dB	0010010	-63.75dB
						1010001	-16.5dB	0010001	-64.5dB
						1010000	-17.25dB	0010000	-65.25dB
						1001111	-18dB	0001111	-66dB
						1001110	-18.75dB	0001110	-66.75dB
						1001101	-19.5dB	0001101	-67.5dB
						1001100	-20.25dB	0001100	-68.25dB
						1001011	-21dB	0001011	-69dB
						1001010	-21.75dB	0001010	-69.75dB
						1001001	-22.5dB	0001001	-70.5dB
						1001000	-23.25dB	0001000	-71.25dB

					1000111	-24dB	0000111	-72dB
					1000110	-24.75dB	0000110	-72.75dB
					1000101	-25.5dB	0000101	-73.5dB
					1000100	-26.25dB	0000100	-74.25dB
					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute
0xCE	R	0	7		0	Reserved		
			6:0	DAC_LEVEL_R [6:0]	1100111 (default 0dB)	DAC right channel digital gain		
					1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB
					1110010	8.25dB	0110010	-39.75dB
					1110001	7.5dB	0110001	-40.5dB
					1110000	6.75dB	0110000	-41.25dB
					1101111	6dB	0101111	-42dB
					1101110	5.25dB	0101110	-42.75dB
					1101101	4.5dB	0101101	-43.5dB
					1101100	3.75dB	0101100	-44.25dB
					1101011	3dB	0101011	-45dB
					1101010	2.25dB	0101010	-45.75dB
					1101001	1.5dB	0101001	-46.5dB
					1101000	0.75dB	0101000	-47.25dB
					1100111	0dB	0100111	-48dB
					1100110	-0.75dB	0100110	-48.75dB
					1100101	-1.5dB	0100101	-49.5dB
					1100100	-2.25dB	0100100	-50.25dB
					1100011	-3dB	0100011	-51dB
					1100010	-3.75dB	0100010	-51.75dB
					1100001	-4.5dB	0100001	-52.5dB
					1100000	-5.25dB	0100000	-53.25dB

					1011111	-6dB	0011111	-54dB
					1011110	-6.75dB	0011110	-54.75dB
					1011101	-7.5dB	0011101	-55.5dB
					1011100	-8.25dB	0011100	-56.25dB
					1011011	-9dB	0011011	-57dB
					1011010	-9.75dB	0011010	-57.75dB
					1011001	-10.5dB	0011001	-58.5dB
					1011000	-11.25dB	0011000	-59.25dB
					1010111	-12dB	0010111	-60dB
					1010110	-12.75dB	0010110	-60.75dB
					1010101	-13.5dB	0010101	-61.5dB
					1010100	-14.25dB	0010100	-62.25dB
					1010011	-15dB	0010011	-63dB
					1010010	-15.75dB	0010010	-63.75dB
					1010001	-16.5dB	0010001	-64.5dB
					1010000	-17.25dB	0010000	-65.25dB
					1001111	-18dB	0001111	-66dB
					1001110	-18.75dB	0001110	-66.75dB
					1001101	-19.5dB	0001101	-67.5dB
					1001100	-20.25dB	0001100	-68.25dB
					1001011	-21dB	0001011	-69dB
					1001010	-21.75dB	0001010	-69.75dB
					1001001	-22.5dB	0001001	-70.5dB
					1001000	-23.25dB	0001000	-71.25dB
					1000111	-24dB	0000111	-72dB
					1000110	-24.75dB	0000110	-72.75dB
					1000101	-25.5dB	0000101	-73.5dB
					1000100	-26.25dB	0000100	-74.25dB
					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute

0xCF	R51	7			Reserved
		6	DAC_DWAEN	0	DAC DWA function enable signal 1: enable 0: disable
		5	DAC_SD_NZ	0	DAC SDM no-zero input signal(for test) 1: no-zero 0: normal
		4	DAC_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)
		3	DAC_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1= enabled Application mode (2nd order, fc = HPFCUT)

		2:0	DAC_HPFCUT[2:0]	000	Application mode cut-off frequency.(Fs=48KHz) 000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz
0xD0	R52	7	DAC_ALCMODE	0	ALC mode selection 0：ALC mode(Normal Operation) 1: Limiter mode
		6:5	DAC_ALCSEL[1:0]	00	DAC ALC function select 00: ALC disabled 01: Right channel ALC enabled 10: left channel ALC enabled 11: both channels ALC enabled
		4	DAC_NG_EN	0	DAC Noise Gate enable signal 1: Enable 0: Disable
		3:0	DAC_NG[3:0]	0111	DAC noise floor level

1111	-84dB	0111	-60 dB
1110	-81 dB	0110	-57 dB
1101	-78 dB	0101	-54 dB
1100	-75 dB	0100	-51 dB
1011	-72 dB	0011	-48 dB
1010	-69 dB	0010	-45 dB
1001	-66 dB	0001	-42 dB
1000	-63 dB	0000	-39 dB

0xD1	R53	7			
		6			
		5	DAC_ERR	1	DAC ALC target error tolerance 1: +- 1.5db 0: +- 0.75db
		4:0	DAC_TARGET[4:0]	00011 (-6db)	DAC ALC target level

11111	-48dB	01111	-24dB
11110	-46.5dB	01110	-22.5dB
11101	-45dB	01101	-21dB
11100	-43.5dB	01100	-19.5dB
11011	-42dB	01011	-18dB
11010	-40.5dB	01010	-16.5dB
11001	-39dB	01001	-15dB
11000	-37.5dB	01000	-13.5dB
10111	-36dB	00111	-12dB
10110	-34.5dB	00110	-10.5dB
10101	-33dB	00101	-9dB
10100	-31.5dB	00100	-7.5dB
10011	-30dB	00011	-6dB
10010	-28.5dB	00010	-4.5dB

					10001	-27dB	00001	-3dB	
					10000	-25.5dB	00000	-1.5dB	
0xD2	R54	7							
		6:0	DAC_ALCMAX_L	1111111	The left channel max digital gain used in ALC model Description similar with DAC_LEVEL_L				
0xD3	R55	7							
		6:0	DAC_ALCMIN_L	0000000	The left channel min digital gain used in ALC model Description similar with DAC_LEVEL_L				
0xD4	R56	7							
		6:0	DAC_ALCMAX_R	1111111	The right channel max digital gain used in ALC model Description similar with DAC_LEVEL_R				
0xD5	R57	7							
		6:0	DAC_ALCMIN_R	0000000	The right channel min digital gain used in ALC model Description similar with DAC_LEVEL_R				
0xD6	R58	7:4	DAC_ALCDCY	0011	DAC decay time(Fs=48KHz) When DAC_ALCMODE=0				
					1111	10.92s	0111	42.67ms	
					1110	5.46s	0110	21.33ms	
					1101	2.73s	0101	10.67ms	
					1100	1.37s	0100	5.33ms	
					1011	682.67ms	0011	2.67ms	
					1010	341.33ms	0010	1.33ms	
					1001	170.67ms	0001	666.7μs	
					1000	85.33ms	0000	333.3μs	
					When DAC_ALCMODE =1				
					1111	2.73s	0111	10.67ms	
					1110	1.37s	0110	5.33ms	
					1101	682.67ms	0101	2.67ms	
					1100	341.33ms	0100	1.33ms	
					1011	170.67ms	0011	666.7μs	
					1010	85.33ms	0010	333.3μs	
					1001	42.67ms	0001	166.7μs	
					1000	21.33ms	0000	83.3μs	
		3:0	DAC_ALCATK	0010	DAC attack time(Fs=48kHz) When DAC_ALCMODE =0				
					1111	2.73s	0111	10.67ms	
					1110	1.37s	0110	5.33ms	
					1101	682.67ms	0101	2.67ms	
					1100	341.33ms	0100	1.33ms	
					1011	170.67ms	0011	666.7μs	
					1010	85.33ms	0010	333.3μs	

					1001	42.67ms	0001	166.6μs
					1000	21.33ms	0000	83.3μs
					When DAC_ALCMODE =1			
					1111	682.67ms	0111	2.67ms
					1110	341.33ms	0110	1.33ms
					1101	170.67ms	0101	666.7μs
					1100	85.33ms	0100	333.3μs
					1011	42.67ms	0011	166.6μs
					1010	21.33ms	0010	83.3μs
					1001	10.67ms	0001	41.7μs
					1000	5.33ms	0000	20.8μs
0xD7	R59							
		3:0	DAC_ALCHLD	0000	DAC hold time(Fs=48kHz)			
					1111	43.69s	0111	170.67ms
					1110	21.85s	0110	85.33ms
					1101	10.92s	0101	42.67ms
					1100	5.46s	0100	21.33ms
					1011	2.73s	0011	10.67ms
					1010	1.37s	0010	5.33ms
					1001	682.67ms	0001	2.67ms
					1000	341.33ms	0000	2.67ms
0xD8	R60	7						
		6:2	EQ1_GAIN	00000	EQ1 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ1_FQ	10	Sub-bass shelving filter's cut-off frequency 00: 60Hz			

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td colspan="4">01: 80
10: 100
11: 120</td></tr>
<tr><td>0xD9</td><td>R61</td><td>7</td><td>EQ2_Q</td><td>0</td><td colspan="4">EQ2 bandwidth
0: 2/3 Octave
1: 4/3 Octave</td></tr>
<tr><td></td><td></td><td>6:2</td><td>EQ2_GAIN</td><td>00000</td><td colspan="4">EQ2 gain</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11111</td><td>15dB</td><td>01111</td><td>-1 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11110</td><td>14 dB</td><td>01110</td><td>-2 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11101</td><td>13 dB</td><td>01101</td><td>-3 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11100</td><td>12 dB</td><td>01100</td><td>-4 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11011</td><td>11 dB</td><td>01011</td><td>-5 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11010</td><td>10 dB</td><td>01010</td><td>-6 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11001</td><td>9 dB</td><td>01001</td><td>-7 dB</td></tr>
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<tr><td></td><td></td><td></td><td></td><td></td><td>10111</td><td>7 dB</td><td>00111</td><td>-9 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10110</td><td>6 dB</td><td>00110</td><td>-10 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10101</td><td>5 dB</td><td>00101</td><td>-11 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10100</td><td>4 dB</td><td>00100</td><td>-12 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10011</td><td>3 dB</td><td>00011</td><td>-13 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10010</td><td>2 dB</td><td>00010</td><td>-14 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10001</td><td>1 dB</td><td>00001</td><td>-15 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10000</td><td>0 dB</td><td>00000</td><td>off (0db)</td></tr>
<tr><td></td><td></td><td>1:0</td><td>EQ2_FQ</td><td>10</td><td colspan="4">bass peak filter’s center frequency
00: 150Hz
01: 200
10: 150
11: 300</td></tr>
<tr><td>0xDA</td><td>R62</td><td>7</td><td>EQ3_Q</td><td>0</td><td colspan="4">EQ3 bandwidth
0: 2/3 Octave
1: 4/3 Octave</td></tr>
<tr><td></td><td></td><td>6:2</td><td>EQ3_GAIN</td><td>00000</td><td colspan="4">EQ3 gain</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11111</td><td>15dB</td><td>01111</td><td>-1 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11110</td><td>14 dB</td><td>01110</td><td>-2 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11101</td><td>13 dB</td><td>01101</td><td>-3 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11100</td><td>12 dB</td><td>01100</td><td>-4 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11011</td><td>11 dB</td><td>01011</td><td>-5 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11010</td><td>10 dB</td><td>01010</td><td>-6 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11001</td><td>9 dB</td><td>01001</td><td>-7 dB</td></tr>
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<tr><td></td><td></td><td></td><td></td><td></td><td>10110</td><td>6 dB</td><td>00110</td><td>-10 dB</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10101</td><td>5 dB</td><td>00101</td><td>-11 dB</td></tr>
</table>

					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ3_FQ	10	mid peak filter's center frequency 00: 600Hz 01: 800 10: 1000 11: 1200			
0xDB	R63	7	EQ4_Q	0	EQ4 bandwidth 0: 2/3 Octave 1: 4/3 Octave			
		6:2	EQ4_GAIN	00000	EQ4 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ4_FQ	10	treble peak filter's center frequency 00: 2000Hz 01: 2700 10: 3400 11: 4100			
0xDC	R64			0	Reserved			
		6:2	EQ5_GAIN	00000	EQ5 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB

					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ5_FQ	10	Presence shelving filter's cut-off frequency 00: 7000Hz 01: 9000 10: 11000 11: 20000			
0xDD	R65	7:0	DAC_OFFSET [15:8]	0000_0000	Added DAC offset MSBs (for testing)			
0xDE	R66	7:0	DAC_OFFSSET [7:0]	0000_0000	DAC offset LSBs			
0xDF	R67	7:5		000	Reserved			
		4	DAC_DITH_BYPASS	1	DAC SDM dither function bypass 1: bypass 0:function used			
		3:2	DAC_DITH_TYPE [1:0]	00	DAC SDM dither type selection (for testing)			
		1:0	DAC_DITH_POW [25:24]	00	DAC SDM dither power (for testing)			
0xE0	R68	7:0	DAC_DITH_POW [23:16]	0000_0000	DAC SDM dither power (for testing)			
0xE1	R69	7:0	DAC_DITH_POW [15:8]	0000_0000	DAC SDM dither power (for testing)			
0xE2	R70	7:0	DAC_DITH_POW [7:0]	0000_0000	DAC SDM dither power (for testing)			
0xE3	R71	7		0	Reserved			
		6	DACLPEN	0	DAC low power enable 0: disable 1: enable			
		5	DACOSR128	1	DAC over-sampling rate 0: 64X 1: 128X			
		4	DAC_RSTN	1	DAC soft reset signal, active low			
		3:2	DACLRC_SEL[1:0]	00	DAC LRC selection 00: from I2S LRCK 01: from PCM SYNC 10: 11: no LRCK			
		1:0	DACCLK_SEL[1:0]	10	DAC 256fs clock selection			

					00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
0xE4	R72	7		000	Reserved
		6	MONO_DAC_DWAEN	0	mono DAC DWA function enable signal 1: enable 0: disable
		5	MONO_DAC_SD_NZ	0	mono DAC SDM no-zero input signal(for test) 1: no-zero 0: normal
		4	MONO_DAC_DITH_BY PASS	1	DAC SDM dither function bypass 1: bypass 0:function used
		3:2	MONO_DAC_DITH_TY PE [1:0]	00	Mono DAC SDM dither type selection (for testing)
		1:0	MONO_DAC_DITH_PO W [25:24]	00	Mono DAC SDM dither power (for testing)
0xE5	R73		MONO_DAC_DITH_PO W [23:16]	0000_0000	Mono DAC SDM dither power (for testing)
0xE6	R74		MONO_DAC_DITH_PO W [15:8]	0000_0000	Mono DAC SDM dither power (for testing)
0xE7	R75		MONO_DAC_DITH_PO W [7:0]	0000_0000	Mono DAC SDM dither power (for testing)
0xE8	R76	7:4			
		3:0	PLL_INT_P[3:0]	0110	Integer part of PLL (Default Case: 12M input, 12.288M output)
0xE9	R77	7:0	PLL_FRC_P[7:0]	11101001	Fractional (K) part of PLL input/output frequency ratio (Default Case: 12M input, 12.288M output)
0xEA	R78	7:0	PLL_FRC_P[15:8]	00100110	
0xEB	R79	7:0	PLL_FRC_P[23:16]	00110001	
0Xec	R80	7:5	CP_P[2:0]	100	PLL internal Charge pump current selection bits 000：20uA 001：25uA 010：30uA 011：35uA 100：40uA（default） 101：45uA 110：50uA 111：55uA
		4	PLL_FRCEN_P	0	Fractional N enable; high active.
		3	RESETN_P	0	PLL1 Reset; low active.
		2:0	POST_DIV1[2:0]	000	Post divider selection: POST_DIV[2:0] / DIV 000 / 2 001 / 4 010 / 8 011 / 16 100 / 32

					101	64
					110	64
					111	64
0xED	R61	7		0		
		6	PRESCALE	0	0: Divide by 1; 1:Divide by 2	
		5	PLLEN	0	PLL1 enable; high active	
		4	TESTVCOB_P	1	0:VCO function test, Vctrl=VDD/2; 1: normal work	
		3:2	RLPF_P[1:0]	10	Low pass filter resister selection	
		1:0	RVI_P[1:0]	01	V to I converter resister selection	
0xEE	R62	7				
		6				
		5	AD1IN5SEL	0	ADC1 select DAC MONO channel signal 0= no select 1= select	
		4	AD1IN4SEL	0	ADC1 select DAC L channel signal 0= no select 1= select	
		3	AD1IN3SEL	0	ADC1 select DAC R channel signal 0= no select 1= select	
		2	AD1IN2SEL	0	ADC1 select MainMIC2—HPMIC PGA OUT channel signal 0= no select 1= select	
		1	AD1IN1SEL	0	ADC1 select MainMIC1 PGA OUTsignal 0= no select 1= select	
		0	AD1MUXMU	1	ADC1 MUX mute signal 0: MUX unmute; 1: MUX mute	
0xEF	R63	7				
		6				
		5	AD2IN5SEL	0	ADC2 select DAC MONO channel signal 0= no select 1= select	
		4	AD2IN4SEL	0	ADC2 select DAC L channel signal 0= no select 1= select	
		3	AD2IN3SEL	0	ADC2 select DAC R channel signal 0= no select 1= select	
		2	AD2IN2SEL	0	ADC2 select MainMIC2&HPMIC PGA OUT channel signal 0= no select 1= select	
		1	AD2IN1SEL	0	ADC2 select MainMIC1 PGA OUTsignal 0= no select 1= select	
		0	AD2MUXMU	1	ADC2 MUX mute signal 0: MUX unmute; 1: MUX mute	
0xF0	R64	7:5	ICTR_DAC[2:0]	011	000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA	
		4:2	VMICSEL[2:0]	101	VMICBIAS Voltage Select different VMICBIAS corresponding different VMID	

						VMID_SEL[2:0]	VMID(V)	VMICSEL[2:0]	VMICBIAS(V)
						111	1.39	000	2.45
						110	1.43	001	2.534
						101	1.49	010	2.623
						100	1.54	011	2.615
						011	1.6	100	2.614
						010	1.66(default)	101	2.62(default)
						001	1.73	110	2.634
						000	1.8	111	2.656
			1	MICBEN	0	Micbias enable; 0 = disable 1 = enable			
			0	MICBSWEN	0	Micbias switch enable 0 = disable 1 = enable			
0xF1	R85		7	MICSTSEL	0	Sidetone select: 0: Select MIC1 1: Select MIC2 or HPMIC			
			6	M_MIC1N2INN	1	Connect MIC1N to input PGA negative terminal.(Main Mic1) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
			5	M_MIC1P2INP	0	Connect input PGA amplifier positive terminal to MIC1P or VREF. (Main Mic1) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
			4	HP_MICN2INN	1	Connect MICN to input PGA negative terminal.(HP Mic) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
			3	HP_MICP2INP	0	Connect input PGA amplifier positive terminal to MICP or VREF. (HP Mic) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
			2	MIC2HPSEL	0	MainMIC2 —HPMIC PGA select input signal 0: Select Main MIC2; 1: Select HP MIC			
			1	M_MIC2N2INN	1	Connect MIC2N to input PGA negative terminal.(Main Mic2) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
			0	M_MIC2P2INP	0	Connect input PGA amplifier positive terminal to MIC2P or VREF. (Main Mic2) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
0xF2	R86		7						
			6	AUXMIXEN	0	AUX Mixer enable signal 1: Enable；0：Disable			
			5	AUXMIXMU	1	AUX Mixer Mute signal: 0: Un-Mute; 1：Mute			
			4	LINLSEL_AUX	0	AUX Select Left Line PGA control signal : 0:unselect; 1: Select			
			3	LINRSEL_AUX	0	AUX Select Right Line PGA control signal : 0:unselect; 1: Select			
			2	DACMONOSEL_AUX	0	AUX Select mono DAC control signal : 0:unselect 1:select			
			1	DACLSEL_AUX	0	AUX Select Left DAC control signal: 0:unselect; 1: Select			
			0	DACRSEL_AUX	0	AUX Select Right DAC control signal: 0:unselect; 1: Select			
0xF3	R87		7	LDOEN	0	LDO Enable signal 1: LDO Enable; 0: Disable			

		6	SPKMIXEN	0	SPK Mixer Enable signal : 1: Enable；0：Disable
		5	SPKMIXMU	1	SPK Mixer Mute signal : 0: Un-Mute; 1:Mute
		4	LINLSEL_SPK	0	SPK Select Left Line PGA: 0:unselect; 1: Select
		3	LINRSEL_SPK	0	SPK Select Right Line PGA: 0:unselect; 1: Select
		2	DACMONOSEL_SPK	0	SPK Select mono DAC: 0:unselect 1:select
		1	DACLSEL_SPK	0	SPK Select Left DAC: 0:unselect; 1: Select
		0	DACRSEL_SPK	0	SPK Select Right DAC: 0:unselect; 1: Select
0xF4	R88	7:5	VMID_SEL[2:0]	010	VMID Voltage Select signal 000 1.804V； 001 1.73V 010 1.661V(DEFAULT)； 011 1.598V 100 1.539V； 101 1.485V 110 1.434V； 111 1.387V
		4:1	LDOVSEL[3:0]	0100	LDO Voltage Select signal: VSEL[3:0] VLDO 0000 3.7 0001 3.6 0010 3.5 0011 3.4 0100 3.3(DEFAULT) 0101 3.2 0110 3.1 0111 3.0 1000 2.9 1001 2.8 1010 2.7 1111 1.8(LDO OUTPUT 1.8V)
		0	LDO_SW	0	LDO work mode select 0: LDO Normal work; 1: Switch mode
0xF5	R89	7			
		6	HPLMIXEN	0	HP L channel Mixer Enable : 1 : Enable 0 : Disable
		5	HPLMIXMU	1	HP L channel Mixer Mute. 0: Un-Mute; 1：Mute
		4	LINLSEL_HPL	0	HP L channel Select Left Line PGA: 0:unselect; 1: Select
		3	DACMONOSEL_HPL	0	HP L channel Select mono DAC: 0:unselect 1:select
		2	DACLSEL_HPL	0	HP L channel Select Left DAC: 0:unselect; 1: Select
		1	DACRSEL_HPL	0	HP L channel Select Right DAC: 0:unselect; 1: Select
		0	SDTSEL_HPL	0	HP L channel Select Side Tone: 0:unselect; 1: Select
0xF6	R90	7			
		6	HPRMIXEN	0	HP R channel Mixer Enable. 1: Enable；0：Disable
		5	HPRMIXMU	1	HP R Mixer Mute. 0: Un-Mute; 1：Mute
		4	LINRSEL_HPR	0	HP R Select Right Line PGA: 0:unselect; 1: Select
		3	DACMONOSEL_HPR	0	HP R Select mono DAC: 0:unselect 1:select

		2	DACLSEL_HPR	0	HP R Select Left DAC: 0:unselect; 1: Select
		1	DACRSEL_HPR	0	HP R Select Right DAC: 0:unselect; 1: Select
		0	SDTSEL_HPR		HP R Select Side Tone: 0:unselect; 1: Select
0xF7	R91	7	RECMIXEN	0	REC Mixer Enable. 1: Enable；0：Disable
		6	RECMIXMU	1	REC Mixer Mute. 0: Un-Mute; 1：Mute
		5	DACMONOSEL_REC	0	REC Select mono DAC: 0:unselect 1:select
		4	DACLSEL_REC	0	REC Select Left DAC: 0:unselect; 1: Select
		3	DACRSEL_REC	0	REC Select right DAC: 0:unselect; 1: Select
		2	SDTSEL_REC	0	REC Select Side Tone: 0:unselect; 1: Select
		1:0	SLOWCLK_SEL[1:0]	00	Slow Clock selection signal 00: 2^21 MCLK 01: 2^20MCLK 10：2^19 MCLK 11: 2^18MCLK
0xF8	R92	7:6	OSCIB_OPT[1:0]	11	ClassG internal OSC Current Control:00:3.75u；01:8.75u; 10:1.25u; 11:6.25uA
		5:4	OSCF_SEL[1:0]	01	ClassG internal OSC Frequency: 00:2M; 01:1M; 10:4M; 11:0.5MHz
		3	NVEN	0	Charge pump CPVSS Power down. 1: Power on. 0: Power down.
		2	VREFEN_CG	0	CLASS G internal VREF Power down 1: Power up. 0: Power down.
		1	OSC_EN	0	ClassG internal OSC Power Down: 1:Enable; 0: Power Down
		0	CG_CK_SEL	0	0: from internal osc, 1: no clock
0xF9	R93	7	CD_CK_SEL	0	0: internal OSC; 1: no clock
		6	CD_ENB_TMNT	0	Time counter of CTRL_LOGIC enable control 0: Enable the time counter. 1: Disable the time counter
		5	CD_TSAT	0	Time counter Start Time control 0: Fast start(about 5ms); 1: Slow start(about 40ms)
		4	LOWPOWER	0	ClassD power consumption control 0: Normal work; 1: Low power mode
		3	PD_OCT	1	OCT detect （over current protect）start up control. 0: Start up; 1: Stop
		2	PD3_CD	1	Function blocks of Class-D （other than op、PWM_osc、bias）power down control 0: Normal work. 1: Power-down
		1	PD2_CD	1	Function blocks Class-D（op、PWM_osc） power down control 0: Normal work. 1: Power-down
		0	PD_CD	1	Class-D（bias） power down control 0: Normal work. 1: Power-down
0xFA	R94	7:6	CD_IBSRMP[1:0]	00	ClassD（Speaker）internal OSC_RAMP bias current select 00 :10U; 01: 9U; 10: 11U; 11: 10U
		5:3	CLGAIN[2:0]	000	Close-loop gain control 000 :6dB; 001: 6.90dB; 010: 6.60 dB; 011: 6.32 dB 100: 5.71 dB; 101: 5.44 dB; 110: 5.15 dB; 111: 4.91 dB
		2:1	CD_ALC[1:0]	00	The trigger point of output signal clipping control 00: n=4; 01: n=2; 10: n=8; 11: n=16
		0	CD_ENB_ALC	0	Clipping ALC function enable control 0: normal work; 1: disable
0xFB	R95	7:6	NOVSEL[1:0]	01	ClassD Dead Time Control

					00:8ns; 01:9ns; 10:10.5ns; 11:13ns;
		5	TSSET	1	ClassD Temp-sensor threshold 0: 134C（protect）/115C（release）; 1: 112C（protect）/92C（release）;
		4	-		
		3	CD_ENB_GLITCH	0	Deglitch function enable control 0: Enable deglitch function; 1: Disable deglitch function
		2	CD_ENB_OCT	0	OCT(Over current protection) function enable control 0: Enable OCT function; 1: Disable OCT function
		1	CD_ENB_POP	0	De-pop function enable control 0: Enable De-pop function; 1: Disable De-pop function
		0	TS_EN	0	over temperature protect enable signal ; 0: Disable; 1: Enable
0xFC	R96	7	VBSPGAEN	0	Vref enable. 0 = disabled;1 = enabled
		6	IBSEN	0	Top Bias current enable signal . 0 = disabled;1 = enabled
		5	BGPEN	0	Vref output generator enable. 0 = disabled;1 = enabled
		4			
		3:1	IBS_SEL[2:0]	011	I-bias is default 5u and gradually increase from 3u to 7u. 000 7.05uA; 001 6.27uA 010 5.64uA; 011 5.13uA(DEFAULT) 100 4.7uA; 101 4.34uA 110 4.03uA; 111 3.76uA
		0	VREFEN	0	Headphone internal VREF BUFFER enable. 0 = disabled;1 = enabled
0xFD	R97	7			
		6			
		5			
		4			
		3	CD_ALC_OUT		CLASSD ALC IRQ SIGNAL; 1: CD ALC IRQ;0:No IRQ;
		2	CD_DTS		CLASSD OVER TEMPERATURE FLAG SIGNAL; 0:normal; 1:OVER TEMP IRQ;
		1	PLL_LD		PLL lock detector signal 1: PLL1 lock 0: PLL1 not lock
		0			
0xFE	R98	7			
		6:4	ICTR_ADC2	011	ADC2 Bias Current control signal: 000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA
		3	LDOSINKEN	1	Codec LDO fast discharge enable control signal: 0= LDO fast discharge disable 1= LDO fast discharge enable
		2:0	ICTR_ADC1	011	ADC1 Bias Current control signal: 000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA

12.3

Reg.Addr	BIT	Register Name	DEFAULT	DESCRIPTION

带格式的： 正文缩进, 正文（首行缩进两字）, 正文（首行缩进两字） Char, 正文（首行缩进两字） Char Char Char Char Char Char Char Char Char, 正文（首行缩进两字） Char Char, 正文（首行缩进两字） Char Char Char, 正文缩进1, 正文（首行缩进两字） Char1, 正文（首行缩进两字） Char Char Char Char Char Char Char Char Char Char1, 正文（首行缩进两字） Char Char1 Char, d

带格式表格

R0		7			
		6	MIC2PGAZCEN	0	MainMIC2 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
		5	MIC2PGAMU	1	MainMIC2 PGA Mute signal 0: Un-Mute; 1: Mute
		4	MIC2PGAEN	0	MainMIC2 PGA Enable signal 1: MIC2PGA Enable；0：MIC2PGA Power Down
		3			
		2	MIC1PGAZCEN	0	MainMIC1 PGA ZeroCross Enable signal 1: ZeroCross Enable; 0: ZeroCross Disable
		1	MIC1PGAMU	1	MainMIC1 PGA Mute signal 0: Un-Mute; 1: Mute
		0	MIC1PGAEN	0	MainMIC1 PGA Enable signal 1: MIC1PGA Enable；0：MIC1PGA Power Down
R1		7	DACREN	0	DAC Right Enable signal 0: Rch DAC disable; 1: Rch DAC enable.
		6	DACLEN	0	DAC Left Enable signal 0: Lch DAC disable; 1: Lch DAC enable.
		5	DACMONOEN	0	DAC MONO Enable signal 0: mono DAC disable 1: mono DAC enable
		4	ADC2EN	0	ADC2 Enable signal 0: ADC2 disable; 1: ADC2 enable.
		3	ADC1EN	0	ADC1 Enable signal 0: ADC1 disable; 1: ADC1 enable.
		2	LINREN	0	Line Right Enable signal 1: Right Line PGA Enable；0：Power Down
		1	LINLEN	0	Line Left Enable signal 1: Left Line PGA Enable；0：Power Down
		0	SLOWCLK_EN	0	Slow clock enable signal 1: enable 0: disable
R2		7	LINLMU	1	Line Left PGA Mute signal 0: Un-Mute; 1: Mute
		6	LINLZCEN	0	Line Left PGA ZeroCross Enable signal 1: Enable；0：Disable
		5:0	LINLVOL[5:0]	011111	Line Left PGA Volume Control:

111111~101000	fix to 12dB		
100111	12dB	010011	-18 dB
100110	10.5 dB	010010	-19.5 dB
100101	9 dB	010001	-21 dB
100100	7.5 dB	010000	-22.5 dB
100011	6 dB	001111	-24 dB
100010	4.5 dB	001110	-25.5 dB

					100001	3 dB	001101	-27 dB	
					100000	1.5 dB	001100	-28.5 dB	
					011111	0dB dB	001011	-30 dB	
					011110	-1.5 dB	001010	-31.5 dB	
					011101	-3 dB	001001	-33 dB	
					011100	-4.5 dB	001000	-34.5 dB	
					011011	-6 dB	000111	-36 dB	
					011010	-7.5 dB	000110	-37.5 dB	
					011001	-9 dB	000101	-39 dB	
					011000	-10.5 dB	000100	-40.5 dB	
					010111	-12 dB	000011	-42 dB	
					010110	-13.5 dB	000010	-43.5 dB	
					010101	-15 dB	000001	-45 dB	
					010100	-16.5 dB	000000	-46.5 dB	
R3		7	LINRMU	1	Line Right PGA Mute signal: 0: Un-Mute; 1: Mute				
		6	LINRZCEN	0	Line Right PGA ZeroCross Enable signal 1: Enable; 0:Disable				
		5:0	LINRVOL[5:0]	011111	Line Right PGA Volume Control:				
					111111~101000	fix to 12dB			
					100111	12dB	010011	-18 dB	
					100110	10.5 dB	010010	-19.5 dB	
					100101	9 dB	010001	-21 dB	
					100100	7.5 dB	010000	-22.5 dB	
					100011	6 dB	001111	-24 dB	
					100010	4.5 dB	001110	-25.5 dB	
					100001	3 dB	001101	-27 dB	
					100000	1.5 dB	001100	-28.5 dB	
					011111	0dB dB	001011	-30 dB	
					011110	-1.5 dB	001010	-31.5 dB	
					011101	-3 dB	001001	-33 dB	
					011100	-4.5 dB	001000	-34.5 dB	
					011011	-6 dB	000111	-36 dB	
					011010	-7.5 dB	000110	-37.5 dB	
					011001	-9 dB	000101	-39 dB	
					011000	-10.5 dB	000100	-40.5 dB	
					010111	-12 dB	000011	-42 dB	
					010110	-13.5 dB	000010	-43.5 dB	
					010101	-15 dB	000001	-45 dB	
					010100	-16.5 dB	000000	-46.5 dB	
R4		7	SDMU	1	Side Tone PGA mute signal: 0: Un-Mute; 1: Mute				

		6	SDEN	0	Side Tone PGA Enable signal: 1: Side Tone PGA Enable; 0: Power Down				
		5	SDZCEN	0	Side Tone PGA ZeroCross Enable signal 1: Enable; 0: Disable				
		4:0	SDVOL[4:0]	11110	Side Tone PGA Volume Control:				
					11111	0dB	01111	-15dB	
					11110	0dB	01110	-16dB	
					11101	-1dB	01101	-17dB	
					11100	-2dB	01100	-18dB	
					11011	-3dB	01011	-19dB	
					11010	-4dB	01010	-20dB	
					11001	-5dB	01001	-21dB	
					11000	-6dB	01000	-22dB	
					10111	-7dB	00111	-23dB	
					10110	-8dB	00110	-24dB	
					10101	-9dB	00101	-25dB	
					10100	-10dB	00100	-26dB	
					10011	-11dB	00011	-27dB	
					10010	-12dB	00010	-28dB	
					10001	-13dB	00001	-29dB	
					10000	-14dB	00000	-30dB	
R5		7	EPMUTE	1	REC Mute control. 1: Mute. 0:unmute				
		6	EPZCEN	0	REC zero crossing enable 1: Enable. 0:disable				
		5	EPEN	0	REC Power down. 1: Power on. 0: Power down.				
		4:0	EPVOL[4:0]	11001	REC Output Volume Control.				
					11111	6dB	01111	-10dB	
					11110	5dB	01110	-11dB	
					11101	4dB	01101	-12dB	
					11100	3dB	01100	-13dB	
					11011	2dB	01011	-14dB	
					11010	1dB	01010	-15dB	
					11001	0dB	01001	-16dB	
					11000	-1dB	01000	-17dB	
					10111	-2dB	00111	-18dB	
					10110	-3dB	00110	-19dB	
					10101	-4dB	00101	-20dB	
					10100	-5dB	00100	-21dB	
					10011	-6dB	00011	-22dB	
					10010	-7dB	00010	-23dB	

					10001	-8dB	00001	-24dB		
					10000	-9dB	00000	-25dB		
R6		7	HPMUTEL	1	HP left channel Mute control. 1: Mute. 0: unmute.					
		6	HPZCENL	0	HP left channel zero crossing enable. 1: Enable. 0: disable.					
		5	HPENL	0	HP left channel Power down. 1: Power on. 0: Power down.					
		4:0	HPVOLL[4:0]	11001	Left Channel Headphone Output Volume Control.					
					11111	6dB	01111	-10dB		
					11110	5dB	01110	-11dB		
					11101	4dB	01101	-12dB		
					11100	3dB	01100	-13dB		
					11011	2dB	01011	-14dB		
					11010	1dB	01010	-15dB		
					11001	0dB	01001	-16dB		
					11000	-1dB	01000	-17dB		
					10111	-2dB	00111	-18dB		
					10110	-3dB	00110	-19dB		
					10101	-4dB	00101	-20dB		
					10100	-5dB	00100	-21dB		
					10011	-6dB	00011	-22dB		
					10010	-7dB	00010	-23dB		
					10001	-8dB	00001	-24dB		
					10000	-9dB	00000	-25dB		
R7		7	HPMUTER	1	HP right channel Mute control. 1: Mute. 0: unmute.					
		6	HPZCENR	0	HP right channel zero crossing enable. 1: Enable. 0: disable					
		5	HPENR	0	HP right channel Power down. 1: Power on. 0: Power down.					
		4:0	HPVOLR[4:0]	11001	Right Channel Headphone Output Volume Control.					
					11111	6dB	01111	-10dB		
					11110	5dB	01110	-11dB		
					11101	4dB	01101	-12dB		
					11100	3dB	01100	-13dB		
					11011	2dB	01011	-14dB		
					11010	1dB	01010	-15dB		
					11001	0dB	01001	-16dB		
					11000	-1dB	01000	-17dB		
					10111	-2dB	00111	-18dB		
					10110	-3dB	00110	-19dB		
					10101	-4dB	00101	-20dB		

					10100	-5dB	00100	-21dB	
					10011	-6dB	00011	-22dB	
					10010	-7dB	00010	-23dB	
					10001	-8dB	00001	-24dB	
					10000	-9dB	00000	-25dB	
R8		7	CD_MUTE	1	Class D Volume mute control. 0: unmute; 1: mute				
		6	SPKZCEN	0	Class D PGA gain control zero-crossing enable 0: Disable; 1: Enable				
		5	TOEN	1	Zero-crossing timeout enable 1: enable 0: disable				
		4:0	CDVOL[4:0]	10100	Class D Volume gain control.				
					11111	5dB	01111	-11dB	
					11110	4dB	01110	-12dB	
					11101	3dB	01101	-13dB	
					11100	2dB	01100	-14dB	
					11011	1dB	01011	-15dB	
					11010	0dB	01010	-16dB	
					11001	-1dB	01001	-17dB	
					11000	-2dB	01000	-18dB	
					10111	-3dB	00111	-19dB	
					10110	-4dB	00110	-20dB	
					10101	-5dB	00101	-21dB	
					10100	-6dB	00100	-22dB	
					10011	-7dB	00011	-23dB	
					10010	-8dB	00010	-24dB	
					10001	-9dB	00001	-25dB	
					10000	-10dB	00000	-26dB	
R9		7:2			Reserved				
		1	CD_ALC_CLR	0	Class D ALC flag clear Writing "1" to clear CD_ALC_FLAG				
		0	CD_DTS_CLR	0	Class D over temperature flag clear Writing "1" to clear CD_DTS_FLAG				
R10		7		0	Reserved				
		6	I2S_RSTN	1	I2S soft reset, active low				
		5:4	I2SCLK_SEL[1:0]	10	I2S 256fs clock selection 00: PLL out 01: EXTCLK 10: MCLK_IN 11: no clock				
		3	I2S_LRCINV	0	I2SLRCK Invert 1: inverted 0: not inverted.				
		2	I2S_BCKINV	0	I2SBICK Invert 1: inverted; 0: not inverted				

		1	I2SBCK_64	1	BCLK frequency selection in master mode 0: 32Fs 1: 64Fs
		0	I2S_MS	0	Master / Slave Mode Control 1: Master Mode; 0: Slave Mode
R11		7		0	Reserved
		6		0	Reserved
		5	I2S_LOOPBACK	0	1: loop back I2S output DAT to input DAT 0: normal
		4	I2S_LRP	0	DSP mode selection 0: Mode A 1: Mode B
		3:2	I2S_WL[1:0]	10	Audio Data Word Length 11 = 32 bits; 10 = 24 bits 01 = 20 bits; 00 = 16 bits
		1:0	I2S_FORMAT[1:0]	10	Audio Data Format Select 11 = DSP/PCM; 10 = I2S Format 01 = Left justified; 00 = Right justified
R12		7:6	I2S_RSEL[1:0]	00	I2S output right channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output
		5:4	I2S_LSEL[1:0]	00	I2S output Left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10, 11: Zero output
		3	I2STXPOL	0	1: invert TX data 0: normal
		2	I2SRXPOL	0	1: invert RX data 0: normal
		1	I2STXLRSWAP	0	Swap Left and Right Channels data of I2S TX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)
		0	I2SRXLRSWAP	0	Swap Left and Right Channels data of I2S RX data 0: No swap (L to L, R to R); 1: Swap (L to R, R to L)
R13		7	PCM_UALAW_INV	1	PCM UALAW inv 1: u-law all bits or A-law even bit inverted 0: not inverted
		6	PCM_DB	0	PCM interface in dual-channel mode 1: dual-channel 0: normal
		5:4	PCM_LSEL[1:0]	00	PCM output left channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10 ,11: Zero output
		3:2	PCM_RSEL[1:0]	00	PCM output right channel data selection 00: ADC1 decimation output 01: ADC2 decimation output 10,11: Zero output

		1:0	PCM_Compand[1:0]	00	PCM Audio Data Format Select 00 = 16bit PCM; 01 = u-law (8bit u-law at PCM[15:7]) 10 = A-law (8bit A-law at PCM[15:7]) 11: reserved.
R15		7		0	reserved
		6	PCM_RSTN	1	PCM soft reset, active low
		5:4	PCMCLK_SEL[1:0]	10	PCM 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
		3	PCM_SYNCSEL	0	PCM sync format selection 1: long frame sync 0: short frame sync
		2	PCM_BCKINV	0	PCM BICK Invert 1: inverted; 0: not inverted
		1	PCMBCK_32	1	PCMBICK frequency selection in master mode 0: 16Fs 1: 32Fs
		0	PCM_MS	0	PCM Master / Slave Mode Control 1: Master Mode; 0: Slave Mode
R16		7:5			reserved
		4:2	MONO_DAC_SEL [2:0]	111	mono DAC data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: from ADC1 output data 101: from ADC2 output data 110: 111: Reserved as Zero
		1	MONODACMU	1	mono DAC mute 1: mute 0: unmute
		0	MONOSOFTMUTE_EN	1	mono DAC soft mute fuction enable 1: enable 0: disable
R17		7	ADC1_ERR	1	ADC1 ALC target error tolerance 1: +- 1.5db 0: +- 0.75db
		6	ADC1_NFEN	0	ADC1 notch filter enable signal 1: enable 0: disable
		5:0	ADC1_NFA0[13:8]	00_0000	ADC1 notch filter A0 coefficient MSBs
R18		7:0	ADC1_NFA0[7:0]	0000_0000	ADC1 notch filter A0 coefficient LSBs
R19		7	ADC1_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)
		6	ADC1_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz)

					0=disabled ;- 1= enabled Application mode (2nd order, fc = HPFCUT)
		5:0	ADC1_NFA1[13:8]	00_0000	ADC1 notch filter A1 coefficient MSBs
R20		7:0	ADC1_NFA1[7:0]	0000_0000	ADC1 notch filter A1 coefficient LSBs
R21		7	ADC1_ALC_DSEL	0	ADC1 ALC data selection 0: after comb filter 1: after HPF filter
		6	ADC1_ALCMODE	0	ADC1 ALC mode selection 0: ALC mode(Normal Operation) 1: Limiter mode
		5	ADC1_ALCSEL	0	ADC1 ALC function enable 1: Enable 0: Disable
		4	ADC1_NG_EN	0	ADC1 Noise Gate enable signal 1: Enable 0: Disable
		3:0	ADC1_NG[3:0]	0111	ADC1 noise floor level
					1111 -84dB 0111 -60 dB
					1110 -81 dB 0110 -57 dB
					1101 -78 dB 0101 -54 dB
					1100 -75 dB 0100 -51 dB
					1011 -72 dB 0011 -48 dB
					1010 -69 dB 0010 -45 dB
					1001 -66 dB 0001 -42 dB
					1000 -63 dB 0000 -39 dB
R22		7:5	ADC1_HPFCUT [2:0]	000	Application mode cut-off frequency.(Fs=48KHz) 000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz
		4:0	ADC1_TARGET [4:0]	00011	ADC1 ALC target level
					11111 -48dB 01111 -24dB
					11110 -46.5dB 01110 -22.5dB
					11101 -45dB 01101 -21dB
					11100 -43.5dB 01100 -19.5dB
					11011 -42dB 01011 -18dB
					11010 -40.5dB 01010 -16.5dB
					11001 -39dB 01001 -15dB
					11000 -37.5dB 01000 -13.5dB
					10111 -36dB 00111 -12dB
					10110 -34.5dB 00110 -10.5dB
					10101 -33dB 00101 -9dB
					10100 -31.5dB 00100 -7.5dB
					10011 -30dB 00011 -6dB
					10010 -28.5dB 00010 -4.5dB
					10001 -27dB 00001 -3dB
					10000 -25.5dB 00000 -1.5dB

R23		7	ADC1MU	1	ADC1 mute signal 1: mute 0: un-mute			
		6:0	ADC1_DIG_VOL [6:0]	1100111 (default 0dB)	ADC1 digital gain			
					1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB
					1110010	8.25dB	0110010	-39.75dB
					1110001	7.5dB	0110001	-40.5dB
					1110000	6.75dB	0110000	-41.25dB
					1101111	6dB	0101111	-42dB
					1101110	5.25dB	0101110	-42.75dB
					1101101	4.5dB	0101101	-43.5dB
					1101100	3.75dB	0101100	-44.25dB
					1101011	3dB	0101011	-45dB
					1101010	2.25dB	0101010	-45.75dB
					1101001	1.5dB	0101001	-46.5dB
					1101000	0.75dB	0101000	-47.25dB
					1100111	0dB	0100111	-48dB
					1100110	-0.75dB	0100110	-48.75dB
					1100101	-1.5dB	0100101	-49.5dB
					1100100	-2.25dB	0100100	-50.25dB
					1100011	-3dB	0100011	-51dB
					1100010	-3.75dB	0100010	-51.75dB
					1100001	-4.5dB	0100001	-52.5dB
					1100000	-5.25dB	0100000	-53.25dB
					1011111	-6dB	0011111	-54dB
					1011110	-6.75dB	0011110	-54.75dB
					1011101	-7.5dB	0011101	-55.5dB
					1011100	-8.25dB	0011100	-56.25dB
					1011011	-9dB	0011011	-57dB
					1011010	-9.75dB	0011010	-57.75dB
					1011001	-10.5dB	0011001	-58.5dB
					1011000	-11.25dB	0011000	-59.25dB

					1010111	-12dB	0010111	-60dB
					1010110	-12.75dB	0010110	-60.75dB
					1010101	-13.5dB	0010101	-61.5dB
					1010100	-14.25dB	0010100	-62.25dB
					1010011	-15dB	0010011	-63dB
					1010010	-15.75dB	0010010	-63.75dB
					1010001	-16.5dB	0010001	-64.5dB
					1010000	-17.25dB	0010000	-65.25dB
					1001111	-18dB	0001111	-66dB
					1001110	-18.75dB	0001110	-66.75dB
					1001101	-19.5dB	0001101	-67.5dB
					1001100	-20.25dB	0001100	-68.25dB
					1001011	-21dB	0001011	-69dB
					1001010	-21.75dB	0001010	-69.75dB
					1001001	-22.5dB	0001001	-70.5dB
					1001000	-23.25dB	0001000	-71.25dB
					1000111	-24dB	0000111	-72dB
					1000110	-24.75dB	0000110	-72.75dB
					1000101	-25.5dB	0000101	-73.5dB
					1000100	-26.25dB	0000100	-74.25dB
					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute
R24		7						
		6	MIC1_0_16_SEL	1	MIC1 1st PGA gain 0: 0dB; 1: 16dB (Default) （Note: total gain=1st PGA gain + 2nd PGA gain）			
		5:0	MIC1_PGA_LEVEL	000000 （6dB）	MIC1 2nd PGA gain			
					111111~101001	fix to 20dB		
					101000	20 dB		
					100111	19.25 dB	010011	4.25 dB
					100110	18.5 dB	010010	3.5 dB
					100101	17.75 dB	010001	2.75 dB
					100100	17 dB	010000	2 dB
					100011	16.25 dB	001111	1.25 dB
					100010	15.5 dB	001110	0.5 dB
					100001	14.75 dB	001101	-0.25 dB
					100000	14 dB	001100	-1 dB
					011111	13.25 dB	001011	-1.75 dB
					011110	12.5 dB	001010	-2.5 dB
					011101	11.75 dB	001001	-3.25 dB

					011100	11 dB	001000	-4 dB	
					011011	10.25 dB	000111	-4.75 dB	
					011010	9.5 dB	000110	-5.5 dB	
					011001	8.75 dB	000101	-6.25 dB	
					011000	8 dB	000100	-7 dB	
					010111	7.25 dB	000011	-7.75 dB	
					010110	6.5 dB	000010	-8.5 dB	
					010101	5.75 dB	000001	-9.25 dB	
					010100	5 dB	000000	-10 dB	
R25		7			Reserved				
		6			Reserved				
		5:0	ADC1_ALCMAX	101000	max PGA gain used in ADC1 ALC model Description similar with MIC1_PGA_LEVEL				
R26		7							
		6							
		5:0	ADC1_ALCMIN	000000	min PGA gain used in ADC1 ALC model Description similar with MIC1_PGA_LEVEL				
R27		7:4	ADC1_ALCDCY	0011	ADC1 decay time(Fs=48KHz) When ADC1_ALCMODE=0				
					1111	10.92s	0111	42.67ms	
					1110	5.46s	0110	21.33ms	
					1101	2.73s	0101	10.67ms	
					1100	1.37s	0100	5.33ms	
					1011	682.67ms	0011	2.67ms	
					1010	341.33ms	0010	1.33ms	
					1001	170.67ms	0001	666.7μs	
					1000	85.33ms	0000	333.3μs	
					When ADC1_ALCMODE =1				
					1111	2.73s	0111	10.67ms	
					1110	1.37s	0110	5.33ms	
					1101	682.67ms	0101	2.67ms	
					1100	341.33ms	0100	1.33ms	
					1011	170.67ms	0011	666.7μs	
					1010	85.33ms	0010	333.3μs	
					1001	42.67ms	0001	166.7μs	
					1000	21.33ms	0000	83.3μs	
		3:0	ADC1_ALCATK	0010	ADC1 attack time (Fs=48kHz) When ADC1_ALCMODE =0				
					1111	2.73s	0111	10.67ms	
					1110	1.37s	0110	5.33ms	

					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs
					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.6μs
					1000	21.33ms	0000	83.3μs
					When ADC1_ALCMODE =1			
					1111	682.67ms	0111	2.67ms
					1110	341.33ms	0110	1.33ms
					1101	170.67ms	0101	666.7μs
					1100	85.33ms	0100	333.3μs
					1011	42.67ms	0011	166.6μs
					1010	21.33ms	0010	83.3μs
					1001	10.67ms	0001	41.7μs
					1000	5.33ms	0000	20.8μs
R28								
		3:0	ADC1_ALCHLD	0000	ADC1 hold time (Fs=48kHz)			
					1111	43.69s	0111	170.67ms
					1110	21.85s	0110	85.33ms
					1101	10.92s	0101	42.67ms
					1100	5.46s	0100	21.33ms
					1011	2.73s	0011	10.67ms
					1010	1.37s	0010	5.33ms
					1001	682.67ms	0001	2.67ms
					1000	341.33ms	0000	2.67ms
R29		7						
		6	ADC1LPEN	0	ADC1 low power enable 1: ADC1 clocks are turned off automatically when ADC1 is disabled 0: ADC1 clocks are not turned off automatically			
		5	ADC1OSR128	1	ADC1 over-sampling rate 0: 64X 1: 128X			
		4	ADC1_RSTN	1	ADC1 soft reset signal, active low			
		3:2	ADC1LRC_SEL[1:0]	00	ADC1 LRC selection 00: from I2S LRCK 01: from PCM SYNC 10,11: no LRCK			
		1:0	ADC1CLK_SEL[1:0]	10	ADC1 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock			
R30		7			Reserved			
		6:0	MONO_DAC_LEVEL[6:	1100111	mono DAC channel digital gain			

			0]	(default 0db)	1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB
					1110010	8.25dB	0110010	-39.75dB
					1110001	7.5dB	0110001	-40.5dB
					1110000	6.75dB	0110000	-41.25dB
					1101111	6dB	0101111	-42dB
					1101110	5.25dB	0101110	-42.75dB
					1101101	4.5dB	0101101	-43.5dB
					1101100	3.75dB	0101100	-44.25dB
					1101011	3dB	0101011	-45dB
					1101010	2.25dB	0101010	-45.75dB
					1101001	1.5dB	0101001	-46.5dB
					1101000	0.75dB	0101000	-47.25dB
					1100111	0dB	0100111	-48dB
					1100110	-0.75dB	0100110	-48.75dB
					1100101	-1.5dB	0100101	-49.5dB
					1100100	-2.25dB	0100100	-50.25dB
					1100011	-3dB	0100011	-51dB
					1100010	-3.75dB	0100010	-51.75dB
					1100001	-4.5dB	0100001	-52.5dB
					1100000	-5.25dB	0100000	-53.25dB
					1011111	-6dB	0011111	-54dB
					1011110	-6.75dB	0011110	-54.75dB
					1011101	-7.5dB	0011101	-55.5dB
					1011100	-8.25dB	0011100	-56.25dB
					1011011	-9dB	0011011	-57dB
					1011010	-9.75dB	0011010	-57.75dB
					1011001	-10.5dB	0011001	-58.5dB
					1011000	-11.25dB	0011000	-59.25dB
					1010111	-12dB	0010111	-60dB
					1010110	-12.75dB	0010110	-60.75dB
					1010101	-13.5dB	0010101	-61.5dB

					1010100	-14.25dB	0010100	-62.25dB	
					1010011	-15dB	0010011	-63dB	
					1010010	-15.75dB	0010010	-63.75dB	
					1010001	-16.5dB	0010001	-64.5dB	
					1010000	-17.25dB	0010000	-65.25dB	
					1001111	-18dB	0001111	-66dB	
					1001110	-18.75dB	0001110	-66.75dB	
					1001101	-19.5dB	0001101	-67.5dB	
					1001100	-20.25dB	0001100	-68.25dB	
					1001011	-21dB	0001011	-69dB	
					1001010	-21.75dB	0001010	-69.75dB	
					1001001	-22.5dB	0001001	-70.5dB	
					1001000	-23.25dB	0001000	-71.25dB	
					1000111	-24dB	0000111	-72dB	
					1000110	-24.75dB	0000110	-72.75dB	
					1000101	-25.5dB	0000101	-73.5dB	
					1000100	-26.25dB	0000100	-74.25dB	
					1000011	-27dB	0000011	-75dB	
					1000010	-27.75dB	0000010	-75.75dB	
					1000001	-28.5dB	0000001	-76.5dB	
					1000000	-29.25dB	0000000	digital mute	
R31		7			Reserved -				
		6							
		5							
		4							
		3							
		2:0							
R32		7			Reserved				
		6	MONO_DACLPEN	0	mono DAC low power enable 0: disable 1: enable				
		5	MONO_DACOSR128	1	mono DAC over-sampling rate 0: 64X 1: 128X				
		4	MONO_DAC_RSTN	1	mono DAC soft reset signal, active low				
		3:2	MONO_DACLRC_SEL[1:0]	00	DAC LRC selection 00: from I2S LRCK 01: from PCM SYNC 10: 11: no LRCK				
		1:0	MONO_DACCLK_SEL[1:0]	10	DAC 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock				
R33		7	ADC2_ERR	1	ADC2 ALC target error tolerance - 1: +- 1.5db 0: +- 0.75db -				

		6	ADC2_NFEN	0	ADC2 notch filter enable signal 1: enable 0:disable			
		5:0	ADC2_NFA0[13:8]	00_0000	ADC2 notch filter A0 coefficient MSBs			
R34		7:0	ADC2_NFA0[7:0]	0000_0000	ADC2 notch filter A0 coefficient LSBs			
R35		7	ADC2_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)			
		6	ADC2_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1= enabled Application mode (2nd order, fc = HPFCUT)			
		5:0	ADC2_NFA1[13:8]	00_0000	ADC2 notch filter A1 coefficient MSBs			
R36		7:0	ADC2_NFA1[7:0]	0000_0000	ADC2 notch filter A1 coefficient LSBs			
R37		7	ADC2_ALC_DSEL	0	ADC2 ALC data selection 0: after comb filter 1: after HPF filter			
		6	ADC2_ALCMODE	0	ADC2 ALC mode selection 0: ALC mode(Normal Operation) 1: Limiter mode			
		5	ADC2_ALCSEL	0	ADC2 ALC function enable 1: Enable 0: Disable			
		4	ADC2_NG_EN	0	ADC2 Noise Gate enable signal 1: Enable 0: Disable			
		3:0	ADC2_NG[3:0]	0111	ADC2 noise floor level			
					1111	-84dB	0111	-60 dB
					1110	-81 dB	0110	-57 dB
					1101	-78 dB	0101	-54 dB
					1100	-75 dB	0100	-51 dB
					1011	-72 dB	0011	-48 dB
					1010	-69 dB	0010	-45 dB
					1001	-66 dB	0001	-42 dB
					1000	-63 dB	0000	-39 dB
R38		7:5	ADC2_HPFCUT	000	Application mode cut-off frequency.(Fs=48KHz)			
			[2:0]		000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz			
		4:0	ADC2_TARGET	00011	ADC2 ALC target level			
			[4:0]		11111	-48dB	01111	-24dB
					11110	-46.5dB	01110	-22.5dB
					11101	-45dB	01101	-21dB
					11100	-43.5dB	01100	-19.5dB
					11011	-42dB	01011	-18dB
					11010	-40.5dB	01010	-16.5dB
					11001	-39dB	01001	-15dB

					11000	-37.5dB	01000	-13.5dB	
					10111	-36dB	00111	-12dB	
					10110	-34.5dB	00110	-10.5dB	
					10101	-33dB	00101	-9dB	
					10100	-31.5dB	00100	-7.5dB	
					10011	-30dB	00011	-6dB	
					10010	-28.5dB	00010	-4.5dB	
					10001	-27dB	00001	-3dB	
					10000	-25.5dB	00000	-1.5dB	
R39		7	ADC2MU	1	ADC2 mute signal 1: mute 0: un-mute				
		6:0	ADC2_DIG_VOL [6:0]	1100111 (default 0db)	ADC2 digital gain				
					1111111	18dB	0111111	-30dB	
					1111110	17.25dB	0111110	-30.75dB	
					1111101	16.5dB	0111101	-31.5dB	
					1111100	15.75dB	0111100	-32.25dB	
					1111011	15dB	0111011	-33dB	
					1111010	14.25dB	0111010	-33.75dB	
					1111001	13.5dB	0111001	-34.5dB	
					1111000	12.75dB	0111000	-35.25dB	
					1110111	12dB	0110111	-36dB	
					1110110	11.25dB	0110110	-36.75dB	
					1110101	10.5dB	0110101	-37.5dB	
					1110100	9.75dB	0110100	-38.25dB	
					1110011	9dB	0110011	-39dB	
					1110010	8.25dB	0110010	-39.75dB	
					1110001	7.5dB	0110001	-40.5dB	
					1110000	6.75dB	0110000	-41.25dB	
					1101111	6dB	0101111	-42dB	
					1101110	5.25dB	0101110	-42.75dB	
					1101101	4.5dB	0101101	-43.5dB	
					1101100	3.75dB	0101100	-44.25dB	
					1101011	3dB	0101011	-45dB	
					1101010	2.25dB	0101010	-45.75dB	
					1101001	1.5dB	0101001	-46.5dB	
					1101000	0.75dB	0101000	-47.25dB	
					1100111	0dB	0100111	-48dB	
					1100110	-0.75dB	0100110	-48.75dB	
					1100101	-1.5dB	0100101	-49.5dB	
					1100100	-2.25dB	0100100	-50.25dB	
					1100011	-3dB	0100011	-51dB	
					1100010	-3.75dB	0100010	-51.75dB	
					1100001	-4.5dB	0100001	-52.5dB	

					1100000	-5.25dB	0100000	-53.25dB	
					1011111	-6dB	0011111	-54dB	
					1011110	-6.75dB	0011110	-54.75dB	
					1011101	-7.5dB	0011101	-55.5dB	
					1011100	-8.25dB	0011100	-56.25dB	
					1011011	-9dB	0011011	-57dB	
					1011010	-9.75dB	0011010	-57.75dB	
					1011001	-10.5dB	0011001	-58.5dB	
					1011000	-11.25dB	0011000	-59.25dB	
					1010111	-12dB	0010111	-60dB	
					1010110	-12.75dB	0010110	-60.75dB	
					1010101	-13.5dB	0010101	-61.5dB	
					1010100	-14.25dB	0010100	-62.25dB	
					1010011	-15dB	0010011	-63dB	
					1010010	-15.75dB	0010010	-63.75dB	
					1010001	-16.5dB	0010001	-64.5dB	
					1010000	-17.25dB	0010000	-65.25dB	
					1001111	-18dB	0001111	-66dB	
					1001110	-18.75dB	0001110	-66.75dB	
					1001101	-19.5dB	0001101	-67.5dB	
					1001100	-20.25dB	0001100	-68.25dB	
					1001011	-21dB	0001011	-69dB	
					1001010	-21.75dB	0001010	-69.75dB	
					1001001	-22.5dB	0001001	-70.5dB	
					1001000	-23.25dB	0001000	-71.25dB	
					1000111	-24dB	0000111	-72dB	
					1000110	-24.75dB	0000110	-72.75dB	
					1000101	-25.5dB	0000101	-73.5dB	
					1000100	-26.25dB	0000100	-74.25dB	
					1000011	-27dB	0000011	-75dB	
					1000010	-27.75dB	0000010	-75.75dB	
					1000001	-28.5dB	0000001	-76.5dB	
					1000000	-29.25dB	0000000	digital mute	
R40		7							
		6	MIC2_0_16_SEL	1	MIC2 1st PGA gain 0: 0dB; 1: 16dB (Default) （Note：total gain=1st PGA gain + 2nd PGA gain）				
		5:0	MIC2_PGA_LEVEL	000000 （6db）	MIC2 2nd PGA gain				
					111111--101001	fix to 20dB			
					101000	20 dB			
					100111	19.25 dB	010011	4.25 dB	
					100110	18.5 dB	010010	3.5 dB	
					100101	17.75 dB	010001	2.75 dB	

					100100	17 dB	010000	2 dB
					100011	16.25 dB	001111	1.25 dB
					100010	15.5 dB	001110	0.5 dB
					100001	14.75 dB	001101	-0.25 dB
					100000	14 dB	001100	-1 dB
					011111	13.25 dB	001011	-1.75 dB
					011110	12.5 dB	001010	-2.5 dB
					011101	11.75 dB	001001	-3.25 dB
					011100	11 dB	001000	-4 dB
					011011	10.25 dB	000111	-4.75 dB
					011010	9.5 dB	000110	-5.5 dB
					011001	8.75 dB	000101	-6.25 dB
					011000	8 dB	000100	-7 dB
					010111	7.25 dB	000011	-7.75 dB
					010110	6.5 dB	000010	-8.5 dB
					010101	5.75 dB	000001	-9.25 dB
					010100	5 dB	000000	-10 dB
R41		7						
		6						
		5:0	ADC2_ALCMAX	101000	max PGA gain used in ADC2 ALC model Descritption similar with MIC2_PGA_LEVEL			
R42		7						
		6						
		5:0	ADC2_ALCMIN	000000	min PGA gain used in ADC2 ALC model Descritption similar with MIC2_PGA_LEVEL			
R43		7:4	ADC2_ALCDCY	0011	ADC2 decay time(Fs=48KHz) When ADC2_ALCMODE=0			
					1111	10.92s	0111	42.67ms
					1110	5.46s	0110	21.33ms
					1101	2.73s	0101	10.67ms
					1100	1.37s	0100	5.33ms
					1011	682.67ms	0011	2.67ms
					1010	341.33ms	0010	1.33ms
					1001	170.67ms	0001	666.7μs
					1000	85.33ms	0000	333.3μs
					When ADC2_ALCMODE =1			
					1111	2.73s	0111	10.67ms
					1110	1.37s	0110	5.33ms
					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs

					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.7μs
					1000	21.33ms	0000	83.3μs
		3:0	ADC2_ALCATK	0010	ADC2 attack time(Fs=48kHz) When ADC2_ALCMODE =0			
					1111	2.73s	0111	10.67ms
					1110	1.37s	0110	5.33ms
					1101	682.67ms	0101	2.67ms
					1100	341.33ms	0100	1.33ms
					1011	170.67ms	0011	666.7μs
					1010	85.33ms	0010	333.3μs
					1001	42.67ms	0001	166.6μs
					1000	21.33ms	0000	83.3μs
					When ADC2_ALCMODE =1			
					1111	682.67ms	0111	2.67ms
					1110	341.33ms	0110	1.33ms
					1101	170.67ms	0101	666.7μs
					1100	85.33ms	0100	333.3μs
					1011	42.67ms	0011	166.6μs
					1010	21.33ms	0010	83.3μs
					1001	10.67ms	0001	41.7μs
					1000	5.33ms	0000	20.8μs
R44								
		3:0	ADC2_ALCHLD	0000	ADC2 hold time(Fs=48kHz)			
					1111	43.69s	0111	170.67ms
					1110	21.85s	0110	85.33ms
					1101	10.92s	0101	42.67ms
					1100	5.46s	0100	21.33ms
					1011	2.73s	0011	10.67ms
					1010	1.37s	0010	5.33ms
					1001	682.67ms	0001	2.67ms
					1000	341.33ms	0000	2.67ms
R45		7						
		6	ADC2LPEN	0	ADC2 low power enable 1: ADC2 clocks are turned off automatically when ADC2 is disabled 0: ADC2 clocks are not turned off automatically			
		5	ADC2OSR128	1	ADC2 over-sampling rate 0: 64X 1: 128X			
		4	ADC2_RSTN	1	ADC2 soft reset signal, active low			
		3:2	ADC2LRC_SEL[1:0]	00	ADC2 LRC selection			

					00: from I2S LRCK 01: from PCM SYNC 10,11: no LRCK
		1:0	ADC2CLK_SEL[1:0]	10	ADC2 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock
R46		7:5	DAC_SEL_L[2:0]	111	DAC left channel data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: 101: 110: 111: Reserved as Zero
		4:2	DAC_SEL_R[2:0]	111	DAC right channel data selection 000: from I2S interface left channel data 001: from I2S interface right channel data 010: from PCM interface left channel data 011: from PCM interface right channel data 100: 101: 110: 111: Reserved as Zero
		1	LDACMU	1	DAC left channel mute signal 1: mute 0: un-mute
		0	RDACMU	1	DAC right channel mute signal 1: mute 0: un-mute
R47		7	SOFTMUTE_EN	1	DAC soft mute function enable signal 1: enable 0: disable
		6:5	ST_SEL_L[1:0]	00	DAC left channel side-tone data selection 00: ADC1 output 01: ADC2 output 10, 11: Reserved
		4:0	STVOL_L[4:0]	00000	DAC left channel side-tone gain

11111	0dB	01111	-16 dB
11110	-1 dB	01110	-17 dB
11101	-2 dB	01101	-18 dB
11100	-3 dB	01100	-19 dB
11011	-4 dB	01011	-20 dB
11010	-5 dB	01010	-21 dB
11001	-6 dB	01001	-22 dB
11000	-7 dB	01000	-23 dB
10111	-8 dB	00111	-24 dB
10110	-9 dB	00110	-25 dB
10101	-10 dB	00101	-26 dB
10100	-11 dB	00100	-27 dB
10011	-12 dB	00011	-28 dB
10010	-13 dB	00010	-29 dB
10001	-14 dB	00001	-30 dB

					10000	-15 dB	00000	mute
R48		7		0	Reserved			
		6:5	ST_SEL_R[1:0]	00	DAC right channel side-tone data selection 00: ADC1 output 01: ADC2 output 10: 11: Reserved			
		4:0	STVOL_R[4:0]	00000	DAC right channel side-tone gain			
					11111	0dB	01111	-16 dB
					11110	-1 dB	01110	-17 dB
					11101	-2 dB	01101	-18 dB
					11100	-3 dB	01100	-19 dB
					11011	-4 dB	01011	-20 dB
					11010	-5 dB	01010	-21 dB
					11001	-6 dB	01001	-22 dB
					11000	-7 dB	01000	-23 dB
					10111	-8 dB	00111	-24 dB
					10110	-9 dB	00110	-25 dB
					10101	-10 dB	00101	-26 dB
					10100	-11 dB	00100	-27 dB
					10011	-12 dB	00011	-28 dB
					10010	-13 dB	00010	-29 dB
					10001	-14 dB	00001	-30 dB
					10000	-15 dB	00000	mute
R49		7		0	Reserved			
		6:0	DAC_LEVEL_L[6:0]	1100111 (default 0dB)	DAC left channel digital gain			
					1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB
					1110010	8.25dB	0110010	-39.75dB
					1110001	7.5dB	0110001	-40.5dB
					1110000	6.75dB	0110000	-41.25dB
					1101111	6dB	0101111	-42dB

					1101110	5.25dB	0101110	-42.75dB	
					1101101	4.5dB	0101101	-43.5dB	
					1101100	3.75dB	0101100	-44.25dB	
					1101011	3dB	0101011	-45dB	
					1101010	2.25dB	0101010	-45.75dB	
					1101001	1.5dB	0101001	-46.5dB	
					1101000	0.75dB	0101000	-47.25dB	
					1100111	0dB	0100111	-48dB	
					1100110	-0.75dB	0100110	-48.75dB	
					1100101	-1.5dB	0100101	-49.5dB	
					1100100	-2.25dB	0100100	-50.25dB	
					1100011	-3dB	0100011	-51dB	
					1100010	-3.75dB	0100010	-51.75dB	
					1100001	-4.5dB	0100001	-52.5dB	
					1100000	-5.25dB	0100000	-53.25dB	
					1011111	-6dB	0011111	-54dB	
					1011110	-6.75dB	0011110	-54.75dB	
					1011101	-7.5dB	0011101	-55.5dB	
					1011100	-8.25dB	0011100	-56.25dB	
					1011011	-9dB	0011011	-57dB	
					1011010	-9.75dB	0011010	-57.75dB	
					1011001	-10.5dB	0011001	-58.5dB	
					1011000	-11.25dB	0011000	-59.25dB	
					1010111	-12dB	0010111	-60dB	
					1010110	-12.75dB	0010110	-60.75dB	
					1010101	-13.5dB	0010101	-61.5dB	
					1010100	-14.25dB	0010100	-62.25dB	
					1010011	-15dB	0010011	-63dB	
					1010010	-15.75dB	0010010	-63.75dB	
					1010001	-16.5dB	0010001	-64.5dB	
					1010000	-17.25dB	0010000	-65.25dB	
					1001111	-18dB	0001111	-66dB	
					1001110	-18.75dB	0001110	-66.75dB	
					1001101	-19.5dB	0001101	-67.5dB	
					1001100	-20.25dB	0001100	-68.25dB	
					1001011	-21dB	0001011	-69dB	
					1001010	-21.75dB	0001010	-69.75dB	
					1001001	-22.5dB	0001001	-70.5dB	
					1001000	-23.25dB	0001000	-71.25dB	
					1000111	-24dB	0000111	-72dB	
					1000110	-24.75dB	0000110	-72.75dB	
					1000101	-25.5dB	0000101	-73.5dB	
					1000100	-26.25dB	0000100	-74.25dB	

					1000011	-27dB	0000011	-75dB
					1000010	-27.75dB	0000010	-75.75dB
					1000001	-28.5dB	0000001	-76.5dB
					1000000	-29.25dB	0000000	digital mute
R50		7		0	Reserved			
		6:0	DAC_LEVEL_R [6:0]	1100111 (default 0dB)	DAC right channel digital gain			
					1111111	18dB	0111111	-30dB
					1111110	17.25dB	0111110	-30.75dB
					1111101	16.5dB	0111101	-31.5dB
					1111100	15.75dB	0111100	-32.25dB
					1111011	15dB	0111011	-33dB
					1111010	14.25dB	0111010	-33.75dB
					1111001	13.5dB	0111001	-34.5dB
					1111000	12.75dB	0111000	-35.25dB
					1110111	12dB	0110111	-36dB
					1110110	11.25dB	0110110	-36.75dB
					1110101	10.5dB	0110101	-37.5dB
					1110100	9.75dB	0110100	-38.25dB
					1110011	9dB	0110011	-39dB
					1110010	8.25dB	0110010	-39.75dB
					1110001	7.5dB	0110001	-40.5dB
					1110000	6.75dB	0110000	-41.25dB
					1101111	6dB	0101111	-42dB
					1101110	5.25dB	0101110	-42.75dB
					1101101	4.5dB	0101101	-43.5dB
					1101100	3.75dB	0101100	-44.25dB
					1101011	3dB	0101011	-45dB
					1101010	2.25dB	0101010	-45.75dB
					1101001	1.5dB	0101001	-46.5dB
					1101000	0.75dB	0101000	-47.25dB
					1100111	0dB	0100111	-48dB
					1100110	-0.75dB	0100110	-48.75dB
					1100101	-1.5dB	0100101	-49.5dB
					1100100	-2.25dB	0100100	-50.25dB
					1100011	-3dB	0100011	-51dB
					1100010	-3.75dB	0100010	-51.75dB
					1100001	-4.5dB	0100001	-52.5dB
					1100000	-5.25dB	0100000	-53.25dB
					1011111	-6dB	0011111	-54dB
					1011110	-6.75dB	0011110	-54.75dB
					1011101	-7.5dB	0011101	-55.5dB
					1011100	-8.25dB	0011100	-56.25dB

					1011011	-9dB	0011011	-57dB	
					1011010	-9.75dB	0011010	-57.75dB	
					1011001	-10.5dB	0011001	-58.5dB	
					1011000	-11.25dB	0011000	-59.25dB	
					1010111	-12dB	0010111	-60dB	
					1010110	-12.75dB	0010110	-60.75dB	
					1010101	-13.5dB	0010101	-61.5dB	
					1010100	-14.25dB	0010100	-62.25dB	
					1010011	-15dB	0010011	-63dB	
					1010010	-15.75dB	0010010	-63.75dB	
					1010001	-16.5dB	0010001	-64.5dB	
					1010000	-17.25dB	0010000	-65.25dB	
					1001111	-18dB	0001111	-66dB	
					1001110	-18.75dB	0001110	-66.75dB	
					1001101	-19.5dB	0001101	-67.5dB	
					1001100	-20.25dB	0001100	-68.25dB	
					1001011	-21dB	0001011	-69dB	
					1001010	-21.75dB	0001010	-69.75dB	
					1001001	-22.5dB	0001001	-70.5dB	
					1001000	-23.25dB	0001000	-71.25dB	
					1000111	-24dB	0000111	-72dB	
					1000110	-24.75dB	0000110	-72.75dB	
					1000101	-25.5dB	0000101	-73.5dB	
					1000100	-26.25dB	0000100	-74.25dB	
					1000011	-27dB	0000011	-75dB	
					1000010	-27.75dB	0000010	-75.75dB	
					1000001	-28.5dB	0000001	-76.5dB	
					1000000	-29.25dB	0000000	digital mute	
R51		7			Reserved				
		6	DAC_DWAEN	0	DAC DWA function enable signal 1: enable 0: disable				
		5	DAC_SD_NZ	0	DAC SDM no-zero input signal(for test) 1: no-zero 0: normal				
		4	DAC_HPF1EN	0	1st High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1=enabled Audio mode (1st order, fc = ~3.7Hz)				
		3	DAC_HPF2EN	0	2nd High Pass Filter Enable Control (Fs=48KHz) 0=disabled ; 1= enabled Application mode (2nd order, fc = HPFCUT)				
		2:0	DAC_HPFCUT[2:0]	000	Application mode cut-off frequency.(Fs=48KHz) 000: 122Hz 001: 153Hz 010: 156Hz 011: 245Hz 100: 306Hz 101: 392Hz 110: 490Hz 111: 612Hz				

R52		7	DAC_ALCMODE	0	ALC mode selection 0: ALC mode(Normal Operation) 1: Limiter mode			
		6:5	DAC_ALCSEL[1:0]	00	DAC ALC function select 00: ALC disabled 01: Right channel ALC enabled 10: left channel ALC enabled 11: both channels ALC enabled			
		4	DAC_NG_EN	0	DAC Noise Gate enable signal 1: Enable 0: Disable			
		3:0	DAC_NG[3:0]	0111	DAC noise floor level			
					1111	-84dB	0111	-60 dB
					1110	-81 dB	0110	-57 dB
					1101	-78 dB	0101	-54 dB
					1100	-75 dB	0100	-51 dB
					1011	-72 dB	0011	-48 dB
					1010	-69 dB	0010	-45 dB
					1001	-66 dB	0001	-42 dB
					1000	-63 dB	0000	-39 dB
R53		7						
		6						
		5	DAC_ERR	1	DAC ALC target error tolerance 1: +- 1.5db 0: +- 0.75db			
		4:0	DAC_TARGET[4:0]	00011 (-6db)	DAC ALC target level			
					11111	-48dB	01111	-24dB
					11110	-46.5dB	01110	-22.5dB
					11101	-45dB	01101	-21dB
					11100	-43.5dB	01100	-19.5dB
					11011	-42dB	01011	-18dB
					11010	-40.5dB	01010	-16.5dB
					11001	-39dB	01001	-15dB
					11000	-37.5dB	01000	-13.5dB
					10111	-36dB	00111	-12dB
					10110	-34.5dB	00110	-10.5dB
					10101	-33dB	00101	-9dB
					10100	-31.5dB	00100	-7.5dB
					10011	-30dB	00011	-6dB
					10010	-28.5dB	00010	-4.5dB
					10001	-27dB	00001	-3dB
					10000	-25.5dB	00000	-1.5dB
R54		7						

<table>
<tr><td></td><td></td><td>6:0</td><td>DAC_ALCMAX_L</td><td>1111111</td><td>The left channel max digital gain used in ALC model
Description similar with DAC_LEVEL_L</td></tr>
<tr><td>R55</td><td></td><td>7</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>6:0</td><td>DAC_ALCMIN_L</td><td>0000000</td><td>The left channel min digital gain used in ALC model
Description similar with DAC_LEVEL_L</td></tr>
<tr><td>R56</td><td></td><td>7</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>6:0</td><td>DAC_ALCMAX_R</td><td>1111111</td><td>The right channel max digital gain used in ALC model
Description similar with DAC_LEVEL_R</td></tr>
<tr><td>R57</td><td></td><td>7</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>6:0</td><td>DAC_ALCMIN_R</td><td>0000000</td><td>The right channel min digital gain used in ALC model
Description similar with DAC_LEVEL_R</td></tr>
<tr><td>R58</td><td></td><td>7:4</td><td>DAC_ALCDCY</td><td>0011</td><td>DAC decay time(Fs=48KHz)
When DAC_ALCMODE=0
<table>
<tr><td>1111</td><td>10.92s</td><td>0111</td><td>42.67ms</td></tr>
<tr><td>1110</td><td>5.46s</td><td>0110</td><td>21.33ms</td></tr>
<tr><td>1101</td><td>2.73s</td><td>0101</td><td>10.67ms</td></tr>
<tr><td>1100</td><td>1.37s</td><td>0100</td><td>5.33ms</td></tr>
<tr><td>1011</td><td>682.67ms</td><td>0011</td><td>2.67ms</td></tr>
<tr><td>1010</td><td>341.33ms</td><td>0010</td><td>1.33ms</td></tr>
<tr><td>1001</td><td>170.67ms</td><td>0001</td><td>666.7μs</td></tr>
<tr><td>1000</td><td>85.33ms</td><td>0000</td><td>333.3μs</td></tr>
</table>
When DAC_ALCMODE =1
<table>
<tr><td>1111</td><td>2.73s</td><td>0111</td><td>10.67ms</td></tr>
<tr><td>1110</td><td>1.37s</td><td>0110</td><td>5.33ms</td></tr>
<tr><td>1101</td><td>682.67ms</td><td>0101</td><td>2.67ms</td></tr>
<tr><td>1100</td><td>341.33ms</td><td>0100</td><td>1.33ms</td></tr>
<tr><td>1011</td><td>170.67ms</td><td>0011</td><td>666.7μs</td></tr>
<tr><td>1010</td><td>85.33ms</td><td>0010</td><td>333.3μs</td></tr>
<tr><td>1001</td><td>42.67ms</td><td>0001</td><td>166.7μs</td></tr>
<tr><td>1000</td><td>21.33ms</td><td>0000</td><td>83.3μs</td></tr>
</table></td></tr>
<tr><td></td><td></td><td>3:0</td><td>DAC_ALCATK</td><td>0010</td><td>DAC attack time(Fs=48kHz)
When DAC_ALCMODE =0
<table>
<tr><td>1111</td><td>2.73s</td><td>0111</td><td>10.67ms</td></tr>
<tr><td>1110</td><td>1.37s</td><td>0110</td><td>5.33ms</td></tr>
<tr><td>1101</td><td>682.67ms</td><td>0101</td><td>2.67ms</td></tr>
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<tr><td>1011</td><td>170.67ms</td><td>0011</td><td>666.7μs</td></tr>
<tr><td>1010</td><td>85.33ms</td><td>0010</td><td>333.3μs</td></tr>
<tr><td>1001</td><td>42.67ms</td><td>0001</td><td>166.6μs</td></tr>
<tr><td>1000</td><td>21.33ms</td><td>0000</td><td>83.3μs</td></tr>
</table></td></tr>
</table>

					When DAC_ALCMODE =1				
					1111	682.67ms	0111	2.67ms	
					1110	341.33ms	0110	1.33ms	
					1101	170.67ms	0101	666.7μs	
					1100	85.33ms	0100	333.3μs	
					1011	42.67ms	0011	166.6μs	
					1010	21.33ms	0010	83.3μs	
					1001	10.67ms	0001	41.7μs	
					1000	5.33ms	0000	20.8μs	
R59									
		3:0	DAC_ALCHLD	0000	DAC hold time(Fs=48kHz)				
					1111	43.69s	0111	170.67ms	
					1110	21.85s	0110	85.33ms	
					1101	10.92s	0101	42.67ms	
					1100	5.46s	0100	21.33ms	
					1011	2.73s	0011	10.67ms	
					1010	1.37s	0010	5.33ms	
					1001	682.67ms	0001	2.67ms	
					1000	341.33ms	0000	2.67ms	
R60		7							
		6:2	EQ1_GAIN	00000	EQ1 gain				
					11111	15dB	01111	-1 dB	
					11110	14 dB	01110	-2 dB	
					11101	13 dB	01101	-3 dB	
					11100	12 dB	01100	-4 dB	
					11011	11 dB	01011	-5 dB	
					11010	10 dB	01010	-6 dB	
					11001	9 dB	01001	-7 dB	
					11000	8 dB	01000	-8 dB	
					10111	7 dB	00111	-9 dB	
					10110	6 dB	00110	-10 dB	
					10101	5 dB	00101	-11 dB	
					10100	4 dB	00100	-12 dB	
					10011	3 dB	00011	-13 dB	
					10010	2 dB	00010	-14 dB	
					10001	1 dB	00001	-15 dB	
					10000	0 dB	00000	off (0db)	
		1:0	EQ1_FQ	10	Sub-bass shelving filter's cut-off frequency 00: 60Hz 01: 80 10: 100 11: 120				

R61		7	EQ2_Q	0	EQ2 bandwidth 0: 2/3 Octave 1: 4/3 Octave			
		6:2	EQ2_GAIN	00000	EQ2 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ2_FQ	10	bass peak filter's center frequency 00: 150Hz 01: 200 10: 150 11: 300			
R62		7	EQ3_Q	0	EQ3 bandwidth 0: 2/3 Octave 1: 4/3 Octave			
		6:2	EQ3_GAIN	00000	EQ3 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB

					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ3_FQ	10	mid peak filter's center frequency 00: 600Hz 01: 800 10: 1000 11: 1200			
R63		7	EQ4_Q	0	EQ4 bandwidth 0: 2/3 Octave 1: 4/3 Octave			
		6:2	EQ4_GAIN	00000	EQ4 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB
					10110	6 dB	00110	-10 dB
					10101	5 dB	00101	-11 dB
					10100	4 dB	00100	-12 dB
					10011	3 dB	00011	-13 dB
					10010	2 dB	00010	-14 dB
					10001	1 dB	00001	-15 dB
					10000	0 dB	00000	off (0db)
		1:0	EQ4_FQ	10	treble peak filter's center frequency 00: 2000Hz 01: 2700 10: 3400 11: 4100			
R64				0	Reserved			
		6:2	EQ5_GAIN	00000	EQ5 gain			
					11111	15dB	01111	-1 dB
					11110	14 dB	01110	-2 dB
					11101	13 dB	01101	-3 dB
					11100	12 dB	01100	-4 dB
					11011	11 dB	01011	-5 dB
					11010	10 dB	01010	-6 dB
					11001	9 dB	01001	-7 dB
					11000	8 dB	01000	-8 dB
					10111	7 dB	00111	-9 dB

					10110	6 dB	00110	-10 dB	
					10101	5 dB	00101	-11 dB	
					10100	4 dB	00100	-12 dB	
					10011	3 dB	00011	-13 dB	
					10010	2 dB	00010	-14 dB	
					10001	1 dB	00001	-15 dB	
					10000	0 dB	00000	off (0db)	
		1:0	EQ5_FQ	10	Presence shelving filter's cut-off frequency 00: 7000Hz 01: 9000 10: 11000 11: 20000				
R65		7:0	DAC_OFFSET [15:8]	0000_0000	Added DAC offset MSBs (for testing)				
R66		7:0	DAC_OFFSSET [7:0]	0000_0000	DAC offset LSBs				
R67		7:5		000	Reserved				
		4	DAC_DITH_BYPASS	1	DAC SDM dither function bypass 1: bypass 0:function used				
		3:2	DAC_DITH_TYPE [1:0]	00	DAC SDM dither type selection (for testing)				
		1:0	DAC_DITH_POW [25:24]	00	DAC SDM dither power (for testing)				
R68		7:0	DAC_DITH_POW [23:16]	0000_0000	DAC SDM dither power (for testing)				
R69		7:0	DAC_DITH_POW [15:8]	0000_0000	DAC SDM dither power (for testing)				
R70		7:0	DAC_DITH_POW [7:0]	0000_0000	DAC SDM dither power (for testing)				
R71		7		0	Reserved				
		6	DACLPEN	0	DAC low power enable 0: disable 1: enable				
		5	DACOSR128	1	DAC over-sampling rate 0: 64X 1: 128X				
		4	DAC_RSTN	1	DAC soft reset signal, active low				
		3:2	DACLRC_SEL[1:0]	00	DAC LRC selection 00: from I2S LRCK 01: from PCM SYNC 10: 11: no LRCK				
		1:0	DACCLK_SEL[1:0]	10	DAC 256fs clock selection 00: PLL1 out 01: EXTCLK 10: MCLK_IN 11: no clock				
R72		7		000	Reserved				

		6	MONO_DAC_DWAEN	0	mono DAC DWA function enable signal 1: enable 0: disable
		5	MONO_DAC_SD_NZ	0	mono DAC SDM no-zero input signal(for test) 1: no-zero 0: normal
		4	MONO_DAC_DITH_BYPASS	1	DAC SDM dither function bypass 1: bypass 0:function used
		3:2	MONO_DAC_DITH_TYPE [1:0]	00	Mono DAC SDM dither type selection (for testing)
		1:0	MONO_DAC_DITH_POW [25:24]	00	Mono DAC SDM dither power (for testing)
R73			MONO_DAC_DITH_POW [23:16]	0000_0000	Mono DAC SDM dither power (for testing)
R74			MONO_DAC_DITH_POW [15:8]	0000_0000	Mono DAC SDM dither power (for testing)
R75			MONO_DAC_DITH_POW [7:0]	0000_0000	Mono DAC SDM dither power (for testing)
R76		7:4			
		3:0	PLL_INT_P[3:0]	0110	Integer part of PLL (Default Case: 12M input, 12.288M output)
R77		7:0	PLL_FRC_P[7:0]	11101001	Fractional (K) part of PLL input/output frequency ratio (Default Case: 12M input, 12.288M output)
R78		7:0	PLL_FRC_P[15:8]	00100110	
R79		7:0	PLL_FRC_P[23:16]	00110001	
R80		7:5	CP_P[2:0]	100	PLL internal Charge pump current selection bits 000：20uA 001：25uA 010：30uA 011：35uA 100：40uA（default） 101：45uA 110：50uA 111：55uA
		4	PLL_FRCEN_P	0	Fractional N enable; high active.
		3	RESETN_P	0	PLL1 Reset; low active.
		2:0	POST_DIV1[2:0]	000	Post divider selection: POST_DIV[2:0] / DIV 000 / 2 001 / 4 010 / 8 011 / 16 100 / 32 101 / 64 110 / 64 111 / 64

R81		7		0	
		6	PRESCALE	0	0: Divide by 1; 1:Divide by 2
		5	PLLEN	0	PLL1 enable; high active
		4	TESTVCOB_P	1	0:VCO function test, Vctrl=VDD/2; 1: normal work
		3:2	RLPF_P[1:0]	10	Low pass filter resister selection
		1:0	RVI_P[1:0]	01	V to I converter resister selection
R82		7			
		6			
		5	AD1IN5SEL	0	ADC1 select DAC MONO channel signal 0= no select 1= select
		4	AD1IN4SEL	0	ADC1 select DAC L channel signal 0= no select 1= select
		3	AD1IN3SEL	0	ADC1 select DAC R channel signal 0= no select 1= select
		2	AD1IN2SEL	0	ADC1 select MainMIC2—HPMIC PGA OUT channel signal 0= no select 1= select
		1	AD1IN1SEL	0	ADC1 select MainMIC1 PGA OUTsignal 0= no select 1= select
		0	AD1MUXMU	1	ADC1 MUX mute signal 0: MUX unmute; 1: MUX mute
R83		7			
		6			
		5	AD2IN5SEL	0	ADC2 select DAC MONO channel signal 0= no select 1= select
		4	AD2IN4SEL	0	ADC2 select DAC L channel signal 0= no select 1= select
		3	AD2IN3SEL	0	ADC2 select DAC R channel signal 0= no select 1= select
		2	AD2IN2SEL	0	ADC2 select MainMIC2&HPMIC PGA OUT channel signal 0= no select 1= select
		1	AD2IN1SEL	0	ADC2 select MainMIC1 PGA OUTsignal 0= no select 1= select
		0	AD2MUXMU	1	ADC2 MUX mute signal 0: MUX unmute; 1: MUX mute
R84		7:5	ICTR_DAC[2:0]	011	000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA
		4:2	VMICSEL[2:0]	101	VMICBIAS Voltage Select different VMICBIAS corresponding different VMID

VMID_SEL[2:0]	VMID(V)	VMICSEL[2:0]	VMICBIAS(V)
111	1.39	000	2.45
110	1.43	001	2.534

					101	1.49	010	2.623
					100	1.54	011	2.615
					011	1.6	100	2.614
					010	1.66(default)	101	2.62(default)
					001	1.73	110	2.634
					000	1.8	111	2.656
		1	MICBEN	0	Micbias enable; 0 = disable 1 = enable			
		0	MICBSWEN	0	Micbias switch enable 0 = disable 1 = enable			
R85		7	MICSTSEL	0	Sidetone select: 0: Select MIC1 1: Select MIC2 or HPMIC			
		6	M_MIC1N2INN	1	Connect MIC1N to input PGA negative terminal.(Main Mic1) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
		5	M_MIC1P2INP	0	Connect input PGA amplifier positive terminal to MIC1P or VREF. (Main Mic1) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
		4	HP_MICN2INN	1	Connect MICN to input PGA negative terminal.(HP Mic) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
		3	HP_MICP2INP	0	Connect input PGA amplifier positive terminal to MICP or VREF. (HP Mic) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
		2	MIC2HPSEL	0	MainMIC2 —HPMIC PGA select input signal 0: Select Main MIC2; 1: Select HP MIC			
		1	M_MIC2N2INN	1	Connect MIC2N to input PGA negative terminal.(Main Mic2) 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.			
		0	M_MIC2P2INP	0	Connect input PGA amplifier positive terminal to MIC2P or VREF. (Main Mic2) 0 = input PGA amplifier positive terminal connected to VREF 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string			
R86		7						
		6	AUXMIXEN	0	AUX Mixer enable signal 1: Enable，0：Disable			
		5	AUXMIXMU	1	AUX Mixer Mute signal: 0: Un-Mute; 1：Mute			
		4	LINLSEL_AUX	0	AUX Select Left Line PGA control signal : 0:unselect; 1: Select			
		3	LINRSEL_AUX	0	AUX Select Right Line PGA control signal : 0:unselect; 1: Select			
		2	DACMONOSEL_AUX	0	AUX Select mono DAC control signal : 0:unselect 1:select			
		1	DACLSEL_AUX	0	AUX Select Left DAC control signal: 0:unselect; 1: Select			
		0	DACRSEL_AUX	0	AUX Select Right DAC control signal: 0:unselect; 1: Select			
R87		7	LDOEN	0	LDO Enable signal 1: LDO Enable; 0: Disable			
		6	SPKMIXEN	0	SPK Mixer Enable signal : 1: Enable，0：Disable			
		5	SPKMIXMU	1	SPK Mixer Mute signal : 0: Un-Mute; 1:Mute			
		4	LINLSEL_SPK	0	SPK Select Left Line PGA: 0:unselect; 1: Select			

		3	LINRSEL_SPK	0	SPK Select Right Line PGA: 0:unselect; 1: Select
		2	DACMONOSEL_SPK	0	SPK Select mono DAC: 0:unselect 1:select
		1	DACLSEL_SPK	0	SPK Select Left DAC: 0:unselect; 1: Select
		0	DACRSEL_SPK	0	SPK Select Right DAC: 0:unselect; 1: Select
R88		7:5	VMID_SEL[2:0]	010	VMID Voltage Select signal 000 1.804V; 001 1.73V 010 1.661V(DEFAULT); 011 1.598V 100 1.539V; 101 1.485V 110 1.434V; 111 1.387V
		4:1	LDOVSEL[3:0]	0100	LDO Voltage Select signal: VSEL[3:0] VLDO 0000 3.7 0001 3.6 0010 3.5 0011 3.4 0100 3.3(DEFAULT) 0101 3.2 0110 3.1 0111 3.0 1000 2.9 1001 2.8 1010 2.7 1111 1.8(LDO OUTPUT 1.8V)
		0	LDO_SW	0	LDO work mode select 0: LDO Normal work; 1: Switch mode
R89		7			
		6	HPLMIXEN	0	HP L channel Mixer Enable : 1 : Enable 0 : Disable
		5	HPLMIXMU	1	HP L channel Mixer Mute. 0: Un-Mute; 1: Mute
		4	LINLSEL_HPL	0	HP L channel Select Left Line PGA: 0:unselect; 1: Select
		3	DACMONOSEL_HPL	0	HP L channel Select mono DAC: 0:unselect 1:select
		2	DACLSEL_HPL	0	HP L channel Select Left DAC: 0:unselect; 1: Select
		1	DACRSEL_HPL	0	HP L channel Select Right DAC: 0:unselect; 1: Select
		0	SDTSEL_HPL	0	HP L channel Select Side Tone: 0:unselect; 1: Select
R90		7			
		6	HPRMIXEN	0	HP R channel Mixer Enable. 1: Enable; 0: Disable
		5	HPRMIXMU	1	HP R Mixer Mute. 0: Un-Mute; 1: Mute
		4	LINRSEL_HPR	0	HP R Select Right Line PGA: 0:unselect; 1: Select
		3	DACMONOSEL_HPR	0	HP R Select mono DAC: 0:unselect 1:select
		2	DACLSEL_HPR	0	HP R Select Left DAC: 0:unselect; 1: Select
		1	DACRSEL_HPR	0	HP R Select Right DAC: 0:unselect; 1: Select
		0	SDTSEL_HPR		HP R Select Side Tone: 0:unselect; 1: Select

R91		7	RECMIXEN	0	REC Mixer Enable. 1: Enable；0：Disable
		6	RECMIXMU	1	REC Mixer Mute. 0: Un-Mute；1：Mute
		5	DACMONOSEL_REC	0	REC Select mono DAC: 0:unselect 1:select
		4	DACLSEL_REC	0	REC Select Left DAC: 0:unselect; 1: Select
		3	DACRSEL_REC	0	REC Select right DAC: 0:unselect; 1: Select
		2	SDTSEL_REC	0	REC Select Side Tone: 0:unselect; 1: Select
		1:0	SLOWCLK_SEL[1:0]	00	Slow Clock selection signal 00: 2^21 MCLK 01: 2^20MCLK 10：2^19 MCLK 11: 2^18MCLK
R92		7:6	OSCIB_OPT[1:0]	11	ClassG internal OSC Current Control:00:3.75u；01:8.75u; 10:1.25u; 11:6.25uA
		5:4	OSCF_SEL[1:0]	01	ClassG internal OSC Frequency: 00:2M; 01:1M; 10:4M; 11:0.5MHz
		3	NVEN	0	Charge pump CPVSS Power down. 1: Power on. 0: Power down.
		2	VREFEN_CG	0	CLASS G internal VREF Power down 1: Power up. 0: Power down.
		1	OSC_EN	0	ClassG internal OSC Power Down: 1:Enable; 0: Power Down
		0	CG_CK_SEL	0	0: from internal osc, 1: no clock
R93		7	CD_CK_SEL	0	0: internal OSC; 1: no clock
		6	CD_ENB_TMNT	0	Time counter of CTRL_LOGIC enable control 0: Enable the time counter. 1: Disable the time counter
		5	CD_TSAT	0	Time counter Start Time control 0: Fast start(about 5ms); 1: Slow start(about 40ms)
		4	LOWPOWER	0	ClassD power consumption control 0: Normal work; 1: Low power mode
		3	PD_OCT	1	OCT detect（over current protect）start up control. 0: Start up; 1: Stop
		2	PD3_CD	1	Function blocks of Class-D（other than op、PWM_osc、bias）power down control 0: Normal work. 1: Power down
		1	PD2_CD	1	Function blocks Class-D（op、PWM_osc） power down control 0: Normal work. 1: Power down
		0	PD_CD	1	Class-D（bias） power down control 0: Normal work. 1: Power down
R94		7:6	CD_IBSRMP[1:0]	00	ClassD（Speaker）internal OSC_RAMP bias current select 00 :10U; 01: 9U; 10: 11U; 11: 10U
		5:3	CLGAIN[2:0]	000	Close-loop gain control 000 :6dB; 001: 6.90dB; 010: 6.60 dB; 011: 6.32 dB 100: 5.71 dB; 101: 5.44 dB; 110: 5.15 dB; 111: 4.91 dB
		2:1	CD_ALC[1:0]	00	The trigger point of output signal clipping control 00: n=4; 01: n=2; 10: n=8; 11: n=16
		0	CD_ENB_ALC	0	Clipping ALC function enable control 0: normal work; 1: disable
R95		7:6	NOVSEL[1:0]	01	ClassD Dead Time Control 00:8ns; 01:9ns; 10:10.5ns; 11:13ns;
		5	TSSET	1	ClassD Temp sensor threshold 0: 134C（protect）/115C（release）; 1: 112C（protect）/92C（release）;

		4	–		
		3	CD_ENB_GLITCH	0	Deglitch function enable control 0: Enable deglitch function; 1: Disable deglitch function
		2	CD_ENB_OCT	0	OCT(Over current protection) function enable control 0: Enable OCT function; 1: Disable OCT function
		1	CD_ENB_POP	0	De-pop function enable control 0: Enable De-pop function; 1: Disable De-pop function
		0	TS_EN	0	over temperature protect enable signal ; 0: Disable; 1: Enable
R96		7	VBSPGAEN	0	Vref enable. 0 = disabled;1 = enabled
		6	IBSEN	0	Top Bias current enable signal . 0 = disabled;1 = enabled
		5	BGPEN	0	Vref output generator enable. 0 = disabled;1 = enabled
		4			
		3:1	IBS_SEL[2:0]	011	I bias is default 5u and gradually increase from 3u to 7u. 000 7.05uA; 001 6.27uA 010 5.64uA; 011 5.13uA(DEFAULT) 100 4.7uA; 101 4.34uA 110 4.03uA; 111 3.76uA
		0	VREFEN	0	Headphone internal VREF BUFFER enable. 0 = disabled;1 = enabled
R97		7			
		6			
		5			
		4			
		3	CD_ALC_OUT		CLASSD ALC IRQ SIGNAL; 1: CD ALC IRQ;0:No IRQ;
		2	CD_DTS		CLASSD OVER TEMPERATURE FLAG SIGNAL; 0:normal; 1:OVER TEMP IRQ;
		1	PLL_LD		PLL lock detector signal 1: PLL1 lock 0: PLL1 not lock
		0			
R98		7			
		6:4	ICTR_ADC2	011	ADC2 Bias Current control signal: 000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA
		3	LDOSINKEN	1	Codec LDO fast discharge enable control signal: 0= LDO fast discharge disable 1= LDO fast discharge enable
		2:0	ICTR_ADC1	011	ADC1 Bias Current control signal: 000=3.5u; 001=4u; 010=4.5u;011=5u (Default) 100=5.5u; 101=6u; 110=6.5u; 111=7uA