INTEGRATED CIRCUIT DATA SHEET

IRIS304

TD-SCDMA/HSPA and GSM/GPRS/EDGE RF Transceiver for User Equipment

Provisional Specifications

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CONFIDENTIALITY	**ACP CONFIDENTIAL**
RELEASE NOTES	Contains target specifications. Data are subject to change.

Zwischenweg 2, 8702 Zollikon, Switzerland, Tel +41 44 390 36 14, Fax +41 44 390 36 34

IRIS304

TD-SCDMA/HSPA and GSM/GPRS/EDGE RF Transceiver for User Equipment

Features

- Triple-band RF transceiver for TD-SCDMA, TD-HSDPA and TD-HSUPA
- Quad-band RF transceiver for GSM, GPRS and EDGE
- No SAW filters required for TD-SCDMA/HSPA receive path
- No SAW filters required for TD-SCDMA/HSPA transmit path
- No SAW filters required for GSM/GPRS/EDGE transmit path
- Fully integrated frequency synthesis, complete with loop filter
- Integrated DCDC-converter and LDO linear regulators
- On-chip DCXO
- Auxiliary DAC for optional AFC support for off-chip TCXO
- Four reference clock outputs with independent enable pins
- Auxiliary ADC for measurement of internal or external temperature sensor
- Support for GGE PA ramping
- Single or dual SPI control; support for four-wire read protocol on SPI2
- Parallel digital IQ data interface for TD-SCDMA/HSPA
- DigRF v1.12 data interface for GSM/GPRS/EDGE
- Optional analog IQ interface (pins shared with TD parallel data interface)

Applications

Mobile phones and data modems in the bands below : GSM 850MHz, GSM 900MHz, DCS 1800MHz, PCS 1900MHz, TD-SCDMA bands 34/F (1880-1920MHz), 39/A (2010-2025MHz) and 40/E (2300-2400MHz).

General Description

IRIS304 is a single-chip RF transceiver supporting both TD-SCDMA/HSPA (3G) and GSM/GPRS/EDGE(2.5G) standards. Housed in a 5*5 mm^2 81-pin BGA package its footprint is 30% smaller than its predecessor IRIS305. Further footprint/BOM reduction is supported by 3 auxiliary reference clock outputs usable as reference for other radios.

In 3G mode high sensitivity, linearity and low EVM are among the receiver's salient features that secure excellent performance in QPSK and 16QAM modes. It offers a unique SAW-less mode to remove both the cost and sensitivity loss of Rx SAW filters, enabling an unprecedented integration level for the RF subsystem.

The transmitter offers low EVM to support 16QAM used in HSUPA for high throughput, and keeps spurious emissions low to relieve the RF sub system equally of the SAW filters commonly found in TD-SCDMA transmitters.

In GSM/EDGE mode, the receiver excels in low power consumption, in addition to low noise figure and high linearity. Standby time, crucial to user satisfaction, can be improved substantially with IRIS304. The transmitter offers high spectral purity that again enables tough spurious emissions requirements to be met without interstage SAW filters. IRIS304 enables a 2G/3G dual mode RF subsystem to be constructed with a minimum number of components on a very small PCB footprint.

IRIS304 comes fully integrated with synthesizer and loop filter, A/D and D/A converters, a DCXO, a DCDC-converter, LDO regulators, and two serial peripheral interfaces. Most of the circuits are shared between GSM/EDGE and TD-SCDMA/HSPA modes to achieve a small overall chip size.

Ordering Information

TYPE NUMBER	PACKAGE	
	NAME	DESCRIPTION
IRIS304	TFBGA	Thin-profile Fine-pitch Ball Grid Array, 81 balls, 5 x 5 x 1 mm

Zwischenweg 2, 8702 Zollikon, Switzerland, Tel +41 44 390 36 14, Fax +41 44 390 36 34

Contents

1. Block Diagram

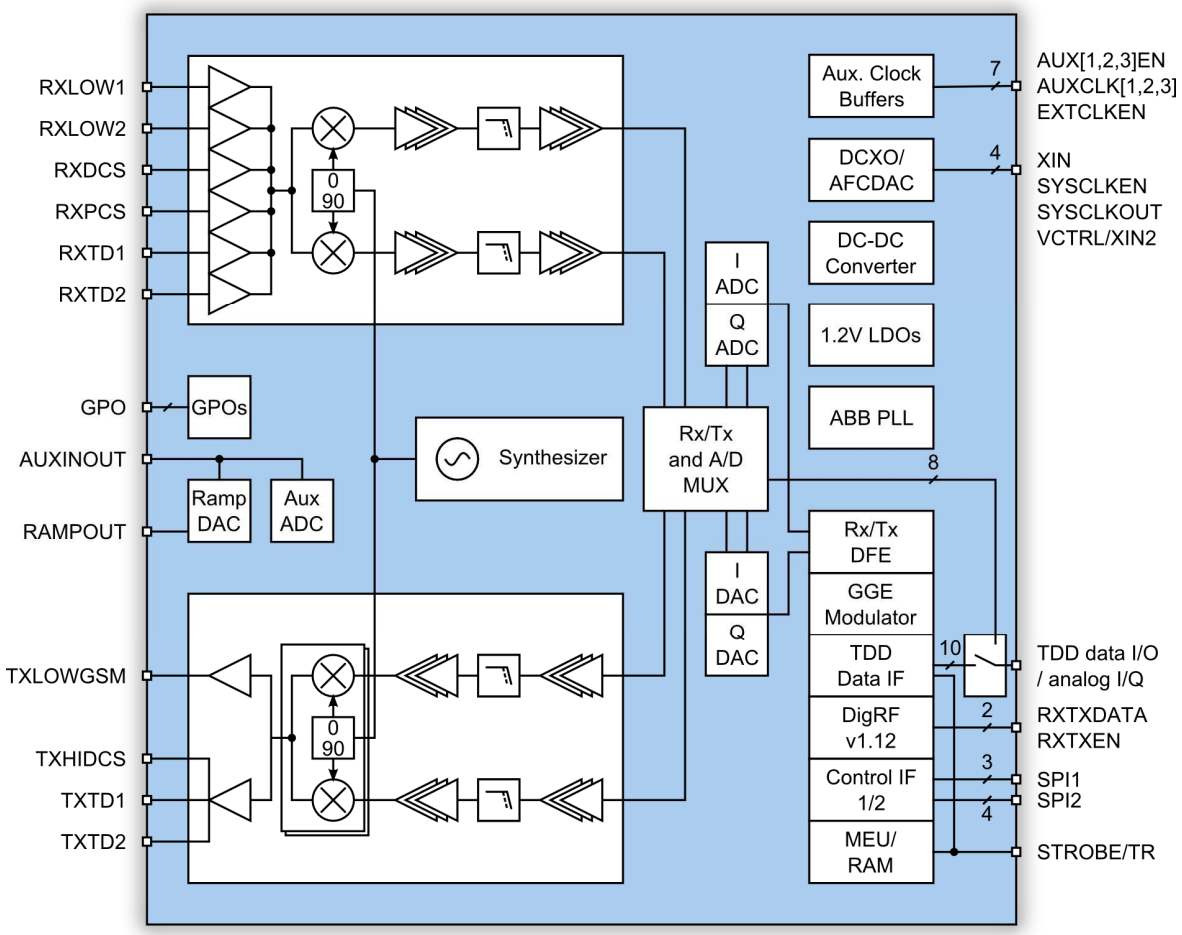

Figure 1: IRIS304 block diagram

2. Pin Assignment

NAME	PIN	DESCRIPTION
RXPCS	A1	Rx input PCS
RXDCS	A2	Rx input DCS
RXLOW2	A3	Rx input GSM 900
RXLOW1	A4	Rx input GSM 850
RXTD1	A5	Rx input TD-SCDMA A/F
RXTD2	A6	Rx input TD-SCDMA E
TXLOWGSM	A7	Tx output GSM 850/900
TXHIDCS	A8	Tx output DCS/PCS A/F
TXTD2	A9	Tx output TD-SCDMA E
AUXINOUT	B1	Aux. output of ramp DAC, input of auxiliary ADC
GND	B2-8	Global ground
TXTD1	B9	Tx output TD-SCDMA A/F
SPI2DO	C1	Serial peripheral interface 2 data output
RAMPOUT	C2	2G ramping signal for PA
GND	C3-5	Global ground
AUX2EN	C6	Enable signal for auxiliary clock output 2
AUX1EN	C7	Enable signal for auxiliary clock output 1
D0	C8	Digital data I/F bit 0; Q- of Rx/Tx analog I/F
LDO1IN	C9	Input to LDO1
VDD3INTF	D1	2.85V Supply
GPO3	D2	General purpose output 3
VDDIO2	D3	Digital IO supply for SPI I/F and GPOs
GND	D4-6	Global ground
AUX3EN	D7	Enable signal for auxiliary clock output 3
D2	D8	Digital data I/F bit 2; I- of Rx/Tx analog I/F
D1	D9	Digital data I/F bit 1; Q+ of Rx/Tx analog I/F
VDDD	E1	1.2V supply (output of internal LDO)
GPO2	E2	General purpose output 2
GND	E3-5	Global ground
AUXCLK1	E6	Auxiliary clock output 1
AUXCLK2	E7	Auxiliary clock output 2
D3	E8	Digital data I/F bit 3; I+ of Rx/Tx analog I/F
VDDIO	E9	Digital IO supply for data I/F and ref. clock outputs
XIN	F1	Reference clock input; pin 1 of Xtal (DCXO mode)
SPI2EN	F2	Serial perpheral interface 2 enable

NAME	PIN	DESCRIPTION
STROBE/TR	F3	Strobe input; can be reconfigured as parallel interface tx/rx switch
GND	F4-5	Global ground
EXTCLKEN	F6	Digital output: SYSCLKEN OR AUX1EN OR AUX2EN OR AUX3EN
GND	F7	Global ground
AUXCLK3	F8	Auxiliary clock output 3
SYSCLKOUT	F9	Sys. clock output to BBIC
VCTRL	G1	AFC DAC output; Xtal pin 2 (DCXO mode)
SPI2CLK	G2	Serial peripheral interface 2 clock
SPI2DIO	G3	Serial peripheral interface 2 data input/output
GND	G4-5	Global ground
VDD3TS1	G6	2.85V Supply
D4	G7	Digital data I/F bit 4; Q- of alt. Tx analog I/F
RXTXDATA	G8	RXTX data signal of DigRF interface
D5	G9	Digital data I/F bit 5; Q+ of alt. Tx analog I/F
VBAT	H1	DCDC converter VBAT
DCDCGND	H2	DCDC converter ground
SPI1CLK	H3	Serial peripheral interface 1 clock
SPI1DIO	H4	Serial peripheral interface 1 data input/output
GND	H5-6	Global ground
D9	H7	Digital data I/F bit 9
D7	H8	Digital data I/F bit 7; I+ of alt. Tx analog I/F
CLK	H9	Digital data I/F clock signal
DCDCOUT	J1	DCDC converter output
SYSCLKEN	J2	System clock enable
SPI1EN	J3	Serial peripheral interface 1 enable
LDO2IN	J4	Input to LDO 2
VDD3TS2	J5-6	2.85V Supply
RXTXEN	J7	RXTX enable signal of DigRF interface
D8	J8	Digital data I/F bit 8
D6	J9	Digital data I/F bit 6; I- of alt. Tx analog I/F

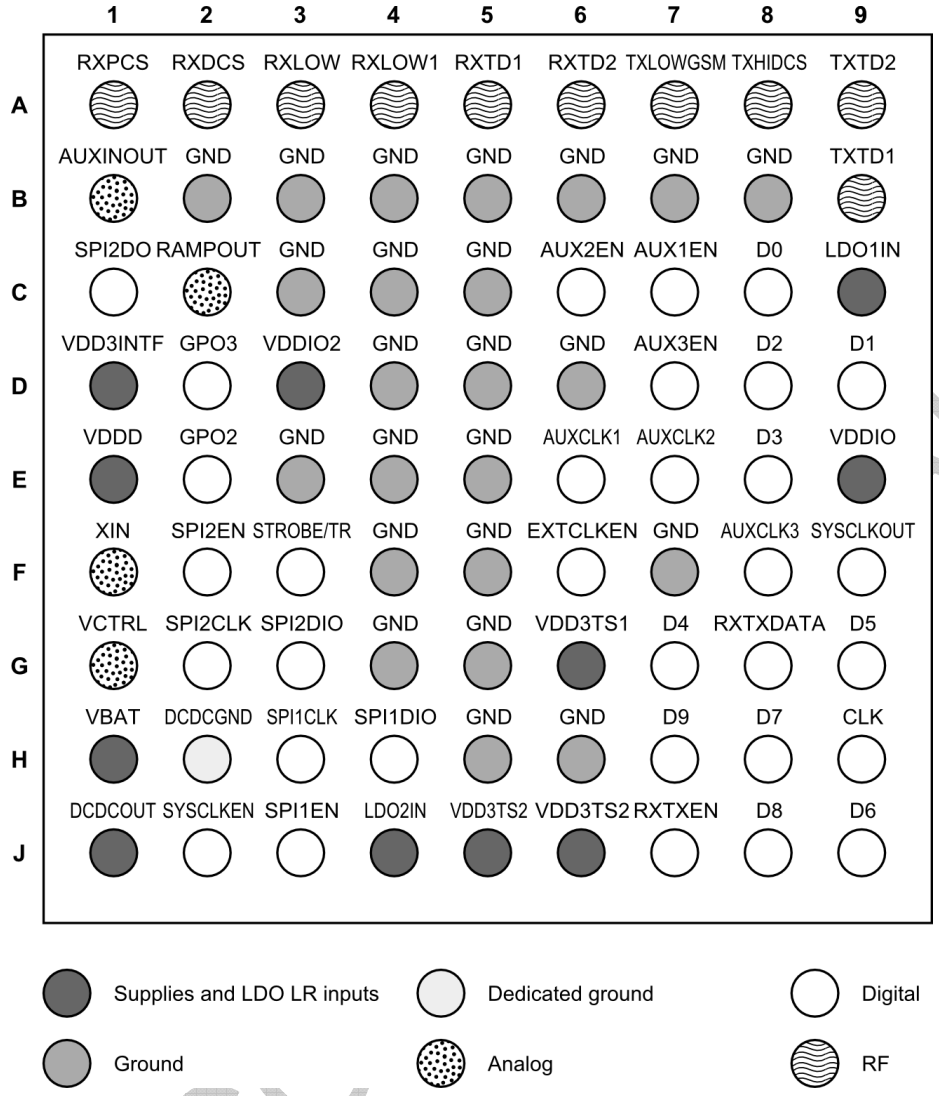

Figure 2: Pin configuration.

3. Absolute Maximum Ratings

DESCRIPTION	SYM.	MIN.	MAX.	UNIT
Battery supply	V_{bat}	-0.3	6.4	V
2.85 V supply	V_{DD3}	-0.3	6.4	V
Digital I/O supply	V_{DDIO}, V_{DDIO2}	-0.3	6.4	V
1.2 V pins (note 1)	$V_{1.2V}$	-0.3	2.1	V
3.3 V pins (note 1)	$V_{3.3V}$	-0.3	6.4	V

DESCRIPTION	SYM.	MIN.	MAX.	UNIT
Operating temp.	T_{amb}	-30	+85	ºC
Storage temp.	T_{sto}	-65	+160	ºC
Soldering temp.	T_{sol}		+300	ºC
LNA input power	P_{in}		+4	dBm

Stresses beyond absolute maximum ratings may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to these conditions for extended periods may affect device reliability.

NOTES:

1. The following nets include 1.2 V pins: all RF pins, VDDD and XIN. All other nets only include 3.3 V pins.

CAUTION! ESD SENSITIVE DEVICE! This device features electrostatic discharge (ESD) protection circuitry. However, permanent damage may occur to devices when subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

4. DC Electrical Characteristics

General condition, unless otherwise noted: V_{bat} = 3.7 V, T_{amb} = +27 ºC.

4.1 Supply Voltages

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Battery supply voltage (PIN: VBAT)	V_{bat}	if on-chip DCDC-converter is used	3.2	3.7	4.5	V
1.2 V LDO LR supply voltage (PINS: LDO1IN, LDO2IN)	V_{LDOin}	if external DCDC-converter is used	1.5	1.6	3.0	V
2.85 V supply voltage (note 1) (PINS: VDD3INTF, VDD3TS2, VDD3TS1)	V_{DD3}		2.7	2.85	3.0	V
Digital I/O supply voltage (PINS: VDDIO, VDDIO2)	V_{DDIO}		1.14		2.0	V

NOTES:
1 In application the 2.85V supply pins are generally connected together on the PCB, supplied by a single PMU output. The connected set of 2.85V supply pins (VDD3INTF, VDD3TS2, VDD3TS1) is referred to as V_{DD3} in the remainder of the data sheet.

4.2 Current Consumption

Multiple power supply options are available for this device. Correspondingly the currents given below specify the total current drawn from the 3.7V battery under the most likely application scenarios. Internal DC-DC converter and LDO are recommended for low cost applications. External DC-DC converter is recommended for low power applications. Currents drawn from V_{DD3} and V_{DDIO} are included.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
SLEEP MODE						
Sleep mode current consumption	I_{slp}	Power-down of chip except V_{DD3} = 1.8V		20		µA
STANDBY MODE						
Standby mode current consumption	I_{stdby}	AFCDAC & SYSCLK buffer on		3.5		mA
IDLE MODE						
Idle mode current consumption	I_{idle}	DC-DC converter in linear mode; main LDO off		6		mA
RECEIVE MODE (TX OFF)						
GSM/EDGE RX operating current consumption (note1)	$I_{op,rx}$	DigRF Interface, ext. DC-DC DigRF Interface, int. DC-DC		50 55		mA
TD-SCDMA RX operating current consumption (note 1)	$I_{op,rx}$	dig. I/Q Interface, ext. DC-DC dig. I/Q Interface, Int. DC-DC		46 51		mA
TRANSMIT MODE (RX OFF)						
GSM/EDGE TX operating current consumption (at +3dBm as in GMSK mode)	$I_{op,tx}$	low bands, external DC-DC low bands, internal LDO high bands, external DC-DC high bands, internal LDO		65 120 78 145		mA
TD-SCDMA TX operating current consumption (note 2)	$I_{op,tx}$	external DC-DC internal DC-DC		68 73		mA

NOTES:
1 RX gain is set to the recommended maximum. No signal is applied.
2 TX gain is set such as to obtain a 23 dBm lowband TX signal at the antenna connector for a typical antenna switch and power amplifier gain. A modulated uplink signal is applied.

4.3 Transceiver Interface In Analog I/Q Mode

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
RECEIVER						
I/Q output common mode voltage	$V_{olQ,CM}$	fixed		0.6		V
I/Q output driving capability	$R_{L,diff}$	resistive, differential	5			kΩ
	$C_{L,diff}$	capacitive, differential			10	pF
RF input pin coupling		single ended, high ohmic DC connection to gnd, LC-matched; AC-coupling needed to other than 0V DC potential				
TRANSMITTER						
I/Q input impedance	$R_{i,diff}$	resistive, differential	160			kΩ
	$C_{i,diff}$	capacitive, differential			5	pF
I/Q input common mode voltage	$V_{ilQ,CM}$	fixed	0.3	0.6	0.8	V
RF output pins common mode voltage		single ended, low ohmic DC connection to gnd, AC-coupling needed to other than 0V DC potential		0		V

4.4 Serial Peripheral Interface

Detailed information for the serial peripheral interface is given in application note AN304SPI. Key numbers are given below.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PINS: SPI[1/2]EN, SPI[1/2]DIO, SPI2DO, SPI[1/2]CLK, SYSCLKOUT, SYSCLKEN						
Output low voltage (= logical 0)	V_{OL}	single-ended, to gnd, I_{OL} = 500 µA			$0.2 \times V_{DDIO}$	V
Output high voltage (= logical 1)	V_{OH}	single-ended, to gnd, I_{OH} = -500 µA	$0.8 \times V_{DDIO}$			V
Input low voltage (= logical 0)	V_{IL}	single-ended, to gnd	-0.3		$0.3 \times V_{DDIO}$	V
Input high voltage (= logical 1)	V_{IH}	single-ended, to gnd	$0.7 \times V_{DDIO}$		V_{DDIO} + 0.3	V
PIN: SYSCLKOUT						
System clock driving capability	$C_{L,sysclk}$	capacitive, single-ended		5	15	pF
PIN: SYSCLKEN						
System clock enable input impedance	$C_{i,sysclken}$	capacitive, single-ended			6	pF

4.5 Digital Parallel I/Q-Data Interface

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PINS: D0-D9, CLK, STROBE/TR						
Output low voltage (= logical 0)	V_{OL}	single-ended, to gnd, I_{OL} = 500 µA			0.2 × V_{DDIO}	V
Output high voltage (= logical 1)	V_{OH}	single-ended, to gnd, I_{OH} = -500 µA	0.8 × V_{DDIO}			V
Input low voltage (= logical 0)	V_{IL}	single-ended, to gnd	-0.3		0.3 × V_{DDIO}	V
Input high voltage (= logical 1)	V_{IH}	single-ended, to gnd	0.7 × V_{DDIO}		V_{DDIO} + 0.3	V

4.6 Digital Serial I/Q-Data Interface

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PINS: RXTXEN, RXTXDATA						
Output low voltage (= logical 0)	V_{OL}	single-ended, to gnd, I_{OL} = 500 µA			0.2 × V_{DDIO}	V
Output high voltage (= logical 1)	V_{OH}	single-ended, to gnd, I_{OH} = -500 µA	0.8 × V_{DDIO}			V
Input low voltage (= logical 0)	V_{IL}	single-ended, to gnd	-0.3		0.3 × V_{DDIO}	V
Input high voltage (= logical 1)	V_{IH}	single-ended, to gnd	0.7 × V_{DDIO}		V_{DDIO} + 0.3	V

4.7 Reference Clock

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PIN: XIN **REQUIREMENT IN TCXO MODE**						
Ref. clock input voltage	V_{refclk}	single-ended	0.8		1.2	Vpp
Ref. clock input DC level			0.5		0.7	V
Ref. clock input impedance	$R_{i,refclk}$	resistive, single-ended	25			kΩ
	$C_{i,refclk}$	capacitive, single-ended			2	pF
PIN: XIN **INTERNAL DCXO MODE: REQUIREMENTS FOR EXTERNAL QUARTZ CRYSTAL**						
Oscillation frequency	f_{refclk}	fundamental oscillation		26		MHz
Frequency tolerance	f_{tol}	T_{amb} = 25˚C			±10	ppm
Frequency temperature tolerance	f_{temp}	in -30 to +85 ˚C interval			±10	ppm
Aging	a_{tol}				2	ppm/y
Series resistance	R_{ser}				80	Ω
Motional capacitance	C_s			2		fF
Load Capacitance	C_{load}			7.5		pF
PIN: XIN **INTERNAL DCXO CAPABILITY**						
Fine tuning range	D_{range}	T_{amb} = 25˚C		52		ppm
One time coarse tuning	D_{coarse}			60		ppm
Tuning step	D_{step}			<0.01		ppm
Start up time	t_{start}			2		ms

4.8 Auxiliary Reference Clock Outputs

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PINS: AUXCLK1, AUXCLK2, AUXCLK3, EXTCLKEN						
Output low voltage (= logical 0)	V_{OL}	single-ended, to gnd, I_{OL} = 500 µA			$0.2 \times V_{DDIO}$	V
Output high voltage (= logical 1)	V_{OH}	single-ended, to gnd, I_{OH} = -500 µA	$0.8 \times V_{DDIO}$			V
PINS: AUX1EN, AUX2EN, AUX3EN						
Input low voltage (= logical 0)	V_{IL}	single-ended, to gnd	-0.3		$0.3 \times V_{DDIO}$	V
Input high voltage (= logical 1)	V_{IH}	single-ended, to gnd	$0.7 \times V_{DDIO}$		3	V

4.9 General Purpose Outputs

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
PINS: GPO2, GPO3						
Output low voltage (= logical 0)	V_{OL}	single-ended, to gnd, I_{OL} = 500 µA			$0.2 \times V_{DDIO2}$	V
Output high voltage (= logical 1)	V_{OH}	single-ended, to gnd, I_{OH} = -500 µA	$0.8 \times V_{DDIO2}$			V

5. AC Electrical Characteristics

5.1 GSM/GPRS/EDGE Receiver

General condition, unless otherwise noted: 3.2V ≤ V_{bat} ≤ 4.5V, 2.7V ≤ V_{DD3} ≤ 3.0V, 1.14V ≤ V_{DDIO} ≤ 2.0V, -30˚C ≤ T_{amb} ≤ 85˚C. Typical values are at V_{bat} = 3.7V, V_{DD3} = 2.85V, V_{DDIO} = 1.8V, T_{amb} = 25˚C. Minimum and maximum numbers apply to all frequency channels and include variations over process, voltage and temperature. All parameters are referred to the input of the Rx matching network. Rx output signal taken either at analog I/Q output or at DigRF data output.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
1. Overall Characteristics						
Receive frequency range	f_{rx}	GSM-850	869		894	MHz
		GSM-900	925		960	
		DCS 1800	1805		1880	
		PCS 1900	1930		1990	
Noise Figure (note 1)	NF	T_{amb} = +25deg				
		low band		2.5		dB
		high band		2.7		
		T_{amb} = -30..+85deg				
		low band			4.5	
		high band			5.0	
Input-referred 1 dB compression point (note 2)	iCPblk	by 0.2MHz offset GMSK blocker (LNAG≤6, PGC1≤2, PGC2≤7)		-63		dBm
		by 0.4MHz offset GMSK blocker (LNAG≤6, PGC1≤2, PGC2≤7)		-34		
		by 0.6MHz offset GMSK blocker (LNAG≤6, PGC1≤2, PGC2≤7)		-27		
		by 0.6MHz offset CW blocker max. Rx gain		-40		
		by 1.6MHz offset CW blocker max. Rx gain		-28		
		by 3MHz offset CW blocker max Rx gain		-24		
		by 20MHz offset CW blocker max. Rx gain		-22		
2nd-order input-referred intercept point	iIP2	of two ≤ 6MHz ± 25kHz offset signals	45			dBm
3rd-order input-referred intercept point	iIP3	of two 0.825/1.6 MHz offset CW signals				dBm
		low band		-4		
		high band		-3		
Error vector magnitude	EVM_{rx}	GMSK rms phase error low band, Pin = -50dBm .. -25dBm		1.5		deg
		GMSK rms phase error high band, Pin = -50dBm .. -25dBm		2.0		
		8-PSK rms EVM low band, Pin = -50dBm .. -25dBm		2.0		%
		8-PSK rms EVM high band, Pin = -50dBm .. -25dBm		2.5		

2. Gain and PGC Characteristics						
Max. voltage gain	$GR_{rx,max}$	T_{amb} = +25˚C		94		dB
Min. voltage gain	$G_{rx,min}$	T_{amb} = +25˚C		-7		dB
Programmable gain range	GR_{rx}			101		dB
Gain variation over temperature	$\Delta G_{rx\,T}$	T_{amb} = -30˚C .. +85˚C	-3		2.5	dB
Gain variation over frequency	$\Delta G_{rx,f}$	single band, fixed gain setting		0.5		dB
Progr. LNA gain range	GR_{LNA}			30		dB
Progr. LNA gain step	GS_{LNA}	GLNA from 4 to 5, 5 to 6, 6 to 7		6		dB
		GLNA<4 to GLNA=4		12		
Progr. LNA gain step accuracy	GA_{LNA}	GLNA from 4 to 5, 5 to 6, 6 to 7		±0.3		dB
		GLNA<4 to GLNA=4		±0.7		
PGC1 gain range	GR_{PGC1}			18		dB
PGC1 gain step	GS_{PGC1}			6		dB
PGC1 gain step accuracy	GA_{PGC1}	any step of 6dB		±0.3		dB
		integral error over 18dB		±0.5		
PGC2 gain range	GR_{PGC2}			53		dB
PGC2 gain step	GS_{PGC2}			1		dB
PGC2 gain step accuracy	GA_{PGC2}	max. 1dB step error		±0.15		dB
		integral error over 53 dB		±0.5		
3. RF Characteristics						
Input return loss	S_{11}	max. value over band, at 50Ω		-10		dB
Max. allowed LNA input power	$P_{in,max}$	LNA off / LNAG<4	-10			dBm
LO leakage to RF at LNA input	X_{LO}			≤ -100		dBm
4. Baseband Characteristics						
Channel selectivity of adjacent signals	BB_{Sel}	of 0.2MHz offset GMSK signal		1		dB
		of 0.4MHz offset GMSK signal		38		
		of 0.6MHz offset GMSK signal		60		
		of 0.6MHz offset CW signal		≥65		
Image rejection ratio	IRR_{rx}	in wanted signal band		40		dB
I/Q differential output voltage	V_{oIQ}	in analog I/Q mode		2		Vpp
Inband group delay	GD_{IB}	nominal corner frequency		5.7		us
5. Rx Synthesizer Characteristics						
Synthesizer switching time	$T_{syn,rx}$	arbitrary frequency step			100	µs
6. Rx ADC						
Resolution	N	2.5G DigRF		12/16		Bit
Output sample frequency	f_s	2.5G DigRF		1.083/ 0.541		MHz
Data Latency	D_{lat}	I channel, 26MHz sampling		8.6		us
		Q channel, 26MHz sampling		9.2		
Rx ADC full scale input voltage	FS_{ADC}			0.56		Vp
Maximum signal to noise ratio	SNR	BW = 100kHz, f_{in} = 67kHz	63	72		dB
Signal to noise & distortion ratio	SNDR	BW = 100kHz, f_{in} = 67kHz	60	69		dB

NOTES:
1 Given values are referred to the input of the LNA matching network and include the losses of the matching network.
2 Given gain conditions correspond to the values written in the Rx gain control register.

5.2 TD-SCDMA/HSDPA Receiver

General condition, unless otherwise noted: 3.2V ≤ V_{bat} ≤ 4.5V, 2.7V ≤ V_{DD3} ≤ 3.0V, 1.14V ≤ V_{DDIO} ≤ 2.0V, -30˚C ≤ T_{amb} ≤ 85˚C. Typical values are at V_{bat} = 3.7V, V_{DD3} = 2.85V, V_{DDIO} = 1.8V, T_{amb} = 25˚C. Minimum and maximum numbers apply to all frequency channels and include variations over process, voltage and temperature. All parameters are referred to the input of the Rx matching network. Rx output signal taken either at analog I/Q output or at digital I/Q output.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
1. Overall Characteristics						
Receive frequency range	f_{rx}	Bands 34(F), 39(A) and 40(E)	1880		2400	MHz
Noise figure (note 1)	NF	T_{amb} = +25˚C				dB
		high-sensitivity configuration		3.0	3.5	
		saw-less config. (Band A/F)		3.5	4.3	
		saw-less config. (Band E)		3.8	4.6	
		T_{amb} = -30˚C .. +85˚C				
		high-sensitivity configuration			4.5	
		saw-less configuration			5.5	
Input-referred 1dB compression point	iCP_{blk}	by 3.2MHz offset TD-SCDMA blocker	-50	-40		dBm
		by 4.8MHz offset TD-SCDMA blocker	-45	-40		
		by 85MHz offset CW blocker high-sensitivity configuration		-21		
		by 85MHz offset CW blocker saw-less configuration		-18		
Input-referred 1dB compression point of wanted signal	iCP_{sig}	min. Rx gain	-15			dBm
Input referred 2nd order intercept point	iIP2	of two 4.8MHz ± 0.25MHz offset CW signals	33			dBm
Input referred 3rd order intercept point	iIP3	of two 3.2/6.3MHz offset CW signals	-7			dBm
Desensitization	D_{sens}	by 3.2MHz offset, -61dBm TD-SCDMA blocker			3	dB
		by 4.8MHz offset, -49dBm TD-SCDMA blocker			3	
		by IM3 test, two 3.2 (CW) / 6.4 (TD-SCDMA) MHz offset, -46dBm signals			3	
Error vector magnitude	EVM_{rx}	QPSK signal at P_{in} = -60dBm		4		%
2. Gain and PGC Characteristics						
Max. voltage gain	$G_{rx,max}$	to one I/Q output, T_{amb} =+25℃		104		dB
Min. voltage gain	$G_{rx,min}$	to one I/Q output, T_{amb} =+25℃		-9		dB
Programmable gain range	GR_{rx}			113		dB
Gain variation over temperature relative to T_{amb} = +25℃	$\Delta Gr_{x,T}$	T_{amb} = -30℃...+85℃	-3		2.5	dB
Gain variation over frequency	$\Delta Gr_{x,f}$	Single band, fixed gain setting		0.5		dB
Progr. LNA gain range	GR_{LNA}			30		dB
Progr. LNA gain step	GS_{LNA}	GLNA from 4 to 5, 5 to 6, 6 to 7		6		dB
		GLNA<4 to GLNA=4		12		
Progr. LNA gain step accuracy	GA_{LNA}	GLNA from 4 to 5, 5 to 6, 6 to 7		±0.3		dB
		GLNA<4 to GLNA=4		±0.7		

PGC1 gain range	GR_{PGC1}			18		dB
PGC1 gain step	GS_{PGC1}			6		dB
PGC1 gain step accuracy	GA_{PGC1}	any step of 6dB		±0.3		dB
		integral error over 18dB		±0.5		
PGC2 gain range	GR_{PGC2}			65		dB
PGC2 gain step	GS_{PGC2}			1		dB
PGC2 gain step accuracy	GA_{PCG2}	max. 1dB step error		±0.15		dB
		integral error over 65dB		±0.5		
3. RF Characteristics						
Input return loss	S11			-10		dB
Max. power at LNA input	$P_{in, max}$	LNA off / LNAG<4	-10			dBm
LO leakage to LNA input pin	X_{LO}			≤-105		dBm
RX spurious emissions	EM_{RX}	30-1000MHz, in 100kHz		≤-90	-60	dBm
		1GHz – 12.75GHz, in 1MHz		≤-90	-50	
		1.88GHz – 2.96GHz, in 1MHz			-68	
4. Baseband Characteristics						
BB filter passband edge	f_c			0.72		MHz
Channel selectivity of adjancent signals	BB_{Sel}	of 1.6MHz TD-SCDMA signal, at IQ output	28	33		dB
		of 1.6MHz TD-SCDMA signal, at digital output	30	35		
		of 3.2MHz TD-SCDMA signal	70			
		of 3.2MHz CW signal	75			
		of 4-8MHz TD-SCDMA signal	90			
Image rejection ratio	IRR_{rx}	in wanted signal bandwidth	30	40		dB
I/Q differential output voltage	V_{oIQ}				2	Vpp
Static differential DC offset at I/Q BB output	$V_{DCoff,s}$	DC notch enabled			20	mV
		DC notch disabled, PGC1 ≤ 1, PGC2 ≤ 6		≤40		
Inband group delay	GD_{IB}	nominal corner frequency		1.6		us
5. Rx Synthesizer Characteristics						
Synthesizer switching time	$T_{syn,rx}$	arbitrary frequency step, 0.1ppm			100	µs
6. Rx ADC						
Resolution	N	default		10		Bit
		enhanced by RXTXDATA and RXTXEN pins as LSBs		12		
Sampling frequency	f_s			5.12		MHz
Data latency	DL	channel I		2.5		µs
		channel Q		3		µs
Rx ADC full scale input voltage	FS_{ADC}			0.56		Vp
Maximum signal to noise ratio	SNR	BW = 640kHz, f_{in} = 160kHz, referenced to full scale	50	60		dB
Maximum signal to noise and distortion ratio	SNDR	BW = 640kHz, f_{in} = 160kHz, referenced to full scale	47	57		dB

NOTES:
1 Given values are referred to the input of the LNA matching network and include the losses of the matching network.

5.3 GSM/GPRS/EDGE Transmitter

General condition, unless otherwise noted: 3.2V ≤ V_{bat} ≤ 4.5V, 2.7V ≤ V_{DD3} ≤ 3.0V, 1.14V ≤ V_{DDIO} ≤ 2.0V, DC-DC converter set to linear regulator mode, -30˚C ≤ T_{amb} ≤ 85˚C. Typical values are at V_{bat} = 3.7V, V_{DD3} = 2.85V, V_{DDIO} = 1.8V, T_{amb} = 25˚C. Minimum and maximum numbers apply to all frequency channels and include variations over process, voltage and temperature. Tx input signal applied either at analog I/Q input or DigRF data interface.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
1. General Characteristics						
Transmit frequency range	f_{tx}	low band, GSM850	824		849	MHz
		low band, GSM900	880		915	
		high band, DCS	1710		1785	
		high band, PCS	1850		1910	
Output return loss	S_{22}			<-10		dB
2. GMSK Mode Low Band						
GMSK mode output power	$P_{outGMSK}$		0.5	2.5	4.5	dBm
Modulation spectrum measurement in 30 kHz resolution BW around the carrier frequency	ModSp	at 200kHz, in 30kHz BW		-35		dBc
		at 250kHz, in 30kHz BW		-40		
		at 400kHz, in 30kHz BW		-67	-64	
		600kHz - 1.8MHz, in 30kHz BW		-67	-64	
		1.8MHz - 3MHz, in 100kHz BW			-66	
		3MHz - 6MHz, in 100kHz BW			-68	
		> 6MHz, in 100kHz			-74	
Phase noise	PhN	at 10MHz offset			-153	dBc/ Hz
		at 20MHz offset		-165		
Modulation accuracy	ModAcc	phase error rms		1		˚
		phase error peak		5		
Harmonic emission	EM	at 2x ftx				dBc
		at 3x ftx				
		at 4x ftx				
		at 5x ftx				
Carrier leakage ratio	CLR	50kHz SSB CW tone		-45		dBc
Image rejection ratio	IRR	50kHz SSB CW tone		45		dB
3rd harmonic	HD3	50kHz SSB CW tone		-45		dBc
5th harmonic	HD5	50kHz SSB CW tone		-55		dBc
3. GMSK Mode High Band						
GMSK mode output power	$P_{outGMSK}$		0.5	3	5.5	dBm
Modulation spectrum (relative to 30kHz measurement at center frequency)	ModSp	at 200kHz, in 30kHz		-35		
		at 250kHz, in 30kHz		-40		
		at 400kHz, in 30kHz		-66	-63	
		600kHz - 1.8MHz, in 30kHz		-66	-63	
		1.8MHz - 3MHz, in 100kHz			-66	
		3MHz - 6MHz, in 100kHz			-68	
		> 6MHz, in 100kHz			-74	
Phase noise	PhN	at 20MHz offset		-158		dBc/Hz
Modulation accuracy	ModAcc	phase error rms		1.5		˚
		phase error peak		5		

Harmonic emission	EM	at 2x ftx				dBc
		at 3x ftx				
		at 4x ftx				
		at 5x ftx				
Carrier leakage ratio	CLR	50kHz SSB CW tone		-45		dBc
Image rejection ratio	IRR	50kHz SSB CW tone		45		dB
3rd harmonic	HD3	50kHz SSB CW tone		-50		dBc
5th harmonic	HD5	50kHz SSB CW tone		-60		dBc
4. 8-PSK Mode Low Band						
Maximum output power	P_{outMax}		-2	0		dBm
Minimum output power	P_{outMin}				-32	dBm
Modulation spectrum measurement in 30 kHz resolution BW around the carrier frequency	ModSp	at 200kHz, in 30kHz		-35		dBc
		at 250kHz, in 30kHz		-40		
		at 400kHz, in 30kHz		-65	-62	
		600kHz - 1.8MHz, in 30kHz		-68	-64	
		1.8MHz - 3MHz, in 100kHz			-66	
		3MHz - 6MHz, in 100kHz			-68	
		> 6MHz, in 100kHz			-74	
Output noise	PhN	at 10MHz offset; P_{out}>-8dBm			-147	dBc/Hz
		at 20MHz offset; P_{out}>-8dBm		-160		
Modulation accuracy	EVM_{RMS}	RMS EVM		2.5		%
	OOS	origin offset suppression	33	40		dB
	EVM_{Pk}	peak EVM				%
Harmonic emission	EM	at 2x ftx				dBc
		at 3x ftx				
		at 4x ftx				
		at 5x ftx				
Carrier leakage ratio	CLR	50kHz SSB CW tone		-45		dBc
Image rejection ratio	IRR	50kHz SSB CW tone		45		dB
3rd harmonic	HD3	50kHz SSB CW tone		-45		dBc
5th harmonic	HD5	50kHz SSB CW tone		-50		dBc
5. 8-PSK Mode High Band						
Maximum output power	P_{outMax}		-2	0		dBm
Minimum output power	P_{outMin}				-40	dBm
Modulation spectrum (relative to 30kHz measurement at center frequency)	ModSp	at 200kHz, in 30kHz		-35		dBc
		at 250kHz, in 30kHz		-40		
		at 400kHz, in 30kHz		-64	-60	
		600kHz - 1.8MHz, in 30kHz		-66	-63	
		1.8MHz - 3MHz, in 100kHz			-66	
		3MHz - 6MHz, in 100kHz			-68	
		> 6MHz, in 100kHz			-74	
Output noise	PhN	at 20MHz offset; Pout>-12dBm	-150	-154		dBc/Hz
Modulation accuracy	EVM_{RMS}	RMS EVM		3.5		%
	OOS	origin offset suppression	33	40		dB
	EVM_{Pk}	peak EVM				%

Harmonic emission	EM	at 2x ftx				dBc
		at 3x ftx				
		at 4x ftx				
		at 5x ftx				
Carrier leakage ratio	CLR	50kHz SSB CW tone		-45		dBc
Image rejection ratio	IRR	50kHz SSB CW tone		45		dB
3rd harmonic	HD3	50kHz SSB CW tone		-50		dBc
5th harmonic	HD5	50kHz SSB CW tone		-60		dBc
6. Baseband Filter Characteristics						
Filter attenuation	Attn	1.8MHz -3MHz	15			dB
		3MHz - 6MHz	38			
		6MHz - 10MHz	65			
		10MHz - 20MHz	85			
		> 20MHz				
7. Analog I/Q Interface						
I/Q differential input voltage	$V_{ilQ1.0}$		0.944	1	1.059	Vpk
Allowed differential DC offset voltage at I/Q input	$V_{DCoffTx}$				15	mV
8. Digital Serial Interface						
Symbol rate, stream mode		DigRF2.5G specification		1.083		Msps
9. Tx Synthesizer Characteristics						
Sythesizer settling time	T_{SynTx}	arbitrary frequency step			100	µs

5.4 TD-SCDMA Transmitter

General condition, unless otherwise noted: 3.2V ≤ V_{bat} ≤ 4.5V, 2.7V ≤ V_{DD3} ≤ 3.0V, 1.14V ≤ V_{DDIO} ≤ 2.0V, -30˚C ≤ T_{amb} ≤ 85˚C. Typical values are at V_{bat} = 3.7V, V_{DD3} = 2.85V, V_{DDIO} = 1.8V, T_{amb} = 25˚C. Minimum and maximum numbers apply to all frequency channels and include variations over process, voltage and temperature. Tx input signal applied either at analog or parallel digital I/Q interface.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
1. Overall Characteristics						
Transmit frequency range	f_{tx}	Bands 34(F), 39(A) and 40(E)	1880		2400	MHz
Maximum output power	$P_{out,max}$		0.5			dBm
Minimum output power	$P_{out,min}$				-80	dBm
Output power variation over Tx channels	$\Delta P_{out,f}$	over all channels within one band (1880-1920MHz and 2010-2025MHz), for fixed PGC setting		0.3		dB
Output power variation with temperature	$\Delta P_{out,T}$	T_{amb} = -30˚C, relative to T_{amb} = 25˚C, at any fixed channel and PGC setting		0.6		dB
		T_{amb} = 85˚C, relative to T_{amb} = 25˚C, at any fixed channel and PGC setting		-1.4		
Adjacent channel leakage ratio at ±1.6MHz	ACLR	Pout =-40dBm..0.5dBm		-45		dBc
		Pout <-40dBm			-85	dBm
Alternate channel leakage ratio at ± 3.2MHz offset	AltCLR	Pout = -23dBm .. 0.5dBm		-62	-55	dBc
		Pout < -23dBm			-85	dBm
Output 1dB compression point	oCP	max. Tx gain		7.5		dBm
Output 3rd-order intercept point	oIP3	max. Tx gain		20		dBm
Carrier leakage ratio	CLR	Pout > -37dBm		-40	-25	dBc
		Pout = -67dBm .. -37dBm			-17	
Error vector magnitude	EVM_{tx}	Pout = -37dBm .. Pout,max		3.5	7	%
		Pout = -67dBm .. 37dBm		7	15	
2. Gain and PGC Characteristics						
Programmable gain range	GR_{tx}		85			dB
Programmable gain step resolution	GS_{tx}			0.125		dB
Programmable gain step accuracy	GSA_{tx}	max. 1dB step error				dB
		$G_{tx,max}$ to $G_{tx,max}$ -20dB			±0.2	
		$G_{tx,max}$ -20dB to $G_{tx,max}$ -44dB			±0.3	
		$G_{tx,max}$ -44dB to $G_{tx,max}$ -70dB			±0.4	
		max. 2dB step error				
		$G_{tx,max}$ to $G_{tx,max}$ -20dB			±0.4	
		$G_{tx,max}$ -20dB to $G_{tx,max}$ -44dB			±0.6	
		$G_{tx,max}$ -44dB to $G_{tx,max}$ -70dB			±0.6	
		max. 3dB step error				
		$G_{tx,max}$ to $G_{tx,max}$ -70dB			±0.6	
		max. 10dB step error				
		$G_{tx,max}$ to $G_{tx,max}$ -70dB			±1	
		max. 20dB step error				
		$G_{tx,max}$ to $G_{tx,max}$ -70dB			±1.5	

		max. integral error $G_{tx,max}$ to $G_{tx,max}$ -70dB			±4	
Phase discontinuity for Tx gain change	$\Delta\phi_{tx}$	for any 1dB step			6	°
		for any 10dB step, $G_{tx,max}$ to $G_{tx,max}$ -20dB			15	
Settling time of output power	T_{tx}	for any Tx gain step, to within 0.5dB		1	3	µs
3. RF Characteristics						
Output return loss	S_{22}	max. value over band, at 50Ω		-10		dB
Spurious emissions at harmonics of Tx frequency	EM_{txh}	at 2x ftx at 3x ftx at 4x ftx at 5x ftx			-25 -25 -25 -30	dBc/ 1MHz
General spurious emissions at $P_{out,max}$	EM_{txg}	9-150kHz, in 1kHz 0.15-30MHz, in 10kHz 30-1000MHz, in 100 kHz 1-12.75GHz, in 1MHz >4MHz offset, excluding Tx harmonics		-105 -85 -85	-65 -65 -65 -54	dBc
Spurious emissions	EM_{txb1}	1805MHz..1850MHz			-95	dBc/ 100kHz
		1850MHz..1880MHz, ftx > 2010MHz			-95	
		1880MHz..1920MHz, ftx > 2010 MHz			-89	dBc/ 1MHz
		2010MHz..2025MHz, ftx < 1920MHz			-89	
		2300MHz..2400MHz			-89	
4. Baseband Characteristics						
BB filter passband edge	f_c			1.33		MHz
BB filter in-band ripple		up to 640kHz		±0.3		dB
BB filter group delay variation		up to 640kHz			100	ns
BB filter stop-band attenuation		fin = 5.12MHz	40	50		dB
Image rejection ratio in wanted signal bandwidth	IRR_{tx}		30	40		dB
Allowed differential DC offset voltage at I/Q input	$V_{DCoff,tx}$				15	mV
5. Tx Synthesizer Characteristics						
Synthesizer switching time	$T_{syn,tx}$	arbitrary freq. step			100	µs
6. Tx DAC						
Resolution	N			10		Bits
Conversion rate	fClk			5.12		MHz
Integral nonlinearity	INL			±0.4		LSB
Differential nonlinearity	DNL			±0.4		LSB
Residual DC offset	V_{DCoff}			±20		mV
Full scale range	FS_{DAC}			1.2		Vpp
Full scale gain error	FSGE			±8		% FS
In-band signal-to-noise ratio	SNR	BW = 640kHz	55	62		dB
Total harmonic distortion	THD	f_{IN} = 640kHz, A_{IN} = FS		-62	-55	dB

5.5 Auxiliary ADC / Ramp DAC / AFC DAC

General condition, unless otherwise noted: 3.2V ≤ V_{bat} ≤ 4.5V, 2.7V ≤ V_{DD3} ≤ 3.0V, 1.14V ≤ V_{DDIO} ≤ 2.0V, -30˚C ≤ T_{amb} ≤ 85˚C. Typical values are at V_{bat} = 3.7V, V_{DD3} = 2.85V, V_{DDIO} = 1.8V, T_{amb} = 25˚C.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
AuxADC (note 1)						
Resolution	N			12		Bit
Input Range	V_{in}	Single ended input at AuxInOut, nominal, selectable by programming	0		1.23/ 2.46	V
Conversion time	T_{conv}	Single conversion duration	20			µs
RampDAC (note 2)						
Resolution	N			12		Bit
Output-Voltage Low	V_{OL}	R_L > 100 kΩ		0.1		V
Output Voltage High	V_{OH}	R_L > 100 kΩ		2.6		V
Settling Time		To within 1% of Output Step		1		µs
AFCDAC (note 3)						
Resolution	N			12		Bit
Output-Voltage Low	V_{OL}	R_L > 100 kΩ		0.1		V
Output Voltage High	V_{OH}	R_L > 100 kΩ		2.6		V
Settling Time		To within 1% of Output Step		1		µs

NOTES:
1 Data acquisition over register read.
2 Data transfer over register write. Digital data scaling and offset adjustment available.
3 Data transfer over register write.

6. Timing Characteristics

6.1 Serial Peripheral Interface

Details for the serial peripheral interface are given in application note AN305SPI. Key numbers are given below. General condition, unless otherwise noted: V_{bat} = 3.7 V, T_{amb} = +27 ºC.

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
SPI CONTROL INTERFACE (PINS: SPI[1/2]EN, SPI[1/2]DIO, SPI[1/2]CLK, SysClkOut, SysClkEn)						
PIN: SPI[1/2]DIO						
input setup time	t_{SUW}	write operation to RF IC	3			ns
input hold time	t_{HW}	write operation to RF IC	3			ns
output stable after driving (falling) clock edge	t_{DSR}	read operation from RF IC			20	ns
output hold time after driving (falling) clock edge	t_{HR}	read operation from RF IC	3			ns
output to tristate input time after rising edge of CtrlEn	t_{OT}				12	ns
PIN: SPI[1/2]EN						
setup time before first rising edge of SPICLK	t_{SUEN}		5			ns
hold time after last falling edge of SPICLK	t_{HEN}		0			ns
PIN: SPI[1/2]CLK						
Control clock frequency	$f_{ctrlclk}$				26	MHz
Control clock high/low time	t_H, t_L	70%-70% / 30%-30% level	13			ns
PIN: SysClkOut						
System clock frequency	f_{sysclk}			26		MHz
System clock high/low time	t_H, t_L	70%-70% / 30%-30% level	13			ns
System clock fall/rise time	t_F, t_R	70%-30% / 30%-70% level	2			ns
REFERENCE CLOCK (PIN: XIN), EXTERNAL TCXO MODE						
Ref. clock frequency	f_{refclk}			26		MHz

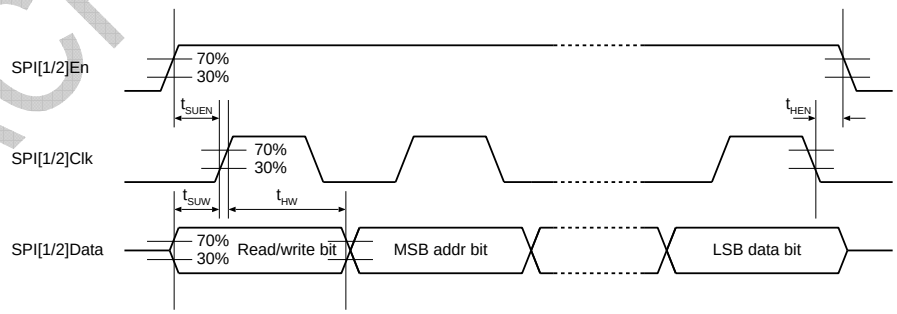

Figure 3: Serial peripheral interface timing, write mode.

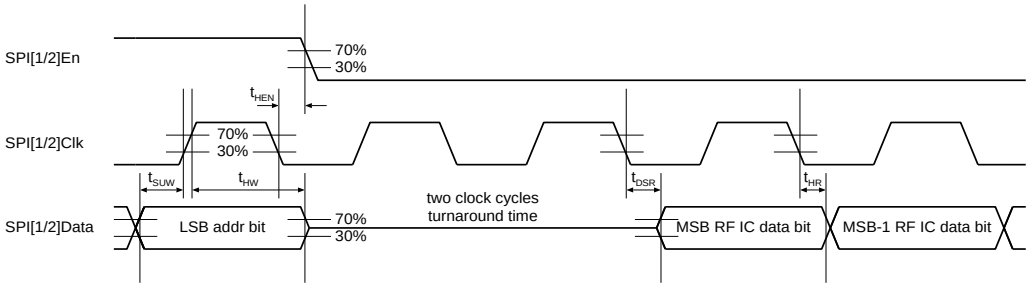

Figure 4: Serial peripheral interface timing, read mode.

6.2 Digital Parallel I/Q-Data Interface

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
DIGITAL PARALLEL I/Q-DATA INTERFACE (PINS: CLK, D0-D9, TR)						
CLK rise to channel-I output data valid	t_{DOI}	Figure 5		3	5	ns
CLK fall to channel-Q output data valid	t_{DOQ}	Figure 5		3	5	ns
CLK rise/fall to DR rise/fall time	t_{DR}	Figure 5		3	5	ns
I-DAC data to CLK fall set up time	t_{DSI}	Figure 6	5			
Q-DAC DATA to CLK rise set up time	t_{DSQ}	Figure 6	5			ns
CLK fall to I-DAC data hold	t_{DHI}	Figure 6	2			ns
CLK rise to Q-DAC data hold	t_{DHQ}	Figure 6	2			ns
CLK duty cycle				50		%
CLK duty-cycle variation				± 5		%
Digital output rise/fall time		20% to 80%		2		ns

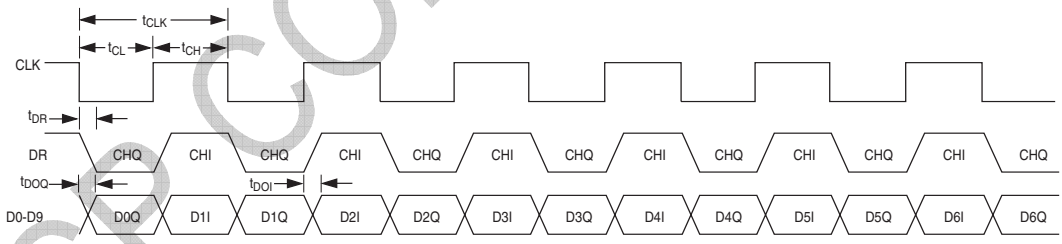

Figure 5: Rx ADC system timing diagram

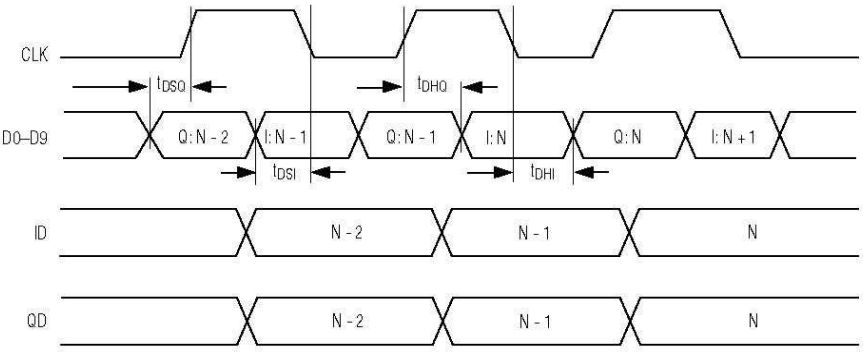

Figure 6: Tx DAC system timing diagram

6.3 Digital Serial I/Q-Data Interface

The specification is compliant with the DigRFv1.12 baseband and RF digital interface specification.

7. Application Information

7.1 Application Diagram

Conceptual application diagram is given below in Figure 7. Detailed evaluation board and reference RF subsystem schematic and layout are available upon request.

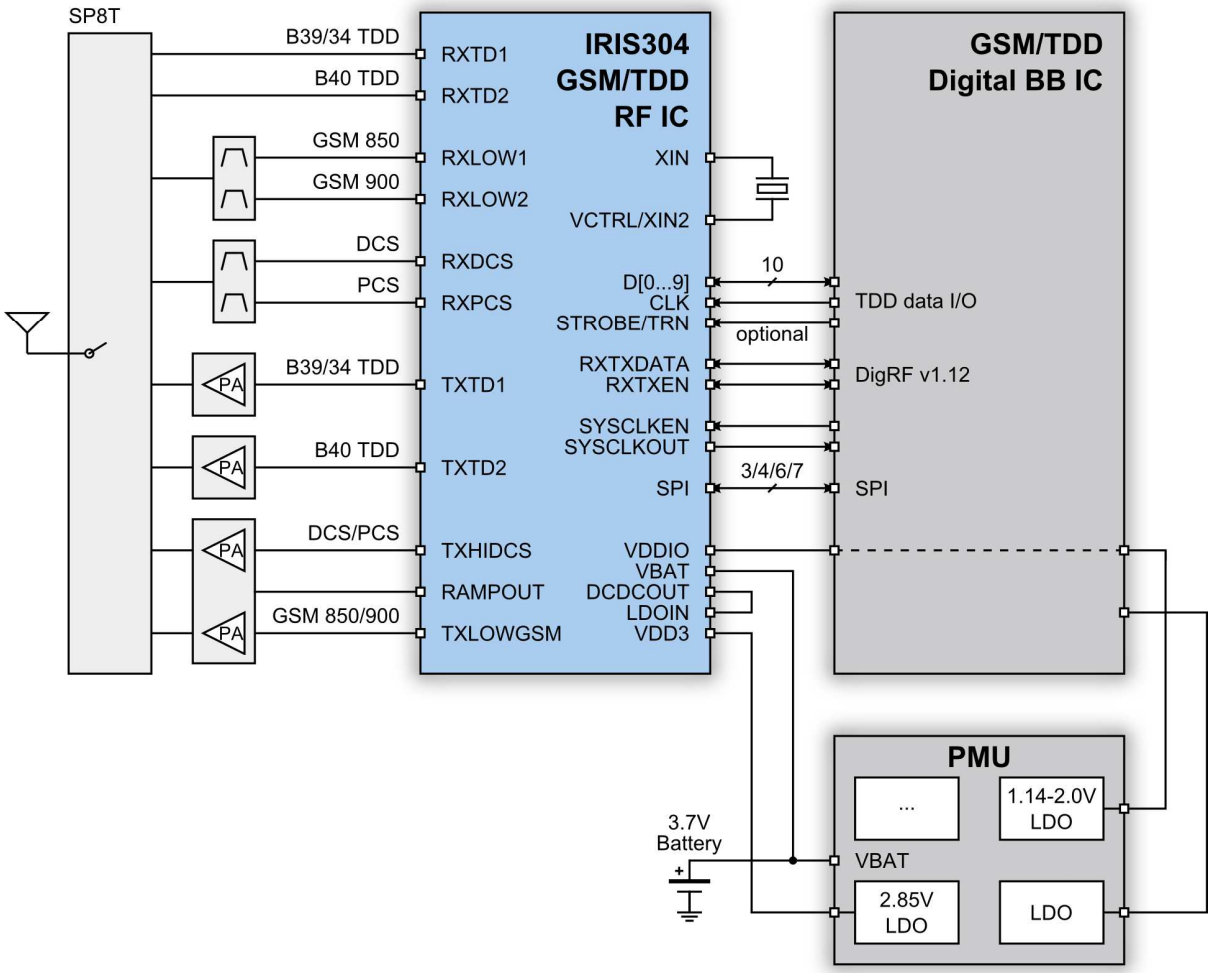

Figure 7: Triple band TD-SCDMA, quad band GSM/EDGE application diagram.

7.2 Initialization / Power-Up Sequence

IRIS304 does not have a dedicated hardware reset pin. To ensure proper IC initialization, respect the following sequence during power up:

- Raise VDDIO voltage to nominal level, while VDD3 is still off
- Set SYSCLKEN=0
- Raise VDD3 to nominal level
- Set SYSCLKEN=1

After this sequence, IRIS304 is in its known reset state and can be programmed through the SPI interfaces. Subsequent setting of SYSCLKEN=0 does not reset the IC state.

When the supplies are up, IRIS304 can still be re-initialized to its reset state using either of two mechanisms:

- By setting a bit in register 3 to 1, the IC is instructed to perform a reset the next time that SYSCLKEN pin is pulled low.

- By applying a short (<1us) SYSCLKEN=1 pulse, the following SYSCLKEN=0 phase re-initializes the IC to its reset state. BBIC must make sure not to generate SYSCLKEN=1 pulses shorter than 10us to avoid unintended resetting of IRIS304.

Note that when SYSCLKEN=0, SYSCLKOUT reference clock output is stopped! Therefore, if SYSCLKEN is used to reset IRIS304, SYSCLKOUT reference clock is interrupted. The BBIC must have an independent clock source to control SYSCLKEN during the Reset pattern!

For platforms that do not make use of all 3 auxiliary clock outputs of IRIS304 (AUCLK1, AUXCLK2, AUXCLK3), it is recommended to use AUXCLK3 and the associated AUX3EN pin as reference clock for the BBIC. SYSCLKEN pin is then only used as Reset input of IRIS304, and SYSCLKOUT is unused. The resulting application diagram is shown in Figure 8. Figure 9 illustrates the initialization of IRIS304 at power up for this case, and Figure 10 shows the case where IRIS304 is reset during operation using SYSCLKEN. AUXCLK3 reference clock to the BBIC continues during this reset.

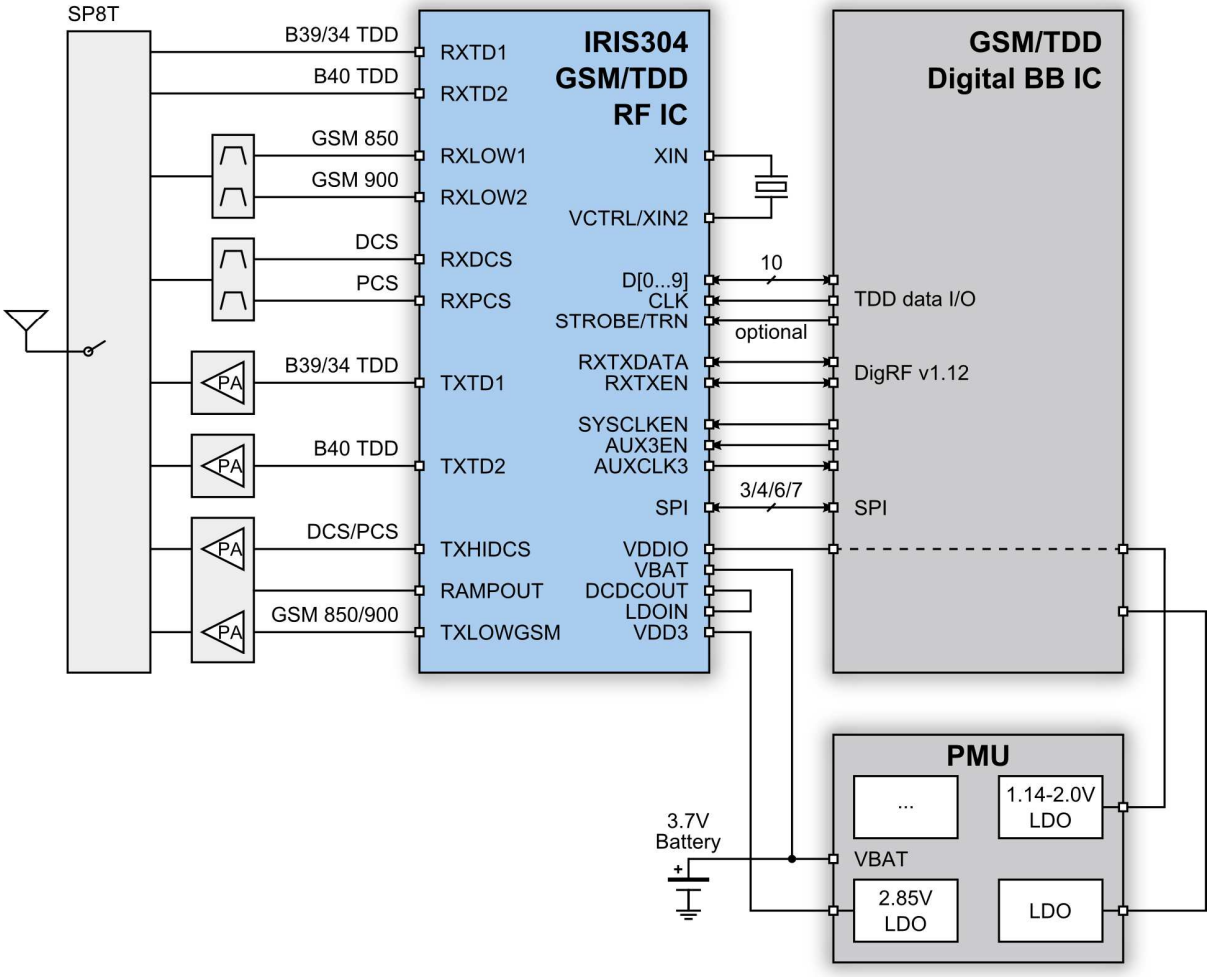

Figure 8: Application diagram with AUX3EN/AUXCLK3 used as reference clock for BBIC.

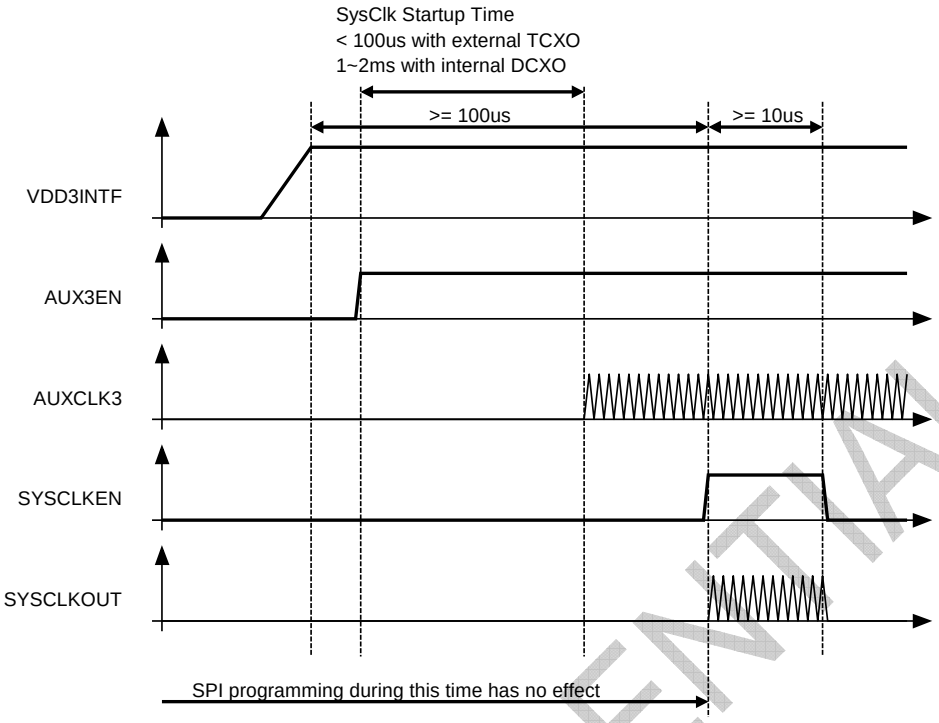

Figure 9: Power-Up Reset illustration (AUXCLK3 used as BBIC ref. clock).

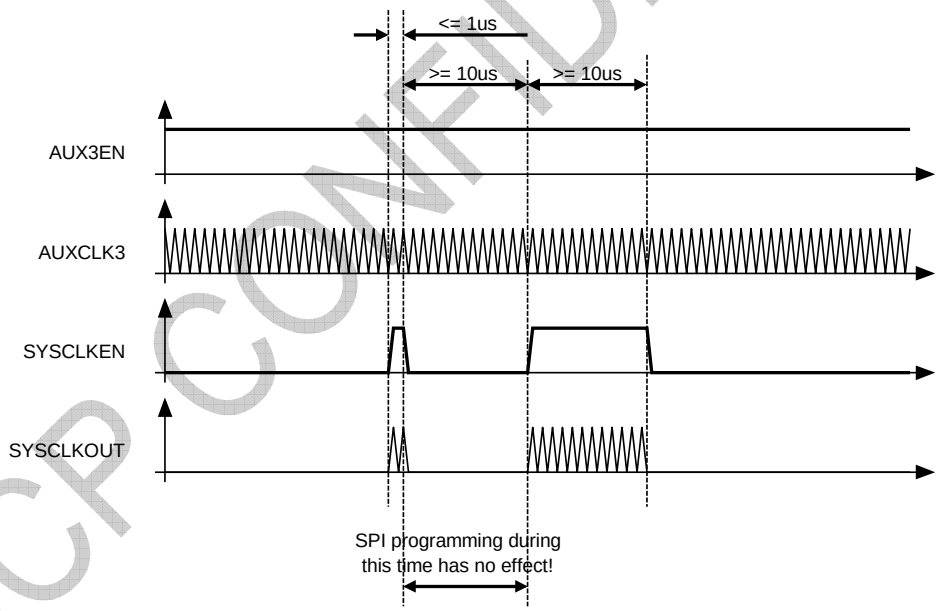

Figure 10: Illustration of reset in operation (AUXCLK3 used as BBIC ref. clock).

7.3 Migrating from IRIS305 to IRIS304

The following is a list of the differences between IRIS305 and IRIS304. Recommendations on how to migrate from IRIS305 to IRIS304 are also given.

- IRIS304 does not have independent analog I/Q interface pins. Analog I/Q operation is still supported, but with reduced flexibility in terms of common-mode levels, and not at the same time as parallel digital data transfer. Platforms employing digital data transfer between RFIC and BBIC are not affected by this.
- IRIS304 uses a single fast-settling synthesizer for TD-SCDMA and GSM/EDGE operation. Programming of the synthesizer must be adapted for both TD-SCDMA and GSM/EDGE modes.
- The TR pin of IRIS305 is replaced by STROBE/TR pin. If hardware flow control using the TR pin is not required by the BBIC, the STROBE/TR pin can be configured to be used as DigRF's STROBE signal. Arbitrary programming sequences can be started using the STROBE signal. Note that both IRIS304 and IRIS305 support parallel interface flow control using SPI programming.
- IRIS304 supports 4-wire SPI operation on SPI2 port. This allows read-operation with BBICs that cannot perform 3-wire read protocol.
- IRIS304 abandons the RESETN pin for initializing the IC. Instead, IRIS304 is initialized by following the proper power up sequence as described above. IRIS304 re-initialization can still be forced by applying a short (<1us) high pulse to the SYSCLKEN pin. The BBIC must make sure not to apply SYSCLKEN=1 pulses shorter than 10us to avoid unintended resetting of IRIS304. If BBIC cannot ensure this, an external RC filter on the SYSCLKEN line is recommended. Alternatively, SYSCLKEN can be connected to a separate BBIC GPO and be used only to reset IRIS304. AUX3EN and AUXCLK3 pins are usd to provide the BBIC reference clock in this case.
- IRIS304 maintains only two of IRIS305's five GPOs. GPO0, GPO1, and GPO4 pins are not supported by IRIS304. GPO2 and GPO3 pins are available, and their programming is identical to IRIS305. Platforms making use of GPO0, GPO1 or GPO4 pins of IRIS305 need to use BBIC GPOs instead when migrating to IRIS304.

8. Package Outline

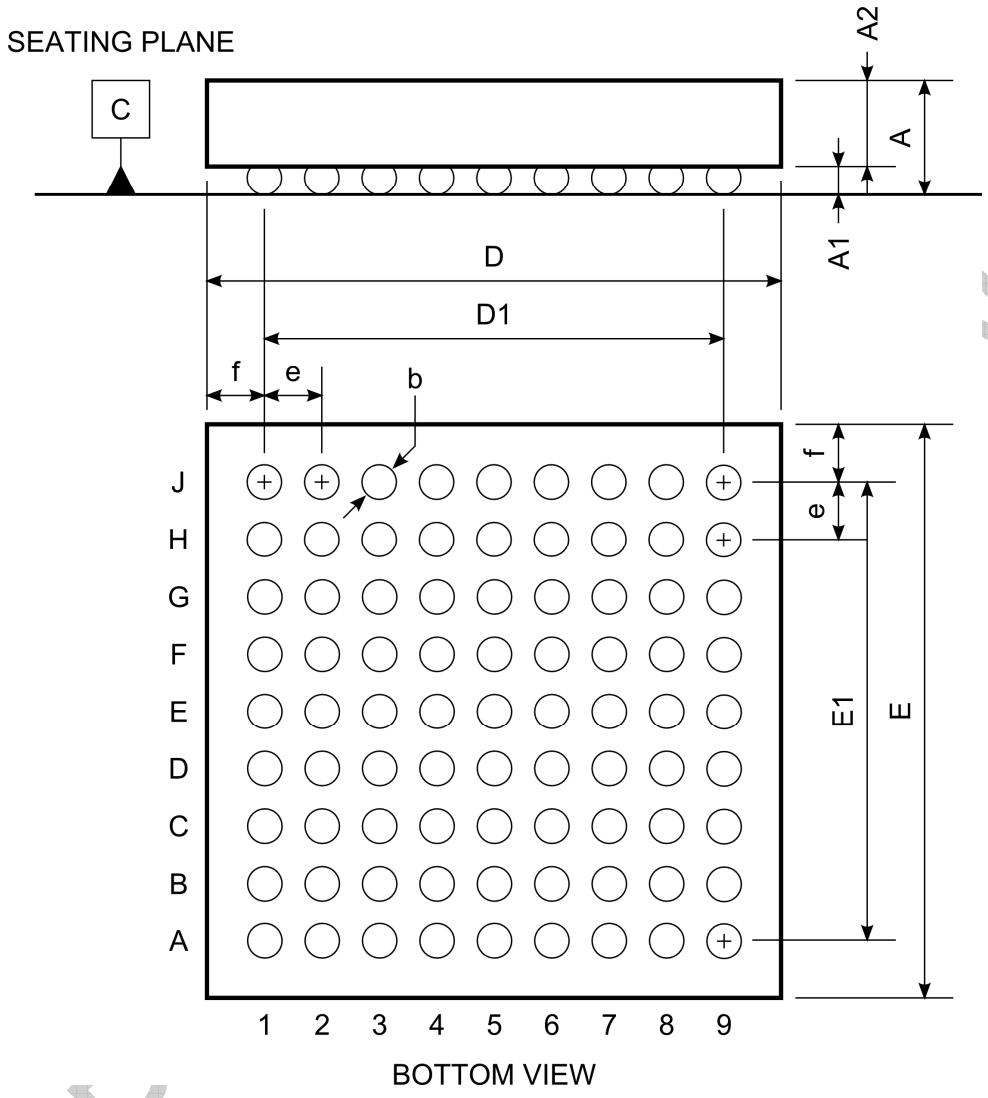

Figure 11: TFBGA81, Thin-profile Fine-pitch Ball Grid Array, 81 balls, 5 x 5 x 1.0 mm (typ.)

Table: Package dimensions (databook values), references to Figure 11.

REF.	MIN.	TYP.	MAX.	UNIT
A			1	mm
A1	0.15			mm
A2		0.7		mm
b	0.25	0.30	0.35	mm
D	4.85	5.00	5.15	mm

REF.	MIN.	TYP.	MAX.	UNIT
D1		4.00		mm
E	4.85	5.00	5.15	mm
E1		4.00		mm
e		0.50		mm
f		0.50		mm

9. Definitions

9.1 List of Abbreviations

ACLR	Adjacent channel leakage ratio	na	not applicable / not available
ACS	Adjacent/alternate channel selectivity	n. c.	not connected
BB	Baseband	PA	Power amplifier
ch.	Channel	PGC	Programmable gain control
CW	Continuous wave, single-tone sine	RF	Radio-frequency
DL	Downlink	RMS	Root-mean-square
DPCH	Dedicated physical channel	RX	Receiver
DSB	Double side-band	SAW	Surface acoustic wave
FDD	Frequency division duplex	sig.	Signal
HSDPA	High-speed downlink packet access	SPI	Serial peripheral interface
LDO	Low drop-out	TCXO	Temp.-compensated crystal oscillator
LNA	Low-noise amplifier	TFBGA	Thin-profile fine-pitch ball grid array
LR	Linear regulator	TX	Transmitter
LSB	Least significant bit	UL	Uplink
MC	Multi carrier	UTRA	Universal Terrestrial Radio Access
MSB	Most significant bit		

9.2 Data Sheet Status

TITLE	DESCRIPTION
Provisional Specification	The data sheet contains provisional specifications. All data are subject to change. Supplementary data may be published later.
Product Specification	The data sheet contains final product specifications.

9.3 Application Information

Where application information is given, it is advisory and does not form part of the specification.

Contact Information

Dr. Qiuting Huang
Advanced Circuit Pursuit AG
Zwischenweg 2
8702 Zollikon
Switzerland

Tel +41 44 390 36 14
Fax +41 44 390 36 34

http://www.newacp.ch