Rockchip RK3168 Datasheet

Revision4.2
Jun. 2015

Revision History

Date	Revision	Description
2015-6-9	V4.2	Update
2013-9-18	V4.1	Add Max CPU frequency and chapter 6
2013-04-23	V4.0	Modify some description and info.
2013-03-03	V3.0	Update arm/gpu voltage with RK3168_ANDROID4.1.1-SDK_V1.00_20130228 release
2012-12-05	V2.0	Update Ball Pin Number Order info, set chipset model to RK3168.
2012-07-04	V1.0	Initial Release.

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Chapter 1 Introduction

1.1 Overview

RK3168 is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates dual-core Cortex-A9 with separate NEON and FPU coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3168 supports almost full-format video decoder by 1080p@60fps, also support H.264 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3168 completely compatible with OpenGL ES2.0 and 1.1, OpenVG 1.1. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

This document will provide guideline on how to use RK3168 correctly and efficiently.

1.2 Features

The features listed below which may or may not be present in actual product,may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 MicroProcessor Unit

- Dual-core ARM Cortex-A9 MPCore processor , a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the two MPUs
- Integrated timer and watchdog timer per MPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 256KB unified L2 Cache
- TrustZone technology support
- Full CoreSight™ debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- One separate power domain for secondary core to support internal power switch and externally turn on/off based on different application scenario
  - PD_A9_1: 2nd Cortex-A9 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM

- External off-chip memory①
  - DDR3/DDR3L
  - LPDDR2 Async SRAM/Nor Flash
  - Async NAND Flash

- Sync Toggle NAND Flash
- Sync ONFI NAND Flash
- LBA NAND Flash

1.2.3 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device :
    - 8bits/16bits Async NAND Flash
    - 8bits ONFI NAND Flash
    - SPI0 interface
    - eMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
    - UART0 Interface

- Internal SRAM
  - Size : 16KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB continuous size

- 128KB or 256KB internal SRAM shared with L2 Cache for Cortex-A9, size is configurable by software.

1.2.4 External Memory or Storage device

- Dynamic Memory Interface(DDR3-1066/DDR3L-1066/LPDDR2-1066)
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR2 SDRAM
  - Support up to 2 ranks (chip selects), totally 2GB(max) address space, maximum address space for one rank is also 2GB, which is software-configurable.
  - 16bits/32bits data width is software programmable
  - 5 host ports with 64bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR2 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/DDR3L/LPDDR2 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and two cke output signals, make SDRAM still in self-refresh state to prevent data missing.

- Static Memory Interface (ASRAM/Nor Flash)
  - Compatible with standard async SRAM or Nor Flash
  - Support up to 2 banks (chip selects)
  - For bank0, 8bits/16bits data width is software programmable; For bank1, 16bits data width is fixed
  - Support separately data and address bus, also support shared data and address bus to save IO numbers

- Nand Flash Interface

- Support 8bits/16bits async NANDFlash, up to 4 banks
- Support 8bits sync Toggle NAND Flash, up to 4 banks
- Support 8bits sync ONFI NAND Flash, up to 4 banks
- Support LBA NANDFlash
- Up to 60bits hardware ECC
- For ToggleNAND Flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
- For async NANDFlash, support configurable interface timing , maximum data rate is 16bit/cycle
- Embedded special DMA interface to do data transfer
- Also support data transfer together with general DMAC1 in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3168
  - One oscillator with 24MHz clock input and 4 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - 6 work modes(slow mode, normal mode, idle mode, stop mode, sleep mode, power-off mode) to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 3 separate voltage domains
  - 6 separate power domains, which can be power up/down by software based on different application scenarios.

- Timer
  - 3 on-chip 32bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock

- Embedded 32-bit timer/counter facility
- Support single-run or continuous-run PWM mode
- Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 64-bit multi-layer AXI/AHB/APB composite bus architecture
  - 5 embedded AXI interconnect
    - CPU interconnect with three 64-bits AXI masters, two 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, one 32-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with six 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master and 64-bits AXI slave ,they are point-to-point AXI-lite architecture
    - VCODEC interconnect also with one 64-bits AXI master and one 32-bits AHB slave ,they are point-to-point AXI-lite architecture
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 76 SPI interrupt sources input from different components inside RK3168
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separately for each MPU, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , DMAC0 is for cpu system, DMAC1 is for peri system
  - DMAC0 features:
    - 6 channels totally
    - 11 hardware request from peripherals
    - 2 interrupt output

- Dual APB slave interface for register config, designated as secure and non-secure
- Support trustzone technology and programmable secure state for each DMA channel

- DMAC1 features:
  - 7 channels totally
  - 13 hardware request from peripherals
  - 2 interrupt output
  - Not support trustzone technology

- Security system
  - Support TrustZone technology for the following components inside RK3168
    - MPU support security and non-security mode, switch by software
    - DMAC0, support some dedicated channels work only in security mode
    - eFuse, only accessed by MPU in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(TrustZone memory adapter) and TZPC(TrustZone protection controller)

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , VP8
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 4.2: 1080p@60fps (1920x1088)③
  - MPEG-4 up to ASP level 5: 1080p@60fps (1920x1088)
  - MPEG-2 up to MP: 1080p@60fps (1920x1088)
  - MPEG-1 up to MP: 1080p@60fps (1920x1088)
  - H.263: 576p@60fps (720x576)
  - VP8: 1080p@60fps (1920x1088)
  - For H.264, Image cropping not supported
  - For MPEG-4,GMC(global motion compensation) is not supported
  - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement de-blocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080③

1.2.7 JPEG CODEC

- JPEG decoder

- Input JPEG file: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
- Output raw image: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
- Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
- Maximum data rate④ is up to 76million pixels per second

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32

1.2.8 Image Enhancement

- Image Post-Processor (IPP)(standalone)
  - memory to memory mode
  - input data format and size
    - RGB888: 16x16 to 8191x8191
    - RGB565: 16x16 to 8191x8191
    - YUV422/YUV420: 16x16 to 8190x8190
    - YUV444: 16x16 to 8190x8190
  - pre scaler
    - integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter
    - deinterlace(up to 1080i) to support YUV422&YUV420 input format
  - post scaler
    - down-scaling with 1/2 ~ 1 arbitary non-integer ratio
    - up-scaling with 1~4 arbitary non-integer ratio
    - 4-tap vertical, 2-tap horizontal filter
    - The max output image width of post scaler is 4096
  - Support rotation with 90/180/270 degrees and x-mirror,y-mirror

1.2.9 Graphics Engine

- 3D Graphics Engine :
  - Advanced Shader Feature Set – in excess of Microsoft VS3.0, PS3.0 & OGL2.0
  - Industry standard API support – Direct3D Mobile, OGL-ES 1.1 and 2.0, OpenVG 1.1, OpenMax
  - Universal Scalable Shader Engine – multi-threaded engine incorporating Pixel and Vertex Shader functionality
  - Fine grained task switching, load balancing and power management
  - Advanced geometry DMA driven operation for minimum MPU interaction
  - Programmable high quality image anti-aliasing
  - Provide MMU and L2 Cache with 64KB size

- 2D Graphics Engine :
  - Bit Blit with Stretch Blit ,Simple Blit and Filter Blit
  - Color fill with gradient fill , and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2,ROP3,ROP4 full alpha blending and transparency

- Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, and pattern mask
- 8K x 8K raster 2D coordinate system
- Arbitrary degrees rotation with anti-aliasing on every 2D primitive
- Programmable bicubic filter to support image scaling
- Blending, scaling and rotation are supported in one pass for stretch blit
- Source format :
  - ABGR8888 , XBGR888 , ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar , YUV420 semi-planar
  - YUV422 planar , YUV422 semi-planar
  - BPP8, BPP4 , BPP2 , BPP1
- Destination formats :
  - ABGR8888 , XBGR888 , ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar,YUV420 semi-planar only in filter and pre-scale mode
  - YUV422 planar , YUV422 semi-planar only in filter and pre-scale mode

1.2.10 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Display Interface
  - 2 independent display controllers
  - Support RGB LCD interfaces up to 1920x1080
  - Parallel RGB LCD Interface: RGB888(24bits),RGB666(18bits),RGB565(15bits)
  - Serial RGB LCD Interface: 3x8bits with RGB delta support, 3x8bitsfollowed by dummy data, 16bits followed by 8bits
  - MCU LCD interface : i-8080 with up to 24bits RGB
  - 4 display layers :
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YUV422, YUV420, AYUV
      - maximum resolution is 1920x1080
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
      - Support 3D display
    - One video layer (win1)
      - RGB888, ARGB888, RGB565, YUV422, YUV420,AYUV
      - maximum resolution is 1920x1080
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
    - Hardware cursor(HWC)

- 32x32x2bpp
- 3-color and transparent mode
- 2-color + transparency + tran_invert mode
- 16 level alpha blending

- 3 x 256 x 8 bits display LUTs
- Win0 and Win1 layer overlay exchangeable
- Support color space conversion:YUV to RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB to YUV
- Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
- Blank and black display
- Standby mode

1.2.11 Audio Interface

- I2S/PCM
  - Up to 2 channels (2TX, 2RX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM mode cannot be used at the same time
- SPDIF
  - Audio resolution : 16bits/20bits/24bits
  - Software configurable sample rates (48KHz, 44.1KHz, 32KHz)
  - Stereo voice replay with 2 channels

1.2.12 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - 4bits data bus widths

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface
  - Support PID filter operation
    - Combined with high-speed ADC interface to implement filter from original TS data
    - Provide PID filter up to 64 channels PID simultaneously
    - Support sync-byte detection in transport packet head
    - Support packet lost mechanism in condition of limited bandwidth

- MAC 10/100MEthernet Controller
  - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
  - Support only RMII(Reduced MII) mode
  - 10Mbps and 100Mbps compatible
  - Automatic retry and automatic collision frame deletion
  - Full duplex support with flow-control
  - Address filtering(broadcast, multicast, logical, physical)

- SPI Controller
  - 2 on-chip SPI controller inside RK3168
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively

- Support 2 chip-selects output in serial-master mode

- Uart Controller
  - 4 on-chip uart controller inside RK3168
  - DMA-based or interrupt-based operation
  - For UART1/UART2/UART3, Embedded two 32Bytes FIFO for TX and RX operation respectively
  - For UART0, two 64Bytes FIFOs are embedded for TX/RX operation
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Auto flow control mode is only for UART0, UART1, UART3

- I2C controller
  - 5 on-chip I2C controller in RK3168
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3,) , 32 GPIOs per group, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to MPU
  - GPIO0 can be used to wakeup system from stop/sleep/power-off mode
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength for all of GPIOs is software-programmable

- USB Host2.0
  - Support USB 2.0 protocol and backward compatible with the USB 1.1 protocol
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Support USB 2.0 protocol and backward compatible with the USB 1.1 protocol
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

- HSIC Interface
  - Compliant with the USB2.0 Specification and Enhanced Host Controller Interface Specification 2.0
  - 1 Port HSIC PHY Interface Operates in host mode
  - Built-in one 840x35 bits FIFO
  - Internal DMA with scatter/gather function

1.2.13 Others

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter

- Conversion speed range is up to 1 MSPS
- SAR-ADC clock must be less than 1MHz
- DNL is less than ±1 LSB , INL is less than ±2.0 LSB
- Power down current is about 0.5uA for analog and digital logic
- Power supply is 1.8V (±10%) for analog interface

- eFuse
  - 256bits (32x8) high-density electrical Fuse
  - Programming condition: VQPS must be 1.5V(±10%)
  - Program time is about 10us(±1us)
  - Read condition : VQPS must be 0V
  - Support standby mode

- Package Type
  - TFBGA453L (body: 19mm x 19mm ; ball size : 0.4mm ; ball pitch : 0.8mm)

Notes :

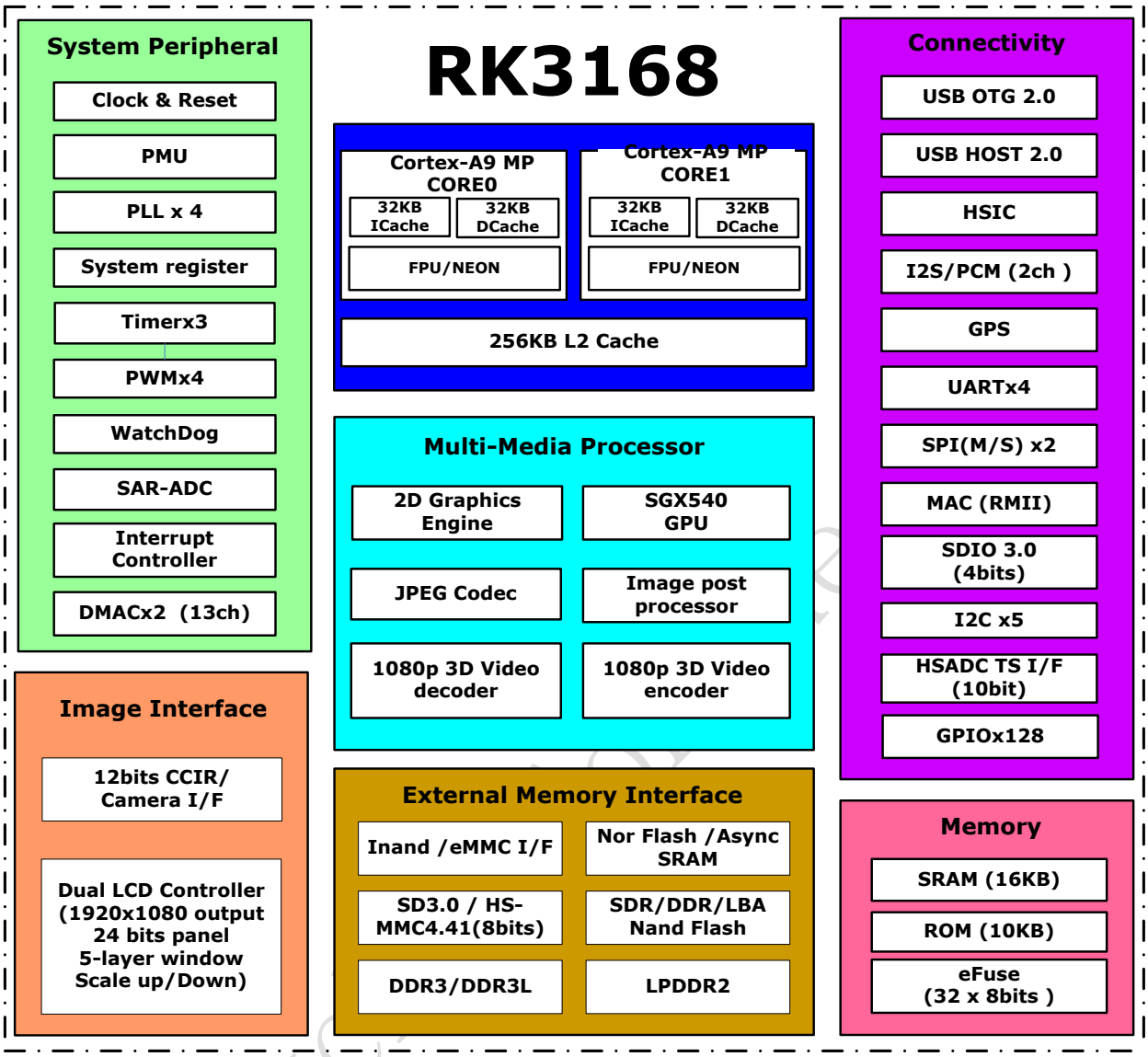
① : DDR3/DDR3L/LPDDR2 are not used simultaneously as well as async and sync Toggle NAND Flash

②: In RK3168, Video decoder and encoder are not used simultaneously because of shared internal buffer

③: Actual maximum frame rate will depend on the clock frequency and system bus performance

④: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.3 Block Diagram



The following diagram shows the basic block diagram for RK3168.

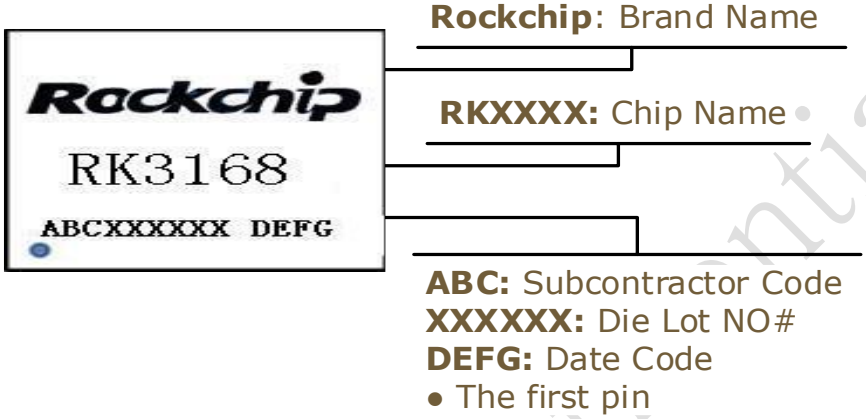
Fig. 1-1 RK3168 Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RK3168	Pb-Free	TFBGA453	700	Dual-core Cortex-A9

2.2 Top Marking



2.3 Dimension

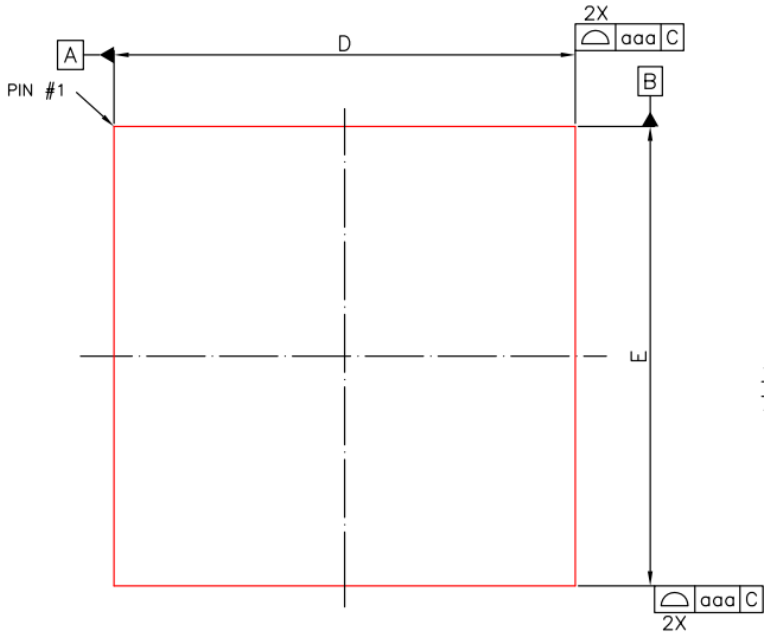
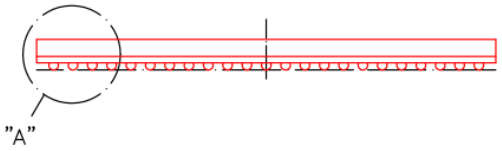


Fig. 2-1 RK3168 TFBGA453L Package Top View



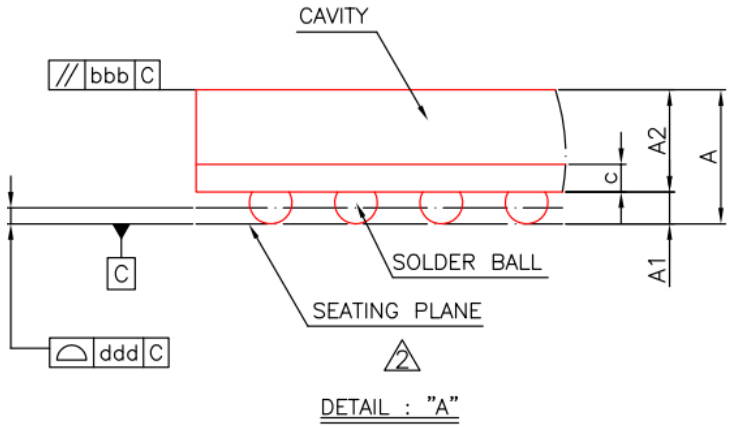


Fig. 2-2 RK3168 TFBGA453L Package Side View

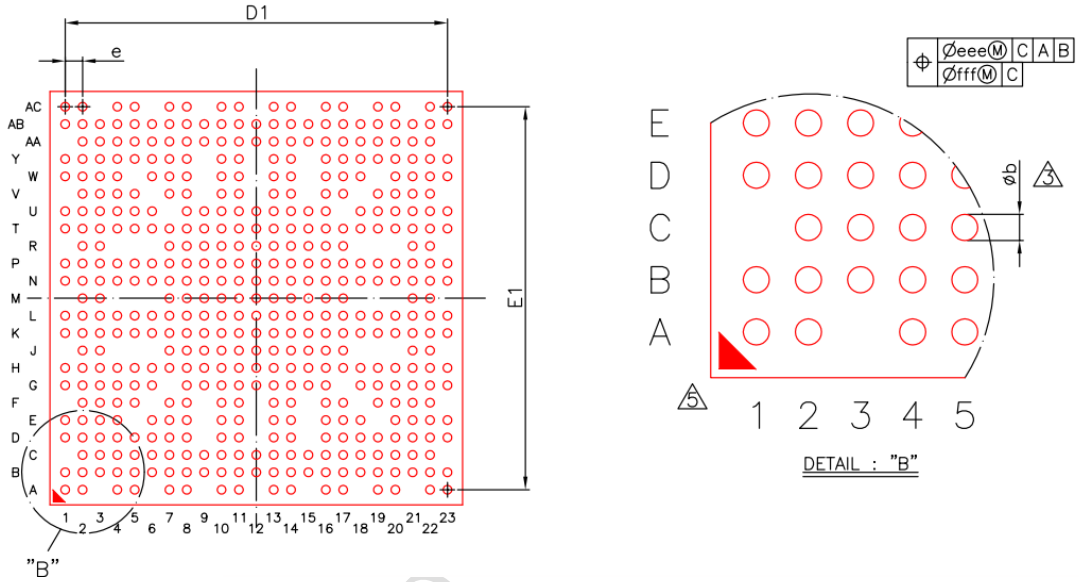
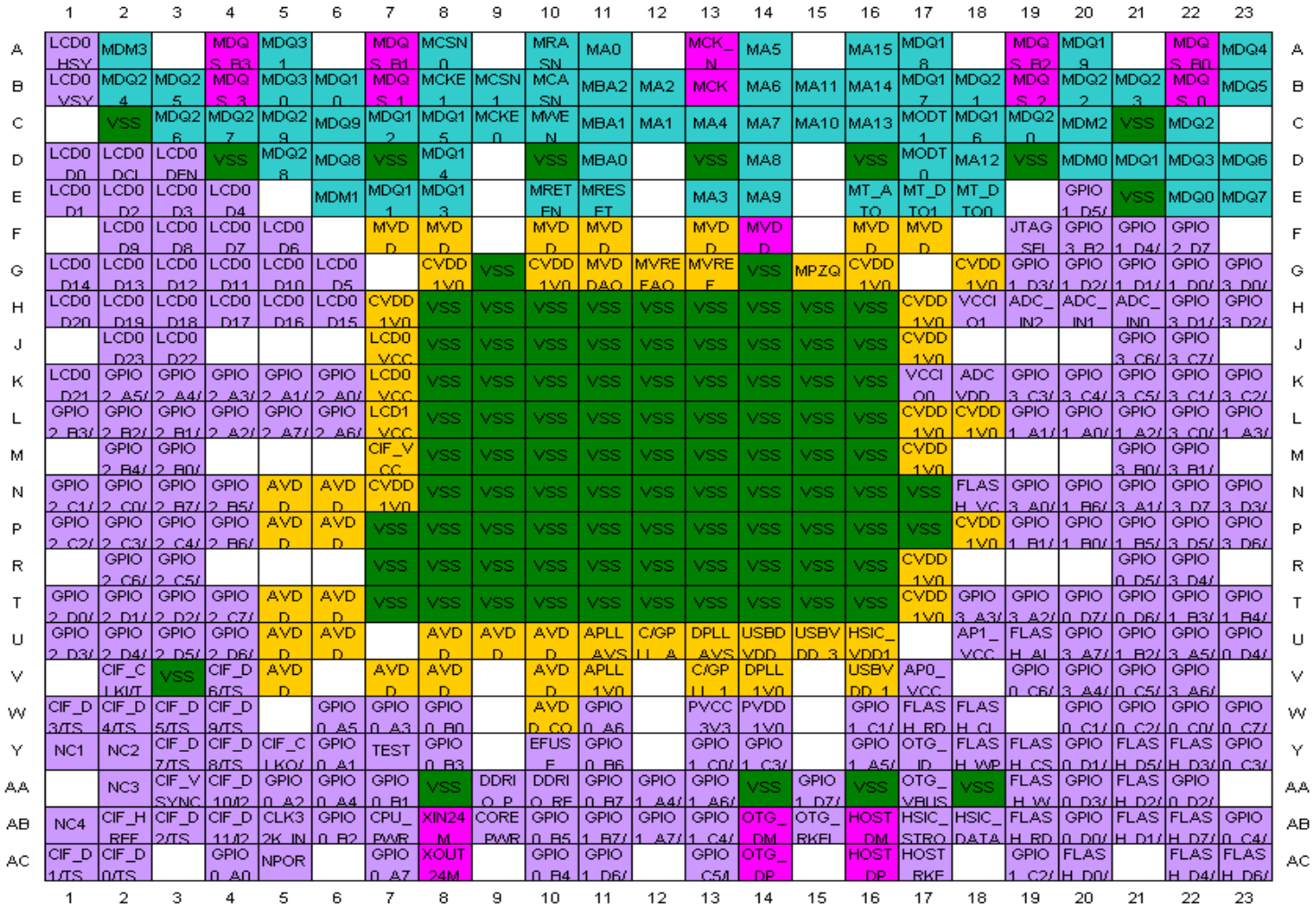


Fig. 2-3 RK3168 TFBGA453L Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Fig. 2-4 RK3168 TFBGA453L Package Dimension

2.4 Ball Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	LCD0_HSY	MDM3		MDQS_B3	MDQ31		MDQS_B1	MCSN0		MRASN	MA0		MCK_N	MA5		MA15	MDQ18		MDQS_B2	MDQ19		MDQS_B0	MDQ4
B	LCD0_VSY	MDQ24	MDQ25	MDQS_3	MDQ30	MDQ10	MDQS_1	MCKE1	MCSN1	MCASN	MBA2	MA2	MCK	MA6	MA11	MA14	MDQ17	MDQ21	MDQS_2	MDQ22	MDQ23	MDQS_0	MDQ5
C		VSS	MDQ26	MDQ27	MDQ29	MDQ9	MDQ12	MDQ15	MCKE0	MWEN	MBA1	MA1	MA4	MA7	MA10	MA13	MODT1	MDQ16	MDQ20	MDM2	VSS	MDQ2	
D	LCD0_D0	LCD0_DCL	LCD0_DEN	VSS	MDQ28	MDQ8	VSS	MDQ14		VSS	MBA0		VSS	MA8		VSS	MODT0	MA12	VSS	MDM0	MDQ1	MDQ3	MDQ6
E	LCD0_D1	LCD0_D2	LCD0_D3	LCD0_D4		MDM1	MDQ11	MDQ13		MRETEN	MRESET		MA3	MA9		MT_ATO	MT_DTO1	MT_DTO0		GPIO1_D5/	VSS	MDQ0	MDQ7
F		LCD0_D9	LCD0_D8	LCD0_D7	LCD0_D6		MVDD	MVDD		MVDD	MVDD		MVDD	MVDD		MVDD	MVDD		JTAG_SEL	GPIO3_B2	GPIO1_D4/	GPIO2_D7	
G	LCD0_D14	LCD0_D13	LCD0_D12	LCD0_D11	LCD0_D10	LCD0_D5		CVDD_1V0	VSS	CVDD_1V0	MVDDAO	MVREFAO	MVREF	VSS	MPZQ	CVDD_1V0		CVDD_1V0	GPIO1_D3/	GPIO1_D2/	GPIO1_D1/	GPIO1_D0/	GPIO3_D0/
H	LCD0_D20	LCD0_D19	LCD0_D18	LCD0_D17	LCD0_D16	LCD0_D15	CVDD_1V0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0	VCCIO1	ADC_IN2	ADC_IN1	ADC_IN0	GPIO3_D1/	GPIO3_D2/
J		LCD0_D23	LCD0_D22				LCD0_VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0				GPIO3_C6/	GPIO3_C7/	
K	LCD0_D21	GPIO2_A5/	GPIO2_A4/	GPIO2_A3/	GPIO2_A1/	GPIO2_A0/	LCD0_VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO0	ADCVDD	GPIO3_C3/	GPIO3_C4/	GPIO3_C5/	GPIO3_C1/	GPIO3_C2/
L	GPIO2_B3/	GPIO2_B2/	GPIO2_B1/	GPIO2_A2/	GPIO2_A7/	GPIO2_A6/	LCD1_VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0	CVDD_1V0	GPIO1_A1/	GPIO1_A0/	GPIO1_A2/	GPIO3_C0/	GPIO1_A3/
M		GPIO2_B4/	GPIO2_B0/				CIF_VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0				GPIO3_B0/	GPIO3_B1/	
N	GPIO2_C1/	GPIO2_C0/	GPIO2_B7/	GPIO2_B5/	AVDD	AVDD	CVDD_1V0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	FLASH_VC	GPIO3_A0/	GPIO1_B6/	GPIO3_A1/	GPIO3_D7	GPIO3_D3/
P	GPIO2_C2/	GPIO2_C3/	GPIO2_C4/	GPIO2_B6/	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0	GPIO1_B1/	GPIO1_B0/	GPIO1_B5/	GPIO3_D5/	GPIO3_D6/
R		GPIO2_C6/	GPIO2_C5/				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0				GPIO0_D5/	GPIO3_D4/	
T	GPIO2_D0/	GPIO2_D1/	GPIO2_D2/	GPIO2_C7/	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD_1V0	GPIO3_A3/	GPIO3_A2/	GPIO0_D7/	GPIO0_D6/	GPIO1_B3/	GPIO1_B4/
U	GPIO2_D3/	GPIO2_D4/	GPIO2_D5/	GPIO2_D6/	AVDD	AVDD		AVDD	AVDD	AVDD	APLL_AVS	C/GPLL_A	DPLL_AVS	USBDVDD	USBVDD_3	HSIC_VDD1		AP1_VCC	FLASH_AI	GPIO3_A7/	GPIO1_B2/	GPIO3_A5/	GPIO0_D4/
V		CIF_CLKIT	VSS	CIF_D6/TS	AVDD		AVDD	AVDD		AVDD	APLL_1V0		C/GPLL_1	DPLL_1V0		USBVDD_1	AP0_VCC		GPIO0_C6/	GPIO3_A4/	GPIO0_C5/	GPIO3_A6/	
W	CIF_D3/TS	CIF_D4/TS	CIF_D5/TS	CIF_D9/TS		GPIO0_A5	GPIO0_A3	GPIO0_B0		AVDD_CO	GPIO0_A6		PVCC_3V3	PVDD_1V0		GPIO1_C1/	FLASH_RD	FLASH_CL		GPIO0_C1/	GPIO0_C2/	GPIO0_C0/	GPIO0_C7/
Y	NC1	NC2	CIF_D7/TS	CIF_D8/TS	CIF_CLKO/	GPIO0_A1	TEST	GPIO0_B3		EFUSE	GPIO0_B6		GPIO1_C0/	GPIO1_C3/		GPIO1_A5/	OTG_ID	FLASH_WP	FLASH_CS	GPIO0_D1/	FLASH_D5/	FLASH_D3/	GPIO0_C3/
AA		NC3	CIF_VSYNC	CIF_D10/2	GPIO0_A2	GPIO0_A4	GPIO0_B1	VSS	DDRIO_P	DDRIO_RF	GPIO0_B7	GPIO1_A4/	GPIO1_A6/	VSS	GPIO1_D7/	VSS	OTG_VBUS	VSS	FLASH_W	GPIO0_D3/	FLASH_D2/	GPIO0_D2/	
AB	NC4	CIF_HREF	CIF_D2/TS	CIF_D11/2	CLK32K_IN	GPIO0_B2	CPU_PWR	XIN24M	CORE_PWR	GPIO0_B5	GPIO1_B7/	GPIO1_A7/	GPIO1_C4/	OTG_DM	OTG_RKFI	HOST_DM	HSIC_STRO	HSIC_DATA	FLASH_RD	GPIO0_D0/	FLASH_D1/	FLASH_D7/	GPIO0_C4/
AC	CIF_D1/TS	CIF_D0/TS		GPIO0_A0	NPOR		GPIO0_A7	XOUT24M		GPIO0_B4	GPIO1_D6/		GPIO_C5/	OTG_DP		HOST_DP	HOST_RKF		GPIO1_C2/	FLASH_D0/		FLASH_D4/	FLASH_D6/

Fig. 2-5 RK3168 Ball Assign

2.5 Ball Pin Number Order

Table 2-1 IO LIST

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
Part A							
A1	LCD0_HSYNC	N/A	O	LCD0_HSYNC	LCDC0_HSYNC		LCDC0
D2	LCD0_DCLK	N/A	O	LCD0_DCLK	LCDC0_DCLK		LCDC0
B1	LCD0_VSYNC	N/A	O	LCD0_VSYNC	LCDC0_VSYNC		LCDC0
D3	LCD0_DEN	N/A	O	LCD0_DEN	LCDC0_DEN		LCDC0
D1	LCD0_D0	N/A	O	LCD0_D0	LCDC0_DATA[0]		LCDC0
E1	LCD0_D1	N/A	O	LCD0_D1	LCDC0_DATA[1]		LCDC0
E2	LCD0_D2	N/A	O	LCD0_D2	LCDC0_DATA[2]		LCDC0
E3	LCD0_D3	N/A	O	LCD0_D3	LCDC0_DATA[3]		LCDC0
E4	LCD0_D4	N/A	O	LCD0_D4	LCDC0_DATA[4]		LCDC0
G6	LCD0_D5	N/A	O	LCD0_D5	LCDC0_DATA[5]		LCDC0
F5	LCD0_D6	N/A	O	LCD0_D6	LCDC0_DATA[6]		LCDC0
F4	LCD0_D7	N/A	O	LCD0_D7	LCDC0_DATA[7]		LCDC0
F3	LCD0_D8	N/A	O	LCD0_D8	LCDC0_DATA[8]		LCDC0
F2	LCD0_D9	N/A	O	LCD0_D9	LCDC0_DATA[9]		LCDC0
G5	LCD0_D10	N/A	O	LCD0_D10	LCDC0_DATA[10]		LCDC0
G4	LCD0_D11	N/A	O	LCD0_D11	LCDC0_DATA[11]		LCDC0
G3	LCD0_D12	N/A	O	LCD0_D12	LCDC0_DATA[12]		LCDC0
G2	LCD0_D13	N/A	O	LCD0_D13	LCDC0_DATA[13]		LCDC0
G1	LCD0_D14	N/A	O	LCD0_D14	LCDC0_DATA[14]		LCDC0
H6	LCD0_D15	N/A	O	LCD0_D15	LCDC0_DATA[15]		LCDC0
H5	LCD0_D16	N/A	O	LCD0_D16	LCDC0_DATA[16]		LCDC0
H4	LCD0_D17	N/A	O	LCD0_D17	LCDC0_DATA[17]		LCDC0
H3	LCD0_D18	N/A	O	LCD0_D18	LCDC0_DATA[18]		LCDC0
H2	LCD0_D19	N/A	O	LCD0_D19	LCDC0_DATA[19]		LCDC0

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
H1	LCD0_D20	N/A	O	LCD0_D20	LCDC0_DATA[20]		LCDC0
K1	LCD0_D21	N/A	O	LCD0_D21	LCDC0_DATA[21]		LCDC0
J3	LCD0_D22	N/A	O	LCD0_D22	LCDC0_DATA[22]		LCDC0
J2	LCD0_D23	N/A	O	LCD0_D23	LCDC0_DATA[23]		LCDC0
K7	LCD0_VCC0	N/A	DP	LCD0_VCC0	LCD0 power		
J7	LCD0_VCC1	N/A	DP	LCD0_VCC1	LCD0 power		
Part B							
K6	GPIO2_A0/LCD1_D0/SMC_D0	down	I/O			SMC_D0	LCDC1/SMC
K5	GPIO2_A1/LCD1_D1/SMC_D1	down	I/O			SMC_D1	LCDC1/SMC
L4	GPIO2_A2/LCD1_D2/SMC_D2	down	I/O			SMC_D2	LCDC1/SMC
K4	GPIO2_A3/LCD1_D3/SMC_D3	down	I/O			SMC_D3	LCDC1/SMC
K3	GPIO2_A4/LCD1_D4/SMC_D4	down	I/O			SMC_D4	LCDC1/SMC
K2	GPIO2_A5/LCD1_D5/SMC_D5	down	I/O			SMC_D5	LCDC1/SMC
L6	GPIO2_A6/LCD1_D6/SMC_D6	down	I/O			SMC_D6	LCDC1/SMC
L5	GPIO2_A7/LCD1_D7/SMC_D7	down	I/O			SMC_D7	LCDC1/SMC
M3	GPIO2_B0/LCD1_D8/SMC_D8	down	I/O				LCDC1/SMC
L3	GPIO2_B1/LCD1_D9/SMC_D9	down	I/O				LCDC1/SMC
L2	GPIO2_B2/LCD1_D10/SMC_D10	down	I/O				LCDC1/SMC
L1	GPIO2_B3/LCD1_D11/SMC_D11	down	I/O				LCDC1/SMC
M2	GPIO2_B4/LCD1_D12/SMC_D12	down	I/O				LCDC1/SMC
N4	GPIO2_B5/LCD1_D13/SMC_D13	down	I/O				LCDC1/SMC
P4	GPIO2_B6/LCD1_D14/SMC_D14	down	I/O				LCDC1/SMC
N3	GPIO2_B7/LCD1_D15/SMC_D15	down	I/O				LCDC1/SMC
N2	GPIO2_C0/LCD1_D16/SMC_A0	down	I/O				LCDC1/SMC
N1	GPIO2_C1/LCD1_D17/SMC_A1	down	I/O				LCDC1/SMC
P1	GPIO2_C2/LCD1_D18/SMC_A2	down	I/O				LCDC1/SMC
P2	GPIO2_C3/LCD1_D19/SMC_A3	down	I/O				LCDC1/SMC
P3	GPIO2_C4/LCD1_D20/SMC_A4	down	I/O				LCDC1/SMC

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
R3	GPIO2_C5/LCD1_D21/SMC_A5	down	I/O				LCDC1/SMC
R2	GPIO2_C6/LCD1_D22/SMC_A6	down	I/O				LCDC1/SMC
T4	GPIO2_C7/LCD1_D23/SMC_A7	down	I/O				LCDC1/SMC
T1	GPIO2_D0/LCD1_DCLK/SMC_CSN0	down	I/O				LCDC1/SMC
T2	GPIO2_D1/LCD1_DEN/SMC_WEN	down	I/O				LCDC1/SMC
T3	GPIO2_D2/LCD1_HSYNC/SMC_OEN	down	I/O				LCDC1/SMC
U1	GPIO2_D3/LCD1_VSYNC/SMC_ADVN	down	I/O				LCDC1/SMC
U2	GPIO2_D4/SMC_BLS_N0	up	I/O	3G_RST	3G module reset out		LCDC1/SMC
U3	GPIO2_D5/SMC_BLS_N1	up	I/O	3G_EN	3G power on		LCDC1/SMC
U4	GPIO2_D6/SMC_CSN1	up	I/O	HDMI_INT	HDMI insert input		LCDC1/SMC
L7	LCD1_VCC	N/A	DP	LCD1_VCC	LCD1 power		
Part C							
AC2	CIF_D0/TS_D8/GPIO3_B4	down	I/O	CIF0_PDN	Front camera power enable	TS_VALID	CIF
AC1	CIF_D1/TS_D9/GPIO3_B5	down	I/O	CIF1_PDN	Rear camera power enable	TS_FAIL	CIF
AB3	CIF_D2/TS_D0	down	I	CIF0_D2	Camera0 data port	TS_D0	CIF
W1	CIF_D3/TS_D1	down	I	CIF0_D3	Camera0 data port	TS_D1	CIF
W2	CIF_D4/TS_D2	down	I	CIF0_D4	Camera0 data port	TS_D2	CIF
W3	CIF_D5/TS_D3	down	I	CIF0_D5	Camera0 data port	TS_D3	CIF
V4	CIF_D6/TS_D4	down	I	CIF0_D6	Camera0 data port	TS_D4	CIF
Y3	CIF_D7/TS_D5	down	I	CIF0_D7	Camera0 data port	TS_D5	CIF
Y4	CIF_D8/TS_D6	down	I	CIF0_D8	Camera0 data port	TS_D6	CIF
W4	CIF_D9/TS_D7	down	I	CIF0_D9	Camera0 data port	TS_D7	CIF
AA4	CIF_D10/I2C3_SDA/GPIO3_B6	up	I/O	I2C3_SDA	I2C3 serial port,for camera		CIF
AB4	CIF_D11/I2C3_SCL/GPIO3_B7	up	I/O	I2C3_SCL	I2C3 serial port,for camera		CIF
Y1	NC	down	I	NC			CIF
Y2	NC	down	I	NC			CIF
AA2	NC	down	I	NC			CIF
AB1	NC	down	I	NC			CIF

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
AA3	CIF_VSYNC/TS_SYNC	down	I	CIF0_VSYNC	Camera0 VYSNC input	TS_SYNC	CIF
AB2	CIF_HREF	down	I	CIF0_HREF	Camera0 HREF input		CIF
V2	CIF_CLKI/TS_CLKO	down	I/O	CIF0_CLKIN	Camera0 clock input	TS_CLK	CIF
Y5	CIF_CLKO/GPIO3_B3	down	I/O	CIF0_CLKO	Camera0 clock output		CIF
M7	CIF_VCC	N/A	DP	CIF_VCC	CIF power		
Part D							
AC4	GPIO0_A0	down	I/O	PWR_HOLD	System power hold up enable		PMU
Y6	GPIO0_A1	down	I/O	PMU_SLEEP	PMIC sleep enable		PMU
AA5	GPIO0_A2	down	I/O	BL_EN	Display panel backlight power enable		PMU
W7	GPIO0_A3	down	I/O	JETTA_PWREN	jetta power enable		PMU
AA6	GPIO0_A4	up	I/O	PWR_KEY	Power key detect input		PMU
W6	GPIO0_A5	up	I/O	BT_HOST_WAKE	BT wake up MPU		PMU
W11	GPIO0_A6	up	I/O	CHG_DET	Charge status detect input		PMU
AC7	GPIO0_A7	up	I/O	OTG_INT	USB insert detect input		PMU
W8	GPIO0_B0	up	I/O	LCD_EN	Display panel power enable		PMU
AA7	GPIO0_B1	up	I/O	BAT_LOW	BAT low interrupt input		PMU
AB6	GPIO0_B2	up	I/O	DC_DET	DC insert detect input		PMU
Y8	GPIO0_B3	up	I/O	PMU_INT	PMU interrupt input		PMU
AA10	DDRIO_RET_EN		O	DDR_RETEN	DDR retention enable		PMU
AB7	CPU_PWROFF	down	O	ARM_PWROFF	ARM power off control		PMU
AB9	CORE_PWROFF	down	O	LOG_PWROFF	LOGIC power off control		PMU
AA9	DDRIO_PWROFF	down	O	DDR_PWROFF	DDR IO power off control		PMU
AB5	CLK32K_IN	down	I	CLK32K_IN	32KHz clock input		PMU
AB8	XIN24M	N/A	I	XIN24M	24MHz clock input		PMU
AC8	XOUT24M	N/A	O	XOUT24M	24MHz clock output		PMU
AC5	NPOR	N/A	I	NPOR	System reset input		PMU
W14	PVDD_1V0	N/A	DP	PVDD_1V0	PMU core power		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
W13	PVCC_3V3	N/A	DP	PVCC_3V3	PMU IO power		
Y10	EFUSE	N/A	AP	EFUSE	Default connect to 0V or floating		eFuse
Y7	TEST	N/A	AP	TEST	Default connect to 0V or floating		
V11	APLL_1V0	N/A	AP	APLL_1V0	ARM PLL power		PLL
V13	C/GPLL_1V0	N/A	AP	C/GPLL_1V0	Core/GPU PLL power		PLL
V14	DPLL_1V0	N/A	AP	DPLL_1V0	Dram PLL power		PLL
U11	APLL_AVSS	N/A	AG	AVSS_APLL	ARM PLL power GND		PLL
U12	C/GPLL_AVSS	N/A	AG	AVSS_DPLL	Core/GPU PLL power GND		PLL
U13	DPLL_AVSS	N/A	AG	AVSS_C/GPLL	Dram PLL power GND		PLL
Part E							
Y17	OTG_ID	N/A	A	OTG_ID	USB OTG ID detect input		USB
U14	USBDVDD_1V0	N/A	DP	USBVDD_1V0	USB core power		USB
AA17	OTG_VBUS	N/A	A	OTG_VBUS	USB device connected detect input		USB
U15	USBVDD_3V3	N/A	AP	USBVDD_3V3	USB IO power		USB
AC14	OTG_DP	N/A	A	OTG_DP	USB OTG data positive port		USB
AB14	OTG_DM	N/A	A	OTG_DM	USB OTG data negative port		USB
AB15	OTG_RKELVIN	N/A	A	OTG_RKELVIN	USB OTG fire reference voltage output,connect a 43.2R%1 resistor		USB
V16	USBVDD_1V8	N/A	AP	USBVDD_1V8	USB analog power		USB
AC16	HOST_DP	N/A	A	HOST_DP	USB host data positive port		USB
AB16	HOST_DM	N/A	A	HOST_DM	USB host data negative port		USB
AC17	HOST_RKELVIN	N/A	A	HOST_RKELVIN	USB HOST fire reference voltage output,connect a 43.2R%1 resistor		USB
H19	ADC_IN2	N/A	A	GPS_LRADC	GPS Vtune input		SAR-ADC
H20	ADC_IN1	N/A	A	ADKEY_IN	AD key input		SAR-ADC

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
H21	ADC_IN0	N/A	A	BAT_DET	SARADC input		SAR-ADC
K18	ADCVDD_1V8	N/A	P	ADCVDD_1V8	SARADC analog power		SAR-ADC
F19	JTAG_SEL	down	I/O				GPIO
AB17	HSIC_STROBE						HSIC
AB18	HSIC_DATA						HSIC
U16	HSIC_VDD12						
Part F							
AC10	GPIO0_B4	up	I/O	GYR_INT	Gyroscope interrupt input		AP1
AB10	GPIO0_B5	up	I/O	RTC_INT	RTC interrupt input		AP1
Y11	GPIO0_B6	up	I/O	TP_RST	Touch panel reset out		AP1
AA11	GPIO0_B7	up	I/O	GSENSOR_INT	G-sensor interrupt input		AP1
AA12	GPIO1_A4/UART1_RX/SPI0_RXD	up	I/O	UART1_SIN	UART1 serial port, for 3G		AP1
Y16	GPIO1_A5/UART1_TX/SPI0_TXD	down	I/O	UART1_SOUT	UART1 serial port, for 3G		AP1
AA13	GPIO1_A6/UART1_CTSN/SPI0_CLK	up	I/O	UART1_CTS	UART1 serial port, for 3G		AP1
AB12	GPIO1_A7/UART1_RTSN/SPI0_CSN0	up	I/O	UART1_RTS	UART1 serial port, for 3G		AP1
AB11	GPIO1_B7/SPI0_CSN1	up	I/O	TP_INT	Touch panel/key interrupt input		AP1
AC11	GPIO1_D6/I2C4_SDA	up	I/O	I2C4_SDA	I2C4 serial port for RK610		AP1
AA15	GPIO1_D7/I2C4_SCL	up	I/O	I2C4_SCL	I2C4 serial port for RK610		AP1
Y13	GPIO1_C0/I2S_CLK	down	I/O	I2S0_CLK	I2S0 port, for audio part		AP1
W16	GPIO1_C1/I2S_SCLK	down	I/O	I2S0_SCLK	I2S0 port, for audio part		AP1
AC19	GPIO1_C2/I2S_LRCK_RX	down	I/O	I2S0_LRCK_RX	I2S0 port, for audio part		AP1
Y14	GPIO1_C3/I2S_LRCK_TX	down	I/O	I2S0_LRCK_TX	I2S0 port, for audio part		AP1
AB13	GPIO1_C4/I2S_SDI	down	I/O	I2S0_SDI	I2S0 port, for audio part		AP1
AC13	GPIO1_C5/I2S_SDO	down	I/O	I2S0_SDO	I2S0 port, for audio part		AP1
U18	AP1_VCC	N/A	DP	AP1_VCC	AP1 power		
Part G							
T19	GPIO3_A2/SDMMC0_CLKO	down	I/O	SDMMC0_CLKO	SD/MMC clock output		GPIO
T18	GPIO3_A3/SDMMC0_CMD	up	I/O	SDMMC0_CMD	SD/MMC command		GPIO

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
V20	GPIO3_A4/SDMMC0_D0	up	I/O	SDMMC0_D0	SD/MMC data port		GPIO
U22	GPIO3_A5/SDMMC0_D1	up	I/O	SDMMC0_D1	SD/MMC data port		GPIO
V22	GPIO3_A6/SDMMC0_D2	up	I/O	SDMMC0_D2	SD/MMC data port		GPIO
U20	GPIO3_A7/SDMMC0_D3	up	I/O	SDMMC0_D3	SD/MMC data port		GPIO
N19	GPIO3_A0/SDMMC0_RSTN	up	I/O	SDMMC0_RSTNO	SD/MMC reset output		GPIO
N21	GPIO3_A1/SDMMC0_PWR	down	I/O	SDMMC0_PWR	SD/MMC power enable		GPIO
M21	GPIO3_B0/SDMMC0_DET	up	I/O	SDMMC0_DET	SD/MMC detect input		GPIO
M22	GPIO3_B1/SDMMC0_WP	down	I/O	SDMMC0_WP	SD/MMC write protection detect input		GPIO
Part H							
L20	GPIO1_A0/UART0_RX	up	I/O	UART0_RX	UART0 serial port, for BT module	GPIO1_A0	AP0
L19	GPIO1_A1/UART0_TX	down	I/O	UART0_TX	UART0 serial port, for BT module	GPIO1_A1	AP0
L21	GPIO1_A2/UART0_CTSN	up	I/O	UART0_CTSN	UART0 serial port, for BT module	GPIO1_A2	AP0
L23	GPIO1_A3/UART0_RTSN	up	I/O	UART0_RTSN	UART0 serial port, for BT module	GPIO1_A3	AP0
L22	GPIO3_C0/SDMMC1_CMD/RMII_TX_EN	up	I/O	SDMMC1_CMD	SDIO1 port, for WIFI module		AP0
K22	GPIO3_C1/SDMMC1_D0/RMII_TX_D1	up	I/O	SDMMC1_D0	SDIO2 port, for WIFI module		AP0
K23	GPIO3_C2/SDMMC1_D1/RMII_TX_D0	up	I/O	SDMMC1_D1	SDIO3 port, for WIFI module		AP0
K19	GPIO3_C3/SDMMC1_D2/RMII_RX_D0	up	I/O	SDMMC1_D2	SDIO4 port, for WIFI module		AP0
K20	GPIO3_C4/SDMMC1_D3/RMII_RX_D1	up	I/O	SDMMC1_D3	SDIO5 port, for WIFI module		AP0
K21	GPIO3_C5/SDMMC1_CLKO/RMII_CLKO	down	I/O	SDMMC1_CLKO	SDIO6 port, for WIFI module		AP0
J21	GPIO3_C6/SDMMC1_DET/RMII_RX_ERR	down	I/O	BT_WAKE	CPU wake up BT module		AP0
J22	GPIO3_C7/SDMMC1_WP/RMII_CSR_VALID	down	I/O	BT_REG_ON	BT internal regulators power enable		AP0
G23	GPIO3_D0/SDMMC1_PWR/MII_MD	down	I/O	WIFI_REG_ON	WIFI internal regulators power enable		AP0
H22	GPIO3_D1/SDMMC1_BACKEND/MII_MDCLK	down	I/O	BT_RST	BT module reset out		AP0

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
H23	GPIO3_D2/SDMMC1_INT	down	I/O	WIFI_HOST_WAKE	WIFI wake up MPU		AP0
V17	AP0_VCC	N/A	DP	AP0_VCC	AP0 power		
Part I							
AC20	FLASH_D0/EMMC_D0	down	I/O	FLASH_D0	NAND flash/EMMC data port	EMMC_D0	FLASH
AB21	FLASH_D1/EMMC_D1	down	I/O	FLASH_D1	NAND flash/EMMC data port	EMMC_D1	FLASH
AA21	FLASH_D2/EMMC_D2	down	I/O	FLASH_D2	NAND flash/EMMC data port	EMMC_D2	FLASH
Y22	FLASH_D3/EMMC_D3	down	I/O	FLASH_D3	NAND flash/EMMC data port	EMMC_D3	FLASH
AC22	FLASH_D4/EMMC_D4	down	I/O	FLASH_D4	NAND flash/EMMC data port	EMMC_D4	FLASH
Y21	FLASH_D5/EMMC_D5	down	I/O	FLASH_D5	NAND flash/EMMC data port	EMMC_D5	FLASH
AC23	FLASH_D6/EMMC_D6	down	I/O	FLASH_D6	NAND flash/EMMC data port	EMMC_D6	FLASH
AB22	FLASH_D7/EMMC_D7	down	I/O	FLASH_D7	NAND flash/EMMC data port	EMMC_D7	FLASH
W17	FLASH_RDY	up	I	FLASH_RDY	NAND flash read/busy output		FLASH
Y18	FLASH_WP/EMMC_PWR	down	O	FLASH_WP/EMMC_PWREN	NAND flash write protect		FLASH
AB19	FLASH_RDN	up	O	FLASH_RDN	NAND flash read enable		FLASH
U19	FLASH_ALE	down	O	FLASH_ALE	NAND flash address latch enable		FLASH
W18	FLASH_CLE	down	O	FLASH_CLE	NAND flash command latch enable		FLASH
AA19	FLASH_WRN	up	O	FLASH_WRN	NAND flash write enable		FLASH
Y19	FLASH_CSN0	up	O	FLASH_CSN0	NAND flash select0 port		FLASH
Y20	GPIO0_D1/FLASH_CSN1	up	I/O	FLASH_CSN1	NAND flash select1 port		FLASH
AA22	GPIO0_D2/FLASH_CSN2/EMMC_CMD	up	I/O	FLASH_CSN2/EMMC_CMD	NAND flash select2 port/EMMC command port		FLASH
AA20	GPIO0_D3/FLASH_CSN3/EMMC_RSTN	up	I/O	FLASH_CSN3/EMMC_RST	NAND flash select3 port/EMMC reset output		FLASH
AB20	GPIO0_D0/FALSH_DQS/EMMC_CLKO	down	I/O	FLASH_DQS/EMMC_CLKO	NANDFlash DQS/EMMC clock out	EMMC_CLKO	FLASH
W22	GPIO0_C0/FLASH_D8	down	I/O	HOST_DRV_VBUS	USB host power control ouput		FLASH
W20	GPIO0_C1/FLASH_D9	down	I/O	CHG_CTL	Charge control		FLASH

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
W21	GPIO0_C2/FLASH_D10	down	I/O	CHG_EN	Charge enable		FLASH
Y23	GPIO0_C3/FLASH_D11	down	I/O	FLASHLED_CTL	Camera flashlight enable		FLASH
AB23	GPIO0_C4/FLASH_D12	down	I/O	3G_WAKEUP_IN	HOST to set 3G module into sleep or wake up		FLASH
V21	GPIO0_C5/FLASH_D13	down	I/O	3G_WAKEUP_OUT	3G module to wake up the HOST		FLASH
V19	GPIO0_C6/FLASH_D14	down	I/O	3G_PWR	3G module power enable		FLASH
W23	GPIO0_C7/FLASH_D15	down	I/O	VIB_CTL	Vibration control		FLASH
N18	FLASH_VCC	N/A	DP	FLASH_VCC1	Flash/EMMC power		
Part J							
G22	GPIO1_D0/I2C0_SDA	up	I/O	I2C0_SDA	I2C0 serial port,for constant power supply device,need external pull-up		GPIO
G21	GPIO1_D1/I2C0_SCL	up	I/O	I2C0_SCL	I2C0 serial port,for constant power supply device,need external pull-up		GPIO
G20	GPIO1_D2/I2C1_SDA	up	I/O	I2C1_SDA	I2C1 serial port, for external PMIC/RTC,need external pull-up		GPIO
G19	GPIO1_D3/I2C1_SCL	up	I/O	I2C1_SCL	I2C1 serial port, for external PMIC/RTC,need external pull-up		GPIO
F21	GPIO1_D4/I2C2_SDA	up	I/O	I2C2_SDA	I2C2 serial port, for touch panel ,need external pull-up		GPIO
E20	GPIO1_D5/I2C2_SCL	up	I/O	I2C2_SCL	I2C2 serial port, for touch panel ,need external pull-up		GPIO
P20	GPIO1_B0/UART2_RX/JTAG_TDI	up	I/O	UART2_RX	UART2 data input,for debug	TDI	GPIO
P19	GPIO1_B1/UART2_TX/JTAG_TDO	down	I/O	UART2_TX	UART2 data output,for debug	TDO	GPIO
U21	GPIO1_B2/UART3_RX/GPS_MAG	up	I/O	UART3_RX/GPS_MAG	UART3 serial port , for GPS module		GPIO
T22	GPIO1_B3/UART3_TX/GPS_SIG	down	I/O	UART3_TX/GPS_SIG	UART3 serial port , for GPS		GPIO

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
					module		
T23	GPIO1_B4/UART3_CTSN/GPS_CLK	up	I/O	UART3_CTSN/GPS_CLK	UART3 serial port , for GPS module		GPIO
P21	GPIO1_B5/UART3_RTSN	up	I/O	UART3_RTSN	UART3 serial port , for GPS module		GPIO
N23	GPIO3_D3/PWM0	down	I/O	ARM CORE_CTL/DVS0_CTL	ARM core power voltage control		GPIO
R22	GPIO3_D4/PWM1/JTAG_TRSTN	down	I/O	CPU CORE_CTL/DVS1_CTL	CPU core power voltage control	TRSTN	GPIO
P22	GPIO3_D5/PWM2/JTAG_TCK	up	I/O	OTG_DRV_VBUS	USB OTG power control output	TCK	GPIO
P23	GPIO3_D6/PWM3/JTAG_TMS	up	I/O	LCD_BL	Display panel backlight brightness control	TMS	GPIO
U23	GPIO0_D4/SPI1_RX	down	I/O	GPS_PWR	GPS module power enable		GPIO
R21	GPIO0_D5/SPI1_TX	down	I/O	SPI1_MOSI/GPS_RST	SPI_MOSI for GPS tuner setting/reset out to GPS module		GPIO
T21	GPIO0_D6/SPI1_CLK	down	I/O	SPI1_CLK	SPI_CLK for GPS tuner setting		GPIO
T20	GPIO0_D7/SPI1_CSN0	down	I/O	SPI1_CS	SPI_CS for GPS tuner setting		GPIO
N20	GPIO1_B6/SPDIF_TX/SPI1_CSN1	down	I/O	LCD_CS/SPDIF_TX	LVDS IC shutdown/Digital audio optical output (SPDIF_TX)		GPIO
N22	GPIO3_D7	down	I/O	COMPASS_INT	Compass interrupt input		GPIO
F22	GPIO2_D7	down	I/O	SPK_CTL	Speaker mute enable		GPIO
F20	GPIO3_B2	down	I/O	JETTA_RESET	Jetta reset output		GPIO
Part K							
E22	MDQ0	N/A	I/O	MDQ0	DRAM data port		DDR
D21	MDQ1	N/A	I/O	MDQ1	DRAM data port		DDR
C22	MDQ2	N/A	I/O	MDQ2	DRAM data port		DDR
D22	MDQ3	N/A	I/O	MDQ3	DRAM data port		DDR
A23	MDQ4	N/A	I/O	MDQ4	DRAM data port		DDR
B23	MDQ5	N/A	I/O	MDQ5	DRAM data port		DDR

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
D23	MDQ6	N/A	I/O	MDQ6	DRAM data port		DDR
E23	MDQ7	N/A	I/O	MDQ7	DRAM data port		DDR
D6	MDQ8	N/A	I/O	MDQ8	DRAM data port		DDR
C6	MDQ9	N/A	I/O	MDQ9	DRAM data port		DDR
B6	MDQ10	N/A	I/O	MDQ10	DRAM data port		DDR
E7	MDQ11	N/A	I/O	MDQ11	DRAM data port		DDR
C7	MDQ12	N/A	I/O	MDQ12	DRAM data port		DDR
E8	MDQ13	N/A	I/O	MDQ13	DRAM data port		DDR
D8	MDQ14	N/A	I/O	MDQ14	DRAM data port		DDR
C8	MDQ15	N/A	I/O	MDQ15	DRAM data port		DDR
C18	MDQ16	N/A	I/O	MDQ16	DRAM data port		DDR
B17	MDQ17	N/A	I/O	MDQ17	DRAM data port		DDR
A17	MDQ18	N/A	I/O	MDQ18	DRAM data port		DDR
A20	MDQ19	N/A	I/O	MDQ19	DRAM data port		DDR
C19	MDQ20	N/A	I/O	MDQ20	DRAM data port		DDR
B18	MDQ21	N/A	I/O	MDQ21	DRAM data port		DDR
B20	MDQ22	N/A	I/O	MDQ22	DRAM data port		DDR
B21	MDQ23	N/A	I/O	MDQ23	DRAM data port		DDR
B2	MDQ24	N/A	I/O	MDQ24	DRAM data port		DDR
B3	MDQ25	N/A	I/O	MDQ25	DRAM data port		DDR
C3	MDQ26	N/A	I/O	MDQ26	DRAM data port		DDR
C4	MDQ27	N/A	I/O	MDQ27	DRAM data port		DDR
D5	MDQ28	N/A	I/O	MDQ28	DRAM data port		DDR
C5	MDQ29	N/A	I/O	MDQ29	DRAM data port		DDR
B5	MDQ30	N/A	I/O	MDQ30	DRAM data port		DDR
A5	MDQ31	N/A	I/O	MDQ31	DRAM data port		DDR
B22	MDQS0	N/A	I/O	MDQS0	DRAM data strobe0		DDR
A22	MDQS0n	N/A	I/O	MDQS0n	DRAM data strobe0		DDR

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
B7	MDQS1	N/A	I/O	MDQS1	DRAM data strobe1		DDR
A7	MDQS1n	N/A	I/O	MDQS1n	DRAM data strobe1		DDR
B19	MDQS2	N/A	I/O	MDQS2	DRAM data strobe2		DDR
A19	MDQS2n	N/A	I/O	MDQS2n	DRAM data strobe2		DDR
B4	MDQS3	N/A	I/O	MDQS3	DRAM data strobe3		DDR
A4	MDQS3n	N/A	I/O	MDQS3n	DRAM data strobe3		DDR
D20	MDM0	N/A	I/O	MDM0	DRAM data mask0		DDR
E6	MDM1	N/A	I/O	MDM1	DRAM data mask1		DDR
C20	MDM2	N/A	I/O	MDM2	DRAM data mask2		DDR
A2	MDM3	N/A	I/O	MDM3	DRAM data mask3		DDR
A11	MA0	N/A	O	MA0	DRAM address port		DDR
C12	MA1	N/A	O	MA1	DRAM address port		DDR
B12	MA2	N/A	O	MA2	DRAM address port		DDR
E13	MA3	N/A	O	MA3	DRAM address port		DDR
C13	MA4	N/A	O	MA4	DRAM address port		DDR
A14	MA5	N/A	O	MA5	DRAM address port		DDR
B14	MA6	N/A	O	MA6	DRAM address port		DDR
C14	MA7	N/A	O	MA7	DRAM address port		DDR
D14	MA8	N/A	O	MA8	DRAM address port		DDR
E14	MA9	N/A	O	MA9	DRAM address port		DDR
C15	MA10	N/A	O	MA10	DRAM address port		DDR
B15	MA11	N/A	O	MA11	DRAM address port		DDR
D18	MA12	N/A	O	MA12	DRAM address port		DDR
C16	MA13	N/A	O	MA13	DRAM address port		DDR
B16	MA14	N/A	O	MA14	DRAM address port		DDR
A16	MA15	N/A	O	MA15	DRAM address port		DDR
B13	MCK	N/A	O	MCK	DRAM differential clock output		DDR
A13	MCKn	N/A	O	MCKn	DRAM differential clock output		DDR

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
D11	MBA0	N/A	O	MBA0	DRAM bank select 0		DDR
C11	MBA1	N/A	O	MBA1	DRAM bank select 1		DDR
B11	MBA2	N/A	O	MBA2	DRAM bank select 2		DDR
D17	MODT0	N/A	O	MODT0	DRAM on die termination control0		DDR
C17	MODT1	N/A	O	MODT1	DRAM on die termination control1		DDR
A8	MCSN0	N/A	O	MCSN0	DRAM chip select0		DDR
B9	MCSN1	N/A	O	MCSN1	DRAM chip select1		DDR
C9	MCKE0	N/A	O	MCKE0	DRAM clock enable0		DDR
B8	MCKE1	N/A	O	MCKE1	DRAM clock enable1		DDR
A10	MRASN	N/A	O	MRASN	DRAM command output		DDR
B10	MCASN	N/A	O	MCASN	DRAM command output		DDR
C10	MWEN	N/A	O	MWEN	DRAM command output		DDR
E11	MRESET	N/A	O	MRESET	DRAM reset output		DDR
G13	MVREF	N/A	P	MVREF	DARM reference voltage input		DDR
G12	MVREFAO	N/A	P	MVREFAO	DARM reference voltage input always on		DDR
G15	MPZQ	N/A	I/O	MPZQ	DRAM reference pin for ZQ calibration		DDR
E10	DDR_RETEN	N/A	I	DDR_RETEN	DDR retention enable input		DDR
E16	DDR_ATO	N/A					DDR
E17	DDR_ODT1	N/A	O	MODT1	DRAM on die termination control1		DDR
E18	DDR_ODT0	N/A	O	MODT0	DRAM on die termination control0		DDR
F7	MVDD1	N/A	DP	MVDD1	DRAM IO power		
F8	MVDD2	N/A	DP	MVDD2	DRAM IO power		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
F10	MVDD3	N/A	DP	MVDD3	DRAM IO power		
F11	MVDD4	N/A	DP	MVDD4	DRAM IO power		
F13	MVDD5	N/A	DP	MVDD5	DRAM IO power		
F14	MVDD6	N/A	DP	MVDD6	DRAM IO power		
F16	MVDD7	N/A	DP	MVDD7	DRAM IO power		
F17	MVDD8	N/A	DP	MVDD8	DRAM IO power		
G11	MVDDAO	N/A	DP	MVDDAO	DRAM IO power always on		
Part L							
K17	VCCIO0	N/A	DP	VCCIO1	CPU IO power		
H18	VCCIO1	N/A	DP	VCCIO2	CPU IO power		
G8	CVDD1	N/A	DP	CVDD1	LOGIC/GPU core power		
G10	CVDD2	N/A	DP	CVDD2	LOGIC/GPU core power		
G16	CVDD3	N/A	DP	CVDD3	LOGIC/GPU core power		
G18	CVDD4	N/A	DP	CVDD4	LOGIC/GPU core power		
H17	CVDD5	N/A	DP	CVDD5	LOGIC/GPU core power		
L17	CVDD6	N/A	DP	CVDD6	LOGIC/GPU core power		
L18	CVDD7	N/A	DP	CVDD7	LOGIC/GPU core power		
M17	CVDD8	N/A	DP	CVDD8	LOGIC/GPU core power		
P18	CVDD9	N/A	DP	CVDD9	LOGIC/GPU core power		
R17	CVDD10	N/A	DP	CVDD10	LOGIC/GPU core power		
T17	CVDD11	N/A	DP	CVDD11	LOGIC/GPU core power		
N7	CVDD12	N/A	DP	CVDD12	LOGIC/GPU core power		
H7	CVDD13	N/A	DP	CVDD13	LOGIC/GPU core power		
J17	CVDD14	N/A	DP	CVDD14	LOGIC/GPU core power		
N5	AVDD1	N/A	DP	AVDD1	ARM core power		
N6	AVDD2	N/A	DP	AVDD2	ARM core power		
P5	AVDD3	N/A	DP	AVDD3	ARM core power		
P6	AVDD4	N/A	DP	AVDD4	ARM core power		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
T5	AVDD5	N/A	DP	AVDD5	ARM core power		
T6	AVDD6	N/A	DP	AVDD6	ARM core power		
U5	AVDD7	N/A	DP	AVDD7	ARM core power		
U6	AVDD8	N/A	DP	AVDD8	ARM core power		
V5	AVDD9	N/A	DP	AVDD9	ARM core power		
V7	AVDD10	N/A	DP	AVDD10	ARM core power		
V8	AVDD11	N/A	DP	AVDD11	ARM core power		
V10	AVDD12	N/A	DP	AVDD12	ARM core power		
U8	AVDD13	N/A	DP	AVDD13	ARM core power		
U9	AVDD14	N/A	DP	AVDD14	ARM core power		
U10	AVDD15	N/A	DP	AVDD15	ARM core power		
W10	AVDD_COM	N/A	DP	AVDD COM	ARM core power feedback output		
Part M							
C2	VSS1	N/A	GP	VSS1	CPU power ground		
D4	VSS2	N/A	GP	VSS2	CPU power ground		
D7	VSS3	N/A	GP	VSS3	CPU power ground		
D10	VSS4	N/A	GP	VSS4	CPU power ground		
D13	VSS5	N/A	GP	VSS5	CPU power ground		
D16	VSS6	N/A	GP	VSS6	CPU power ground		
D19	VSS7	N/A	GP	VSS7	CPU power ground		
C21	VSS8	N/A	GP	VSS8	CPU power ground		
E21	VSS9	N/A	GP	VSS9	CPU power ground		
V3	VSS10	N/A	GP	VSS10	CPU power ground		
AA8	VSS11	N/A	GP	VSS11	CPU power ground		
AA14	VSS12	N/A	GP	VSS12	CPU power ground		
AA16	VSS13	N/A	GP	VSS13	CPU power ground		
AA18	VSS14	N/A	GP	VSS14	CPU power ground		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
G9	VSS15	N/A	GP	VSS15	CPU power ground		
G14	VSS16	N/A	GP	VSS16	CPU power ground		
H8	VSS17	N/A	GP	VSS17	CPU power ground		
H9	VSS18	N/A	GP	VSS18	CPU power ground		
H10	VSS19	N/A	GP	VSS19	CPU power ground		
H11	VSS20	N/A	GP	VSS20	CPU power ground		
H12	VSS21	N/A	GP	VSS21	CPU power ground		
H13	VSS22	N/A	GP	VSS22	CPU power ground		
H14	VSS23	N/A	GP	VSS23	CPU power ground		
H15	VSS24	N/A	GP	VSS24	CPU power ground		
H16	VSS25	N/A	GP	VSS25	CPU power ground		
J8	VSS26	N/A	GP	VSS26	CPU power ground		
J9	VSS27	N/A	GP	VSS27	CPU power ground		
J10	VSS28	N/A	GP	VSS28	CPU power ground		
J11	VSS29	N/A	GP	VSS29	CPU power ground		
J12	VSS30	N/A	GP	VSS30	CPU power ground		
J13	VSS31	N/A	GP	VSS31	CPU power ground		
J14	VSS32	N/A	GP	VSS32	CPU power ground		
J15	VSS33	N/A	GP	VSS33	CPU power ground		
J16	VSS34	N/A	GP	VSS34	CPU power ground		
K8	VSS35	N/A	GP	VSS35	CPU power ground		
K9	VSS36	N/A	GP	VSS36	CPU power ground		
K10	VSS37	N/A	GP	VSS37	CPU power ground		
K11	VSS38	N/A	GP	VSS38	CPU power ground		
K12	VSS39	N/A	GP	VSS39	CPU power ground		
K13	VSS40	N/A	GP	VSS40	CPU power ground		
K14	VSS41	N/A	GP	VSS41	CPU power ground		
K15	VSS42	N/A	GP	VSS42	CPU power ground		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
K16	VSS43	N/A	GP	VSS43	CPU power ground		
L8	VSS44	N/A	GP	VSS44	CPU power ground		
L9	VSS45	N/A	GP	VSS45	CPU power ground		
L10	VSS46	N/A	GP	VSS46	CPU power ground		
L11	VSS47	N/A	GP	VSS47	CPU power ground		
L12	VSS48	N/A	GP	VSS48	CPU power ground		
L13	VSS49	N/A	GP	VSS49	CPU power ground		
L14	VSS50	N/A	GP	VSS50	CPU power ground		
L15	VSS51	N/A	GP	VSS51	CPU power ground		
L16	VSS52	N/A	GP	VSS52	CPU power ground		
M8	VSS53	N/A	GP	VSS53	CPU power ground		
M9	VSS54	N/A	GP	VSS54	CPU power ground		
M10	VSS55	N/A	GP	VSS55	CPU power ground		
M11	VSS56	N/A	GP	VSS56	CPU power ground		
M12	VSS57	N/A	GP	VSS57	CPU power ground		
M13	VSS58	N/A	GP	VSS58	CPU power ground		
M14	VSS59	N/A	GP	VSS59	CPU power ground		
M15	VSS60	N/A	GP	VSS60	CPU power ground		
M16	VSS61	N/A	GP	VSS61	CPU power ground		
N8	VSS62	N/A	GP	VSS62	CPU power ground		
N9	VSS63	N/A	GP	VSS63	CPU power ground		
N10	VSS64	N/A	GP	VSS64	CPU power ground		
N11	VSS65	N/A	GP	VSS65	CPU power ground		
N12	VSS66	N/A	GP	VSS66	CPU power ground		
N13	VSS67	N/A	GP	VSS67	CPU power ground		
N14	VSS68	N/A	GP	VSS68	CPU power ground		
N15	VSS69	N/A	GP	VSS69	CPU power ground		
N16	VSS70	N/A	GP	VSS70	CPU power ground		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
N17	VSS71	N/A	GP	VSS71	CPU power ground		
P7	VSS72	N/A	GP	VSS72	CPU power ground		
P8	VSS73	N/A	GP	VSS73	CPU power ground		
P9	VSS74	N/A	GP	VSS74	CPU power ground		
P10	VSS75	N/A	GP	VSS75	CPU power ground		
P11	VSS76	N/A	GP	VSS76	CPU power ground		
P12	VSS77	N/A	GP	VSS77	CPU power ground		
P13	VSS78	N/A	GP	VSS78	CPU power ground		
P14	VSS79	N/A	GP	VSS79	CPU power ground		
P15	VSS80	N/A	GP	VSS80	CPU power ground		
P16	VSS81	N/A	GP	VSS81	CPU power ground		
P17	VSS82	N/A	GP	VSS82	CPU power ground		
R7	VSS83	N/A	GP	VSS83	CPU power ground		
R8	VSS84	N/A	GP	VSS84	CPU power ground		
R9	VSS85	N/A	GP	VSS85	CPU power ground		
R10	VSS86	N/A	GP	VSS86	CPU power ground		
R11	VSS87	N/A	GP	VSS87	CPU power ground		
R12	VSS88	N/A	GP	VSS88	CPU power ground		
R13	VSS89	N/A	GP	VSS86	CPU power ground		
R14	VSS90	N/A	GP	VSS87	CPU power ground		
R15	VSS91	N/A	GP	VSS88	CPU power ground		
R16	VSS92	N/A	GP	VSS89	CPU power ground		
T7	VSS93	N/A	GP	VSS90	CPU power ground		
T8	VSS94	N/A	GP	VSS91	CPU power ground		
T9	VSS95	N/A	GP	VSS92	CPU power ground		
T10	VSS96	N/A	GP	VSS93	CPU power ground		
T11	VSS97	N/A	GP	VSS94	CPU power ground		
T12	VSS98	N/A	GP	VSS95	CPU power ground		

Pin	Ball Pin Name	IO Pull	Default Dir①	Default function	Defual function description	Function 2	IO domain②
T13	VSS99	N/A	GP	VSS96	CPU power ground		
T14	VSS100	N/A	GP	VSS97	CPU power ground		
T15	VSS101	N/A	GP	VSS98	CPU power ground		
T16	VSS102	N/A	GP	VSS99	CPU power ground		

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring

2.6 RK3168 power/ground IO descriptions

Table 2-2 Power/Ground IO information

Group	Ball #	Descriptions
GND	C2,C21,D4,D7,D10,D13,D16,D19,E21,V3,AA8,AA14,AA16,AA18,G9,G14,H8,H9,H10,H11,H12,H13,H14,H15,H16,J8,J9,J10,J11,J12,J13,J14,J15,J16,K8,K9,K10,K11,K12,K13,K14,K15,K16,L8,L9,L10,L11,L12,L13,L14,L15,L16,M8,M9,M10,M11,M12,M13,M14,M15,M16,N8,N9,N10,N11,N12,N13,N14,N15,N16,N17,P7,P8,P9,P10,P11,P12,P13,P14,P15,P16,P17,R7,R8,R9,R10,R11,R12,R13,R14,R15,R16,T7,T8,T9,T10,P7,R7,T7,T14,T15,T16	Internal Core Ground and Digital IO Ground
AVDD	N5,N6,P5,P6,T5,T6,U5, U6,U8,U9,U10,V5,V7,V8,V9	Internal CPU Power Supply (@ cpu frequency <= 1GHz)
		Internal CPU Power Supply (@ cpu frequency <= 1.5GHz)
CVDD	G8,G10,G16,G18,H7,H17,J17,L17,L18,M17,N7,P18,R17,T17	Internal Core Digital Logic Power Supply
PVDD_1V0	W14	PMU Domain Digital Logic Power Supply
PVCC_3V3	W13	PMU Domain Digital IO Power Supply
VCCIO0	K17	Digital GPIO Power Supply
VCCIO1	H18	
LCD0_VCC0	K7	LCDC0 Digital IO Power Supply
LCD0_VCC1	J7	
LCD1_VCC	L7	LCDC1 Digital IO Power Supply
CIF_VCC	M7	Camera Digital IO Power Supply
FLASH_VCC	N18	NAND Flash Digital IO Power Supply
AP0_VCC	V17	UART0/SDIO/MAC Digital IO Power Supply
AP1_VCC	U18	UART1/SPI0/I2S/I2C4 Digital IO Power Supply
MVDD	F7,F8,F10,F11,F13,F14,F16,F17,G11	DDR3 Digital IO Power LPDDR2 Digital IO Power
APLL_AVSS	U11	ARM PLL Analog Ground
APLL_1V0	V11	ARM PLL Power Supply
DPLL_AVSS	U13	DDR PLL Analog Ground

Group	Ball #	Descriptions
DPLL_1V0	V14	DDR PLL Power Supply
C/GPLL_AVSS	U12	CODEC/GENERAL PLL Analog Ground
C/GPLL_1V0	V13	CODEC/GENERAL PLL Power Supply
ADCVDD_1V8	K18	SAR-ADC Analog Power
USBVDD_1V0	U14	USB OTG2.0/Host2.0 Digital Power Supply
USBVDD_1V8	V16	USB OTG2.0/Host2.0 Analog Power Supply
USBVDD_3V3	U15	USB OTG2.0/Host2.0 Analog Power
EFUSE_VDDQ	Y10	eFuse IO Digital Power

2.7 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-3 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	CLKIN_32K	I	Clock input of 32.768KHz.
	CPU_PWROFF	O	Request signal to external PMIC for power down CPU subsystem with dual-core Cortex-A9 .
	CORE_PWROFF	O	Request signal to external PMIC for SoC Core logic w/o MPU subsystem and PMU logic.
	NPOR	I	Power on reset for chip.

Interface	Pin Name	Direction	Description
JTAG	JTAG_SEL	I	JTAG function select input
	TRST_n	I	JTAG interface reset input
	TCK	I	JTAG interface clock input/SWD interface clock input
	TDI	I	JTAG interface TDI input
	TMS	I/O	JTAG interface TMS input/SWD interface data out
	TDO	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
ETM Trace	TRACE_CLK	O	Cortex-A9 ETM trace port clk
	TRACE_CTL	O	Cortex-A9 ETM trace port control
	TRACE_DATA*i*(*i*=0~15)	I/O	Cortex-A9 ETM trace port data

Interface	Pin Name	Direction	Description
SD/MMC0	SDMMC0_CLKOUT	O	Sdmmc0 card clock

Interface	Pin Name	Direction	Description
Host	SDMMC0_CMD	I/O	Sdmmc0 card command output and reponse input
	SDMMC0_DATA*i* (*i*=0~3)	I/O	Sdmmc0 card data input and output
	SDMMC0_DETECT_n	I	Sdmmc0 card detect signal, a logic-low represents presence of card
	SDMMC0_WRITE_PRT	I	Sdmmc0 card write protect signal, a logic-high represents write is protected
	SDMMC0_RSTN_OUT	O	Sdmmc0 card reset signal
	SDMMC0_PWR_EN	O	Sdmmc0 card power-enable control signal

Interface	Pin Name	Direction	Description
SD/MMC1 Host	SDMMC1_CLKOUT	O	Sdmmc1 card clock
	SDMMC1_CMD	I/O	Sdmmc1 card command output and reponse input
	SDMMC1_DATA*i* (*i*=0~3)	I/O	Sdmmc1 card data input and output
	SDMMC1_DETECT_n	I	Sdmmc1 card detect signal, a logic-low represents presence of card
	SDMMC1_WRITE_PRT	I	Sdmmc1 card write protect signal, a logic-high represents write is protected
	SDMMC1_PWR_EN	O	Sdmmc1 card power-enable control signal
	SDMMC1_INT_n	O	Sdmmc1 card interrupt indication
	SDMMC1_BACKEND	O	Sdmmc1 back-end power supply for embedded device

Interface	Pin Name	Direction	Description
eMMC	EMMC_CLKOUT	O	Emmc card clock.
	EMMC_CMD	I/O	Emmc card command output and response input.
	EMMC_DATA*i* (*i*=0~7)	I/O	Emmc card data input and output.
	EMMC_PWR_EN	O	Emmc card power-enable control signal
	EMMC_RSTN_OUT	O	Emmc card reset signal

Interface	Pin Name	Direction	Description
DMC	CK	O	Active-high clock signal to the memory device
	CK_n	O	Active-low clock signal to the memory device
	CKE*i* (*i*=0,1)	O	Active-high clock enable signal to the memory device for two chip select
	CS_n*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. There are two chip select
	RAS_n	O	Active-low row address strobe to the memory device
	CAS_n	O	Active-low column address strobe to the memory device
	WE_n	O	Active-low write enable strobe to the memory device
	BA*i* (*i*=0~2)	O	Bank address signal to the memory device
	DA*i* (*i*=0~15)	O	Address signal to the memory device
	DQ*i* (*i*=0~31)	I/O	Bidirectional data line to the memory device

Interface	Pin Name	Direction	Description
	DQS*i* (*i*=0~3)	I/O	Active-high bidirectional data strobes to the memory device
	DQS_n*i* (*i*=0~3)	I/O	Active-low bidirectional data strobes to the memory device
	DM*i* (*i*=0~3)	O	Active-low data mask signal to the memory device
	ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select
	RET_EN	I	Active-low retention latch enable input
	RESET	O	DDR3 reset signal to the memory device
	VREF	I/O	Reference Voltage input for three regions of DDR IO
	VREFAO	I/O	DARM reference voltage input always on
	ATO	I/O	Analog signal output in test mode
	ZQ_PIN	I/O	ZQ calibration pad which connects 240ohm±1% resistor

Interface	Pin Name	Direction	Description
SMC	SMC_OE_n	O	SMC output enable signal
	SMC_BLS_n*i* (*i*=0,1)	O	SMC byte lane strobe signal for two bytes
	SMC_WE_n	O	SMC write enable signal
	SMC_CSn*i* (*i*=0,1)	O	SMC chip enable signal
	SMC_ADV_n	O	SMC address valid signal in shared mode
	SMC_ADDR*i* (*i*=0~7)	O	SMC address signal
	SMC_DATA*i* (*i*=0~15)	I/O	SMC directional data line to memory device

Interface	Pin Name	Direction	Description
NAND	FLASH_WP	O	Flash write-protected signal
	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_DATA*i* (*i*=0~7)	I/O	Low 8bits of flash data inputs/outputs signal
	FLASH_DATA*i* (*i*=8~15)	I/O	High 8bits of flash data inputs/outputs signal
	FLASH_DQS	I/O	Flash data strobe signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH_CSn*i* (*i*=0~3)	O	Flash chip enable signal

Interface	Pin Name	Direction	Description
HSADC	HSADC_CLKOUT	O	Hsadc/tsi/gps reference clock
	HSADC_DATA*i* (*i*=0~9)	I	Hsadc(i=0~9)/tsi(i=0~7)/gps data(i=0,1)
	TS_SYNC	I	Ts synchronizer signal

Interface	Pin Name	Direction	Description
I2S/PCM	I2S_CLK	O	I2S/PCM clock source
	I2S_SCLK	I/O	I2S/PCM serial clock
	I2S_LRCK_RX	I/O	I2S/PCM left & right channel signal for receiving serial

Interface	Pin Name	Direction	Description
			data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S_SDI	I	I2S/PCM serial data input
	I2S_SDO	O	I2S/PCM serial data ouput
	I2S_LRCK_TX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPDIF	SPDIF_TX	O	SPDIF biphase data output

Interface	Pin Name	Direction	Description
SPI	SPI*x*_CLK*(x=0,1)*	I/O	SPI serial clock
	SPI*x*_CSn*y* *(x=0,1)(y=0,1)*	I/O	SPI chip select signal,low active
	SPI*x*_TXD*(x=0,1)*	O	SPI serial data output
	SPI*x*_RXD*(x=0,1)*	I	SPI serial data input

Interface	Pin Name	Direction	Description
LCDC	LCDC*x*_DCLK*(x=0,1)*	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC*x*_VSYNC*(x=0,1)*	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LCDC*x*_HSYNC*(x=0,1)*	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	LCDC*x*_DEN*(x=0,1)*	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC*x*_DATA*i* *(x=0,1)*(*i*=0~23)	I/O	LCDC data output/input

Interface	Pin Name	Direction	Description
CAMERA	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_CLKOUT	O	Camera interface output work clock
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_HREF	I	Camera interface horizontal sync signal
	CIF_DATA*i* (*i*=0~1)	I	Camera interface low 2-bit input pixel data
	CIF_DATA*i* (*i*=2~9)	I	Camera interface middle 8-bit input pixel data
	CIF_DATA*i* (*i*=10~11)	I	Camera interface high 2-bit input pixel data

Interface	Pin Name	Direction	Description
RMII	RMII_CLKOUT	O	RMII REC_CLK output

Interface	Pin Name	Direction	Description
	RMII_TX_EN	O	RMII transfer enable
	RMII_TXD1	O	RMII transfer data 1
	RMII_TXD0	O	RMII transfer data 0
	RMII_RX_ERR	I	RMII receive error
	RMII_CRS_VALID	I	RMII carrier sense / receive data valid input
	RMII_RXD1	I	RMII receive data 1
	RMII_RXD0	I	RMII receive data 0
	RMII_MD	I/O	RMII management interface data
	RMII_MDCLK	O	RMII management interface clock

Interface	Pin Name	Direction	Description
PWM	PWM0	O	Pulse Width Modulation output 0
	PWM1	O	Pulse Width Modulation output 1
	PWM2	O	Pulse Width Modulation output 2
	PWM3	O	Pulse Width Modulation output 3

Interface	Pin Name	Direction	Description
GPS	GPS_CLK	I	GPS sample clock input
	GPS_SIG	I	GPS SIGN input data
	GPS_MAG	I	GPS MAG input data

Interface	Pin Name	Direction	Description
I2C	I2C0_SDA	I/O	I2C0 data
	I2C0_SCL	I/O	I2C0 clock
	I2C1_SDA	I/O	I2C1 data
	I2C1_SCL	I/O	I2C1 clock
	I2C2_SDA	I/O	I2C2 data
	I2C2_SCL	I/O	I2C2 clock
	I2C3_SDA	I/O	I2C3 data
	I2C3_SCL	I/O	I2C3 clock
	I2C4_SDA	I/O	I2C4 data
	I2C4_SCL	I/O	I2C4 clock

Interface	Pin Name	Direction	Description
UART	UART0_SIN	I	UART0 serial data input
	UART0_SOUT	O	UART0 serial data output
	UART0_CTS_n	I	UART0 clear to send
	UART0_RTS_n	O	UART0 request to send
	UART1_SIN	I	UART1 serial data input
	UART1_SOUT	O	UART1 serial data output
	UART1_CTS_n	O	UART1 clear to send
	UART1_RTS_n	I	UART1 request to send
	UART2_SIN	I	UART2 serial data input

Interface	Pin Name	Direction	Description
	UART2_SOUT	O	UART2 serial data output
	UART3_SIN	I	UART3 serial data input
	UART3_SOUT	O	UART3 serial data output
	UART3_CTS_n	I	UART3 clear to send
	UART3_RTS_n	O	UART3 request to send

Interface	Pin Name	Direction	Description
USB OTG 2.0	OTG_DM	N/A	USB OTG 2.0 Data signal DM
	OTG_DP	N/A	USB OTG 2.0 Data signal DP
	OTG_RKELVIN	N/A	USB OTG 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	OTG_VBUS	N/A	USB OTG 2.0 connected detect input
	OTG_ID	N/A	USB OTG 2.0 ID detect input

Interface	Pin Name	Direction	Description
USB Host 2.0	HOST_DM	N/A	USB HOST 2.0 Data signal DM
	HOST_DP	N/A	USB HOST 2.0 Data signal DP
	HOST_RKELVIN	N/A	USB HOST 2.0 Transmitter Kelvin Connection to Resistor Tune Pin

Interface	Pin Name	Direction	Description
HSIC	HSIC_DATA	N/A	HSIC DATA signal
	HSIC_STROBE	N/A	HSIC STROBE signal

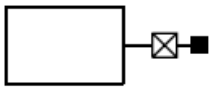
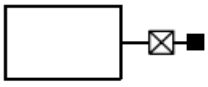
Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN*i* (*i*=0~2)	N/A	SAR-ADC input signal for 3 channel

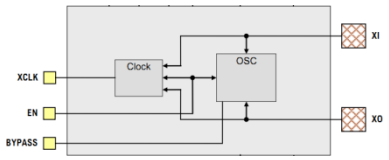
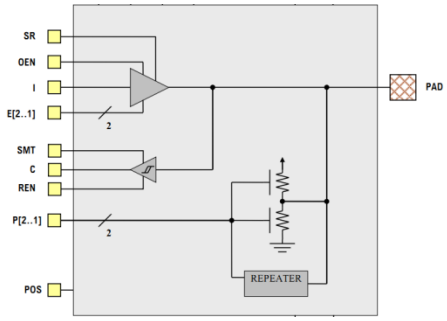
Interface	Pin Name	Direction	Description
eFuse	EFUSE_VDDQ	N/A	eFuse program and sense power supply

2.8 RK3168 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 2-4 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]

Type	Diagram	Description	Pin Name
C		Crystal Oscillator with high enable	XIN24M XOUT24M
D		Tri-state output pad with input, which pullup/pulldown, slew rate and drive strength is configurable	Part of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 4.2, Recommended Operating Conditions, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3-1 Absolute Maximum Ratings Over Junction Temperature Range

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD, CVDD, PVDD, USBDVDD	1.4	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	LCD0_VCC0,LCD0_VCC1, LCD1_VCC, CIF_VCC, PVCC_3V3, AP0_VCC,AP1_VCC, FLASH_VCC, VCCIO0,VCCIO1	3.6	V
DC supply voltage for DDR IO	MVDD	1.95	V
DC supply voltage for Analog part of SAR-ADC	ADCVDD_1V8	1.98	V
DC supply voltage for PLL	APLL_1V0 DPLL_1V0 C/GPLL_1V0	1.1	V
DC supply voltage for Analog part of USB OTG/Host2.0	USBVDD_1V8 USBVDD_3V3	1.98 3.63	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long -term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 6.

Table 3-2 Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power (except USB OTG)	AVDD, CVDD, PVDD	0.9	1.0	1.4	V
Digital GPIO Power(3.3V)	VCCIO0,VCCIO1,	3	3.3	3.6	V

Parameters	Symbol	Min	Typ	Max	Units
Digital GPIO Power(3.3V/1.8V)	LCD0_VCC0, LCD0_VCC1, LCD1_VCC, CIF_VCC, PVCC, FLASH_VCC, AP0_VCC, AP1_VCC	3 1.62	3.3 1.8	3.6 1.98	V
DDR IO(DDR3 mode) Power	MVDD	1.425	1.5	1.575	V
DDR IO(DDR3L mode) Power	MVDD	1.30	1.35	1.45	V
DDR IO(LPDDR2 mode) Power	MVDD	1.14	1.2	1.3	V
DDR reference supply (VREF) Input	VREF	0.49 x MVDD	0.5 x MVDD	0.51 x MVDD	V
DDR External termination voltage		VREF-40mV	VREF	VREF+40mV	V
PLL Analog Power	APLL_1V0 DPLL_1V0 C/GPLL_1V0	0.9	1.0	1.1	V
SAR-ADC Analog Power	ADCVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USBDVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(1.8V)	USBVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Analog Power(3.3V)	USBVDD_3V3	3.069	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	N/A	200	N/A	Ohm
HSIC Analog Power	HSIC_VDD12	1.08	1.2	1.32	V
PLL input clock frequency		N/A	24	N/A	MHz
Max CPU Frequency			1.5		GHz
Ambient Operating Temperature ②	Ta	0	25	80	℃

Notes :①' Symbol name is same as the pin name in the io descriptions

② with the reference software setup, the reference software will limit the chipset temperature about 80℃

3.3 Recommended Operating Frequency

Table 3-3 Recommended operating frequency for PD_ALIVE domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.0V , 25℃	IO_XIN24M	24	24	24	MHz
	1.1V , -40℃		24	24	24	
	0.9V , 125℃		24	24	24	
DDR PLL	1.0V , 25℃	ddr_pll_clk	N/A	N/A	1790	MHz
	1.1V , -40℃		N/A	N/A	2000	
	0.9V , 125℃		N/A	N/A	1280	
ARM PLL	1.0V , 25℃	arm_pll_clk	N/A	N/A	1500	MHz
	1.1V , -40℃		N/A	N/A	2000	
	0.9V , 125℃		N/A	N/A	1100	

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
CODEC PLL	1.0V , 25 ℃	cocec_pll_clk	N/A	N/A	1305	MHz
	1.1V , -40 ℃		N/A	N/A	1850	
	0.9V , 125 ℃		N/A	N/A	965	
GENERAL PLL	1.0V , 25 ℃	general_pll_clk	N/A	N/A	1305	MHz
	1.1V , -40 ℃		N/A	N/A	1850	
	0.9V , 125 ℃		N/A	N/A	965	
UART1CLK	1.0V , 25 ℃	clk_uart1	N/A	N/A	225	MHz
	1.1V , -40 ℃		N/A	N/A	260	
	0.9V , 125 ℃		N/A	N/A	188	
TIMER3 CLK	1.0V , 25 ℃	clk_timer3	N/A	N/A	253	MHz
	1.1V , -40 ℃		N/A	N/A	395	
	0.9V , 125 ℃		N/A	N/A	176	

3.4 Electrical Characteristics for General IO

Table 3-4 DC Electrical Characteristics for General IO

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	N/A	N/A	V
	Output High Voltage	Voh	N/A	N/A	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	N/A	N/A	V
	Output High Voltage	Voh	N/A	N/A	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.09	N/A	MVDD	V
	Input Low Voltage	Vil_ddr	-0.3	0	VREF - 0.09	V
	Output High Voltage	Voh_ddr	0.8xMVDD	N/A	N/A	V
	Output Low Voltage	Vol_ddr	N/A	N/A	0.2xMVDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.09	N/A	MVDD	V
	Input Low Voltage	Vil_ddr	-0.3	N/A	VREF - 0.13	V
	Output High Voltage	Voh_ddr	0.9 xMVDD	N/A	N/A	V
	Output Low Voltage	Vol_ddr	N/A	N/A	0.1 xMVDD	V

Table 3-5 Current Electrical Characteristics for General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	N/A	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	N/A	N/A	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	N/A	N/A	10	uA
			Vin = 3.3V, pulldown enabled	N/A	N/A	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	N/A	N/A	10	uA
			Vin = 0V, pullup enabled	N/A	N/A	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	N/A	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	N/A	N/A	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	N/A	N/A	10	uA
			Vin = 1.8V, pulldown enabled	N/A	N/A	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	N/A	N/A	10	uA
			Vin = 0V, pullup enabled	N/A	N/A	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-6 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input clock frequency	Fin	Fin = Fref * NR① @1.0V	0.032	N/A	2200	MHz
Comparison frequency	Fref	Fref = Fin/NR @1.0V	0.032	N/A	50	MHz
VCO operating range	Fvco	Fvco = Fref * NF② @1.0V	1100	N/A	2200	MHz
Output clock frequency	Fout	Fout = Fvco/NO③ @1.0V	30	N/A	2200	MHz
Lock time	Tlt		N/A	350	500	Cycles of divided reference clock
Power consumption (normal mode)	N/A		N/A	4	N/A	mW
Power consumption (standby mode)	N/A		N/A	100	N/A	uW
Power consumption (power-down mode)	N/A	No clock input to PLL, power down signal high, 80C temperature	N/A	10	N/A	uW

Notes :

① :NR is the input divider value;

②:NF is the feedback divider value;

③:NO is the output divider value

3.6 Electrical Characteristics for SAR-ADC

Table 3-7 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Conversion speed	Fs	The duty cycle should be between 40%~60%	N/A	N/A	1	MSPS
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Nn Linearity	INL		N/A	±2	N/A	LSB
Gain Error	Egain		-8	N/A	8	LSB
Offset Error	Eoffset		-8	N/A	8	mV
Analog Supply Current(VDDA_SARADC)			N/A	200	N/A	uA
Digital Supply Current			N/A	50	N/A	uA
Power Down Current from AVDD			N/A	0.5	N/A	uA
Power Down Current from DVDD			N/A	1	N/A	uA
Power up time			N/A	7	N/A	1/Fs

3.7 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 3-8 Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters		Symbol	Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		55℃ , USBDVDD_1V0 = 1.0V USBVDD_1V8=1.8V USBVDD_3V3=3.3V, 15-cm USB cable attached to DP/DM	N/A	6.151	N/A	mA
	Current From OTG_VDD33			N/A	4.97	N/A	mA
	Current From OTG_VDD18			N/A	18.5	N/A	mA
HS transmit, minimum transition density (all 1's data in DP/DM)	Current From OTG_DVDD			N/A	5.521	N/A	mA
	Current From OTG_VDD33			N/A	3.63	N/A	mA
	Current From OTG_VDD18			N/A	15.5	N/A	mA
HS idle mode	Current From OTG_DVDD			N/A	5.841	N/A	mA
	Current From OTG_VDD33			N/A	3.19	N/A	mA
	Current From OTG_VDD18			N/A	6.58	N/A	mA
FS transmit,	Current From			N/A	4.251	N/A	mA

Parameters		Symbol	Test condition	Min	Typ	Max	Units
maximum transition density (all 0's data in DP/DM)	OTG_DVDD						
	Current From OTG_VDD33			N/A	11.81	N/A	mA
	Current From OTG_VDD18			N/A	6.56	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD			N/A	5.171	N/A	mA
	Current From OTG_VDD33			N/A	12.81	N/A	mA
	Current From OTG_VDD18			N/A	6.61	N/A	mA
Suspend mode	Current From OTG_DVDD			N/A	53.4	N/A	uA
	Current From OTG_VDD33			N/A	1.1	N/A	uA
	Current From OTG_VDD18			N/A	6.6	N/A	uA
Sleep mode	Current From OTG_DVDD			N/A	0.113	N/A	mA
	Current From OTG_VDD33			N/A	0.1	N/A	uA
	Current From OTG_VDD18			N/A	0.004	N/A	mA

3.8 Electrical Characteristics for HSIC Interface

Table 3-9 Electrical Characteristics for HSIC Interface

Parameters		Symbol	Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density	Current From DVDD		55℃ , VDD12 = 1.2V, DVDD = 1.0V , 12MHz reference clock 10pF load on STROBE	N/A	3.26	N/A	mA
	Current From VDD12			N/A	10.2	N/A	mA
HS transmit, minimum transition density	Current From DVDD			N/A	3.05	N/A	mA
	Current From VDD12			N/A	8.28	N/A	mA
HS idle mode	Current From DVDD			N/A	2.71	N/A	mA
	Current From VDD12			N/A	0.001	N/A	mA
HS Receive	Current From DVDD			N/A	3.07	N/A	mA
	Current From VDD12			N/A	1.58	N/A	mA
Suspend mode	Current From DVDD			N/A	0.012	N/A	mA
	Current From VDD12			N/A	0.3	N/A	uA
Sleep mode	Current From DVDD			N/A	0.049	N/A	mA
	Current From VDD12			N/A	0.6	N/A	uA

3.9 Electrical Characteristics for DDR IO

Table 3-10 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	VDDIO_DDR standby current, ODT OFF		@ 1.5V , 125℃	N/A	0.01	2.11	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	0	0.53	uA
DDR IO @LPDDR2 mode	Input leakage current		@ 1.2V , 125℃	N/A	0	0.49	nA
	VDD(1.2V) quiescent current		@ 1.2V , 125℃	N/A	0	1.89	uA

3.10 Electrical Characteristics for eFuse

Table 3-11 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	N/A	N/A	8	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	N/A	N/A	0.2	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	N/A	N/A	14	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	N/A	N/A	60	uA

Chapter 4 Hardware Guideline

4.1 Reference design for oscillator PCB connection

RK3168 only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram , the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model . Especially C1 and C2 value is advised to meet formula (C1 * C2)/(C1+C2) = ~8pF

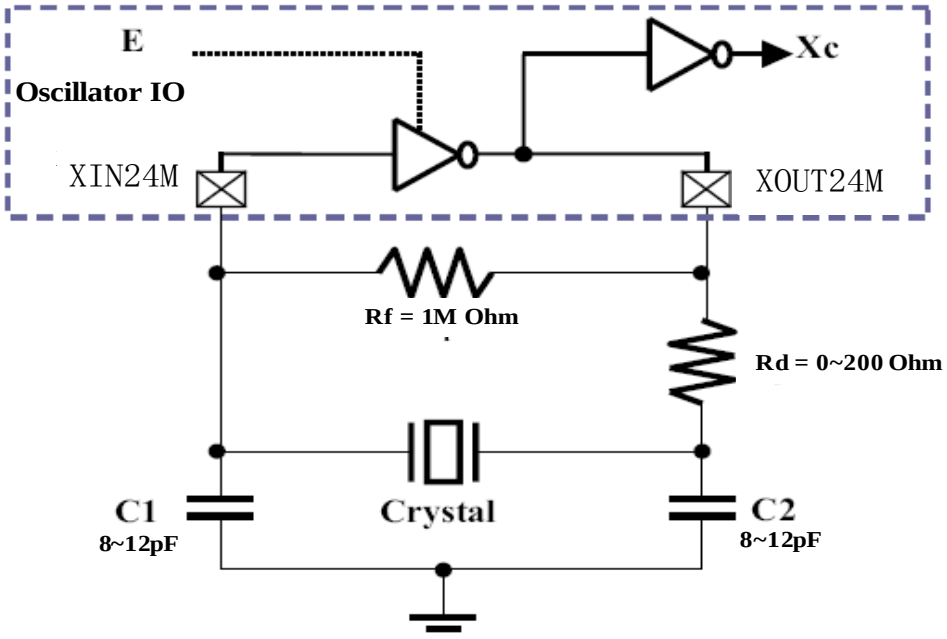


Fig. 4-1 External Reference Circuit for 24MHzOscillators

4.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK3168.

The PLL's two analog supplies should be filtered with two series ferrite beads and two shunt 0.1uF and 0.01uF capacitors. The ferrite on VSS is preferred but optional. Adding the ferrite on VSS converts supply noise to substrate noise as seen by the PLL. The PLLs are designed to berelatively insensitive to supply and substrate noise, so the presence of this ferrite is a second order issue.

The AVDD is mapped to APLL_1V0, DPLL_1V0 and GPLL_1V0.

The AVSS is mapped to AVSS_APLL, AVSS_DPLL and AVSS_C/GPLL.

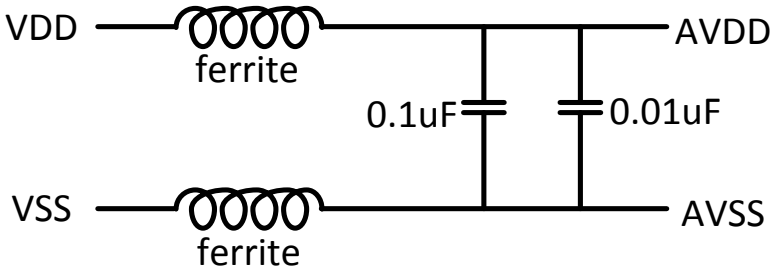


Fig. 4-2 External reference circuit for PLL

The ferrite beads should be similar one of the following from Murata:

Table 4-1 Ferrite Bead Selection

Part number	R@DC	Z@10MHz	Z@100MHz	size
BLM18EG601SN1	0.35	200	600	0603
BLM18PG471SN1	0.2	130	470	0603
BLM18KG601SN1	0.15	160	600	0603
BLM18AG601SN1	0.38	180	600	0603
BLM18AG102SN1	0.5	280	1000	0603
BLM18TG601TN1	0.45	190	600	0603
BLM15AG601SN1	0.6	200	600	0402
BLM15AX601SN1	0.34	190	600	0402
BLM15AX102SN1	0.49	250	1000	0402
BLM03AX601SN1	0.85	120	600	0201

Similar ferrite beads are also available from Panasonic. The key characteristics to select are:

- DC resistance less than 0.40 ohms
- impedance at 10MHz equal to or greater 180 ohms
- impedance at 100MHz equal to or greater than 600 ohms

The capacitors should be mounted as close to the package balls as possible.

4.3 Reference design for USB OTG/Host2.0 connection

In RK3168 there are USB OTG and USB Host2.0 interface, in fact, same interface is for them. The following diagram shows external reference design. Of course, for USB Host2.0some signals can be removed based on different application.

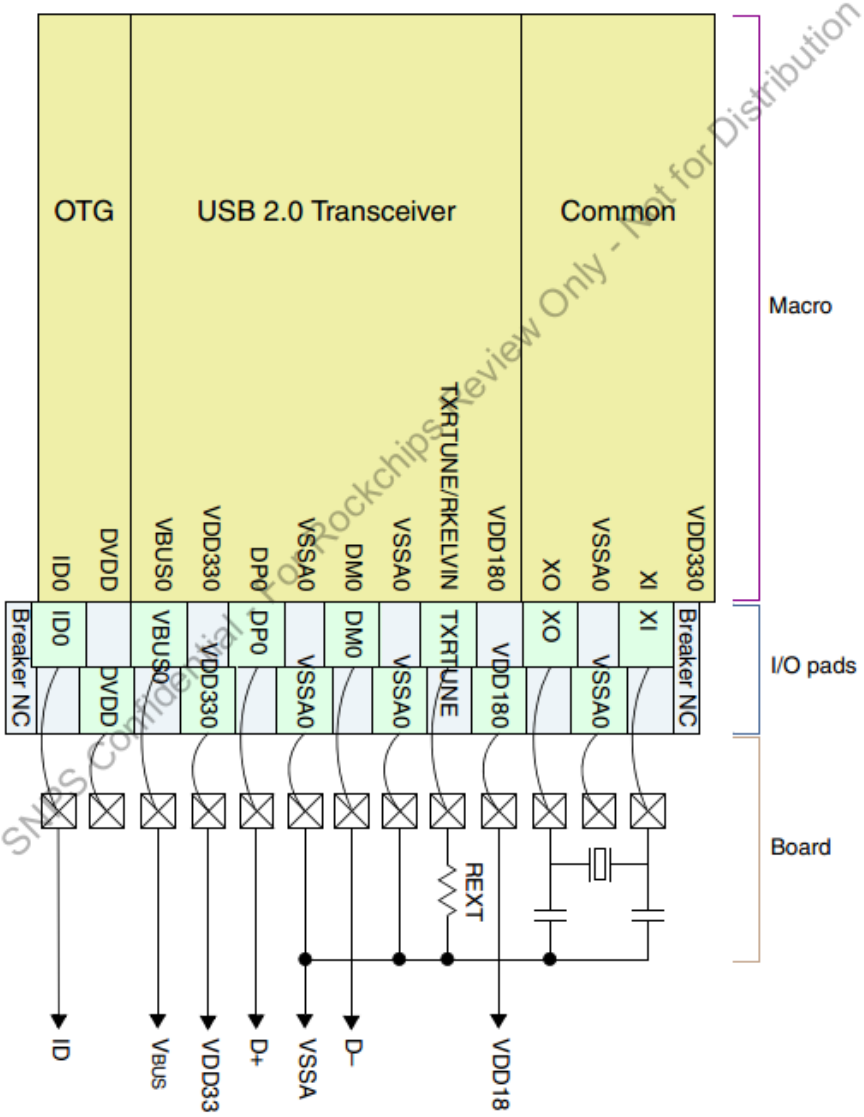


Fig. 4-3 USB OTG/Host2.0 interface reference connection

4.4 Power up/down sequence requirement

For all of the power supply in RK3168, there is no any specific requirement of power up/down sequence except power supply between core logic and DDR3/DDR3L/LPDDR2 IO or digital GPIO , between USB OTG/Host2.0 power supply .

- Power supply sequence for core logic(CVDD/AVDD/PVDD) and DDR3/DDR3L/LPDDR2 IO (MVDD)

It is generally recommended that the core logic and DDR IO be powered-up together, and it is also acceptable for core logic supply to power-up a very short time before the DDR IO supply. If DDR IO supply must power-up before the core logic supply, it is advised to keep the time between these two events less than 100ms to limit excessive DDR IO current draws.

- Power supply sequence for core logic(CVDD/AVDD/PVDD) and digital GPIO power①

It is generally recommended that "turn on the higher GPIO voltage first and then the lower core voltage" so that the crowbar current would not occur on the power-up stage.

Also it is acceptable that "turn on the lower core voltage first and then higher GPIO voltage" only if the GPIO control pins are set to a fixed state. However, the ramp-up time for them can not be less than 10us.

- Power supply sequence for USB OTG/Host2.0

Please follow the following sequence for power up and recommended ramp-up time is more than 10us.

USBDVDD _1V0(1.0V)->USBVDD_1V8 (1.8V)->USBVDD_3V3 (3.3V)

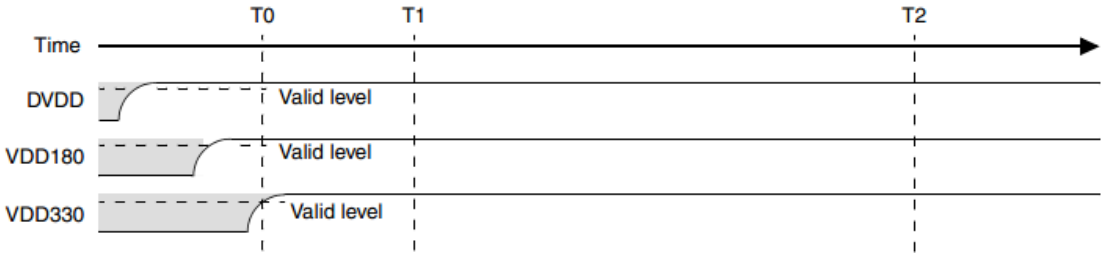


Fig. 4-4 USB OTG/Host2.0 interface power-on operation

- Power supply sequence for Power down

There is no requirement on the power-down sequence for two above groups.Customers can decide which voltage to be down first based on the application need. It is recommended to keep the time between collapsing of power supplies as short as possible.

Notes:① digital GPIO power include LCD0_VCCj, LCD1_VCC, CIFj_VCC, PVCC, APj_VCC, FLASH_VCC, VCCIOj.

4.5 Power on reset descriptions

The following figure shows power-on-reset sequence. External power-on-reset input signal NPOR is released after stabilization of oscillator input clock XIN24M. Internal signal sysrstn is generated after NPOR is filtered glitch , which can filter out 5 clock cycles(24MHz) for low pulse of NPOR, so 208ns low pulse of NPOR will not be recognized as valid power-on-reset signal for RK3168.

To make PLLs work normally, the internal power down signal(pllpd) for PLLs must be high after power-on-reset, and maintains high level for more than 1us after sysrstn is deasserted. Then PLL reset signals(pllrstn) are asserted for about 10.6us, and PLLs start to lock when pllrstn deassert, and consume about to 1330us to lock.

So the system will wait about 1330us, then deactive internal reset signal chiprstn, which is used to control generation logic of all the clock inside CRU.

After 256 cycles or about 10.7us , rstn_pre for reset signal of all internal IPs will be deasserted , in other words, about 10.7us of clock has been generated before reset of every internal module is released.

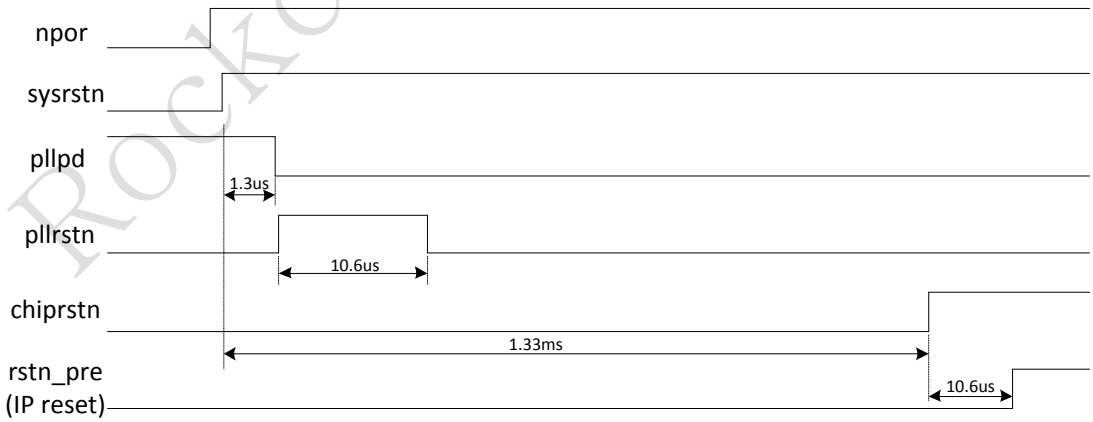


Fig. 4-5 Reset signals sequence

Chapter 5 Thermal Management

5.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3168 has to be below 125ºC.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

5.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 5-1 Thermal Resistance Characteristics

PACKAGE	POWER(W)	$\boldsymbol{\theta_{JA}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{JB}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{Jc}}$(℃/$\boldsymbol{W}$)
RK3168	4.78	20.9	12.6	7.4

Note: The testing PCB is based on 6 layers, 208mm x 39 mm, 1 mm Thickness, Ambient temperature is 25°C。