RK3026/RK3028A Application Processor

Datasheet

Revision 1.2

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Revision History

This document is now Production Data.

Date	Revision	Description
2013-09-16	V1.0	Initial Release
2013-10-18	V1.1	Add RK3028A
2013-11-30	V1.2	Add HDMI and EPD/EBC description

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chapter 1 Introduction

1.1 Overview

RK3026/RK3028Ais a low power, high performance processor solution for tablet, Android Portable GPS and other digital multimedia applications, and integrates Dual-core Cortex-A9 with separatelyNeon and FPU coprocessor ,and also with256KB L2 Cache.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3026/RK3028A supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder and special image preprocessor and postprocessor .

Embedded 3D GPU makes RK3026/RK3028A completely compatible with OpenGL ES1.1 and 2.0, OpenVG1.1 etc. Special 2D hardware engine with MMU will maximize display performance.

RK3026/RK3028A has high-performance external memory interface(DDR3/LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications as follows :

This document will provide guideline on how to use RK3028A correctly and efficiently. In them , the chapter 1 and chapter 2 will introduce the features, block diagram, signal descriptions and system usage of RK3028A, the chapter 3 through chapter 5 will describe the function,electricalcharacteristics and hardware guideline.

1.2 Features

1.2.1 MicroProcessor

- Dual-core ARM Cortex-A9 processor is a high-performance, low-power, cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- Integrated timer and watchdog timer in CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache, 4-way set associative
- 256KB unified L2 Cache
- coresight debug solution
  - Invasive debug
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - 16KBBootRom
  - 8KB internal SRAM
- External off-chip memory①

- DDR3-1600, 16bits data width, 2 ranks, 256MB(max) address space per rank
- LVDDR3-1600, 16bits data width, 2 ranks, 256MB(max) address space per rank
- Async/ Sync Toggle/Sync ONFI Nand Flash(include LBA Nand), 8bits data width,4 banks

1.2.3 Internal Memory

- Internal BootRom
  - Size : 16KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - SPI interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG
    - UART2
- Internal SRAM
  - Size : 8KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LVDDR3)
  - Compatible with JEDEC standard DDR3/ LVDDR3 SDRAM
  - Data rates of up to 1200Mbps(600MHz) for DDR3/LVDDR3 for RK3028A, RK3026 can up to 1066Mbps(533MHz)
  - Support up to 2 ranks (chip selects), maximum 256MB address space per rank
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/ LVDDR3 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation
- Nand Flash Interface
  - Support 8bits async/toggle/sync Nand Flash, up to 4 banks
  - Support LBA Nand Flash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For Sync Toggle Nand Flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 66.5MHz
  - For async/Toggle Nand Flash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC
- eMMCInterface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate

- Support block size from 1 to 65535Bytes
- 8bits data bus width

- SD/MMC Interface
  - Compatible with SD2.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components
  - Support flexible clock solution, including clock source, clock mux, clock frequency division
  - One oscillator with 24MHz clock and 4 embedded PLLs

- Timer
  - On-chip 64bits Timers with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - 24MHz/PCLK clock input for operating domain, and PCLK input for bus interface domain.

- PWM
  - Three on-chip PWMs with interrupt-based operation in RK3028A and 2 in RK3026
  - Programmable 4-bit pre-scalar from APB bus clock
  - Embedded 32-bit timer/counter facility
  - Support single-run or continuous-run PWM mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - QoS function is supported to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 96 SPI interrupt sources input from different components inside RK3026/RK3028A

- Support 16 software-triggered interrupts
- Input interrupt level is fixed , only high-level sensitive
- Two interrupt output (nFIQ and nIRQ) to per Cortex-A9, both are low-level sensitive
- Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - One embedded DMA controller inperi system
  - DMAC features:
    - 8 channels totally
    - 13 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

1.2.6 Video CODEC

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , VC-1 , RV , VP6/VP8 , Sorenson Spark
  - Error detection and concealment support for all video formats
  - Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, For H.264, YCbCr 4:0:0(monochrome) is also supported
  - Minimum image size is 48x48 for all video formats
  - H.264 up to HP level 4.2 : 1080p@60fps (1920x1080)®
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1080)
  - MPEG-2 up to MP : 1080p@60fps (1920x1080)
  - MPEG-1 up to MP : 1080p@60fps (1920x1080)
  - H.263 : 576p@60fps (720x576)
  - Sorenson Spark : 1080p@60fps (1920x1080)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1080)
  - RV8/RV9/RV10 : 1080p@60fps (1920x1080)
  - VP6/VP8 : 1080p@60fps (1920x1080)
  - For H.264, Image cropping not supported
  - For MPEG-4,GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Encoder only for H.264 (BP@level4.0, MP@level4.0,HP@level4.0) standard
  - Only support I and P slices, not B slices
  - Entropy encoding is CAVLC in BP and CABAC in MP
  - Support error resilience based on constrained intra prediction and slices
  - Maximum MV length is ±14 pixels in vertical direction and ±30 pixels in horizontal direction
  - Motion vector pixel accuracy is up to 1/4 pixels in 720p resolution and 1/2 pixels in 1080p resolution

- 12 intra prediction modes
- Number of reference frames is 1
- Maximum number of slice groups is 1
- Input data format :
  - YCbCr 4:2:0 planar
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2
  - CbYCrY 4:2:2 interleaved
  - RGB444 and BGR444
  - RGB555 and BGR555
  - RGB565 and BGR565
  - RGB888 and BRG888
  - Output data format : H.264 byte unit stream and H.264 NAL unit stream
  - Image size is from 96x96 to 1920x1080(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080④
  - Bit rate supported is from 10Kbps to 20Mbps

1.2.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Maximum data rate④ is up to 76million pixels per second
- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second

1.2.8 Image Enhancement

- Image pre-processor(embedded inside video encoder)
  - Only used together with HD video encoder inside RK3026/RK3028A , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees
- Video stabilization(embedded inside video encoder)
  - Work in combined mode with HD video encoder inside RK30xx and stand-alone mode

- Adaptive motion compensation filter
- Support scene detection from video sequence, encodes key frame when scene change noticed

- Image post-processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Ouput data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888,RGB565,ARGB4444 etc.
  - Input image size:
    - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
    - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
    - Step size is 16 pixels
  - Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
  - Support image up-scaling :
    - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Maximum output width is 3x input width
    - Maximum output height is 3x input height
  - Support image down-scaling:
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Unlimited down-scaling ratio
  - Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
  - Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision
  - Support programmable alpha channel and alpha blending operation with the following overlay input formats:
    - 8bit alpha +YUV444, big endian channel order with AYUV8888
    - 8bit alpha +24bit RGB, big endian channel order with ARGB8888
  - Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
  - Support RGB image contrast / brightness / color saturation adjustment
  - Support image cropping & digital zoom only for JPEG or stand-alone mode
  - Support picture in picture

- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

1.2.9 Image Enhancement(New IEP lite module)

- Image formatsupport
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - ARGB/XRGB/RGB565/YUV swap
  - UV SP/P
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - RGB dither up/down
  - YUV up/down sampling
  - Max source image resolution: 8192x8192
  - Max scaled image resolution: 4096x4096
- YUV enhancement &denoise
  - Hue, Saturation, Brightness, Contrast adjustment
- RGB enhancement &denoise
  - Contrast enhancement
  - Color enhancement
  - Gamma adjustment
- High quality scale
  - Averaging filter down-scaling
  - Bi-cubic up-scaling
  - Arbitrary non-integer horizontal & vertical scaling ratio range from 1/16 to 16
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configure high frequency de-interlace
  - I4O2 (Input 4 field,output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Interface
  - Configure direct path to LCDC if source width no more than 1920
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

1.2.10 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 32KB size
  - Triangle rate : 30M triangles/s
  - Pixel rate: 300 pixels/s @ 150MHz
- 2D Graphics Engine(RGA module) :
  - Pixel rate: 300M pixel/s without scale, 150M pixel/s with bilinear scale, 66.5M pixel/s with bicubic scale.
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill

- Line drawing with anti-aliasing and specified width
- High-performance stretch and shrink
- Monochrome expansion for text rendering
- ROP2, ROP3, ROP4 full alpha blending and transparency
- Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask
- 8K x 8K raster 2D coordinate system
- Arbitrary degrees rotation with anti-aliasing on every 2D primitive
- Programmable bicubic filter to support image scaling
- Blending, scaling and rotation are supported in one pass for stretch blit
- Source formats :
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar
  - YUV422 planar, YUV422 semi-planar
  - BPP8, BPP4, BPP2, BPP1
- Destination formats :
  - ABGR8888, XBGR888, ARGB8888, XRGB888
  - RGB888, RGB565
  - RGBA5551, RGBA4444
  - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
  - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.11 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support image crop with arbitrary windows
- Display Interface
  - Support LCD or TFT interfaces up to 1920x1080
  - Support HDMI 1.4 output up to 1080p@30fps only by RK3028A
  - Parallel RGB LCD Interface : RGB888(24bits),RGB666(18bits) ,RGB565(15bits)
  - Serial RGB LCD Interface: 2x12-bit, 3x8-bit(RGB delta support), 3x8-bit + dummy
  - MCU LCD interface: i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
  - TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i)
  - Max output resolution 1920x1080
  - 4 display layers :
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - maximum resolution is 1920x1080,support virtual display
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
      - 3D display support
      - Direct path support

- One video layer (win1)
  - RGB888, ARGB888, RGB565, 1/2/4/8bpp
  - Support virtual display
  - 256 level alpha blending (pre-multiplied alpha support)
  - Support transparency color key
  - Direct path support
- Hardware cursor(win3)
  - 2BPP , two transparent modes
  - Support two size: 32x32 and 64x64
  - 16 level alpha blending

- Win0 and Win1 layer overlay exchangeable
- 3 x 256 x 8 bits display LUTs
- Support color space conversion : YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
- Deflicker support for interlace output
- Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
- Blank and blank display
- Standby mode
- Support non-scaler and scaler output(max up to 1024x768)

- HDMI TX 1.4
  - Only for RK3028A
  - HDMI version 1.4a, HDCP revision 1.2 and DVI version 1.0 compliant transmitter
  - Supports DTV from 480i to 1080i/p HD resolution
  - Supports 3D function defined in HDMI 1.4 spec
  - Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
  - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
  - Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
  - Multiphase 4MHz fixed bandwidth PLL with low jitter
  - HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
  - Support HDMI LipSync if needed as addon feature
  - Lower power operation with optimal power management feature
  - The EDID and CEC function are also supported by Innosilicon HDMI Transmitter Controller
  - Optional Monitor Detection supported through Hot Plug

- LVDS interface
  - 135MHz clock support
  - 28:4 data sub_channel compression at data rates up to 945 Mbps per channel
  - Support VGA,SVGA,XGA and single pixel SXGA
  - PLL requires no external components
  - Comply with the Standard TIA/EIA-644-A LVDS standard
  - Support alternative LVDS output or LVTTL output

- EPD interface
  - EPD T-CON compatible
  - Up to 2048x2048 resolution
  - Up to 16 level gray scale

- Up to 128 frames every scanning
- LUT updateable (8KB)
- Direct mode and LUT mode
- All-update mode and Diff-update mode
- Single-phase and multi-phase mode
- Support window display

1.2.12 Audio Interface

- I2S/PCM
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- Audio Codec
  - 18 to 24 bit High Order Sigma-Delta modulation for DAC for >93 dB SNR configurable
  - 16 to 18 bit High Order Sigma-Delta modulation for ADC for >90 dB SNR configurable
  - Digital interpolation and decimation filter integrated
  - Microphone in and Speaker out Interface
  - On-Chip Analog Post Filter and digital filters
  - Single–ended or differential Input and Output
  - Sampling Rate of 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz
  - Support 16ohm to 32ohm Head Phone and Speaker Phone Output
  - Mono, Stereochannel supported
  - Optional Fractional PLL available that support 6Mhz to 20Mhz clock input to any clockoutput that meets 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz and 128 time oversampling ratio.

1.2.13 Connectivity

- SDIO interface
  - Compatible with SDIO 2.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - 4bits data bus width

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- UartController
  - Three UARTinterface in RK3028A and Two interface in RK3026
  - DMA-based or interrupt-based operation
  - UART0 Embeddeds two 64Bytes FIFO for TX and RX operation respectively
  - UART1/UART2 Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other

special baud rate
- Support non-integer clock divides for baud clock generation
- Support auto flow control mode

- I2C controller
  - 4 on-chip I2C controller in RK3028A and 3 in RK3026
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Compatible with usb host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with usb otg2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.2.14 Others

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter in RK3028A and 2-channel in RK3026
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL less than1 LSB , INL less than 2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface, power dissipation is less than 900uW

- eFuse
  - Two 256bits (32x8) high-density electrical Fuse
  - Programming condition : VP must be 2.5V(±10%)
  - Program time is 10us.
  - Read condition : VP must be 2.5V(±10%)
  - Provide inactive mode

- Operation Temperature Range

- -40°C to +85°C

- Operation Voltage Range
  - Core supply: 1.1V (±10%)
  - IO supply：3.3V (±10%)
- Process
  - SMIC40nm LP
- Package Type
  - BGA313LD (body: 16mm x 16mm ; ball size：0.4mm ; ball pitch：0.8mm)
  - LQFP176L(body: 20mm x 20mm)
- Power
  - TBA

Notes :

① : **DDR3/LVDDR3 are not used simultaneously as well as async and sync ddrnand flash**

②: **In RK3028A, Video decoder and encoder are not used simultaneously because of shared internal buffer**

③: **Actual maximum frame rate will depend on the clock frequency and system bus performance**

④: **Actual maximum data rate will depend on the clock frequency and JPEG compression rate**

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3026/RK3028A.

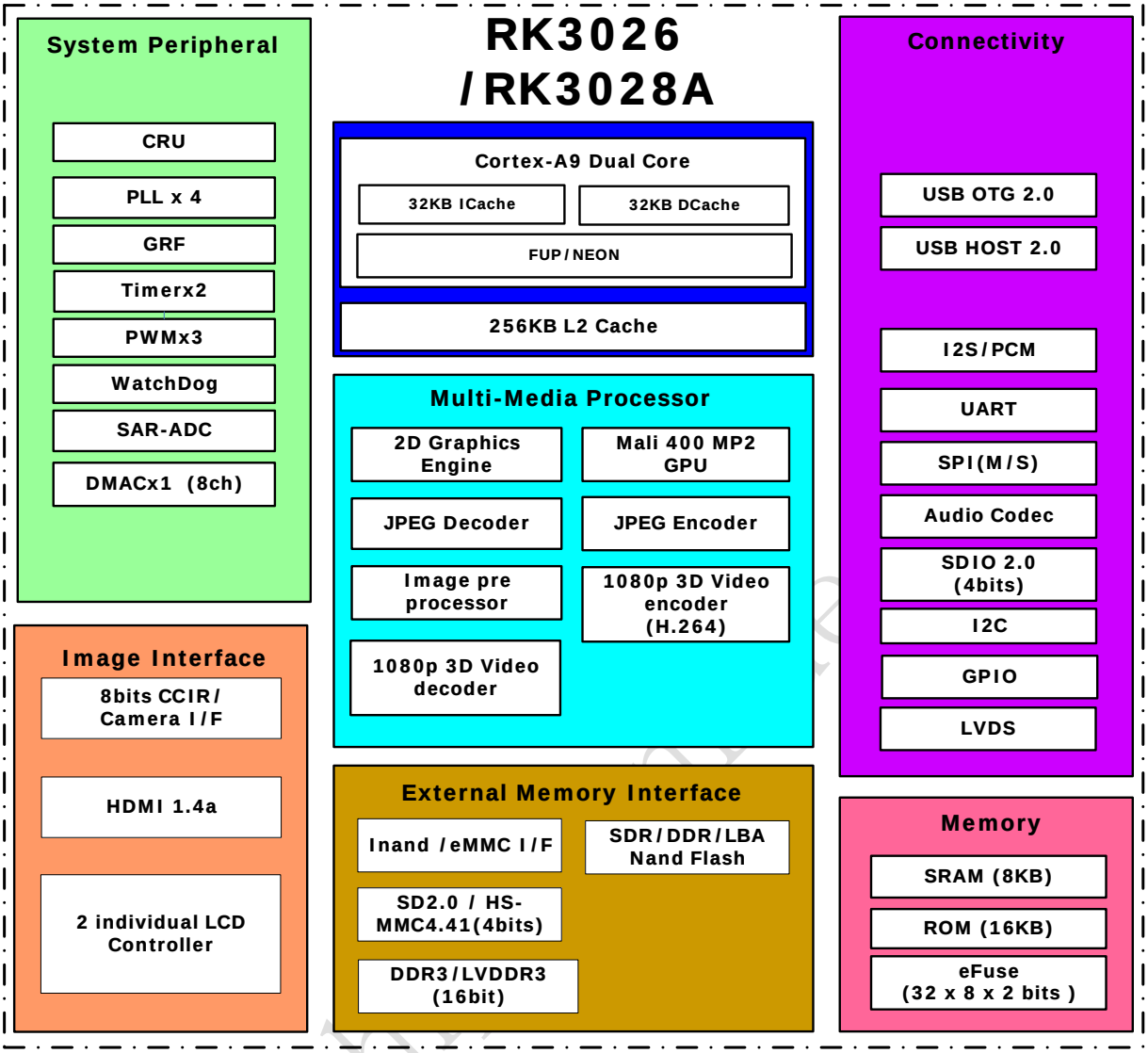


Fig. 1RK3026/RK3028A Block Diagram

chapter 2 Pin Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 1-1, include analog power/ground, another is all the function signals descriptions in Table 1-2, also include analog power/ground.

2.1 RK3026 power/ground IO descriptions

Table 1 RK3026 Power/Ground IO informations

Pin Name	Pin No.	Min(V)	Typ(V)	Max(V)	Descriptions
GND	ePAD		0		Internal Core Ground and Digital IO Ground
AVDD	86,88,89,90,91	0.99	1.1	1.21	Internal CPU Power
CVDD	13,29,69,108,126,161	0.99	1.1	1.21	Core digital Power Supply
VCCIO	35,87,100,115	2.97	3.3	3.63	IO Power Supply
DDR_VDD	10,18,142,150,169	1.425	1.5	1.575	DDR Power Supply
DDR_VSS	139				DDR Power Ground
XVSS	27		0		PLL Power Ground
C/DPLL_DVDD11	22	0.99	1.1	1.21	CODEC/DDR PLL Digital Power
A/GPLL_DVDD11	24	0.99	1.1	1.21	ARM/GENERAL PLL Digital Power
PLL_VCC33	23	2.97	3.3	3.63	PLL Analog Supply
SAR_AVDD33	66	2.97	3.3	3.63	SAR-ADC Analog Power Supply

USB_DVDD11	60	0.99	1.1	1.21	USB Digital Power Supply
USB_AVDD33	59	2.97	3.3	3.63	USB Analog Power Supply
CODEC_AVDD	137	2.97	3.3	3.63	Audio Codec Analog Power Supply
CODEC_AVSS	134,138		0		Audio Codec Ground
LVDS_VCC	44,46	2.97	3.3	3.63	LCD/LVDS Analog Supply

2.2 RK3028A power/ground IO descriptions

Table 2 RK3028A Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C4,F7,F8,F9,F10,F11,F12,G6,G7,G8,G9,G10,G11,G12,G13,H6,H7,H8,H9,H10,H11,H12,H13,J7,J8,J9,J10,J11,J12,J13,J14,K7,K8,K9,K10,K11,K12,K13,L7,L8,L9,L10,L11,L12,L13,M7,M8,M9,M10,M11,M12,M13,M14,N7,N8,N9,N10,N11,N12,N13,V6		0		Internal Core Ground and Digital IO Ground
AVDD	P13,P15,N14,R14,T14	0.99	1.1	1.21	Internal CPU Power
CVDD	J6,P11,K14,E8	0.99	1.1	1.21	Core digital Power Supply
VCCIO	N6,P12,L14,G14	2.97	3.3	3.63	IO Power Supply
DDR_VDD	E6,E9,E11,F5,H5	1.425	1.5	1.575	DDR Power Supply
PLL_VSS1	K6		0		PLL Power Ground
PLL_VSS2	L6		0		PLL Power Ground

APLL_DVDD11	L5	0.99	1.1	1.21	ARM PLL Digital Power
DPLL_DVDD11	M5	0.99	1.1	1.21	DDR PLL Digital Power
C/GPLL_DVDD11	J5	0.99	1.1	1.21	CODEC/GENERAL PLL Digital Power
PLL_VCCIO	M6	2.97	3.3	3.63	PLL Analog Supply
SAR_AVDD33	P10	2.97	3.3	3.63	SAR-ADC Analog Power Supply
USB_DVDD11	P8	0.99	1.1	1.21	USB Digital Power Supply
USB_AVDD33	P9	2.97	3.3	3.63	USB Analog Power Supply
CODEC_AVDD	A13	2.97	3.3	3.63	Audio Codec Analog Power Supply
CODEC_AVSS	B13		0		Audio Codec Ground
HDMI_DVDD11	T5	0.99	1.1	1.21	HDMI Digital Power Supply
HDMI_AVDD33	U4	2.97	3.3	3.63	HDMI Analog Power Supply
HDMI_VSS	P3,R3,T3,U3		0		HDMI Analog Ground
LVDS_DVDD11	T6	0.99	1.1	1.21	LCD/LVDS Digital Supply
LVDS_VCC	P7	2.97	3.3	3.63	LCD/LVDS Analog Supply

2.3 RK3026 function IO descriptions

Table 3 RK3026 IO descriptions

Pin No.	Pin Name	func1	func2	pad① type	driving②	Pull up /down	ResetState③
1	DDR_A0			O	N/A	N/A	O
2	DDR_A2			O	N/A	N/A	O
3	DDR_A5			O	N/A	N/A	O
4	DDR_A9			O	N/A	N/A	O
5	DDR_A13			O	N/A	N/A	O
6	DDR_A7			O	N/A	N/A	O
7	DDR_ODT1			O	N/A	N/A	O
8	DDR_DQ10			I/O	N/A	N/A	I
9	DDR_DQ8			I/O	N/A	N/A	I
11	DDR_DQS1			I/O	N/A	N/A	I
12	DDR_DQS1_N			I/O	N/A	N/A	I
14	DDR_DQ14			I/O	N/A	N/A	I
15	DDR_DQ12			I/O	N/A	N/A	I
16	DDR_DQ15			I/O	N/A	N/A	I
17	DDR_DQ13			I/O	N/A	N/A	I
19	DDR_DQ9			I/O	N/A	N/A	I
20	DDR_DM1			I/O	N/A	N/A	I
21	DDR_DQ11			I/O	N/A	N/A	I
25	XOUT24M			O	N/A	N/A	O
26	XIN24M			I	N/A	N/A	I
28	LCDC_D19/I2C2_SCL/GPIO2_C5/ Ebc_sdshr	lcdc_d19	Ebc_sdshr	I/O	8	down	I
30	LCDC_D18/I2C2_SDA/GPIO2_C4/ Ebc_gdrl	lcdc_d18	Ebc_gdrl	I/O	8	down	I
31	LCDC_D17/GPIO2_C3/ Ebc_gdpwr0	lcdc_d17	Ebc_gdpwr0	I/O	8	down	I
32	LCDC_D16/GPIO2_C2/ Ebc_gdsp	lcdc_d16	Ebc_gdsp	I/O	8	down	I
33	LCDC_D15/GPIO2_C1/ Ebc_gdoe	lcdc_d15	Ebc_gdoe	I/O	8	down	I

34	LCDC_D14/GPIO2_C0/ Ebc_vcom	lcdc_d14	Ebc_vcom	I/O	8	down	I
36	LCDC_D13/GPIO2_B7/ Ebc_sdce5	lcdc_d13	Ebc_sdce5	I/O	8	down	I
37	LCDC_D12/GPIO2_B6/ Ebc_sdce4	lcdc_d12	Ebc_sdce4	I/O	8	down	I
38	LCDC_D11/GPIO2_B5/ Ebc_sdce3	lcdc_d11	Ebc_sdce3	I/O	8	down	I
39	LCDC_D10/GPIO2_B4/ Ebc_sdce2	lcdc_d10	Ebc_sdce2	I/O	8	down	I
40	LCDC_DEN/GPIO2_B3/ Ebc_gdclk	lcdc_den	Ebc_gdclk	I/O	8	down	I
41	LCDC_VSYNC/GPIO2_B2/ Ebc_sdoe	lcdc_vsync	Ebc_sdoe	I/O	8	down	I
42	LCDC_HSYNC/GPIO2_B1/ Ebc_sdle	lcdc_hsync	Ebc_sdle	I/O	8	down	I
43	LCDC_CLK/GPIO2_B0/ Ebc_sdclk	lcdc_dclk	Ebc_sdclk	I/O	12	down	I
45	LVDS_EXTR			A	N/A	N/A	N/A
47	LVDS_CLKN/LCDC_D9/ Ebc_sdce1	lvds_clkn	Ebc_sdce1	A	N/A	N/A	N/A
48	LVDS_CLKP/LCDC_D8/ Ebc_sdce0	lvds_clkp	Ebc_sdce0	A	N/A	N/A	N/A
49	LVDS_TX3N/LCDC_D7/ Ebc_sddo7	lvds_n3	Ebc_sddo7	A	N/A	N/A	N/A
50	LVDS_TX3P/LCDC_D6/ Ebc_sddo6	lvds_p3	Ebc_sddo6	A	N/A	N/A	N/A
51	LVDS_TX2N/LCDC_D5/ Ebc_sddo5	lvds_n2	Ebc_sddo5	A	N/A	N/A	N/A
52	LVDS_TX2P/LCDC_D4/ Ebc_sddo4	lvds_p2	Ebc_sddo4	A	N/A	N/A	N/A
53	LVDS_TX1N/LCDC_D3/ Ebc_sddo3	lvds_n1	Ebc_sddo3	A	N/A	N/A	N/A
54	LVDS_TX1P/LCDC_D2/ Ebc_sddo2	lvds_p1	Ebc_sddo2	A	N/A	N/A	N/A
55	LVDS_TX0N/LCDC_D1/ Ebc_sddo1	lvds_n0	Ebc_sddo1	A	N/A	N/A	N/A
56	LVDS_TX0P/LCDC_D0/ Ebc_sddo0	lvds_p0	Ebc_sddo0	A	N/A	N/A	N/A
57	HOST_DP			A	N/A	N/A	N/A
58	HOST_DM			A	N/A	N/A	N/A
61	USB_EXTR			A	N/A	N/A	N/A
62	OTG_VBUS			A	N/A	N/A	N/A
63	OTG_ID			A	N/A	N/A	N/A
64	OTG_DM			A	N/A	N/A	N/A
65	OTG_DP			A	N/A	N/A	N/A
67	ADCIN0			A	N/A	N/A	N/A
68	ADCIN3/EFUSE			A	N/A	N/A	N/A
70	CIF_D0			I	N/A	down	I
71	CIF_D1			I	N/A	down	I

72	CIF_D2			I	N/A	down	I
73	CIF_D3			I	N/A	down	I
74	CIF_D4			I	N/A	down	I
75	CIF_D5			I	N/A	down	I
76	CIF_D6			I	N/A	down	I
77	CIF_D7			I	N/A	down	I
78	CIF_VSYNC			I	N/A	down	I
79	CIF_HREF			I	N/A	down	I
80	CIF_CLKI			I	N/A	down	I
81	CIF_CLKO			I/O	4	down	I
82	DRIVE_VBUS/GPIO3_C1		drive_vbus	I/O	4	down	I
83	GPIO3_B3/CIF_PDN			I/O	4	up	I
84	PWM0/GPIO0_D2		pwm_0	I/O	4	down	I
85	PWM1/GPIO0_D3		pwm_1	I/O	4	down	I
92	FLASH_CS2/EMMC_CMD/GPIO1_C6		emmc_cmd	I/O	4	up	I
93	FLASH_D0/EMMC_D0/GPIO1_D0		emmc_d0	I/O	8	up	I
94	FLASH_D1/EMMC_D1/GPIO1_D1		emmc_d1	I/O	8	up	I
95	FLASH_D2/EMMC_D2/GPIO1_D2		emmc_d2	I/O	8	up	I
96	FLASH_D3/EMMC_D3/GPIO1_D3		emmc_d3	I/O	8	up	I
97	FLASH_D4/EMMC_D4/GPIO1_D4		emmc_d4	I/O	8	up	I
98	FLASH_D5/EMMC_D5/GPIO1_D5		emmc_d5	I/O	8	up	I
99	FLASH_D6/EMMC_D6/GPIO1_D6		emmc_d6	I/O	8	up	I
100	FLASH_D7/EMMC_D7/GPIO1_D7		emmc_d7	I/O	8	up	I
102	FLASH_ALE/GPIO2_A0			I/O	8	down	I
103	FLASH_CLE/GPIO2_A1			I/O	8	down	I
104	FLASH_WRN/GPIO2_A2			I/O	8	up	I
105	FLASH_RDN/GPO2_A3			I/O	8	up	I
106	FLASH_RDY/GPIO2_A4			I/O	8	up	I
107	FLASH_CS0/GPIO2_A6			I/O	8	up	I
109	FLASH_DQS/EMMC_CLKO/GPIO2_A7		emmc_clkout	I/O	8	up	I
110	NPOR			I	N/A	down	I

111	SDMMC0_D3/JTAG_tms1/GPIO1_C5		Jtag_tms1	I/O	4	up	I
112	SDMMC0_D2/JTAG_tck1/GPIO1_C4		Jtag_tck1	I/O	4	up	I
113	SDMMC0_D1/GPIO1_C3			I/O	4	up	I
114	SDMMC0_D0/GPIO1_C2			I/O	4	up	I
116	SDMMC0_CLKO/GPIO1_C0		mmc0_clkout	I/O	4	down	I
117	SPI_CSN0/UART1_RTSN/GPIO1_B3		spi_csn0	I/O	4	up	I
118	SPI_RXD/UART1_RX/GPIO1_B2		spi_rxd	I/O	4	up	I
119	SPI_TXD/UART1_TX/GPIO1_B1		spi_txd	I/O	4	up	I
120	SPI_CLK/UART1_CTSN/GPIO1_B0		spi_clk	I/O	4	up	I
121	I2S_SDI/GPIO1_A5		i2s_sdi	I/O	4	down	I
122	I2S_SDO/GPIO1_A4		i2s_sdo	I/O	4	down	I
123	I2S_LRCK_RX/GPIO1_A2		i2s_lrckrx	I/O	4	down	I
124	I2S_SCLK/GPIO1_A1		i2s_sclk	I/O	4	down	I
125	I2S_MCLK/GPIO1_A0		i2s_mclk	I/O	4	down	I
127	SDMMC0_CMD/GPIO1_B7		mmc0_cmd	I/O	4	up	I
128	I2C1_SDA/GPIO0_A3		i2c1_tpsda	I/O	4	up	I
129	I2C1_SCL/GPIO0_A2		i2c1_tpscl	I/O	4	up	I
130	I2C0_SDA/GPIO0_A1		i2c0_pmusda	I/O	4	up	I
131	I2C0_SCL/GPIO0_A0		i2c0_pmuscl	I/O	4	up	I
132	CODEC_VCM			A	N/A	N/A	N/A
133	CODEC_MIC			A	N/A	N/A	N/A
135	CODEC_AOL			A	N/A	N/A	N/A
137	CODEC_AOR			A	N/A	N/A	N/A
140	DDR_DQ2			I/O	N/A	N/A	I
141	DDR_DQ0			I/O	N/A	N/A	I
143	DDR_DQS0			I/O	N/A	N/A	I
144	DDR_DQS0_N			I/O	N/A	N/A	I
145	DDR_DQ6			I/O	N/A	N/A	I
146	DDR_DQ4			I/O	N/A	N/A	I
147	DDR_DQ7			I/O	N/A	N/A	I
148	DDR_DQ5			I/O	N/A	N/A	I

150	DDR_DQ1			I/O	N/A	N/A	I
151	DDR_DM0			I/O	N/A	N/A	I
152	DDR_DQ3			I/O	N/A	N/A	I
153	DDR_A8			O	N/A	N/A	O
154	DDR_A6			O	N/A	N/A	O
155	DDR_A14			O	N/A	N/A	O
156	DDR_A15			O	N/A	N/A	O
157	DDR_A11			O	N/A	N/A	O
158	DDR_A1			O	N/A	N/A	O
159	DDR_A4			O	N/A	N/A	O
160	DDR_A12			O	N/A	N/A	O
162	DDR_BA1			O	N/A	N/A	O
163	DDR_BA0			O	N/A	N/A	O
164	DDR_A10			O	N/A	N/A	O
165	DDR_CKE			O	N/A	N/A	O
166	DDR_ODT0			O	N/A	N/A	O
167	DDR_CLK_N			O	N/A	N/A	O
168	DDR_CLK			O	N/A	N/A	O
170	DDR_RASN			O	N/A	N/A	O
171	DDR_CASN			O	N/A	N/A	O
172	DDR_CSN1			O	N/A	N/A	O
173	DDR_CSN0			O	N/A	N/A	O
174	DDR_WEN			G	N/A	N/A	O
175	DDR_BA2			O	N/A	N/A	O
176	DDR_A3			O	N/A	N/A	O

2.4 RK3028A function IO descriptions

Table 4 RK3028A IO descriptions

Ball No.	Ball Name	func1	func2	func3	pad① type	driving②	Pull up /down	ResetState③
C1	DDR_A0				O	N/A	N/A	O
C2	DDR_A2				O	N/A	N/A	O
D1	DDR_A5				O	N/A	N/A	O
D2	DDR_A9				O	N/A	N/A	O
D3	DDR_A13				O	N/A	N/A	O
E1	DDR_A7				O	N/A	N/A	O
E2	DDR_ODT1				O	N/A	N/A	O
E3	DDR_RESETN				O	N/A	N/A	O
E4	DDR_DQ10				I/O	N/A	N/A	I
F3	DDR_DQ8				I/O	N/A	N/A	I
F1	DDR_DQS1				I/O	N/A	N/A	I
F2	DDR_DQS1_N				I/O	N/A	N/A	I
F4	DDR_DQ14				I/O	N/A	N/A	I
G1	DDR_DQ12				I/O	N/A	N/A	I
G2	DDR_DQ15				I/O	N/A	N/A	I
H1	DDR_DQ13				I/O	N/A	N/A	I
H2	DDR_DQ9				I/O	N/A	N/A	I
H3	DDR_DM1				I/O	N/A	N/A	I
H4	DDR_DQ11				I/O	N/A	N/A	I
K1	XOUT24M				O	N/A	N/A	O
K2	XIN24M				I	N/A	N/A	I
L3	LCDC_D20/EBC_border0/UART2_RX/GPIO2_C6		lcdc0_d20	Ebc_border0	I/O	8	down	I
L2	LCDC_D21/EBC_border1/UART2_TX/GPI		lcdc0_d21	Ebc_border1	I/O	8	down	I

	O2_C7							
J3	LCDC_D19/EBC_sdshr/I2C2_SCL/GPIO2_C5		lcdc0_d19	Ebc_sdshr	I/O	8	down	I
J4	LCDC_D18/EBC_gdrl/I2C2_SDA/GPIO2_C4		lcdc0_d18	Ebc_gdrl	I/O	8	down	I
J2	LCDC_D17/EBC_gdpwr0/GPIO2_C3		lcdc0_d17	Ebc_gdpwr0	I/O	8	down	I
J1	LCDC_D16/EBC_gdsp/GPIO2_C2		lcdc0_d16	Ebc_gdsp	I/O	8	down	I
L1	LCDC_D15/EBC_gdoe/GPIO2_C1		lcdc0_d15	Ebc_gdoe	I/O	8	down	I
M1	LCDC_D14/EBC_vcom/GPIO2_C0		lcdc0_d14	Ebc_vcom	I/O	8	down	I
M2	LCDC_D23/EBC_gdpwr2/GPIO2_D1		lcdc0_d23	Ebc_gdpwr2	I/O	8	down	I
M3	LCDC_D22/EBC_gdpwr1/GPIO2_D0		lcdc0_d22	Ebc_gdpwr1	I/O	8	down	I
L4	LCDC_D13/EBC_sdce5/GPIO2_B7		lcdc0_d13	Ebc_sdce5	I/O	8	down	I
M4	LCDC_D12/EBC_sdce4/GPIO2_B6		lcdc0_d12	Ebc_sdce4	I/O	8	down	I
N2	LCDC_D11/EBC_sdce3/GPIO2_B5		lcdc0_d11	Ebc_sdce3	I/O	8	down	I
N1	LCDC_D10/EBC_sdce2/GPIO2_B4		lcdc0_d10	Ebc_sdce2	I/O	8	down	I
P4	LCDC_DEN/EBC_gdclk/GPIO2_B3		lcdc0_den	Ebc_gdclk	I/O	8	down	I
R6	LCDC_VSYNC/EBC_sdoe/GPIO2_B2		lcdc0_vsync	Ebc_sdoe	I/O	8	down	I
P5	LCDC_HSYNC/EBC_sdle/GPIO2_B1		lcdc0_hsync	Ebc_sdle	I/O	8	down	I
R4	LCDC_CLK/EBC_sdclk/GPIO2_B0		lcdc0_dclk	Ebc_sdclk	I/O	12	down	I
U5	HDMI_EXTR				A	N/A	N/A	N/A
P2	HDMI_TX3N				A	N/A	N/A	N/A
P1	HDMI_TX3P				A	N/A	N/A	N/A
R2	HDMI_TX0N				A	N/A	N/A	N/A
R1	HDMI_TX0P				A	N/A	N/A	N/A
T2	HDMI_TX1N				A	N/A	N/A	N/A
T1	HDMI_TX1P				A	N/A	N/A	N/A
U2	HDMI_TX2N				A	N/A	N/A	N/A
U1	HDMI_TX2P				A	N/A	N/A	N/A
W6	LVDS_XRES				A	N/A	N/A	N/A
W2	LVDS_CLKN/LCDC_D9/EBCsdce1		lvds_clkn	Ebc_sdce1	A	N/A	N/A	N/A

V2	LVDS_CLKP/LCDC_D8/EBCsdce0		lvds_clkp	Ebc_sdce0	A	N/A	N/A	N/A
W1	LVDS_TX3N/LCDC_D7/EBCsddo7		lvds_n3	Ebc_sddo7	A	N/A	N/A	N/A
V1	LVDS_TX3P/LCDC_D6/EBCsddo6		lvds_p3	Ebc_sddo6	A	N/A	N/A	N/A
W3	LVDS_TX2N/LCDC_D5/EBCsddo5		lvds_n2	Ebc_sddo5	A	N/A	N/A	N/A
V3	LVDS_TX2P/LCDC_D4/EBCsddo4		lvds_p2	Ebc_sddo4	A	N/A	N/A	N/A
W4	LVDS_TX1N/LCDC_D3/EBCsddo3		lvds_n1	Ebc_sddo3	A	N/A	N/A	N/A
V4	LVDS_TX1P/LCDC_D2/EBCsddo2		lvds_p1	Ebc_sddo2	A	N/A	N/A	N/A
W5	LVDS_TX0N/LCDC_D1/EBCsddo1		lvds_n0	Ebc_sddo1	A	N/A	N/A	N/A
V5	LVDS_TX0P/LCDC_D0/EBCsddo0		lvds_p0	Ebc_sddo0	A	N/A	N/A	N/A
W7	USB1_DP				A	N/A	N/A	N/A
V7	USB1_DN				A	N/A	N/A	N/A
U6	USB_RBIAS				A	N/A	N/A	N/A
T8	USB0_VBUS				A	N/A	N/A	N/A
U8	USB0_ID				A	N/A	N/A	N/A
V8	USB0_DN				A	N/A	N/A	N/A
W8	USB0_DP				A	N/A	N/A	N/A
U9	ADCIN0				A	N/A	N/A	N/A
T9	ADCIN1				A	N/A	N/A	N/A
R9	ADCIN2				A	N/A	N/A	N/A
R8	EFUSE				A	N/A	N/A	N/A
V9	CIF_D0				I	N/A	down	I
W9	CIF_D1				I	N/A	down	I
V10	CIF_D2				I	N/A	down	I
W10	CIF_D3				I	N/A	down	I
R11	CIF_D4				I	N/A	down	I
T11	CIF_D5				I	N/A	down	I
U11	CIF_D6				I	N/A	down	I
V11	CIF_D7				I	N/A	down	I
W11	CIF_VSYNC				I	N/A	down	I
T12	CIF_HREF				I	N/A	down	I

V12	CIF_CLKI				I	N/A	down	I
U12	CIF_CLKO				I/O	4	down	I
W12	DRIVE_VBUS/GPIO3_C1/CIF_PDN0		drive_vbus		I/O	4	down	I
V13	GPIO3_B3/CIF_PDN1				I/O	4	up	I
W13	PWM0/GPIO0_D2		pwm_0		I/O	4	down	I
U14	PWM1/GPIO0_D3		pwm_1		I/O	4	down	I
R12	PWM2/GPIO0_D4		pwm_2		I/O	4	up	I
V14	FLASH_WP/EMMC_PWR/GPIO2_A5		nand_wp	emmc_pwren	I/O	8	down	I
U15	FLASH_CS2/EMMC_CMD/GPIO1_C6		nand_cs2	emmc_cmd	I/O	4	up	I
T15	FLASH_CS3/EMMC_RST/GPIO1_C7		nand_cs3	emmc_rstnout	I/O	4	up	I
W14	FLASH_D0/EMMC_D0/GPIO1_D0		nand_d0	emmc_d0	I/O	8	up	I
V15	FLASH_D1/EMMC_D1/GPIO1_D1		nand_d1	emmc_d1	I/O	8	up	I
W15	FLASH_D2/EMMC_D2/GPIO1_D2		nand_d2	emmc_d2	I/O	8	up	I
U16	FLASH_D3/EMMC_D3/GPIO1_D3		nand_d3	emmc_d3	I/O	8	up	I
V16	FLASH_D4/EMMC_D4/GPIO1_D4		nand_d4	emmc_d4	I/O	8	up	I
W16	FLASH_D5/EMMC_D5/GPIO1_D5		nand_d5	emmc_d5	I/O	8	up	I
T17	FLASH_D6/EMMC_D6/GPIO1_D6		nand_d6	emmc_d6	I/O	8	up	I
U17	FLASH_D7/EMMC_D7/GPIO1_D7		nand_d7	emmc_d7	I/O	8	up	I
V17	FLASH_ALE/GPIO2_A0		nand_ale		I/O	8	down	I
W17	FLASH_CLE/GPIO2_A1		nand_cle		I/O	8	down	I
T18	FLASH_WRN/GPIO2_A2		nand_wrn		I/O	8	up	I
U18	FLASH_RDN/GPO2_A3		nand_rdn		I/O	8	up	I
V18	FLASH_RDY/GPIO2_A4		nand_rdy		I/O	8	up	I
W18	FLASH_CS0/GPIO2_A6		nand_cs0		I/O	8	up	I
V19	FLASH_DQS/EMMC_CLKO/GPIO2_A7		nand_dqs	emmc_clkout	I/O	8	up	I
W19	FLASH_CS1/GPIO0_C7		nand_cs1		I/O	4	up	I
L15	TEST				I	N/A	down	I
M15	JTAG_RSTN				I	N/A	down	I
J15	JTAG_TCK				I	N/A	down	I
H15	JTAG_TDI				I	N/A	up	I

F15	JTAG_TDO				I/O	4	down	I
F16	JTAG_TMS				I/O	4	down	I
U19	SDMMC0_PWR/GPIO1_B6		mmc0_pwren		I/O	4	down	I
T19	NPOR				I	N/A	down	I
R16	SDMMC0_D3/JTAG_tms1/GPIO1_C5		mmc0_d3	Jtag_tms1	I/O	4	up	I
R17	SDMMC0_D2/JTAG_tck1/GPIO1_C4		mmc0_d2	Jtag_tck1	I/O	4	up	I
R18	SDMMC0_D1/GPIO1_C3		mmc0_d1		I/O	4	up	I
R19	SDMMC0_D0/GPIO1_C2		mmc0_d0		I/O	4	up	I
P17	SDMMC0_DET/GPIO1_C1		mmc0_detn		I/O	4	up	I
P18	SDMMC1_D3/GPIO0_B6		mmc1_d3		I/O	4	up	I
P16	TEST_CLKO/GPIO3_D7		testclk_out		I/O	4	down	I
P19	SDMMC1_D2/GPIO0_B5		mmc1_d2		I/O	4	up	I
N18	SDMMC1_D1/GPIO0_B4		mmc1_d1		I/O	4	up	I
N19	SDMMC1_D0/GPIO0_B3		mmc1_d0		I/O	4	up	I
M16	SDMMC1_CLKO/GPIO0_B1		mmc1_clkout		I/O	4	up	I
M17	SDMMC1_CMD/GPIO0_B0		mmc1_cmd		I/O	4	up	I
M18	GPIO3_C7				I/O	4	up	I
M19	GPIO3_C6				I/O	4	up	I
L16	GPIO3_C5				I/O	4	down	I
L17	SDMMC0_CLKO/GPIO1_C0		mmc0_clkout		I/O	4	down	I
L19	GPIO3_C4				I/O	4	down	I
L18	SPI_CSN0/UART1_RTSN/GPIO1_B3		spi_csn0	uart1_rtsn	I/O	4	up	I
K18	GPIO3_C3				I/O	4	down	I
J16	SPI_RXD/UART1_RX/GPIO1_B2		spi_rxd	uart1_sin	I/O	4	down	I
K19	GPIO3_C2				I/O	4	down	I
J17	SPI_TXD/UART1_TX/GPIO1_B1		spi_txd	uart1_sout	I/O	4	down	I
J18	GPIO3_C0				I/O	4	down	I
J19	SPI_CLK/UART1_CTSN/GPIO1_B0		spi_clk	uart1_ctsn	I/O	4	down	I
H16	I2S_SDI/GPS_SIGN/GPIO1_A5		i2s_sdi	gps_sign	I/O	4	down	I
H17	I2S_SDO/GPS_MAG/GPIO1_A4		i2s_sdo	gps_mag	I/O	4	down	I

H18	I2S_LRCK_TX/GPIO1_A3		i2s_lrcktx		I/O	4	down	I
H19	I2S_LRCK_RX/GPS_CLK/GPIO1_A2		i2s_lrckrx	gps_clk	I/O	4	down	I
G18	I2S_SCLK/GPIO1_A1		i2s_sclk		I/O	4	down	I
G19	I2S_MCLK/GPIO1_A0		i2s_mclk		I/O	4	down	I
F17	SDMMC0_CMD/GPIO1_B7		mmc0_cmd		I/O	4	up	I
F18	I2C1_SDA/GPIO0_A3		i2c1_tpsda		I/O	4	up	I
F19	I2C1_SCL/GPIO0_A2		i2c1_tpscl		I/O	4	up	I
E19	I2C0_SDA/GPIO0_A1		i2c0_pmusda		I/O	4	up	I
E18	I2C0_SCL/GPIO0_A0		i2c0_pmuscl		I/O	4	up	I
E16	SPI_CSN1/GPIO1_B4		spi_csn1		I/O	4	up	I
D19	SDMMC0_WP/GPIO1_A7		mmc0_wrprt		I/O	4	down	I
E17	SDMMC1_PWR/GPIO0_D6		mmc1_pwren		I/O	4	down	I
D17	UART2_CTSN/GPIO0_D1		urt2_ctsn		I/O	4	up	I
C19	UART2_RTSN/GPIO0_D0		urt2_rtsn		I/O	4	up	I
C18	GPIO0_C6				I/O	4	up	I
D18	GPIO0_C5				I/O	4	up	I
A17	HDMI_CEC/GPIO0_C4		hdmi_cecsda		I/O	4	up	I
B19	UART0_CTSN/GPIO0_C3		urt0_ctsn		I/O	4	up	I
B18	UART0_RTSN/GPIO0_C2		urt0_rtsn		I/O	4	up	I
A18	UART0_RX/GPIO0_C1		urt0_sin		I/O	4	up	I
A19	UART0_TX/GPIO0_C0		urt0_sout		I/O	4	down	I
B17	GPIO3_D6				I/O	4	down	I
C17	GPIO3_D5				I/O	4	down	I
A16	GPIO3_D4				I/O	4	down	I
B16	GPIO3_D3				I/O	4	up	I
C16	GPIO3_D2				I/O	4	up	I
A15	GPIO3_D1				I/O	4	up	I
B15	I2C3_SDA/HDMI_SDA/GPIO0_A7		i2c3_cifsda	hdmi_ddcsda	I/O	4	up	I
C15	I2C3_SCL/HDMI_SCL/GPIO0_A6		i2c3_cifscl	hdmi_ddcscl	I/O	4	up	I
D15	HDMI_HPD/GPIO0_B7		hdmi_hotplugi		I/O	4	down	I

			n					
B14	CODEC_MICL				A	N/A	N/A	N/A
A14	CODEC_AIL				A	N/A	N/A	N/A
D14	CODEC_VCM				A	N/A	N/A	N/A
C14	CODEC_MICBIAS				A	N/A	N/A	N/A
C12	CODEC_AIR				A	N/A	N/A	N/A
D12	CODEC_MICR				A	N/A	N/A	N/A
A12	CODEC_AOL				A	N/A	N/A	N/A
E14	CODEC_AOMS				A	N/A	N/A	N/A
E12	CODEC_AOM				A	N/A	N/A	N/A
F13	CODEC_HPDET				A	N/A	N/A	N/A
B12	CODEC_AOR				A	N/A	N/A	N/A
C11	DDR_DQ2				I/O	N/A	N/A	I
D11	DDR_DQ0				I/O	N/A	N/A	I
A11	DDR_DQS0				I/O	N/A	N/A	I
B11	DDR_DQS0_N				I/O	N/A	N/A	I
B10	DDR_DQ6				I/O	N/A	N/A	I
A10	DDR_DQ4				I/O	N/A	N/A	I
D9	DDR_DQ7				I/O	N/A	N/A	I
C9	DDR_DQ5				I/O	N/A	N/A	I
B9	DDR_DQ1				I/O	N/A	N/A	I
A9	DDR_DM0				I/O	N/A	N/A	I
D8	DDR_DQ3				I/O	N/A	N/A	I
C8	DDR_A8				O	N/A	N/A	O
B8	DDR_A6				O	N/A	N/A	O
A8	DDR_A14				O	N/A	N/A	O
B7	DDR_A15				O	N/A	N/A	O
A7	DDR_A11				O	N/A	N/A	O
D6	DDR_A1				O	N/A	N/A	O
C6	DDR_A4				O	N/A	N/A	O

B6	DDR_A12				O	N/A	N/A	O
A6	DDR_BA1				O	N/A	N/A	O
D5	DDR_BA0				O	N/A	N/A	O
C5	DDR_A10				O	N/A	N/A	O
B5	DDR_CKE				O	N/A	N/A	O
A5	DDR_ODT0				O	N/A	N/A	O
B4	DDR_CLK_N				O	N/A	N/A	O
A4	DDR_CLK				O	N/A	N/A	O
B3	DDR_RASN				O	N/A	N/A	O
A3	DDR_CASN				O	N/A	N/A	O
A2	DDR_CSN1				O	N/A	N/A	O
C3	DDR_CSN0				O	N/A	N/A	O
B2	DDR_WEN				G	N/A	N/A	O
A1	DDR_BA2				O	N/A	N/A	O
B1	DDR_A3				O	N/A	N/A	O

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②:Output Drive Unit is mA , only Digital IO have drive value

③:Reset state : I = input without any pull resistor ,O = output without any pull resistor ,

2.5 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 5 RK3026/RK3028A IO function description list

Interface	Pin Name	Direction	Description
Misc	xin24m	I	Clock input of 24MHz crystal
	xout24m	O	Clock output of 24MHz crystal
	npor	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	trst_n	I	JTAG interface reset input
	tck	I	JTAG interface clock input/SWD interface clock input
	tdi	I	JTAG interface TDI input
	tms	I/O	JTAG interface TMS input/SWD interface data out
	tdo	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_pwr_en	O	sdmmc card power-enable control signal

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.
	sdio_pwr_en	O	sdio card power-enable control signal

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.

	emmc_pwr_en	O	emmc card power-enable control signal

Interface	Pin Name	Direction	Description
DMC	CLK	O	Active-high clock signal to the memory device.
	CLK_n	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSn*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASn	O	Active-low row address strobe to the memory device.
	CASn	O	Active-low column address strobe to the memory device.
	WEn	O	Active-low write enable strobe to the memory device.
	BA*i*(*i*=0~2)	O	Bank address signal to the memory device.
	A*i*(*i*=0~15)	O	Address signal to the memory device.
	DQi_A(i=0~7) DQi_B(i=0~7)	I/O	Bidirectional data line to the memory device.
	DQS_A DQS_B	I/O	Active-high bidirectional data strobes to the memory device.
	DQSn_A DQSn_B	I/O	Active-low bidirectional data strobes to the memory device.
	DM_A DM_B	O	Active-low data mask signal to the memory device.
	ODT*i*(*i*=0,1)	O	On-Die Termination output signal for two chip select.
	RESETN	O	DDR3 reset signal to the memory device

Interface	Pin Name	Direction	Description
Nand Controller	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal
	flash_data*i*(*i*=0~7)	I/O	8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn*i*(*i*=0~3)	O	Flash chip enable signal for chip i, i=0~3

Interface	Pin Name	Direction	Description
I2S/PCM Controller	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock

	i2s_lrck_rx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo	O	I2S/PCM serial data ouput
	i2s_lrck_tx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPI Controller	spi_clk	I/O	spi serial clock
	spi_csn*i* *(i=0,1)*	I/O	spi chip select signal,low active
	spi_txd	O	spi serial data output
	spi_rxd	I	spi serial data input

Interface	Pin Name	Direction	Description
EBC	ebc_sdclk	O	Eink panel source clock
	ebc_sdle	O	Eink panel source latch pulse
	ebc_sdoe	O	Eink panel source data output enable
	ebc_sdce *i* *(i=0~5)*	O	Eink panel source data shift enable
	ebc_sddo *i* *(i=0~7)*	O	Eink panel source data
	ebc_sdshr	O	Eink panel source scan direction
	ebc_gdclk	O	Eink panel gate clock
	ebc_gdoe	O	Eink panel gate output mode
	ebc_gdsp	O	Eink panel gate start pulse
	ebc_gdrl	O	Eink panel gate scan direction
	ebc_vcom	O	Eink panel com voltage enable
	ebc_border *i* *(i=0,1)*	O	Eink panel border output signal
	ebc_gdpwr *i* *(i=0~2)*	O	Eink panel power control signal

Interface	Pin Name	Direction	Description
LCDC	lcdc_dclk	O	LCDC RGB interface display clock out, MCU i80 interface RS signal

	lcdc_vsync	O	LCDC RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc_hsync	O	LCDC RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc_den	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	lcdc_data*i*(*i*=0~23)	I/O	LCDC data output/input

Interface	Pin Name	Direction	Description
Camera IF	cif_clkin	I	Camera interface input pixel clock
	cif_clkout	O	Camera interface output work clock
	cif_vsync	I	Camera interface vertical sync signal
	cif_href	I	Camera interface horizontial sync signal
	cif_data*i*(*i*=0~7)	I	Camera interface 8-bit input pixel data

Interface	Pin Name	Direction	Description
GPS	gps_sign	I	GPS sign data input
	gps_mag	I	GPS mag data input
	gps_clk	I	GPS rf clock input

Interface	Pin Name	Direction	Description
PWM	Pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output

	uart2_cts_n	O	UART2 clear to send
	uart2_rts_n	I	UART2 request to send

Interface	Pin Name	Direction	Description
USB OTG2.0 /HOST 2.0	otg_dp	I/O	USB OTG 2.0 Data signal DP
	otg_dm	I/O	USB OTG 2.0 Data signal DM
	otg_vbus	N/A	USB OTG 2.0 5V power supply pin
	otg_id	I	USB OTG 2.0 ID indicator
	otg_drv	O	USB OTG 2.0 drive VBUS
	host_dp	I/O	USB HOST 2.0 Data signal DP
	host_dm	I/O	USB HOST 2.0 Data signal DM
	host_extr	N/A	133 Ohm Reference external resistance

Interface	Pin Name	Direction	Description
LVDS	lvds_extr	I	Connected to external 12Komh through bonding pad
	lvds_txp_n	O	Transmit serial data out(Positive), n=1~4
	lvds_txn_n	O	Transmit serial data out(Negative), n=1~4
	lvds_clkp	O	Output clock
	lvds_clkn	O	Output clock(Negative)

Interface	Pin Name	Direction	Description
Audio Codec	codec_micl	A	Left channel microphone input
	codec_ail	A	Left channel line-in input
	codec_vcm	A	Decoupling for voltage reference
	codec_micbias	A	Microphone bias voltage output
	codec_air	A	Right channel line-in input
	codec_micr	A	Right channel microphone input
	codec_aol	A	Left channel DAC driver amplifier output
	codec_aor	A	Right channel DAC driver amplifier output
	codec_aoms	A	Headphone virtual ground feedback
	codec_aom		Headphone virtual ground
	codec_hpdet		Headphone jack detection

Interface	Pin Name	Direction	Description
HDMI	hdmi_extr	O	Connect 2.0Kohm resistor to ground to generate reference current
	hdmi_cec	I/O	HDMI CEC communication
	hdmi_hpd	I/O	HDMI hot plug detection interrupt
	hdmi_TXCN	O	TMDS negative clock line
	hdmi_TXCP	O	TMDS positive clock line

	hdmi_TX*i*N(*i*=0~2)	O	TMDS negative serial data line
	hdmi_TX*i*P(*i*=0~2)	O	TMDS positive serial data line

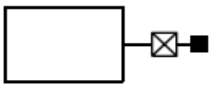
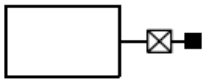
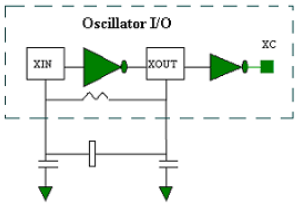
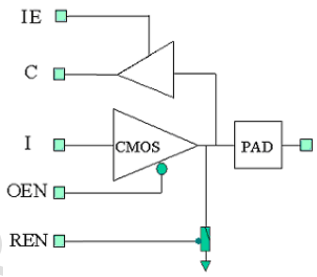
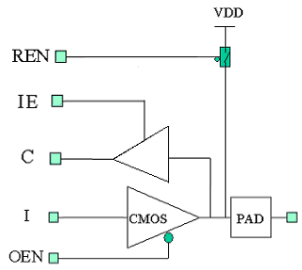
Interface	Pin Name	Direction	Description
SAR-ADC	saradc_ain*i* (i=0~2)	N/A	SAR-ADC input signal for 3 channel

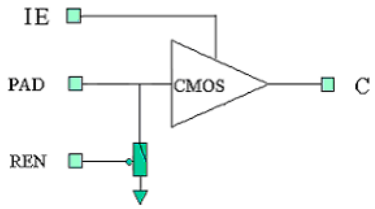
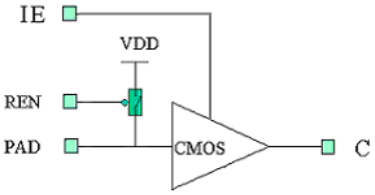
Interface	Pin Name	Direction	Description
eFuse	Efuse_vp	N/A	eFuse program and sense power

2.6 RK3026/RK3028A IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 6 RK3026/RK3028A IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VP
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with internal register	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRN)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRN)

F		controllable input pad with controllable pulldown	Part of digital GPIO (PICDRN)
G		controllable input pad with controllable pullup	Part of digital GPIO (PICURN)

chapter 3 Package information

3.1 RK3026 package

RK3026 has type of package LQFP176
body: 20mm x 20mm ; pin pitch : 0.4mm

3.2 LQFP176 Dimension

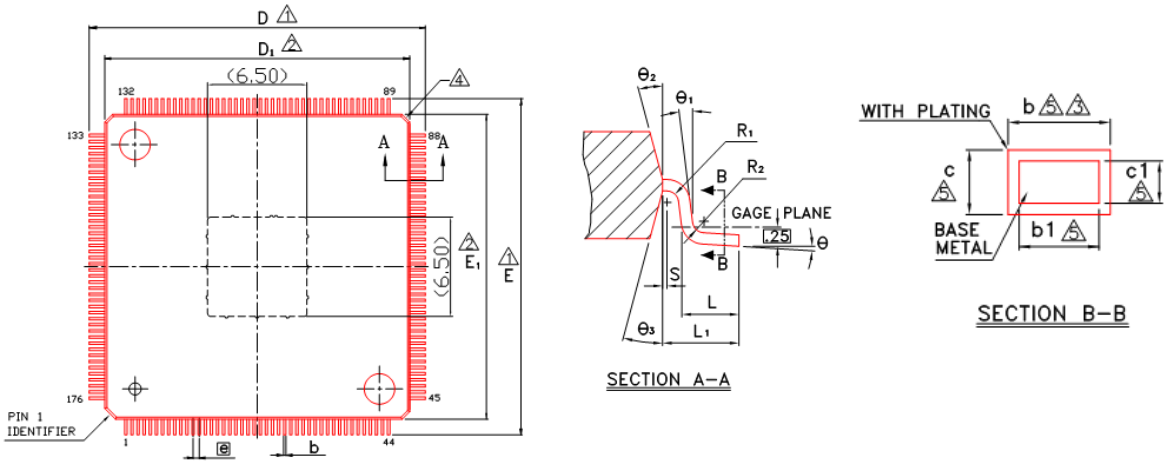


Fig. 2RK3026LQFP176 Package Top View

Fig. 3RK3026LQFP176 Package Side View

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Fig. 4RK3026LQFP176 Package Dimension

3.3 RK3028A package

RK3028A has type of package TFBGA313
body: 16mm x 16mm ; ball size : 0.4mm ; ball pitch : 0.8mm

3.4 TFBGA313 Dimension

TFBGA313 Dimension

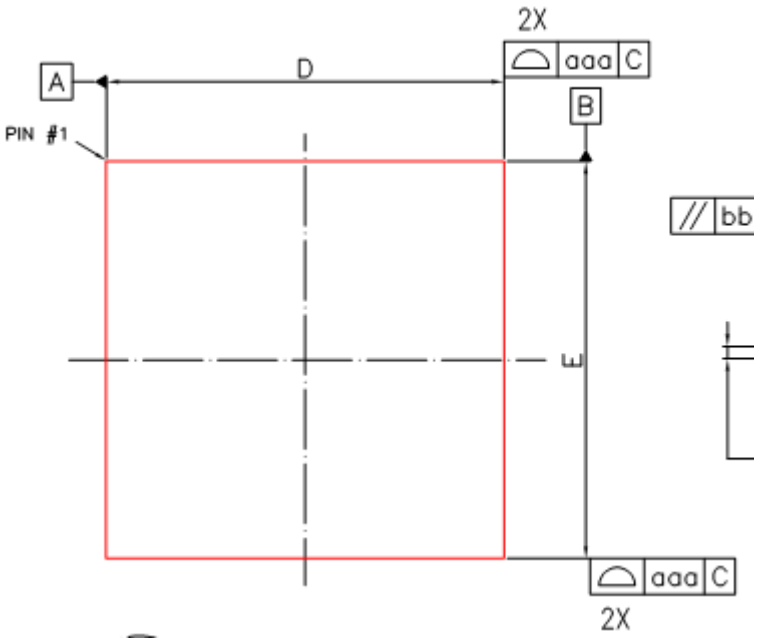


Fig. 5RK3028A TFBGA313 Package Top View

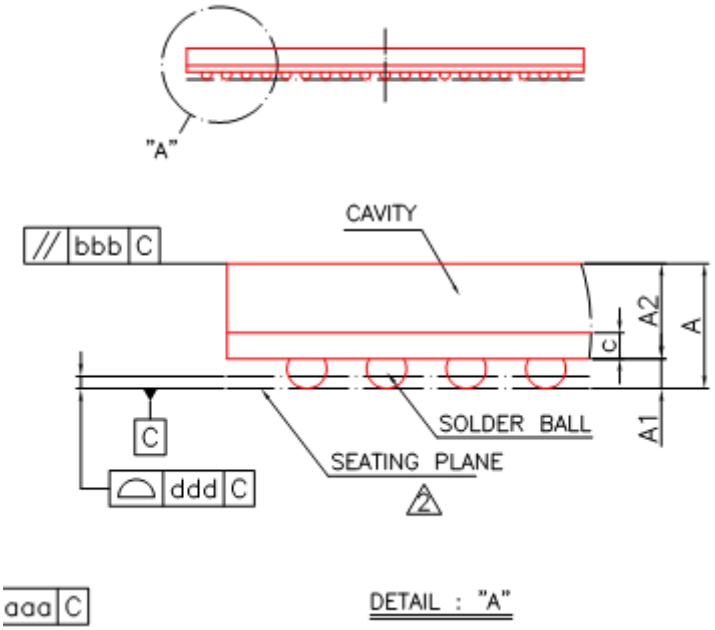


Fig. 6RK3028A TFBGA313 Package Side View

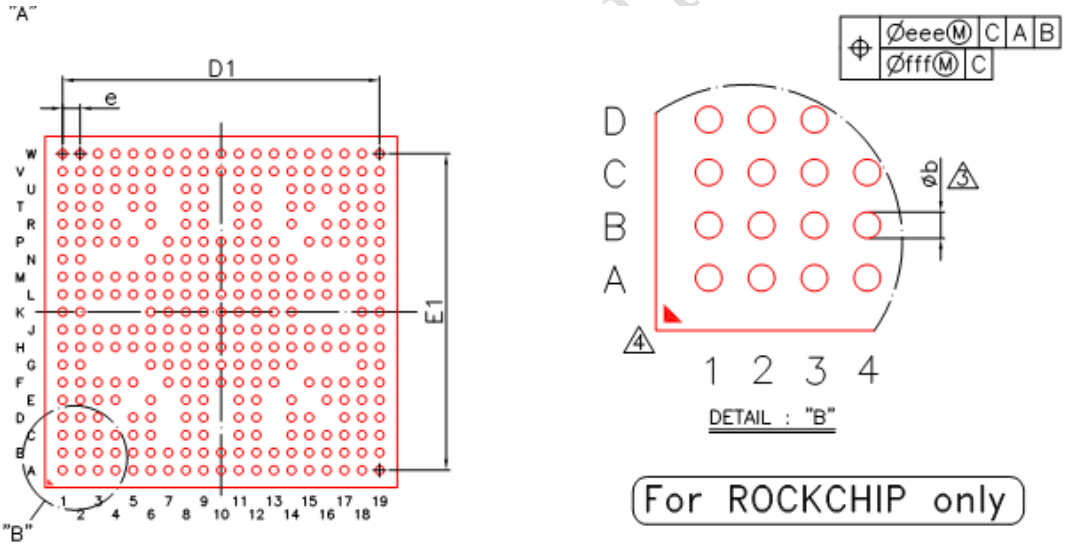


Fig. 7RK3028A TFBGA313 Package Bottom View

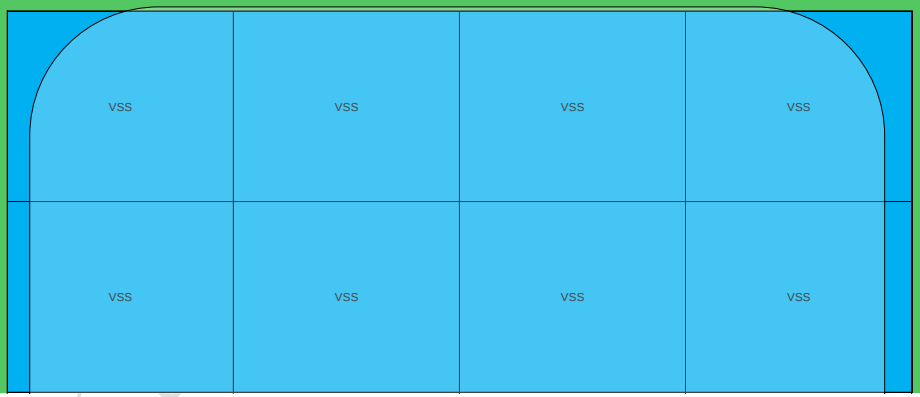
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.40	---	---	0.567	---
E1	---	14.40	---	---	0.567	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	19/19			19/19		

Fig. 8RK3028A TFBGA313 Package Dimension

3.5 RK3026 PIN Map

Pin Number	Pin Name	Pin Number
1	DDR_A0	132 CVDD
2	DDR_A2	131 I2C0_SCL/GPIO0_A0
3	DDR_A5	130 I2C0_SDA/GPIO0_A1
4	DDR_A9	129 I2C1_SCL/GPIO0_A2
5	DDR_A13	128 I2C1_SDA/GPIO0_A3
6	DDR_A7	127 SDMMC0_CMD/GPIO1_B7
7	DDR_ODT1	126 VCCIO
8	DDR_DQ10	125 I2S_MCLK/GPIO1_A0
9	DDR_DQ8	124 I2S_SCLK/GPIO1_A1
10	DDR_VDD	123 I2S_LRCK_RX/GPS_CLK/GPIO1_A2
11	DDR_DQS1	122 I2S_SDO/GPS_MAG/GPIO1_A4
12	DDR_DQS1_N	121 I2S_SDI/GPS_SIGN/GPIO1_A5
13	CVDD	120 SPI_CLK/UART1_CTSN/GPIO1_B0
14	DDR_DQ14	119 SPI_TXD/UART1_TX/GPIO1_B1
15	DDR_DQ12	118 SPI_RXD/UART1_RX/GPIO1_B2
16	DDR_DQ15	117 SPI_CSN0/UART1_RTSN/GPIO1_B3
17	DDR_DQ13	116 SDMMC0_CLKO/GPIO1_C0
18	DDR_VDD	115 VCCIO
19	DDR_DQ9	114 SDMMC0_DET/GPIO1_C1
20	DDR_DM1	113 SDMMC0_D0/GPIO1_C2
21	DDR_DQ11	112 SDMMC0_D1/GPIO1_C3
22	C/DPLL_DVDD12	111 SDMMC0_D2/GPIO1_C4

Pin Number	Pin Name
176	DDR_VDD
175	DDR_A3
174	DDR_BA2
173	DDR_WEN
172	DDR_CSN0
171	DDR_CSN1
170	DDR_CASN
169	DDR_RASN
168	DDR_VDD
167	DDR_CLK
166	DDR_CLK_N
165	DDR_ODT0
164	DDR_CKE
163	DDR_A10
162	DDR_BA0
161	DDR_BA1
160	CVDD
159	DDR_A12
158	DDR_A4
157	DDR_A1
156	DDR_A11
155	DDR_A15
154	DDR_A14
153	DDR_A6
152	DDR_A8
151	DDR_DQ3
150	DDR_DM0
149	DDR_DQ1
148	DDR_VDD
147	DDR_DQ5
146	DDR_DQ7
145	DDR_DQ4
144	DDR_DQ6
143	CVDD
142	DDR_DQS0_N
141	DDR_DQS0
140	DDR_VDD
139	DDR_DQ0
138	DDR_DQ2
137	CODEC_AOR
136	CODEC_AVDD
135	CODEC_AOL
134	CODEC_MICR
133	CODEC_VCM



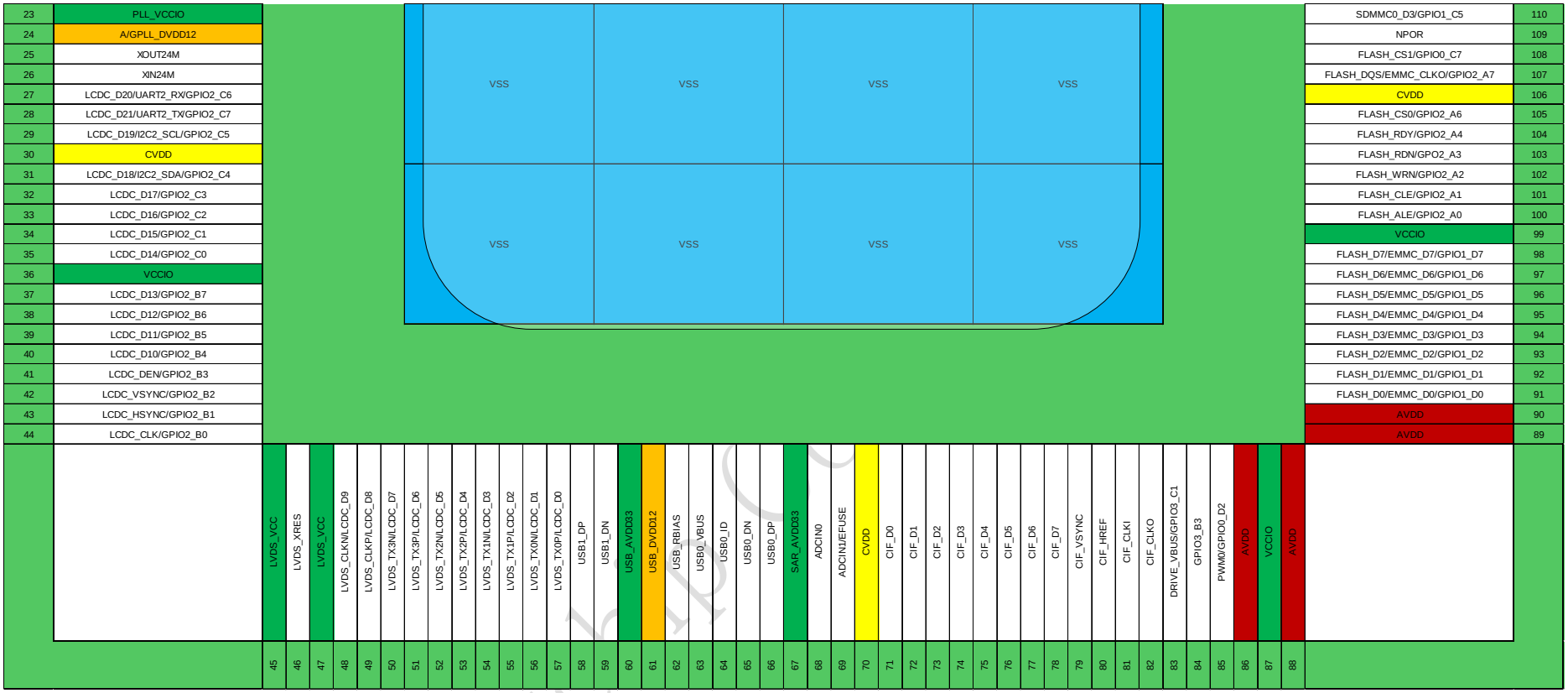


Fig. 9 RK3026 LQFP176PIN Map

3.6 RK3028A Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	DDR_BA2	DDR_CSN1	DDR_CASN	DDR_CLK	DDR_ODT0	DDR_BA1	DDR_A11	DDR_A14	DDR_DM0	DDR_DQ4	DDR_DQS0	CODEC_AOL	CODEC_AVDD	CODEC_AIL	GPIO3_D1	GPIO3_D4	HDMI_CEC/GPIO0_C4	UART0_RX/GPIO0_C1	UART0_TX/GPIO0_C0	A
B	DDR_A3	DDR_WEN	DDR_RASN	DDR_CLK_N	DDR_CKE	DDR_A12	DDR_A15	DDR_A6	DDR_DQ1	DDR_DQ6	DDR_DQS0_N	CODEC_AOR	CODEC_AVSS	CODEC_MICL	I2C3_SDA/HDMI_SDA/GPIO0_A7	GPIO3_D3	GPIO3_D6	UART0_RTSN/GPIO0_C2	UART0_CTSN/GPIO0_C3	B
C	DDR_A0	DDR_A2	DDR_CSN0	VSS	DDR_A10	DDR_A4		DDR_A8	DDR_DQ5		DDR_DQ2	CODEC_AIR		CODEC_MICBIAS	I2C3_SCL/HDMI_SCL/GPIO0_A6	GPIO3_D2	GPIO3_D5	GPIO0_C6	UART2_RTSN/GPIO0_D0	C
D	DDR_A5	DDR_A9	DDR_A13		DDR_BA0	DDR_A1		DDR_DQ3	DDR_DQ7		DDR_DQ0	CODEC_MICR		CODEC_VCM	HDMI_HPD/GPIO0_B7		UART2_CTSN/GPIO0_D1	GPIO0_C5	SDMMC0_WP/GPIO1_A7	D
E	DDR_A7	DDR_ODT1	DDR_RESETN	DDR_DQ10		DDR_VDD		CVDD	DDR_VDD		DDR_VDD	VSS		VSS		SPI_CSN1/GPIO1_B4	SDMMC1_PWR/GPIO0_D6	I2C0_SCL/GPIO0_A0	I2C0_SDA/GPIO0_A1	E
F	DDR_DQS1	DDR_DQS1_N	DDR_DQ8	DDR_DQ14	DDR_VDD		VSS	VSS	VSS	VSS	VSS	VSS	VSS		JTAG_TDO	JTAG_TMS	SDMMC0_CMD/GPIO1_B7	I2C1_SDA/GPIO0_A3	I2C1_SCL/GPIO0_A2	F
G	DDR_DQ12	DDR_DQ15				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO				I2S_SCLK/GPIO1_A1	I2S_MCLK/GPIO1_A0	G
H	DDR_DQ13	DDR_DQ9	DDR_DM1	DDR_DQ11	DDR_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_TDI	I2S_SDI/GPS_SIGN/GPIO1_A5	I2S_SDO/GPS_MAG/GPIO1_A4	I2S_LRCK_TX/GPIO1_A3	I2S_LRCK_RX/GPS_CLK/GPIO1_A2	H
J	LCDC_D16/GPIO2_C2	LCDC_D17/GPIO2_C3	LCDC_D19/I2C2_SCL/GPIO2_C5	LCDC_D18/I2C2_SDA/GPIO2_C4	C/GPLL_DVDD12	CVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_TCK	SPI_RXD/UART1_RX/GPIO1_B2	SPI_TXD/UART1_TX/GPIO1_B1	GPIO3_C0	SPI_CLK/UART1_CTSN/GPIO1_B0	J

K	XOUT24M	XIN24M				PLL_VSS1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD				GPIO3_C3	GPIO3_C2	K
L	LCDC_D15/GPIO2_C1	LCDC_D21/UART2_TX/GPIO2_C7	LCDC_D20/UART2_RX/GPIO2_C6	LCDC_D13/GPIO2_B7	APLL_DVDD12	PLL_VSS2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO	TEST	GPIO3_C5	SDMMC0_CLKO/GPIO1_C0	SPI_CSN0/UART1_RTSN/GPIO1_B3	GPIO3_C4	L
M	LCDC_D14/GPIO2_C0	LCDC_D23/GPIO2_D1	LCDC_D22/GPIO2_D0	LCDC_D12/GPIO2_B6	DPLL_DVDD12	PLL_VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_RSTN	SDMMC1_CLKO/GPIO0_B1	SDMMC1_CMD/GPIO0_B0	GPIO3_C7	GPIO3_C6	M
N	LCDC_D10/GPIO2_B4	LCDC_D11/GPIO2_B5				VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD				SDMMC1_D1/GPIO0_B4	SDMMC1_D0/GPIO0_B3	N
P	HDMI_TX3P	HDMI_TX3N	HDMI_VSS	LCDC_DEN/GPIO2_B3	LCDC_HSYNC/GPIO2_B1		LVDS_VCC	USB_DVDD12	USB_AVDD33	SAR_AVDD33	CVDD	VCCIO	AVDD		AVDD	TEST_CLKO/GPIO3_D7	SDMMC0_DET/GPIO1_C1	SDMMC1_D3/GPIO0_B6	SDMMC1_D2/GPIO0_B5	P
R	HDMI_TX0P	HDMI_TX0N	HDMI_VSS	LCDC_CLK/GPIO2_B0		LCDC_VSYNC/GPIO2_B2		EFUSE	ADCIN2		CIF_D4	PWM2/GPIO0_D4		AVDD		SDMMC0_D3/GPIO1_C5	SDMMC0_D2/GPIO1_C4	SDMMC0_D1/GPIO1_C3	SDMMC0_D0/GPIO1_C2	R
T	HDMI_TX1P	HDMI_TX1N	HDMI_VSS		HDMI_DVDD12	LVDS_DVDD12		USB0_VBUS	ADCIN1		CIF_D5	CIF_HREF		AVDD	FLASH_CS3/EMMC_RST/GPIO1_C7		FLASH_D6/EMMC_D6/GPIO1_D6	FLASH_WRN/GPIO2_A2	NPOR	T
U	HDMI_TX2P	HDMI_TX2N	HDMI_VSS	HDMI_AVDD33	HDMI_EXTR	USB_RBIAS		USB0_ID	ADCIN0		CIF_D6	CIF_CLKO		PWM1/GPIO0_D3	FLASH_CS2/EMMC_CMD/GPIO1_C6	FLASH_D3/EMMC_D3/GPIO1_D3	FLASH_D7/EMMC_D7/GPIO1_D7	FLASH_RDN/GPIO2_A3	SDMMC0_PWR/GPIO1_B6	U
V	LVDS_TX3P/LCDC_D6	LVDS_CLKP/LCDC_D8	LVDS_TX2P/LCDC_D4	LVDS_TX1P/LCDC_D2	LVDS_TX0P/LCDC_D0	VSS	USB1_DN	USB0_DN	CIF_D0	CIF_D2	CIF_D7	CIF_CLKI	GPIO3_B3/CIF_PDN1	FLASH_WP/EMMC_PWR/GPIO2_A5	FLASH_D1/EMMC_D1/GPIO1_D1	FLASH_D4/EMMC_D4/GPIO1_D4	FLASH_ALE/GPIO2_A0	FLASH_RDY/GPIO2_A4	FLASH_DQS/EMMC_CLKO/GPIO2_A7	V
W	LVDS_TX3N/LCDC_D7	LVDS_CLKN/LCDC_D9	LVDS_TX2N/LCDC_D5	LVDS_TX1N/LCDC_D3	LVDS_TX0N/LCDC_D1	LVDS_XRES	USB1_DP	USB0_DP	CIF_D1	CIF_D3	CIF_VSYNC	DRIVE_VBUS/GPIO3_C1/CIF_PDN0	PWM0/GPIO0_D2	FLASH_D0/EMMC_D0/GPIO1_D0	FLASH_D2/EMMC_D2/GPIO1_D2	FLASH_D5/EMMC_D5/GPIO1_D5	FLASH_CLE/GPIO2_A1	FLASH_CS0/GPIO2_A6	FLASH_CS1/GPIO0_C7	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Fig. 10 RK3028A TFBGA313 Ball Map

chapter 4 Electrical Specification

4.1 Absolute Maximum Ratings

Table 7 RK3026/RK3028A absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for CPU and Core	AVDD,CVDD	1.4	V
DC supply voltage for Internal digital logic	USB_DVDD11,HDMI_DVDD11,LVDS_DVDD11	1.21	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	VCCIO	3.63	V
DC supply voltage for DDR IO	VCC_DDR	1.95	V
DC supply voltage for Analog part of SAR-ADC and PLL	SAR_AVDD33,PLL_VCCIO	3.63	V
DC supply voltage for Analog part of PLL	APLL_DVDD11,DPLL_DVDD11,C/GPLL_DVDD11	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD33	3.63	V
DC supply voltage for Analog part of Audio codec	CODEC_AVDD	3.63	V
DC supply voltage for Analog part of LVDS	LVDS_VCC	3.63	V
Analog Input voltage for SAR-ADC		3.63	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5.25	V
Digital input voltage for input buffer of GPIO		3.63	V
Digital output voltage for output buffer of GPIO		3.63	V
Storage Temperature		150	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

4.2 Recommended Operating Conditions

Table 8 RK3026/RK3028A recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
CPU and Core Power	AVDD,CVDD	0.9	1.1	1.35	V

Internal digital logic Power	USB_DVDD11,HDMI_DVDD11,LVDS_DVDD11	0.9	1.1	1.21	V
Digital GPIO Power	VDDIO	2.97	3.3	3.63	V
DDR IO (DDR3 mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (LVDDR3 mode) Power	DDR_VDD	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	APLL_DVDD12,DPLL_DVDD12, C/GPLL_DVDD12	0.99	1.1	1.21	V
SAR-ADC Analog Power	SAR_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 external resistor	EXTR	122	135	147	Ohm
Acodec Analog Power	CODEC_AVDD33	2.97	3.3	3.63	V
HDMI Analog Power	HDMI_AVDD33	2.97	3.3	3.63	V
EFUSE programming voltage		2.25	2.5	2.75	V
PLL input clock frequency			24		MHz
Operating Temperature		-40	25	85	°C

4.3 DC Characteristics

Table 9 RK3026/RK3028A DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol		0	0.4	V
	Output High Voltage	Voh	2.4	3.3		V
	Threshold Point	Vt	1.21	1.42	1.64	V
	Schmitt trig Low to High threshold point	Vt+	1.36	1.6	1.86	V
	Schmitt trig High to Low threshold point	Vt-	0.93	1.09	1.3	V
	Pullup Resistor	Rpu	33	41	62	Kohm
	Pulldown Resistor	Rpd	33	42	68	Kohm
DDR IO (Data)	DC Input High Voltage	Vih(DC)	VREF + 0.1		VDDQ+ 0.4	V
	AC Input High Voltage	Vih(AC)	VREF + 0.15		VDDQ+ 0.4	V
	DC Input Low Voltage	Vil(DC)	-0.4		VREF - 0.1	V
	AC Input Low Voltage	Vil(AC)	-0.4		VREF + 0.15	V
	Differential input logic high	Vihdiff	+0.2		VDDQ + 0.4	V

	Differential input logic low	Vildiff	-0.4		-0.2	V
	Output High Voltage	Voh	0.9 * VDDQ	VDDQ		V
	Output Low Voltage	Vol		0	0.1 * VDDQ	V
DDR IO (Address and command)	Output High Voltage	Voh	0.9 * VDDQ		VDDQ+0.4	V
	Output Low Voltage	Vol	-0.4	0	0.1 * VDDQ	V
DDR IO (Clock)	DC output voltage	Von	-0.4		VDDQ+0.4	V
	DC output Differentialvoltage	Vod(DC)	0.4 * VDDQ		VDDQ+0.6	V
	AC output Differentialvoltage	Vod(AC)	0.6 * VDDQ		VDDQ+0.6	V
	AC differential crossing voltage	Vox	0.4 * VDDQ		0.6 * VDDQ	V
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V
SAR-ADC	Input Range	2-channel single-ended input	0.01* SAR_AVDD33		0.99* SAR_AVDD33	V
	Input Voltage High (Logic “1”)	Vih	0.7* SAR_AVDD33	SAR_AVDD33		V
	Input Voltage Low (Logic “0”)	Vil		0	0.3* SAR_AVDD33	V
	Output Voltage High (Logic “1”)	Voh	0.7* SAR_AVDD33			V
	Output Voltage Low (Logic “0”)	Vol			0.3* SAR_AVDD33	V
USB	Input Voltage High	Vih		1.1		V
	Input Voltage Low	Vil		0		V
HDMI	single-ended high level output voltage, VH(when sink <=165Mhz)	Voh	HDMI_AVDD33-10mv		HDMI_AVDD33+10mv	mV

	single-ended high level output voltage, VH(when sink > 165Mhz)	Voh	HDMI_AVDD33-200mv		HDMI_AVDD33+10mv	mV
	single-ended low level output voltage, VL (when sink <= 165Mhz)	Vol	HDMI_AVDD33 -600mv		HDMI_AVDD33-400mv	mV
	single-ended low level output voltage, VL (when sink > 165Mhz)	Vol	HDMI_AVDD33-700mv		HDMI_AVDD33-400mv	mv
	single-ended output swing voltage, Vswing	Vswing	400		600	mV
	single-ended standby (off) output voltage,	Voff	HDMI_AVDD33 -10mv		HDMI_AVDD33+10mv	mv
	single-ended standby (off) output current	Ioff	-10		10	uA

4.4 Recommended Operating Frequency

Table 10 Recommended operating frequency for PLL and oscillator domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.1V , 25°C	XIN24M		24		MHz
	1.21V , -40 °C			24		
	0.99V , 125 °C			24		
DDR PLL	1.1V , 25 °C	ddr_pll_clk			1390	MHz
	1.21V , -40 °C				1690	
	0.99V , 125 °C				800	
ARM PLL	1.1V , 25 °C	arm_pll_clk			1530	MHz
	1.21V , -40 °C				1960	
	0.99V , 125 °C				800	
CODEC PLL	1.1V , 25 °C	cocec_pll_clk			1030	MHz
	1.21V , -40 °C				1380	
	0.99V , 125 °C				600	
GENERAL PLL	1.1V , 25 °C	general_pll_clk			1010	MHz
	1.21V , -40 °C				1350	
	0.99V , 125 °C				600	

Table 11 Recommended operating frequency for PD_CPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
CPU AXI interconnect	1.1V , 25 °C	CPU_ACLK			520	MHz
	1.21V , -40 °C				710	
	0.99V , 125 °C				300	

	1.1V , 25 °C	CPU_HCLK			190	MHz
	1.21V , -40 °C				350	
	0.99V , 125 °C				150	
	1.1V , 25 °C	CPU_PCLK			170	MHz
	1.21V , -40 °C				250	
	0.99V , 125 °C				75	
DMC	1.1V , 25 °C	DDR_PHY1X_CLK			760	MHz
	1.21V , -40 °C				1000	
	0.99V , 125 °C				400	

Table 12 Recommended operating frequency for PD_PERI domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
PERI AXI interconnect	1.1V , 25 °C	PERI_ACLK			498	MHz
	1.21V , -40 °C				700	
	0.99V , 125 °C				300	
	1.1V , 25 °C	PERI_HCLK			259	MHz
	1.21V , -40 °C				330	
	0.99V , 125 °C				150	
	1.1V , 25 °C	PERI_PCLK			140	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				75	
NAND	1.1V , 25 °C	FLASH_HCLK			250	MHz
	1.21V , -40 °C				340	
	0.99V , 125 °C				150	
USB OTG	1.1V , 25 °C	UTMI_CLK_0/ UTMI_CLK_1			30	MHz
	1.21V , -40 °C				30	
	0.99V , 125 °C				30	
UART0/1/2	1.1V , 25 °C	UART0_CLK/ UART1_CLK/ UART2_CLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
SDMMC/SDIO	1.1V , 25 °C	MMC0_CLK/ SDIO_CLK			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	
EMMC	1.1V , 25 °C	EMMC_CLK			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	
GPS	1.1V , 25 °C	GPS_RFCLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
	1.1V , 25 °C	GPS_HCLK			300	MHz
	1.21V , -40 °C				300	
	0.99V , 125 °C				300	
I2S	1.1V , 25 °C	I2S_CLK			50	MHz

	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
SPI0	1.1V , 25 °C	SPI0_CLK			50	MHz
	1.21V , -40 °C				50	
	0.99V , 125 °C				50	
SAR-ADC	1.1V , 25 °C	SARADC_CLK			12	MHz
	1.21V , -40 °C				12	
	0.99V , 125 °C				12	
Timer0/1	1.1V , 25 °C	TIMER0_CLK/ TIMER1_CLK			24	MHz
	1.21V , -40 °C				24	
	0.99V , 125 °C				24	
	1.1V , 25 °C	TIMER0_PCLK/ TIMER1_PCLK			140	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				75	

Table 13 Recommended operating frequency for PD_VIO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
Display AXI interconnection	1.1V , 25 °C	DISP_ACLK			530	MHz
	1.21V , -40 °C				720	
	0.99V , 125 °C				300	
	1.1V , 25 °C	DISP_HCLK			370	MHz
	1.21V , -40 °C				500	
	0.99V , 125 °C				200	
LCDC	1.1V , 25 °C	LCDC_DCLK			179	MHz
	1.21V , -40 °C				190	
	0.99V , 125 °C				160	
	1.1V , 25 °C	LCDC1_DCLK			230	MHz
	1.21V , -40 °C				290	
	0.99V , 125 °C				160	
CIF	1.1V , 25 °C	IO_CIF_CLKIN			100	MHz
	1.21V , -40 °C				100	
	0.99V , 125 °C				100	

Table 14 Recommended operating frequency for PD_GPU domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
GPU	1.1V , 25 °C	GPU_ACLK			510	MHz
	1.21V , -40 °C				691	
	0.99V , 125 °C				300	

Table 15 Recommended operating frequency for PD_VIDEO domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
VIDEO	1.1V , 25 °C	VEPU_ACLK			520	MHz
	1.21V , -40 °C				690	
	0.99V , 125 °C				300	
	1.1V , 25 °C	hclk_vepu			320	MHz

	1.21V , -40 °C				400	
	0.99V , 125 °C				150	
	1.1V , 25 °C	VDPU_ACLK			520	MHz
	1.21V , -40 °C				690	
	0.99V , 125 °C				300	
	1.1V , 25 °C	hclk_vdpu			320	MHz
	1.21V , -40 °C				490	
	0.99V , 125 °C				150	

4.5 Electrical Characteristics for General IO

Table 16 RK3026/RK3028A Electrical Characteristics for Digital General IO

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input leakage current	II	Vin = 3.3V or 0V	-10		10	uA
Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-10		10	uA

4.6 Electrical Characteristics for PLL

Table 17 RK3026/RK3028A Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Fractional accuracy				24		bits
Input clock frequency	Fin	Normal mode	1		800	MHz
		Fractional mode	10		800	MHz
Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.1V	12		2400	MHz
VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.1V	600		2400	MHz
Lock time②	Tlt	FREF=24M,REFDIV=1 @ 3.3V/1.1V,		41.7	66.7	us
AVDD Current consumption ③		Fvco = 1GHz, @3.3V, 27°C		1	1.2	mA
DVDD Power consumption (normal mode)		@3.3V/1.1V, 27°C		1.3	1.56	uA/MHz
AVDD Power Down Leakage		@3.3V/1.1V, 27°C		10		nA
DVDD Power Down Leakage		@3.3V/1.1V, 27°C		10		uA
Output Duty Cycle		Even divides @ FOUT=1GHz(falling edge error is ±20ps)	48	50	52	%
		Odd divides @ FOUT=1GHz(falling edge error is ±30ps)	47	50	53	%

		FOUTvco at any frequency	45	50	55	%

Notes :

①:REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value
②Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.
③Current scale as $(Fvco/1GHz)^{1.5}$

4.7 Electrical Characteristics for SAR-ADC

Table 18 RK3026/RK3028A Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution				10		bits
Conversion speed	Fs				1	MSPS
Differential Non Linearity	DNL				1	LSB
Integral Non Linearity	INL				1.5	LSB
Input Capacitance	CIN			1		pF
Sampling Clock	SOC				1	MHz
Main Clock Frequency	CLK				11	MHz
Data Latency				10		Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=1.03K Fin=499K		59.56 57.03		dB
Spurious-Free Dynamic Range	SFDR	Fin=1.03K Fin=499K		78.59 65.75		dB
Second-Harmonic Distortion	2HD	Fin=1.03K Fin=499K		-93.32 -70.76		dB
Third-Harmonic Distortion	3HD	Fin=1.03K Fin=499K		-88.16 -65.75		dB
Effective Number of Bits	ENOB	Fin=1.03K Fin=499K		9.55 9.18		Bits
Analog Supply Current(SARADC_AVDD)				580		uA
Digital Supply Current				30		uA

Power Down Current				0.5		uA

4.8 Electrical Characteristics for USB

Table 19 RK3026/RK3028A Electrical Characteristics for USB 2.0

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output resistance	Rout	Classic mode HS mode	40.5	45	49.5	ohm
Output Capacitance	Cout				3	pF
Differential output signal high	Voh	Classic(LS/FS),Io=0mA	2.97	3.3	3.63	V
		Classic(LS/FS),Io=6mA	2.2	2.7		V
		HS mode,Io=0mA	360	400	440	mV
Differential output signal low	Vol	Classic(LS/FS),Io=0mA	-0.33	0	0.33	V
		Classic(LS/FS),Io=6mA		0.3	0.8	V
		HS mode,Io=0mA	-40	400	40	mV
Output Common Mode Voltage	VM	Classic(LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Rise and fall time	Tr/Tf	LS mode	75	87.5	300	ns
		FS mode	4	12	20	ns
		HS mode	0.8	1.0	1.2	ns
Propagation delay(data to D+/D-)		LS mode	30		300	ns
		FS mode	0		12	ns
		HS mode		TBD		ns
Propagation delay(tx_en to D+/D-)	Tpzh/Tpzl	Classic(LS/FS) mode			2	ns
		HS mode			2	ns
Receiver sensitivity	Rsens	Classic(LS/FS) mode		±250		mV
		HS mode		±250		mV
Receiver common mode	RCM	Classic(LS/FS) mode	0.8	1.65	2.5	V
		HS mode(differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode(disconnect comparator)	0.5	0.6	0.7	V
Input capacitance	Cin	Seen at D+ or D-			3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	Voh			1.1		V
Low output level	Vol			0		V
Pulldown Resistor on DP/DM	Rpu		14.5	15	16	Kohm
Pullup Resistor on	Rpd		2.35	2.4	2.5	Koh

DP/DM						m
UID Pullup resistor			160	200	240	Kohm

4.9 Electrical Characteristics for HDMI

Table 20 RK3026/RK3028A Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
DDC control signals High Voltage level			-3.0		3.8	V
DDC control signals low Voltage level			-0.5		1.5	V
DDC control signals SCL clock frequency					100	kHz
DDC control signals rise time					1000	ns
DDC control signals fall time					300	ns
DDC control signals capacitive load on bus line				400		pF
TMDS rise time/fall time(20%-80%)	Tfall/Trise		75		0.4Tbit	ps
TMDS overshoot, max			15% of full differential amplitude(Vswing*2)			ps
TMDS undershoot, max			25% of full differential amplitude(Vswing*2)			ps
TMDS intra-pair skew at transmitter connector, max				0.15 Tbit		ps
TMDS inter-pair skew at transmitter connector, max				0.2 Tpixel		ps
TMDS Differential clock jitter, max				0.25 Tbit		ps
TMDS clock duty cycle			40%		60%	

4.10 Electrical Characteristics for DDR

Table 21 RK3026/RK3028A Electrical Characteristics for DDR

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input leakage current Any input 0V≤VIN≤VDD (All other balls not under test=0V)	Ii		-5		5	uA
Onput leakage current (DQ are disabled; 0V≤VOUT≤VDDQ)	Ioz		-5		5	uA

4.11 Electrical Characteristics for TTL output

Table 22 RK3026/RK3028A Electrical Characteristics for TTL output

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output low voltage	Vol	Iol=8mA			0.4	V
Output high voltage	Voh	Ioh=8mA	2.4			V
Low level output current	Iol	Vol=0.4V	6.6	11	15.6	mA
Output low voltage	Ioh	Voh=2.4V	8.98	19.9	34.5	mA

4.12 Electrical Characteristics for LVDS Transmitter

Table 23 RK3026/RK3028A Electrical Characteristics for LVDS Transmitter

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output voltage low, Voa or Vob	Vol	Rload=100ohm±1%	925		N/A	mV
Output voltage high, Voa or Vob	Voh	Rload=100ohm±1%	N/A		1475	mV
Output differential voltage	|Vod|	Rload=100ohm± 1%,Rs=0V	250		450	mV
		Rload=100ohm± 1%,Rs=VDD	150		250	mV
Output offset voltage	Vos	Rload=100ohm±1%	1125		1375	mV
Change in |Vod| between '0' and '1'	|△Vod|	Rload=100ohm±1%			50/150	mV
change in Vos between '0' and '1'	△Vos	Rload=100ohm±1%			50	mV
Output current	Isa,Isb	Transmitter shorten to ground			24	mA
Output current	Isab	Transmitter shorten to ground			12	mA
Leakage current	Ileakage	Power down	-10			uA
Clock in/out frequency	Clk_freq		20		170	MHz
Clock out duty cycle	Clk_dco			57		%
Data(Dn_m) setup to CK_REF	Tts		2			ns
Data(Dn_m) hold to CK_REF	Tth		0.5			ns
Serial-Data Skew to Clkout edge	SDsdew		-200	0	200	ps

4.13 Electrical Characteristics for eFuse

Table 24 RK3026/RK3028A Electrical Characteristics for eFuse

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Burn voltage	VQPS		2.25	2.5	2.75	V
Programming voltage	Vpgm			VQPS		V
Read voltage	Vrd			VQPS		V
Active mode	Iactive	STROBE high		3		mA
standby mode	Istandby				230	nA
Peak program current	Iprog			14.4		mA

chapter 5 Hardware Guideline

5.1 Reference design for oscillator PCB connection

RK3026/RK3028A only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram , Rf is used to bias the inverter in the high gain region. The recommend value is 1Mohm.

Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Rd of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.

C1 and C2 are deciding regard to the crystal or resonator CL specification.

the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model .

In RK3028A, the crystal oscillator I/O cells have embedded internal resistor, so we need not add feedback resistor (Rf) as above description.

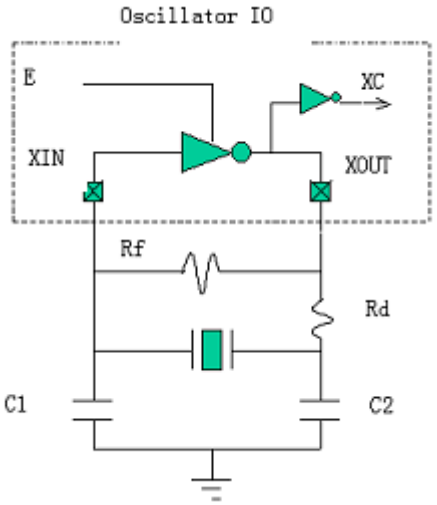


Fig. 11RK3026/RK3028A External Reference Circuit for 24MHzOscillators

5.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK3026/RK3028A.

For optimal jitter performance it is suggested to connect PLL_DVDD-VSS(PLL_VSS1) and PLL_VCCIO-VSS(PLL_VSS2) on the board. VDDREF is typically connected to the global chipsupply and does not require dedicated decoupling.

It is recommended to use at least one large capacitor (e.g. 4.7uF) capacitor for each separate supply.Additionally, a 100nF and 10nF capacitor may be placed in parallel since the lead inductance of the4.7uF capacitor may be large.

Capacitors with minimal lead inductance should be selected. Ceramic type capacitors work well.Thecapacitors should be placed as close to the package pins as possible. No series impedance shouldbe added anywhere on the board, and impedance to the voltage source should be minimized.

5.3 Reference design for USB OTG/Host2.0 connection

In RK3026/RK3028A there are USB OTG and USB Host2.0 interface, and they share a common PHY. As integrated high speed mixed signal circuits,the USB 2.0 PHY supports not only the High Speed (HS) traffic at 480Mbps,but also the Full Speed (FS) traffic at 12Mbps and the Low Speed (LS) traffic at 1.5Mbps,while remaining backward compatible with USB1.1 legacy protocol.

- Decouple Capacitance

We should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 1-9. Place these components as closely as possible to the power pins.

- Differential Lines

The differential lines should be routed together, minimizing the number of vias through which the signal lines are routed. Layout the differential pairs with controlled impedance of 100 ohm differential.

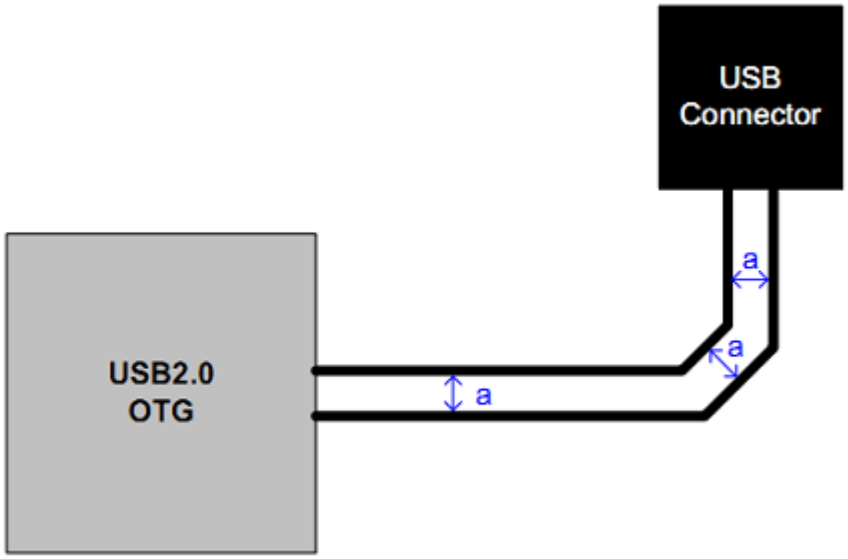


Fig. 12 RK3026/RK3028A USB OTG/Host2.0 differential lines requirement

If high-speed signals are routed on the Top layer, best results will be obtained if the

Layer 2 is a Ground plane. Furthermore, there must have only one ground plane under high-speed signals in order to avoid the high-speed signals to cross another ground plane.

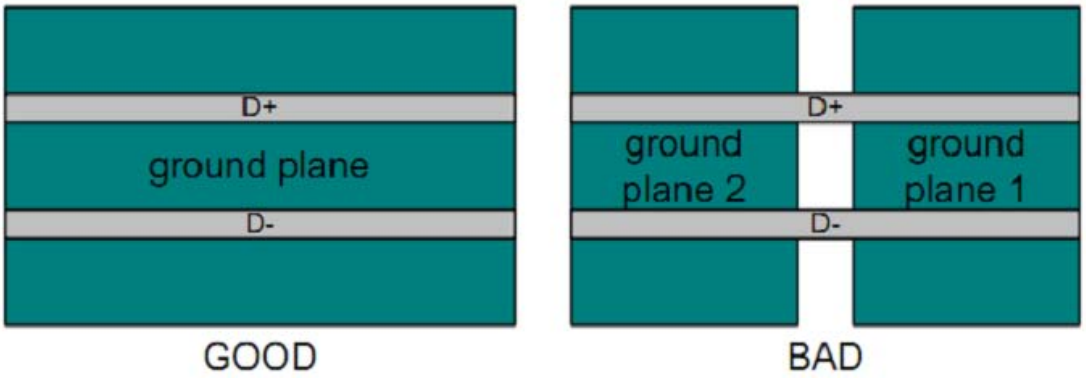


Fig. 13 RK3026/RK3028A USB OTG/Host2.0 ground plane guide

- Component Placement

It is very important to not create stubs on the high-speed lines, to avoid that, the placement of component should be the closed as possible from D+ and D- lines, like shown in the following figure.

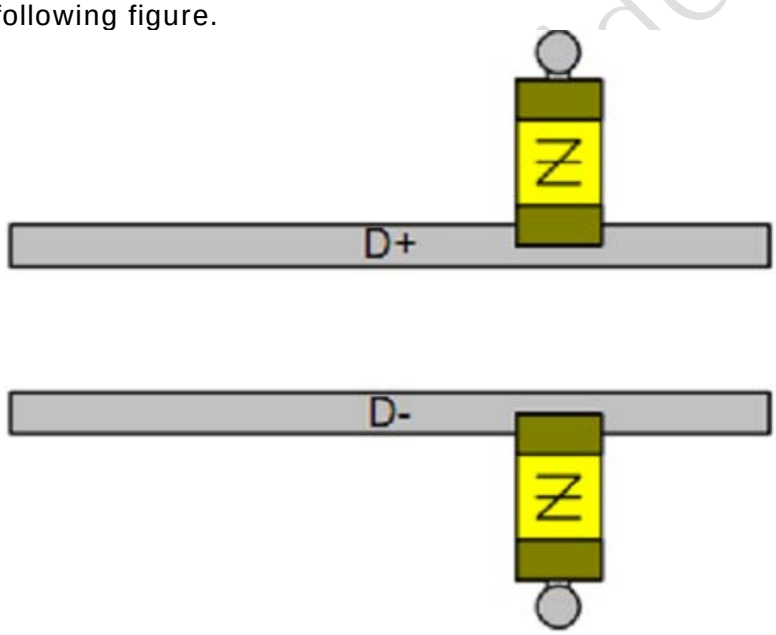


Fig. 14 RK3026/RK3028A USB OTG/Host2.0 component placement

5.4 Reference design for HDMI connection

In RK3028A, the following diagram shows external PCB reference design for HDMI Tx PHY.It mainly introduces how to connect the TMDS channel, DDC channel, CEC channel and HPD signal of RK3028A HDMI Transmitter to the HDMI port type A.

- TMDS channel

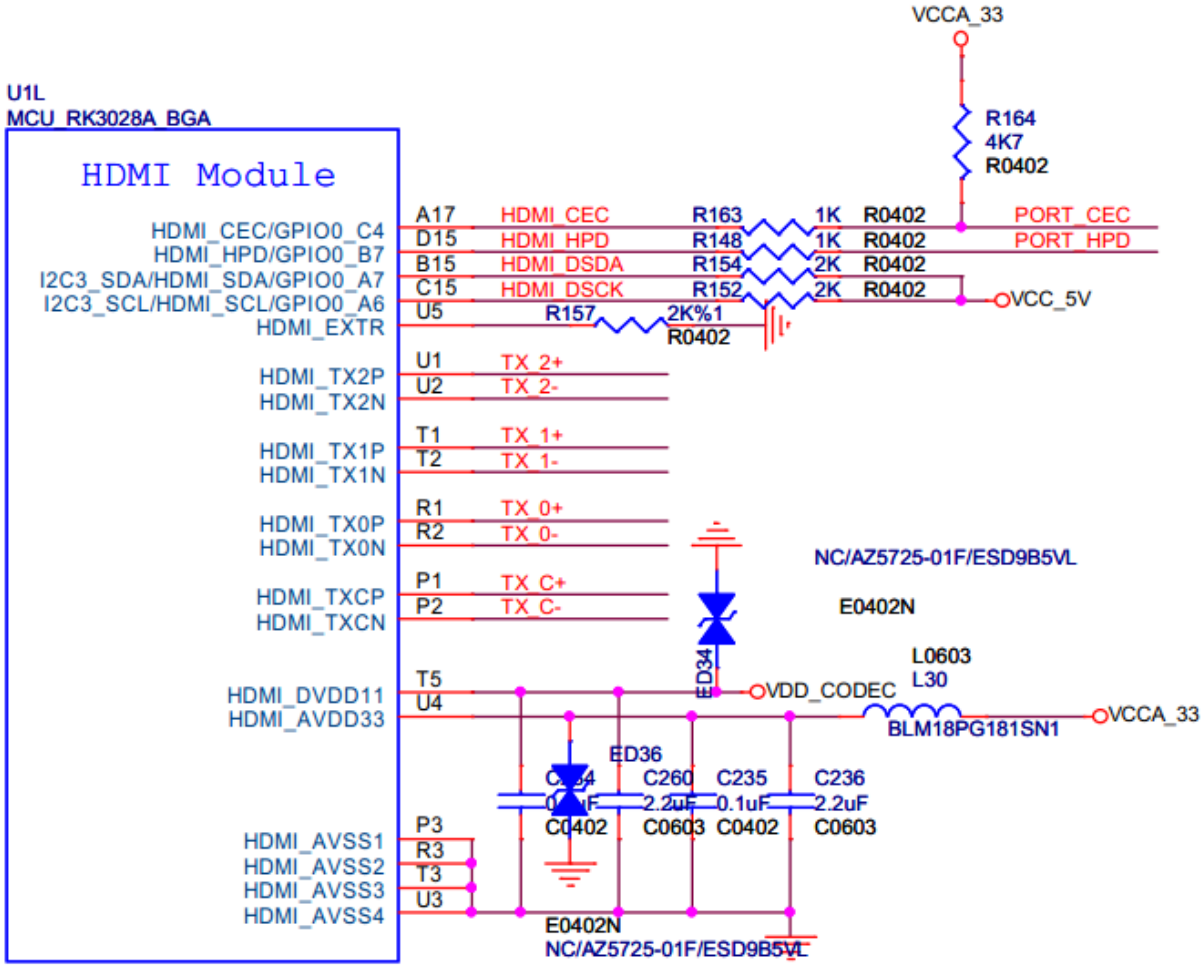


Fig. 15RK3028A HDMI interface reference connection

- DDC channel

  RK3028A can accept DDC_sda/DDC_scl 5V voltage input, it's no need to add additional transmitter to transfer the DDC_sda/DDC_scl from 5V to 3.3V outside the chip.

- CEC channel

  RK3028A can accept CEC 5V voltage input, it's no need to add additional Transmitter to transfer the CEC from 5V to 3.3V outside the chip.

- HPD

  RK3028A can accept HPD 5V voltage input, it's no need to add additional Transmitter to transfer the HPD from 5V to 3.3V outside the chip.

- ESD

  If ESD suppression devices or common mode chokes are used, place them near the HDMI connector.

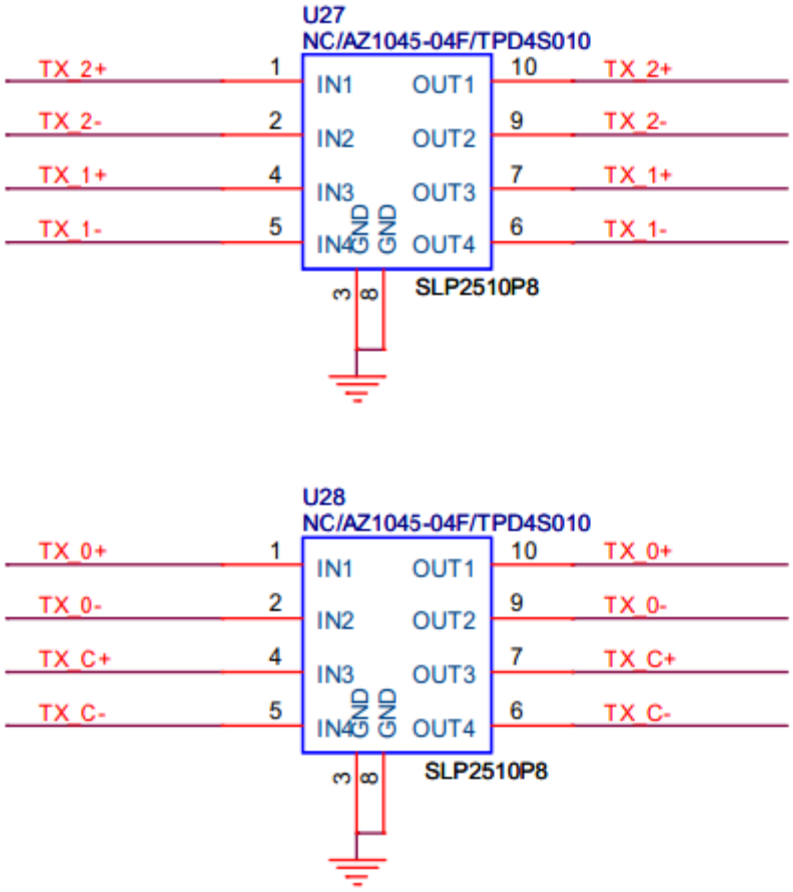


Fig. 16RK3028A HDMI ESD interface reference connection

5.5 Reference design for Audio Codec connection

In RK3026/RK3028A, the following diagram shows external PCB reference design for Audio Codec(virtual ground).

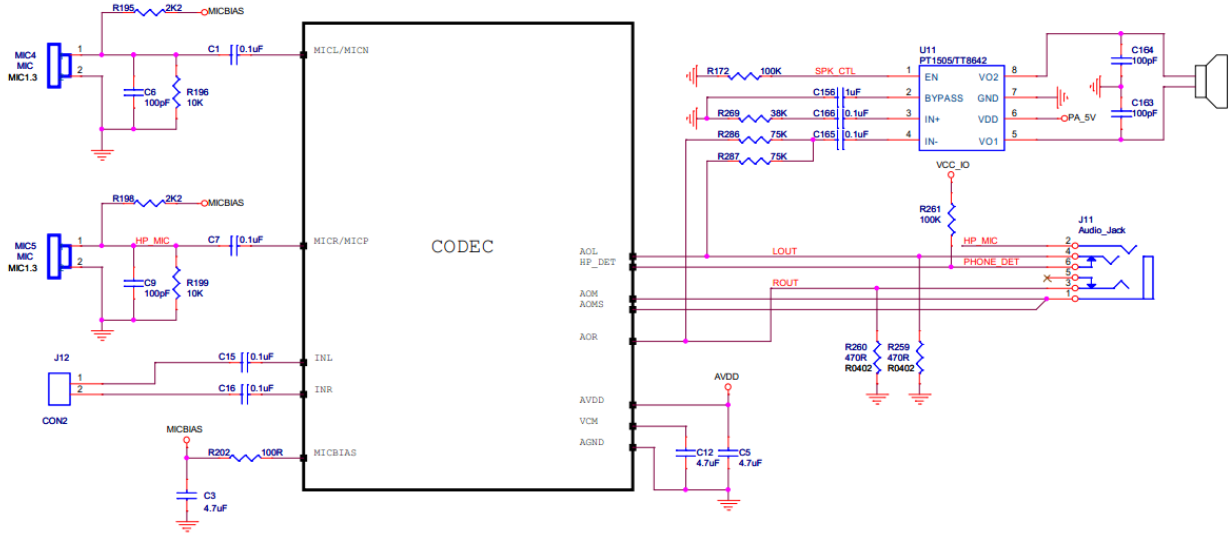


Fig. 17RK3026/RK3028A Audio Codec interface reference connection

As above diagram shows, the MICL and MICR are each connected with a MIC

through a 0.1uf CAP, the INL and INR have the same function as the MICL and MICR. The R202 and C3 are formed a filter for the MIC. The MIC_BIAS is used for bias the MIC through a resistor. The resistor value should be changed according the MIC type. The AVDD should be supplied by 3.3V. The CAP connected with AVDD should be placed as close as possible

The VCM is connected with GND through a 4.7Uf CAP. The CAP should be placed as close as possible. The AOL and AOR could be connected with a speaker or an earphone.

5.6 Reference design for GPS connection

Please refer to the GPS_HV5820_设计指南_V1.1.pdf for detail PCB layout guideline.

5.7 RK3028A Power on reset descriptions

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstndeassert, andthe PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

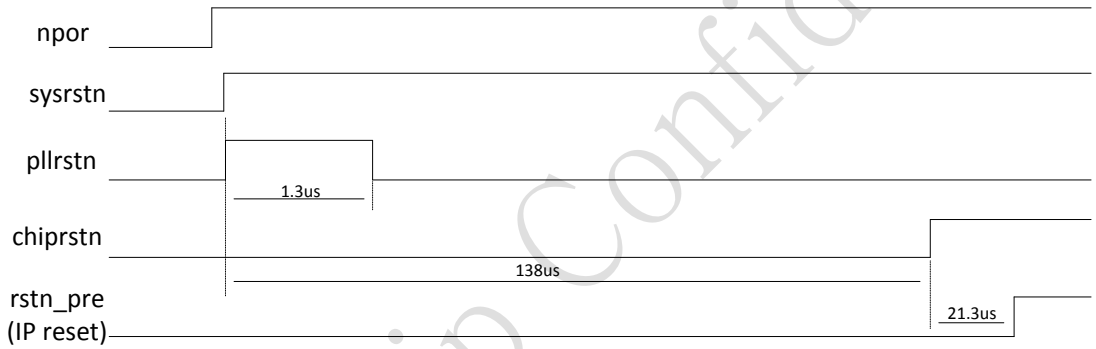


Fig. 18RK3026/RK3028A reset signals sequence