

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

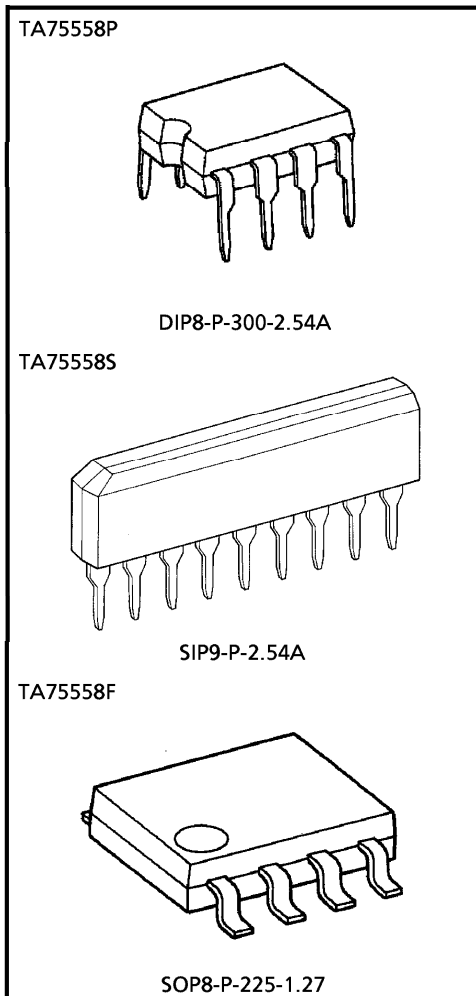
TA75558P, TA75558S, TA75558F

DUAL OPERATIONAL AMPLIFIER

The TA75558P, TA75558S and TA75558F are Low-Noise Operational Amplifiers with High Speed and Wide Bandwidth.

FEATURES

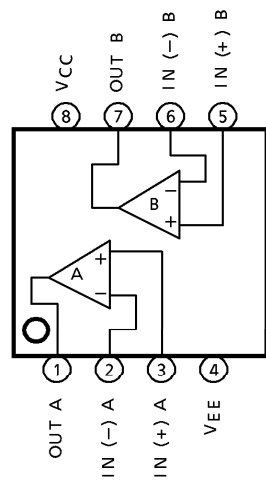
- Internal Frequency Compensation Type
- Pin Compatible with TA75458P, TA75458S and TA75458F
- Possible to Exchange the Position of 9 Pin for 1 Pin Because of Pin Connection Being Symmetric.
(TA75558S Device Only)
- Wide Band Range : $f_T = 3\text{MHz}$ (Typ.)
- Suitable Application for Active Filter Equalizer Amplifier and Headphone Amplifier.



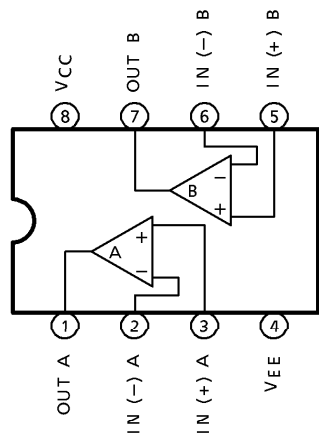
Weight
DIP8-P-300-2.54A : 0.5g (Typ.)
SIP9-P-2.54A : 0.9g (Typ.)
SOP8-P-225-1.27 : 0.1g (Typ.)

PIN CONNECTION (TOP VIEW)

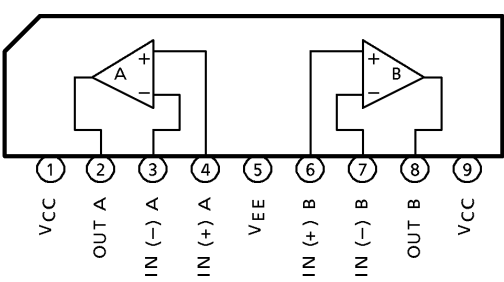
TA75558F



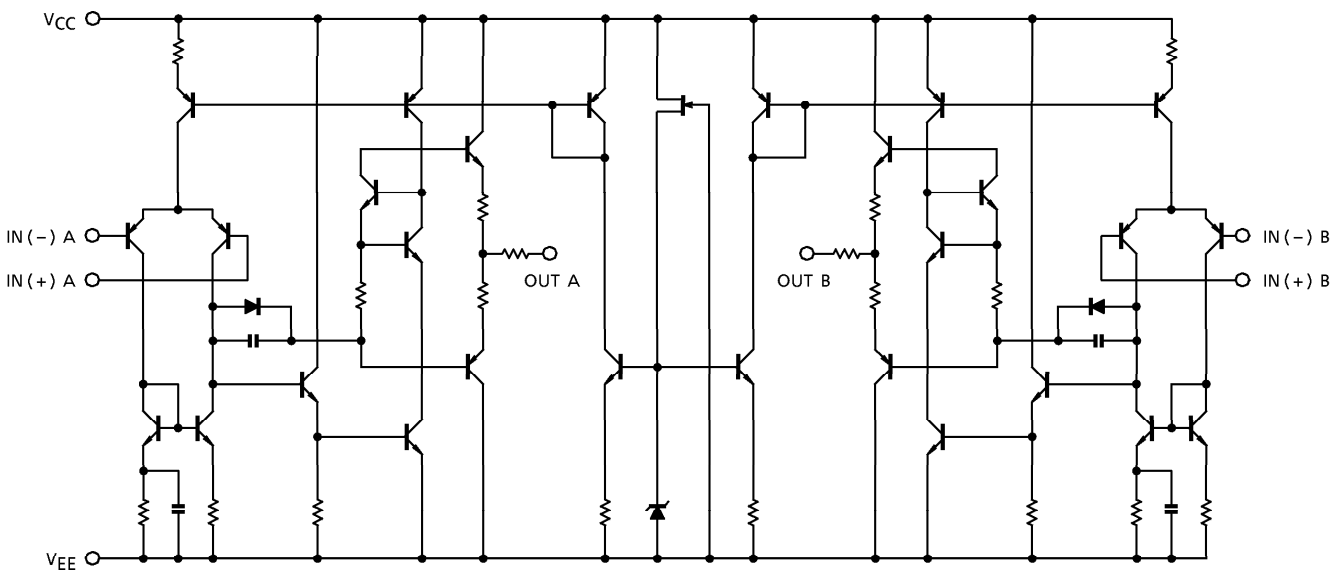
TA75558P



TA75558S



EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Ta = 25°C)

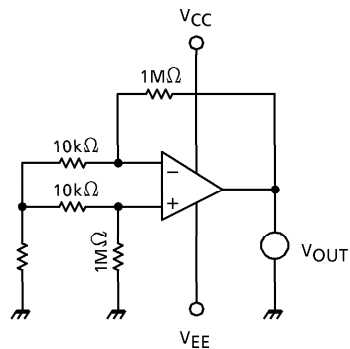
CHARACTERISTIC	SYMBOL	TA75558P TA75558S	TA75558F	UNIT
Supply Voltage	V _{CC}	+ 18	+ 18	V
	V _{EE}	– 18	– 18	
Differential Input Voltage	DV _{IN}	± 30	± 30	V
Input Voltage	V _{IN}	V _{CC} ~V _{EE}	V _{CC} ~V _{EE}	V
Power Dissipation	P _D	500	240	mW
Operating Temperature	T _{opr}	– 40~85	– 30~70	°C
Storage Temperature	T _{stg}	– 55~125	– 55~125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, V_{EE} = – 15V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V _{IO}	1	R _g ≤ 10kΩ	—	0.5	6	mV
Input Offset Current	I _{IO}	2	—	—	5	200	nA
Input Bias Current	I _I	2	—	—	60	500	nA
Common Mode Input Voltage	CMV _{IN}	3	—	± 12	± 14	—	V
Maximum Output Voltage	V _{OM}	6	R _L = 10kΩ	± 12	± 14	—	V
	V _{OMR}		R _L = 2kΩ	± 10	± 13	—	
Source Current	I _{source}	8	—	—	40	—	mA
Sink Current	I _{sink}	7	—	—	40	—	mA
Voltage Gain (Open Loop)	G _V	5	V _{OUT} = ± 10V, R _L = 2kΩ	86	100	—	dB
Common Mode Input Signal Rejection Ratio	CMRR	3	R _g ≤ 10kΩ	70	90	—	dB
Supply Voltage Rejection Ratio	SVRR	1	R _g ≤ 10kΩ	—	30	150	μV/V
Slew Rate	SR	9	G _V = 1, R _L = 2kΩ	—	1.0	—	V/μs
Unity Gain Cross Frequency	f _T	5	Open Loop	—	3.0	—	MHz
Supply Current	I _{CC} , I _{EE}	4	—	—	4.0	6.0	mA
Equivalent Input Noise Voltage	V _{NI}	—	R _S = 1kΩ, f = 30Hz~30kHz	—	2.5	—	μV _{rms}

TEST CIRCUIT

(1) V_{IO} , $SVRR$



- $V_{IO} = V_{OUT} / 100$
- $SVRR = 20 \log E \text{ (dB)}$

$$E = \left| \frac{V_{OUT1} - V_{OUT2}}{(V_{CC1} - V_{EE1}) - (V_{CC2} - V_{EE2})} \right| \times \frac{1}{100}$$

V_{OUT1} : V_{OUT} (V_{CC} , $V_{EE} = \pm 8V$)

V_{OUT2} : V_{OUT} (V_{CC} , $V_{EE} = \pm 18V$)

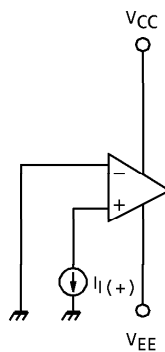
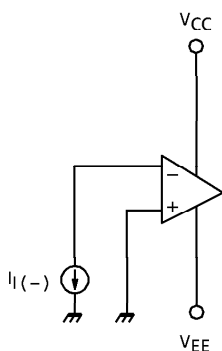
V_{CC1} : $V_{CC} = -8V$

V_{EE1} : $V_{EE} = -8V$

V_{CC2} : $V_{CC} = +18V$

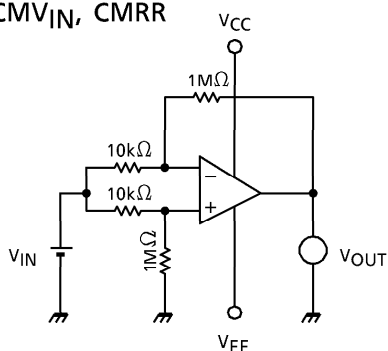
V_{EE2} : $V_{EE} = -18V$

(2) I_I , I_{IO}



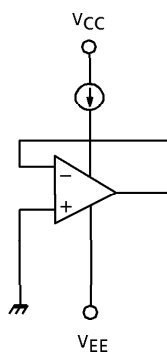
$$I_{IO} = |I_I(-) - I_I(+)|$$

(3) CMV_{IN} , $CMRR$



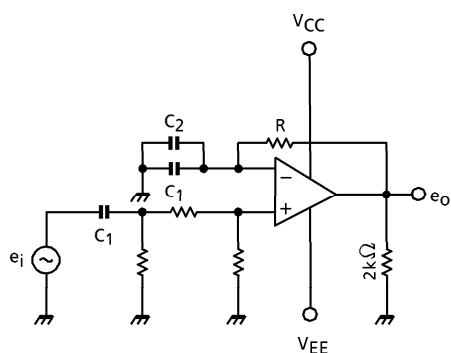
- $CMRR = 20 \log G_D / G_C \text{ (dB)}$
 G_D : DIFFERENTIAL VOLTAGE GAIN
 G_C : COMMON MODE VOLTAGE GAIN
- CMV_{IN} : $V_{IN} = -12V, 12V \text{ SUPPLIES}$

(4) I_{CC}



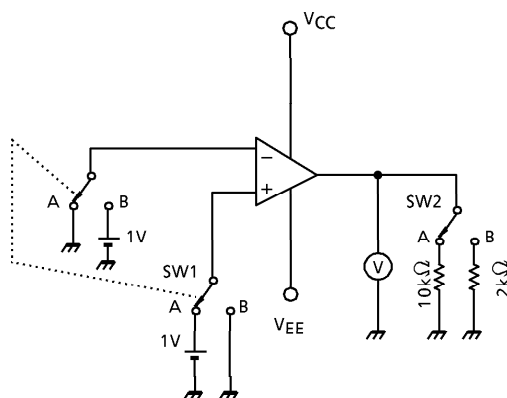
- I_{CC} : V_{CC} , $V_{EE} = \pm 15V$

(5) G_V , f_T



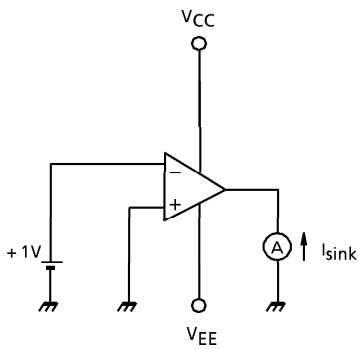
- $G_V = 20 \log e_o / e_i$ (dB)
 $R \gg 1 / W_{C1}$
 C_1 : COUPLING CONDENSER
 C_2 : HIGH FREQUENCY BYPASS CONDENSER
- f_T : INPUT FREQUENCY AT $e_i = e_o$

(6) V_{OM} , V_{OMR}

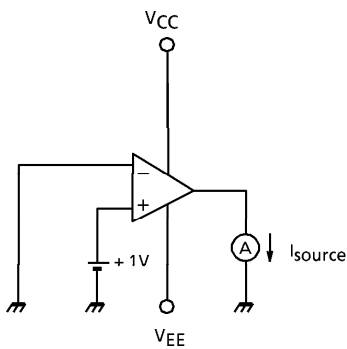


- V_{OM} : (+) : SW1 IS SIDE A, SW2 IS SIDE A
 (-) : SW1 IS SIDE B, SW2 IS SIDE A
- V_{OMR} : (+) : SW1 IS SIDE A, SW2 IS SIDE B
 (-) : SW1 IS SIDE B, SW2 IS SIDE B

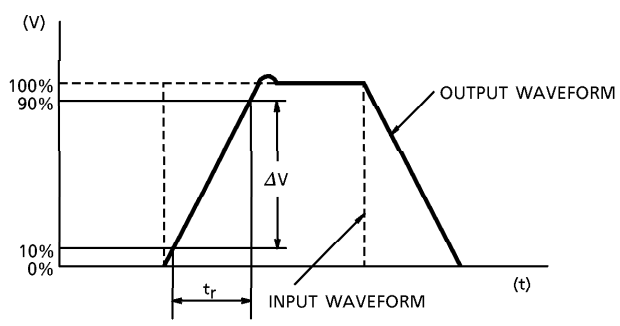
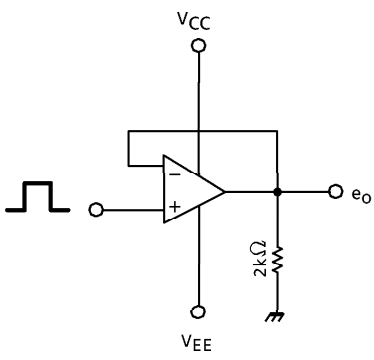
(7) I_{sink}



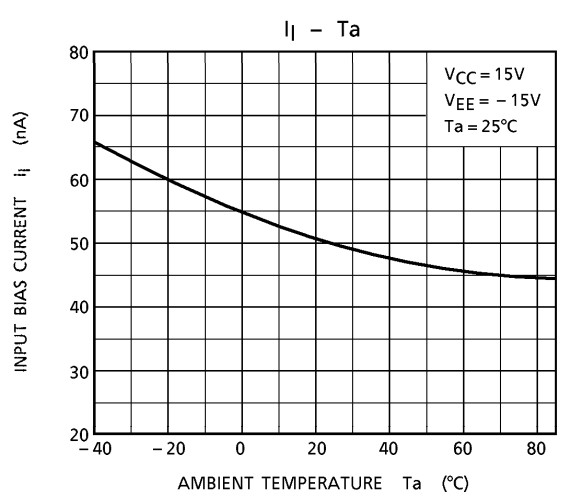
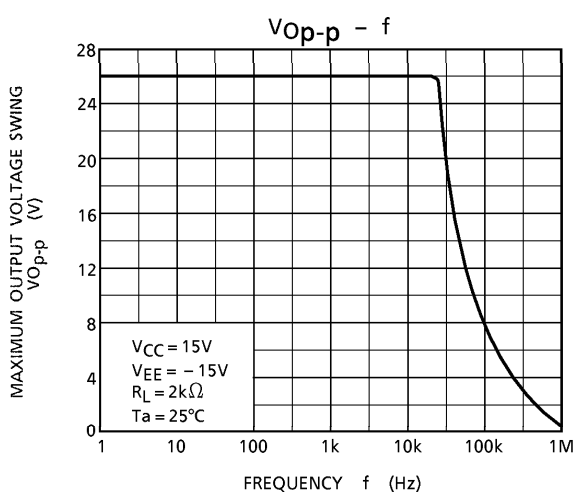
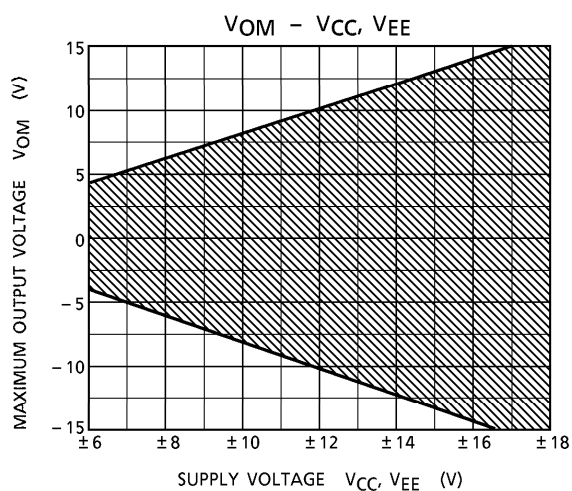
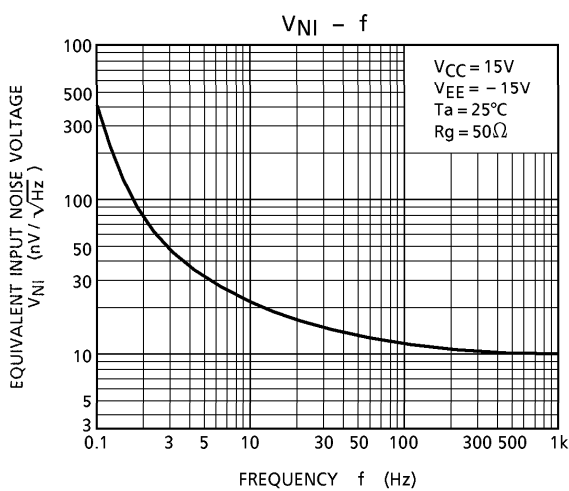
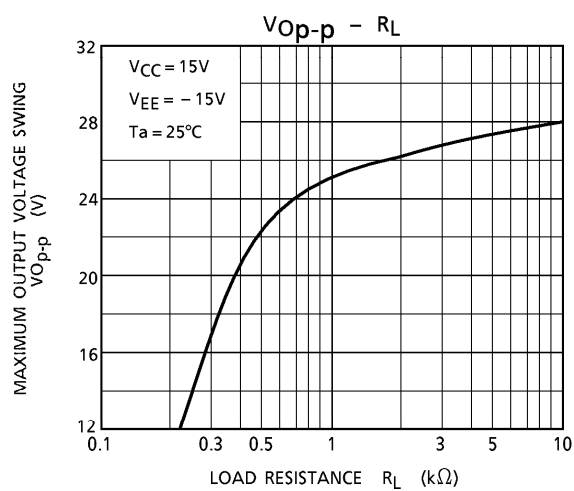
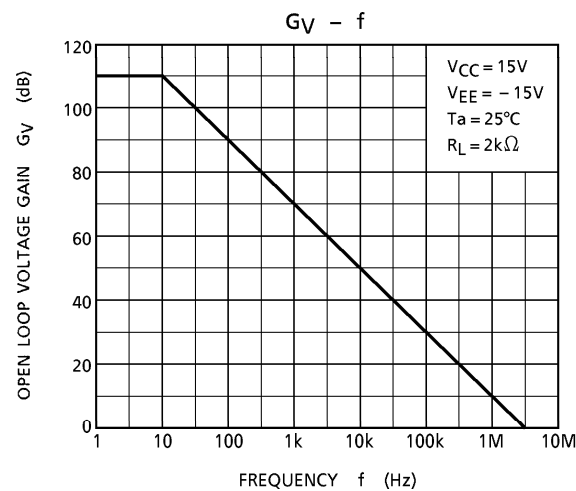
(8) I_{source}

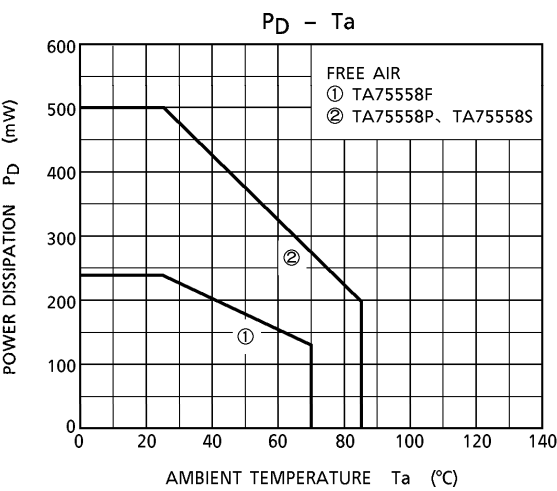


(9) SR



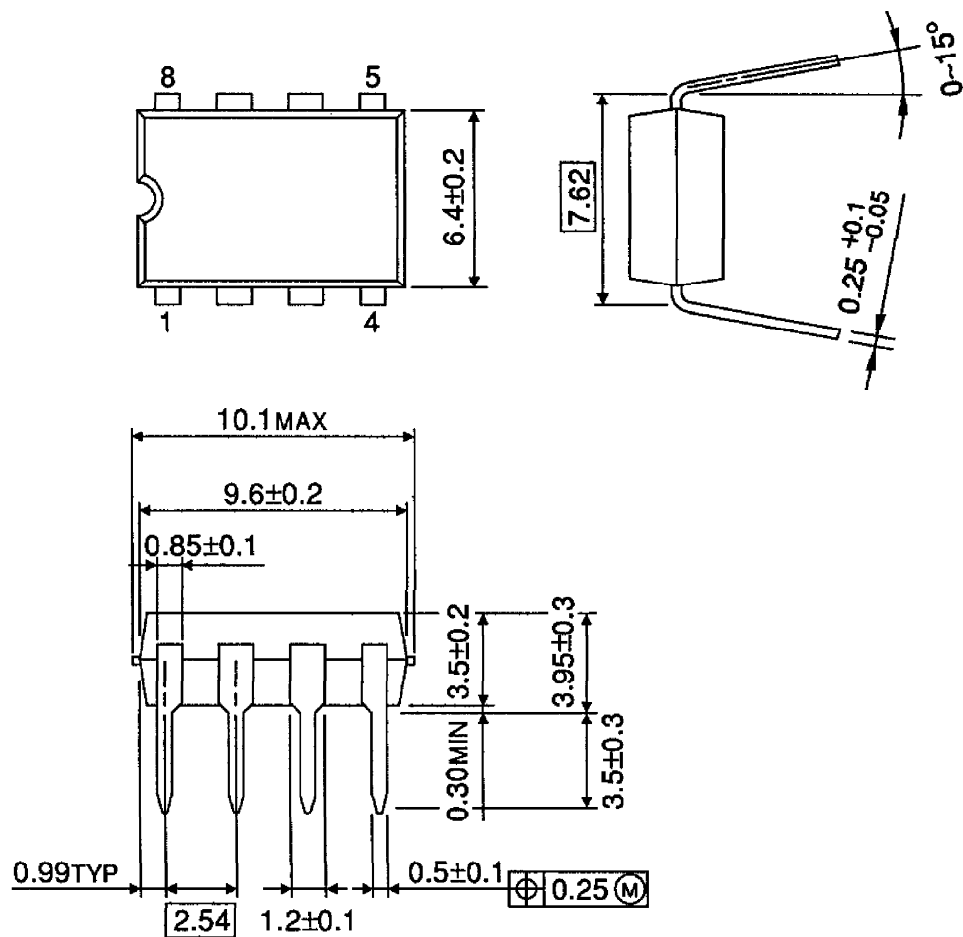
CHARACTERISTIC





PACKAGE DIMENSIONS
DIP8-P-300-2.54A

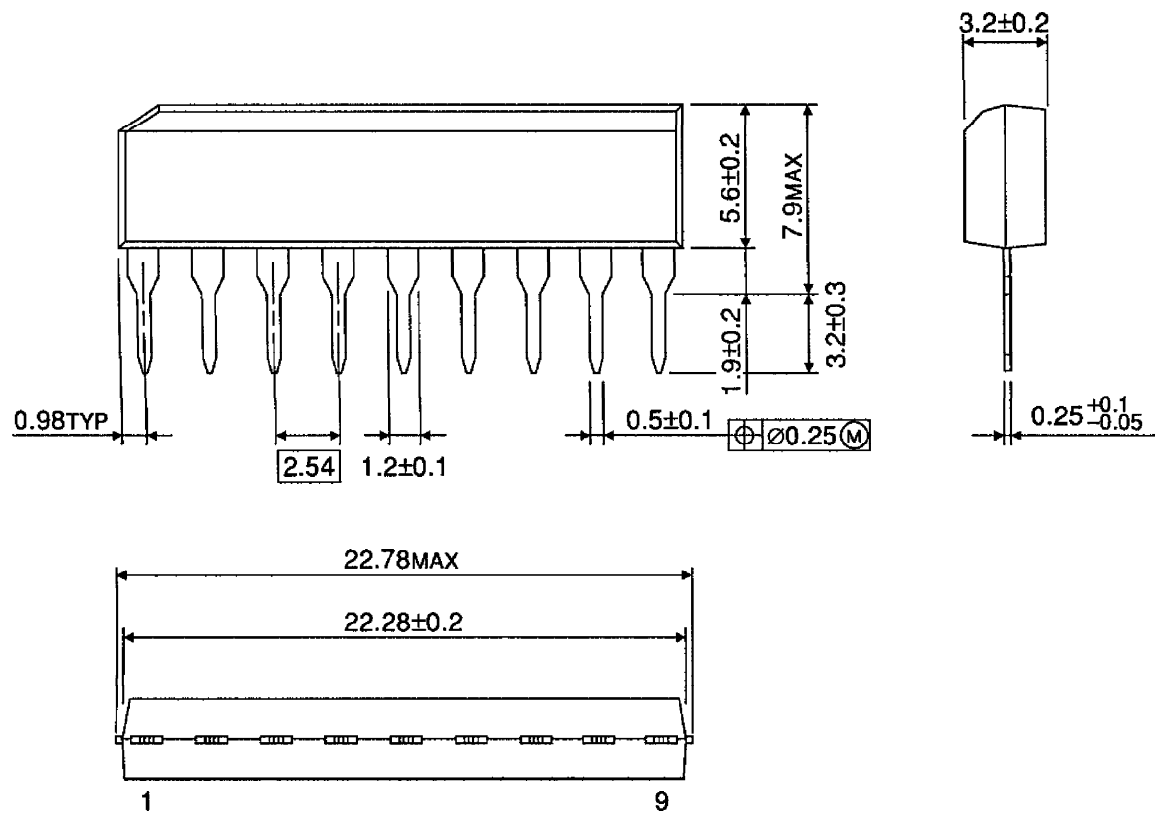
Unit : mm



Weight : 0.5g (Typ.)

PACKAGE DIMENSIONS
SIP9-P-2.54A

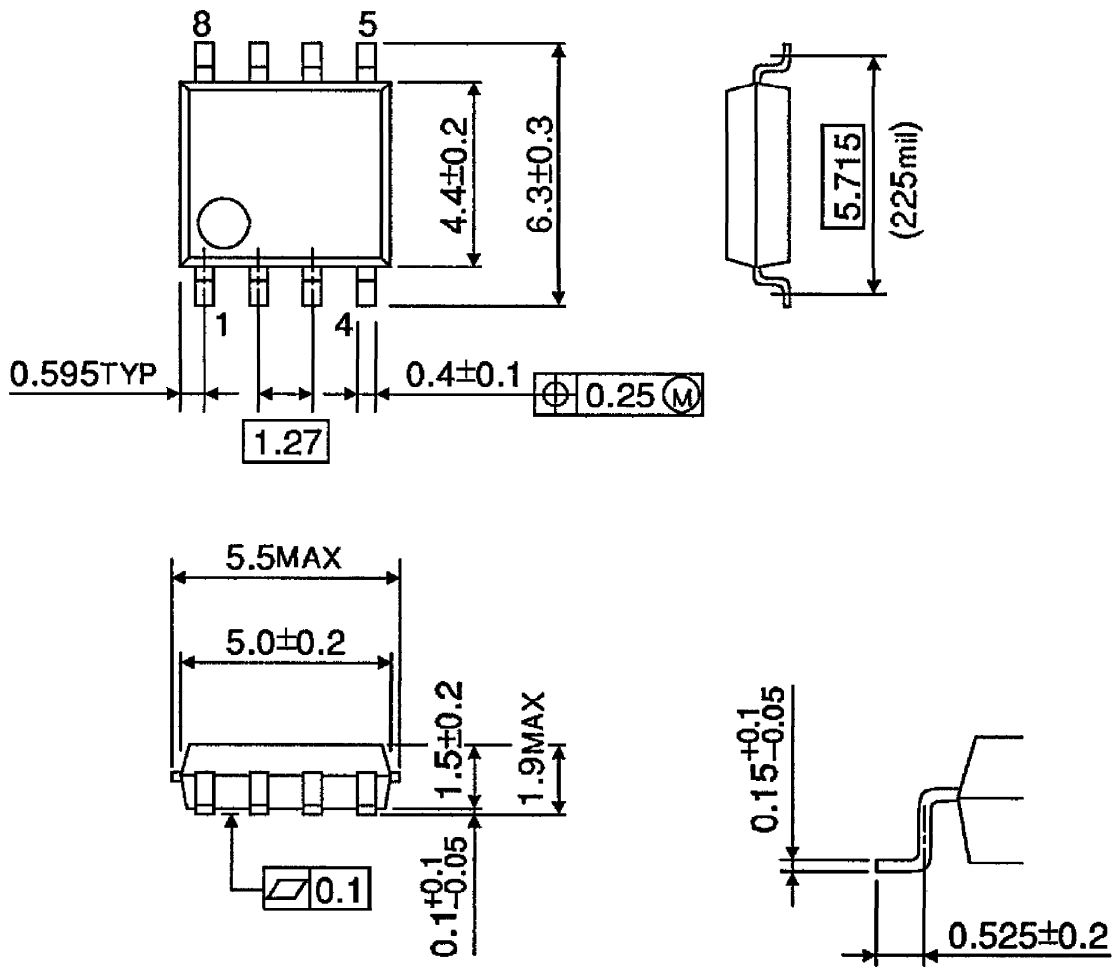
Unit : mm



Weight : 0.9g (Typ.)

PACKAGE DIMENSIONS
SOP8-P-225-1.27

Unit : mm



Weight : 0.1g (Typ.)

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000707EBA

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