EM78P156K

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.3

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Official Original Specification	2012/03/22
1.1	Corrected the package type	2012/04/12
1.2	1. Modified the numbers of I/O description in the Features section. 2. Modified the diagram of the data memory configuration 3. Added Ordering and Manufacturing Information 4. Modified the Instruction Table, not the Instruction Set 5. Added diagram of Frequency to Voltage Curve in Section 8.3 *Device Characteristics* 6. Modified the part number 7. Modified the description about POR and LVR in the Features section.	2012/05/11
1.3	Rectified the part numbers	2012/07/25

1 General Description

The EM78P156K is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 1024 ×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option words are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P156K provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development code.

2 Features

- CPU configuration
  - 1k × 13 bits on-chip ROM
  - 48 × 8 bits on-chip registers (SRAM, general purpose)
  - 5-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V / 4MHz
  - Typically 15 µA at 3V / 32kHz
  - Typically 1 µA during Sleep mode
- I/O port configuration
  - 2 bidirectional I/O ports : P5, P6
  - 12 I/O pins
  - Wake-up port : P6
  - 5 Programmable pull-down I/O pins (P50 ~ P52, P60 ~ P63)
  - 6 programmable pull-high I/O pins (P60 ~ P67)
  - 6 programmable open-drain I/O pins (P60 ~ P67)
  - 2 programmable R-option pins
  - External interrupt : P60
- Operating voltage range:
  - 2.1V ~ 5.5V at 0 ~ 70 (C (Commercial)
  - 2.3V ~ 5.5V at -40 ~ 85 (C (Industrial)
- Operating frequency range (base on 2 clocks):
  - Crystal mode:
    DC ~ 20MHz / 2clks @ 5V
    DC ~ 8MHz / 2clks @ 3V
    DC ~ 4MHz / 2clks @ 2.1V
  - ERC mode:
    DC ~ 2MHz / 2clks @ 2.1V
  - IRC mode:

Internal RC Freq.	Drift Rate			
	Temp. (-40~85°C)	Voltage	Process	Total
4 MHz	± 1%	± 3% @ 2.1~5.5V	± 2%	± 6%
16 MHz	± 1%	± 1% @ 4.0~5.5V	± 2%	± 4%
8 MHz	± 1%	± 2% @ 3.0~5.5V	± 2%	± 5%
1 MHz	± 1%	± 3% @ 2.1~5.5V	± 2%	± 6%

- Peripheral configuration
  - 8-bit real time clock / counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power on reset and 3 programmable level voltage reset
    POR: 1.8V (Default), LVR: 4.0, 3.5, 2.7V
  - 2 / 4 clocks per instruction cycle selected by code option
  - High EFT immunity
- Three available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
- Special Features
  - Programmable free running watchdog timer
  - Power saving sleep mode
  - Selectable oscillation mode
- Package type:
  - 18-pin DIP 300mil : EM78P156KD18J
  - 18-pin SOP 300mil : EM78P156KSO18J
  - 20-pin SSOP 209mil : EM78P156KJSS20J

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

(1) 18-Pin DIP / SOP

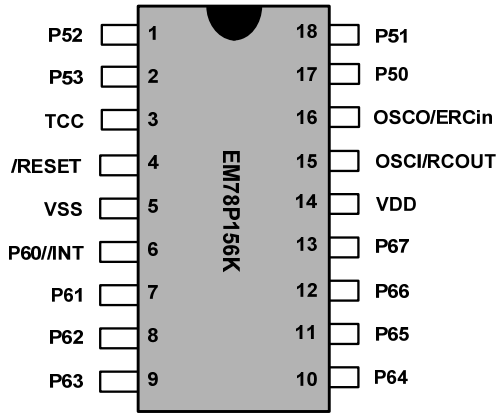


Figure 3-1 18-pin EM78P156KD18J/SO18J

(2) 20-Pin SSOP

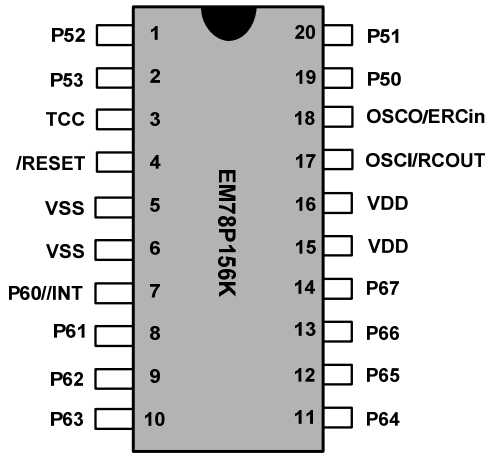


Figure 3-2 20-pin EM78P156KJSS20J

4 Pin Description

Name	Function	Input Type	Output Type	Description
P53	P53	ST	CMOS	Bidirectional I/O pin
P52 P51 P50	P52 P51 P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down.
P67 P66 P65 P64	P67 P66 P65 P64	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up.
P63 P62 P61	P63 P62 P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	/INT	ST	–	External interrupt pin
TCC	TCC	ST	–	Real Time Clock/Counter clock input
/RESET	/RESET	ST	–	External pull-high reset pin
OSCI/RCOUT	OSCI	XTAL	–	Clock input of crystal / resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
OSCO/ERCin	OSCO	–	XTAL	Clock output of crystal / resonator oscillator
	ERCin	AN	–	External RC input pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

***Legend*:** *ST: Schmitt Trigger input* *CMOS: CMOS output*
AN: analog pin *XTAL: oscillation pin for crystal / resonator*

5 Block Diagram

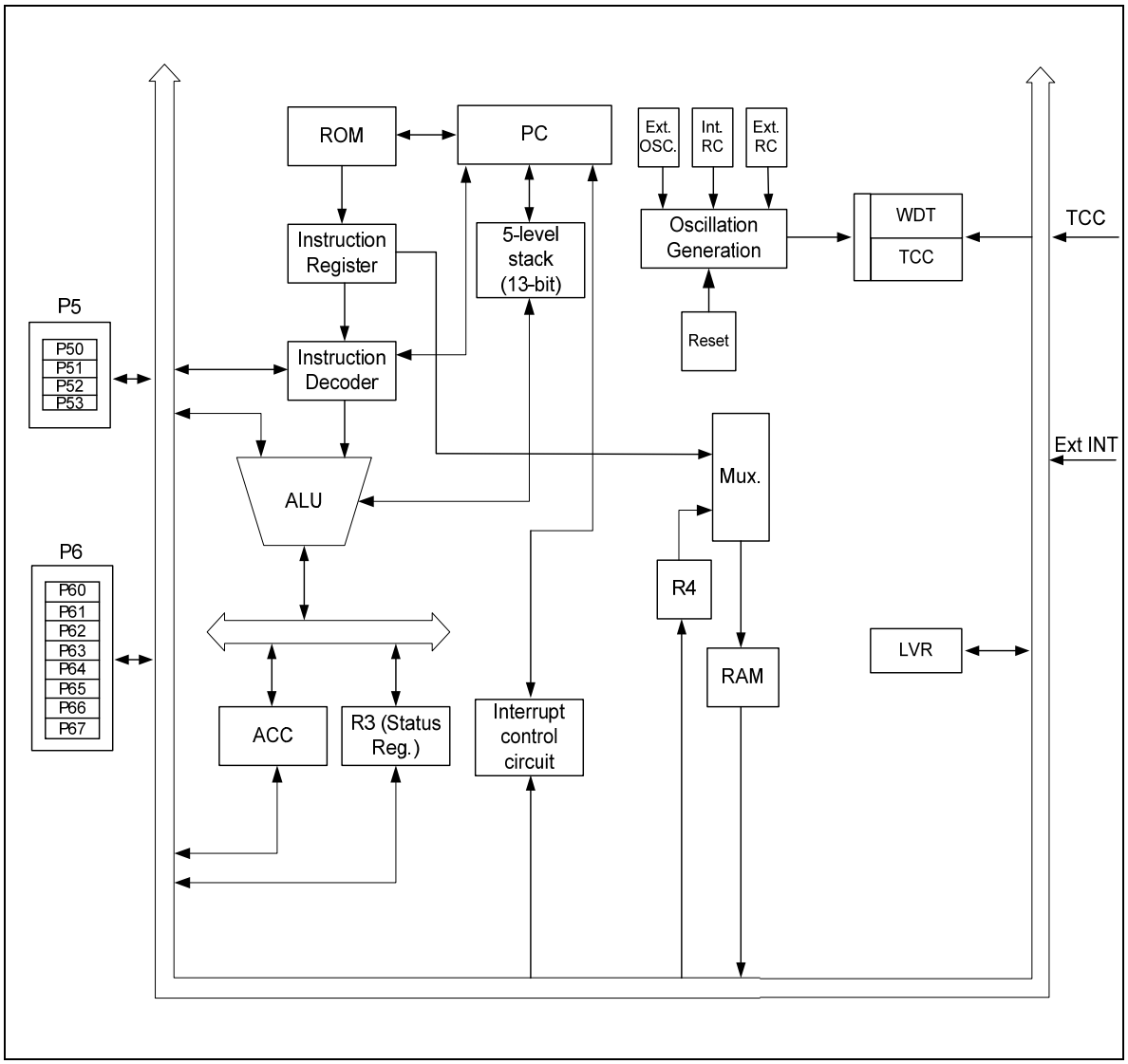


Figure 5-1 EM78P156K Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock / Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

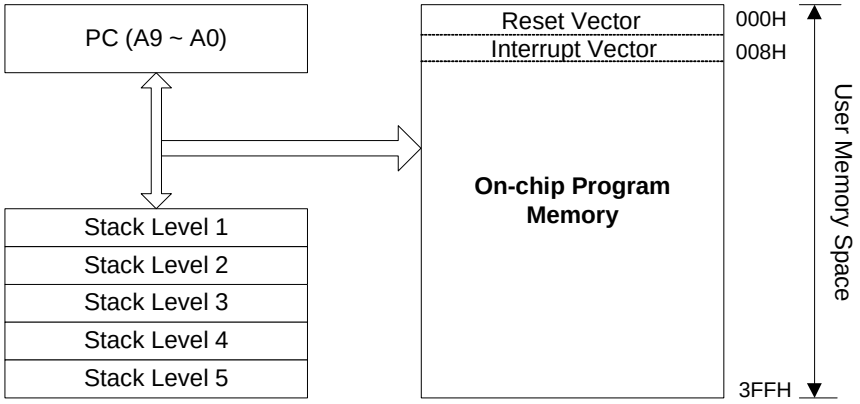


Figure 6-1 Program Counter Organization

- The configuration structure generates 1024 × 13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.
- Any instruction written to R2 (e.g. "ADD R2, A" , "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (F_{CLK} / 2 or F_{CLK} / 4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.
- The Data Memory Configuration is as follows:

Address	R Registers	IOC Registers
		CONT (Control Register)
00	R0 (Indirect Addressing Register)	Reserve
01	R1 (TCC Buffer)	Reserve
02	R2 (Program Counter)	Reserve
03	R3 (Status Register)	Reserve
04	R4 (RSR)	Reserve
05	R5 (Port 5 I/O Data)	IOC5 (I/O Port Control Register)
06	R6 (Port 6 I/O Data)	IOC6 (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	IOCA (Prescaler Control Register)
0B	Reserve	IOCB (Pull-down Control Register)
0C	Reserve	IOCC (Open-drain Control Register)
0D	Reserve	IOCD (Pull-high Control Register)
0E	Reserve	IOCE (WDT Control Register)
0F	RF (Interrupt Status Register)	IOCF (Interrupt Mask Register)
10 : 3F	General Registers	

Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP2	GP1	GP0	T	P	Z	DC	C

Bits 7 ~ 5 (GP2 ~ GP0): General-purpose read / write bits

Bit 4 (T): Time-out bit

Set to “1” with the "SLEP" and "WDTC" commands, or during power up; and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

- Bits 7 ~ 6 are not used (read only).
- Bits 7 ~ 6 set to “1” at all time.
- Bits 5 ~ 0 are used to select registers (Address: 0x00 ~ 0x06, 0x0F ~ 0x3F) in the indirect addressing mode.
- See the Data Memory Configuration in Figure 6-2.

6.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and R6 are I/O registers.

Only the lower 4 bits of R5 are available.

The upper 4 bits of R5 are fixed to “0”.

6.1.7 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

Note: “ 1 ” means with interrupt request **“ 0 ”** means no interrupt occurs

Bits 7 ~ 3: Not used.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.1.8 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (GP): General purpose register

Bit 6 (/INT): Interrupt Enable flag

0: masked by DISI or hardware interrupt

1: enabled by ENI / RETI instructions

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock

1: transition on TCC pin

Bit 4 (TE): TCC Signal Edge

0: increment if the transition from low to high takes place on the TCC pin

1: increment if the transition from high to low takes place on the TCC pin

Bit 3 (PAB): Prescaler Assigned Bit

0: TCC

1: WDT

Bits 2 ~ 0 (PSR2 ~ PSR0): TCC / WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC6 (I/O Port Control Register)

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

Only the lower 4 bits of IOC5 are available to be defined.

The IOC5 and IOC6 registers are both readable and writable.

6.2.4 IOCA (Prescaler Counter Register)

- The IOCA register is readable.
- The value of IOCA is equal to the contents of the Prescaler counter.
- Down counter.

6.2.5 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	-	/PD52	/PD51	/PD50

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bit 3: Not used. Set to “1” at all time.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

The IOCB Register is both readable and writable.

6.2.6 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3 (OD63): Control bit used to enable open-drain of the P63 pin.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

6.2.7 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit is used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.8 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	ROC	-	-	-	-

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0: P60, bidirectional I/O pin.

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1".

When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 6 (R6). See Figure 6-6 under Section 6.4 for reference.

EIS is both readable and writable.

Bit 3: Not used. Set to "**1**" at all time.

Bit 4 (ROC): ROC is used for the R-option.

Setting the ROC to "1" will enable the status of R-option pins (P50~P51) that are read by the controller. Clearing the ROC will disable the R-option function. If the R-option function is selected, user must connect the P51 pin and/or P50 pin to VSS with a 430K external resistor (Rex). If the Rex is connected / disconnected, the status of P50 & P51 is read as "0" / "1". Refer to Figure 6-8 *Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-Up*.

Bits 3 ~ 0: Not used. Set to "**1**" at all time.

6.2.9 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bits 7 ~ 3: Not used. Set to "1" at all time.

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 *Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up*.

Bit 2 (EXIE): EXIF interrupt enable bit

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: disable TCIF interrupt

1: enable TCIF interrupt

The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0 ~ PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. If the prescaler is earlier assigned to TCC and later assigned to WDT, or vice versa, the contents of the prescaler counter would be cleared automatically. Figure 6-4 depicts the circuit diagram of TCC / WDT.

- R1 (TCC) is an 8-bit timer / counter. The TCC clock source can be internal or external clock input (edge selectable from the TCC pin). If the TCC signal source is from an internal clock, the TCC will be incremented by 1 at every instruction cycle (without prescaler). Referring to Figure 5-4, CLK = F_{OSC} / 2 or CLK=F_{OSC} / 4, depends on the Code Option bit CLK. CLK=F_{OSC} / 2 is used if CLK bit is "0", and CLK=F_{OSC} / 4 is used if CLK bit is "1". If the TCC signal source is from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.

- The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

[1] V_{DD} = 5V, WDT time-out period = 16.8ms ± 30% at 25°C
V_{DD} = 3V, WDT time-out period = 18ms ± 30% at 25°C

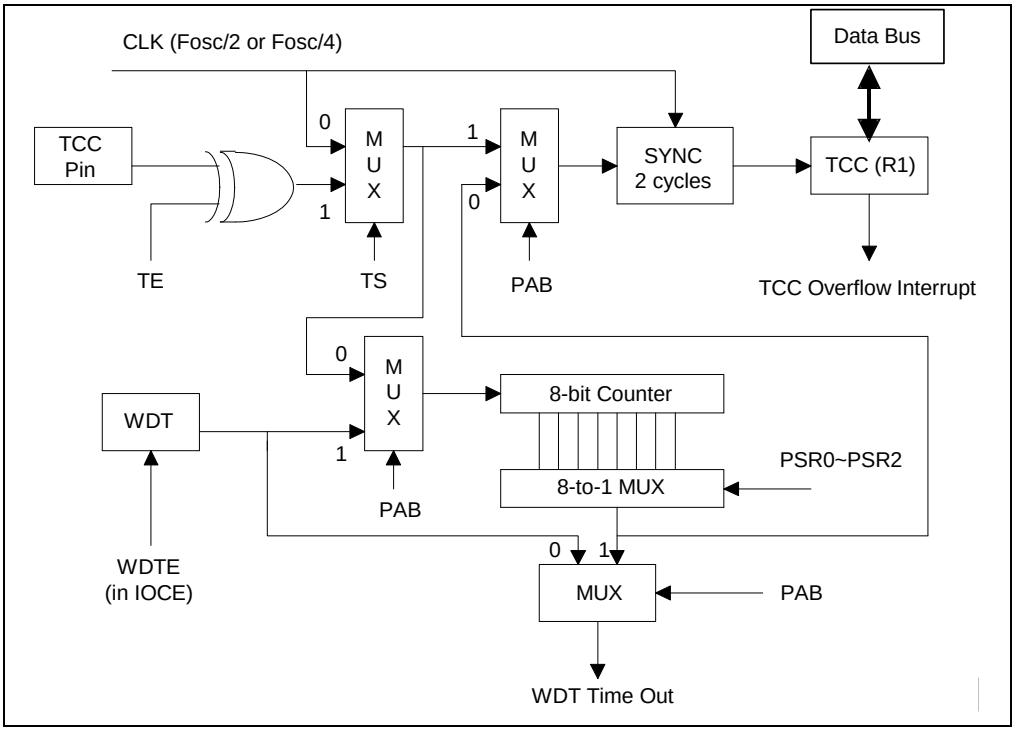
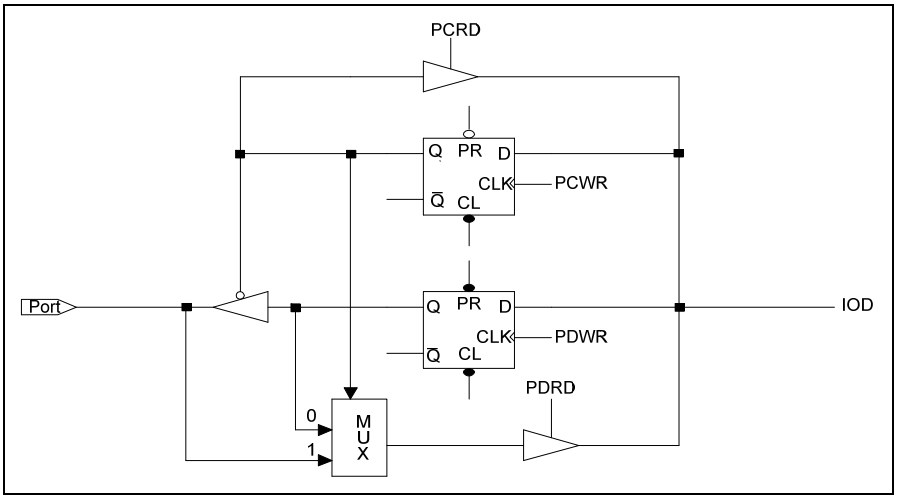


Figure 6-4 TCC and WDT Block Diagram

6.4 I/O Ports

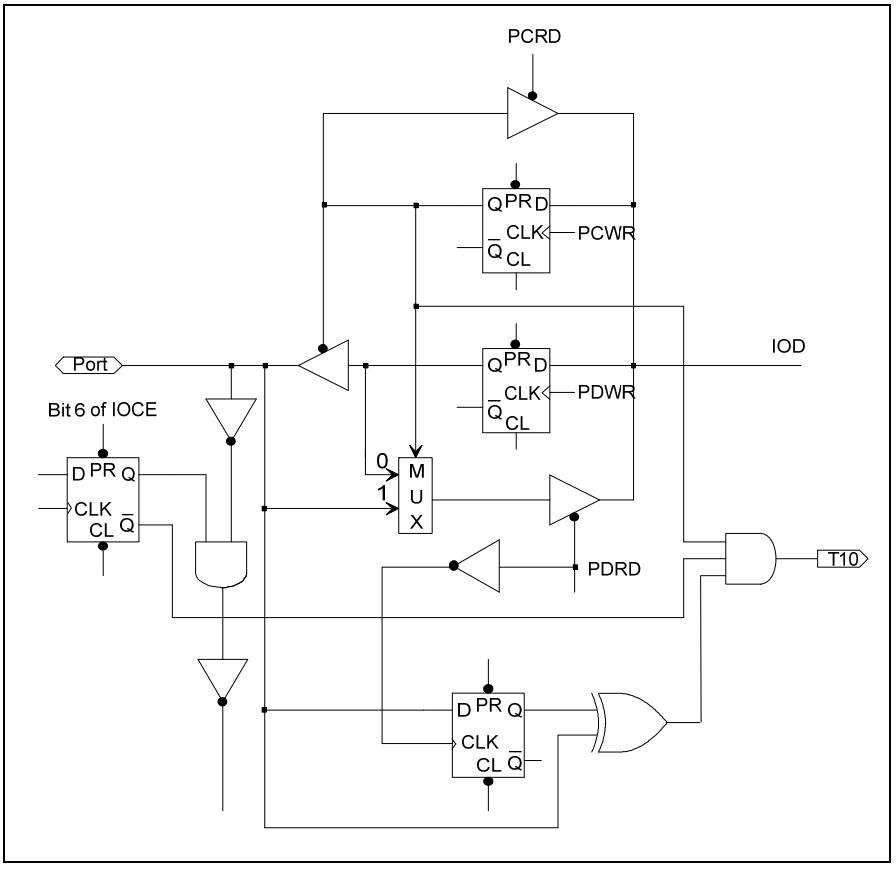
The I/O registers, both Port 5 and Port 6, are bidirectional tri-state I/O ports. Port 6 can be pulled high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function is available from Port 6. P50 ~ P52 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). P50 ~ P51 are the R-option pins enabled by setting the ROC bit in the IOCE register to “1”. When the R-option function is used, it is recommended that P50 ~ P51 are used as output pins. When R-option is in enable state, P50 ~ P51 must be programmed as input pins. Under R-option mode, the current / power consumption by R_{EX} should be taken into consideration to promote energy conservation.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following Figure 6-5 ~ Figure 6-9 respectively.



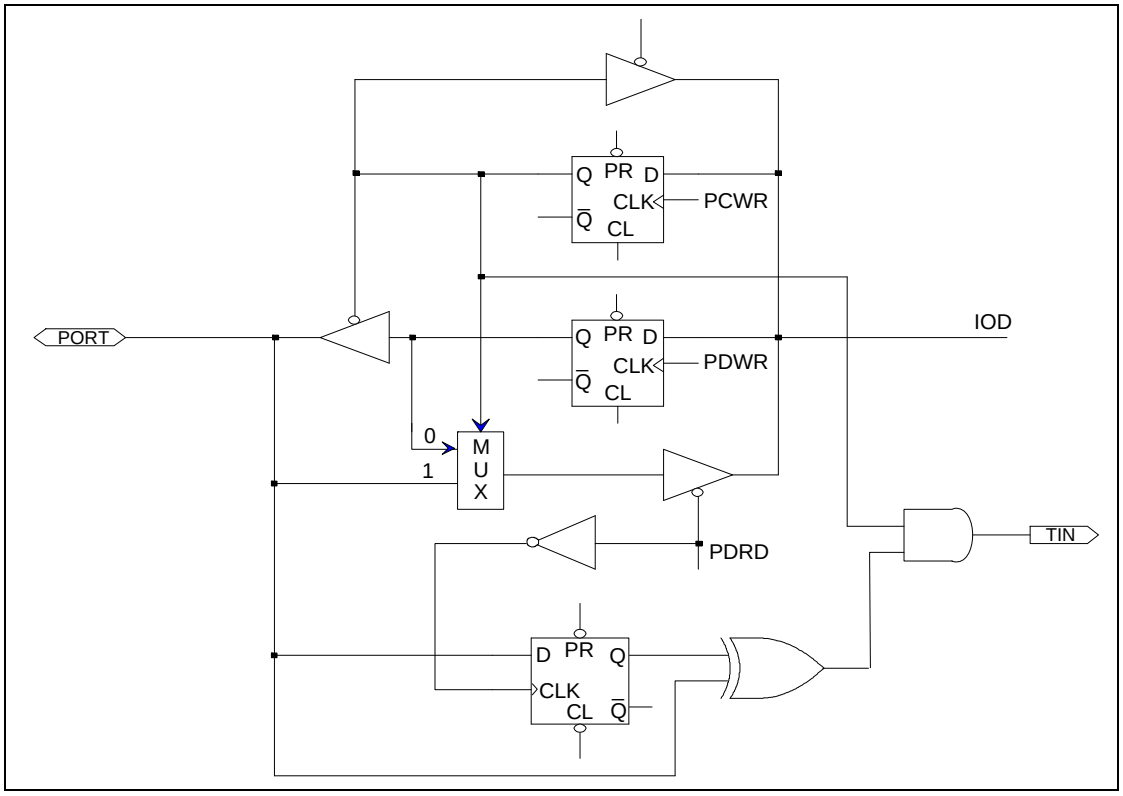
Note: *Pull-down is not shown in the figure.*

Figure 6-5 I/O Port and I/O Control Register Circuit for Ports 5 and 6



Note: *Pull-high (down) and open-drain are not shown in the figure.*

Figure 6-6 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: *Pull-high (down) and open-drain are not shown in the figure.*

Figure 6-7 I/O Port and I/O Control Register Circuit for P61 ~ P67

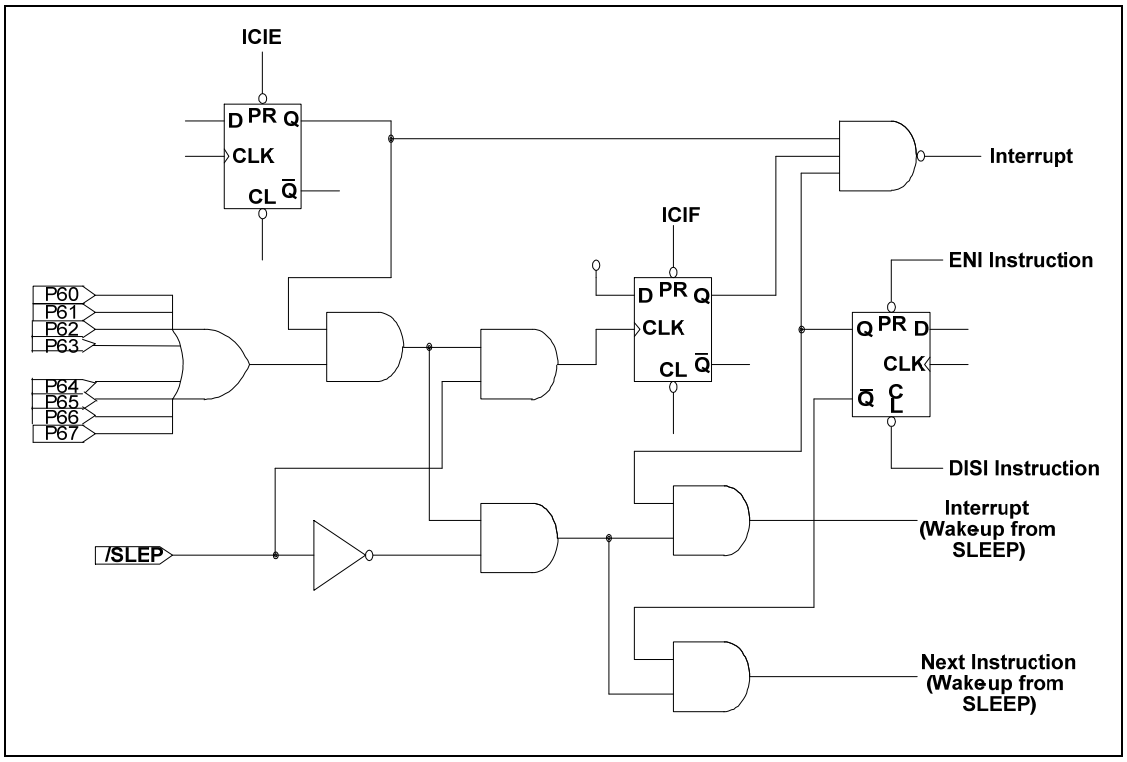


Figure 6-8 Block Diagram of I/O Port 6 with Input Change Interrupt / Wake-up

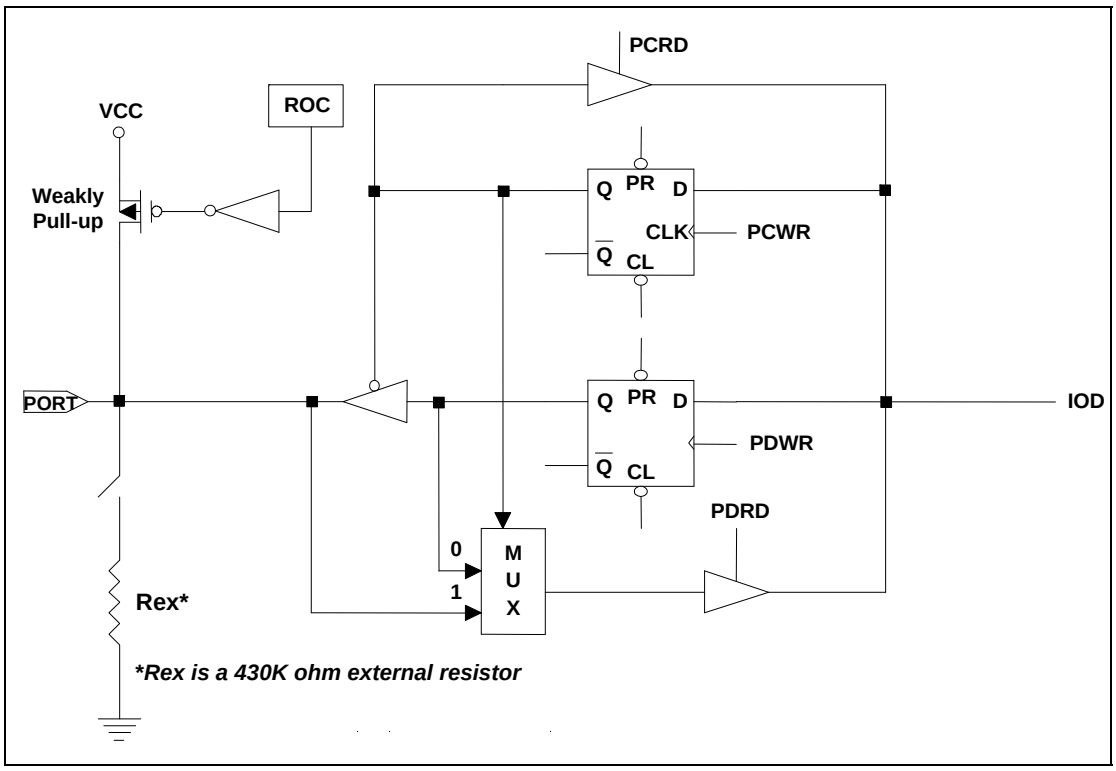


Figure 6-9 Circuit of I/O Port with R-Option (P50, P51)

Table 6-1 Usage of Port 6 Input Change Wake-up / Interrupt Function

Usage of Port 6 Input Status Change Wake-up / Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt Vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute “ENI” 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events:

1) Power-on reset

2) /RESET pin input "low"

3) WDT time-out (if enabled)

4) Low Voltage Reset

The device is kept under reset condition for a period of approximately 18 ms or 150 µs (one oscillator start-up timer period. Events 1 and 4 are approximately 18 ms and Events 2 and 3 are approximately 150 µs) after a reset is detected. Once a reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCA register are set to all "1."
- The bits of the IOCB register are set to all "1."
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up, in IRC mode (IRC 4 MHz / 5V) wake-up time 1.5 µs, in XT mode (4 MHz / 5V) wake-up time is 1.5 ms.

The controller can be awakened by:

1) External reset input on /RESET pin

2) WDT time-out (if enabled)

3) Port 6 Input Status changed (if enabled)

The first two cases will cause the EM78P156K to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered a continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after a wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after a wake-up.

After a wake-up in IRC mode (IRC 4 MHz / 5V), the wake-up time is 1.5 µs, in XT mode (4 MHz / 5V), the wake-up time is 1.5 ms.

Only one of Cases 2 and 3 can be enabled before going into Sleep mode. That is,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P156K can be awakened only by Case 1 or Case 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P156K can be awakened only by Case 1 or Case 2. Refer to Section 6.6, *Interrupt* for further details.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P156K (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                      ; set over 1:1
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

After waking up from sleep mode, WDT is automatically enabled. The WDT enable / disable operation after waking up from sleep mode should be appropriately defined in the software.

6.5.2 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up	P	P	P	*	*	P	P	P
0×04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-up	1	1	P	P	P	P	P	P
0×05	P5	Bit Name	×	×	×	×	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR)	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	CONT	Bit Name	GP	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC5	Bit Name	×	×	×	×	C53	C52	C51	C50
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	-	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	1	P	P	P
0×0C	IOCC	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	WDTE	EIS	-	ROC	-	-	-	-
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up	1	P	1	P	1	1	1	1
0×0F	IOCF	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-up	1	1	1	1	1	P	P	P
0×10~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up	P	P	P	P	P	P	P	P

Legend: *×: Not used* ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*

* *Refer to the tables provided in the next section (Section 6.5.3).*

6.5.3 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events

1) A power-on condition

2) A high-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of T and P listed in the table below are used to check how the processor wakes up.

Table 6-2 Values of RST, T, and P after a Reset

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operation mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operation mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

The following table shows the events that may affect the status of T and P.

Table 6-3 Status of T and P Being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

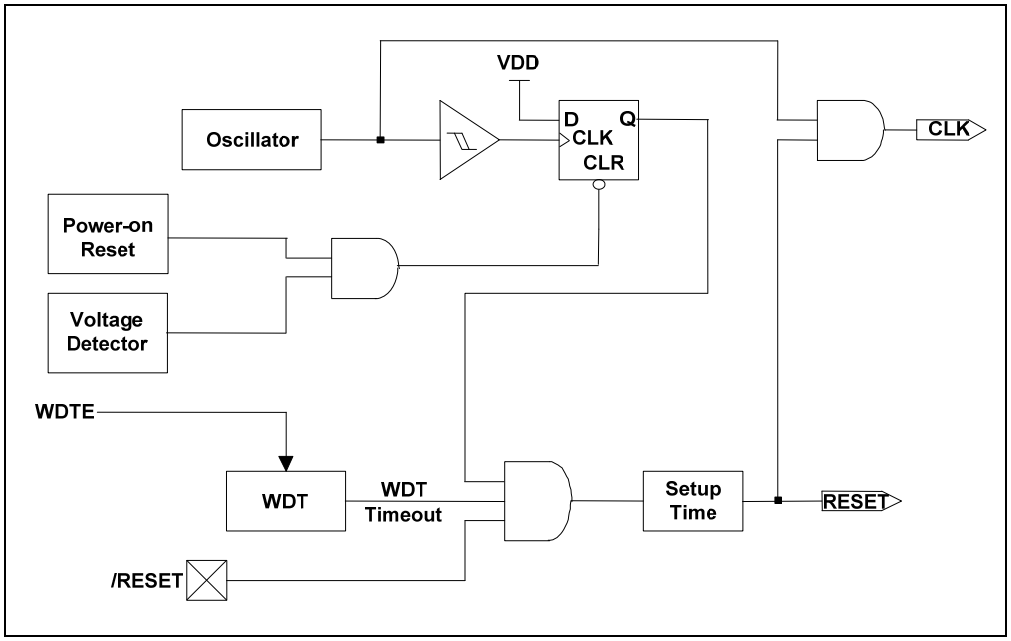


Figure 6-10 Controller Reset Block Diagram

6.6 Interrupt

The EM78P156K has three interrupts as listed below:

1) TCC overflow interrupt
2) Port 6 Input Status Change Interrupt
3) External interrupt [(P60, /INT) pin]

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6, R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P156K from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the IC wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags/ bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions prior to leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Figure 6-11 *Interrupt Input Circuit*). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from Address 001H.

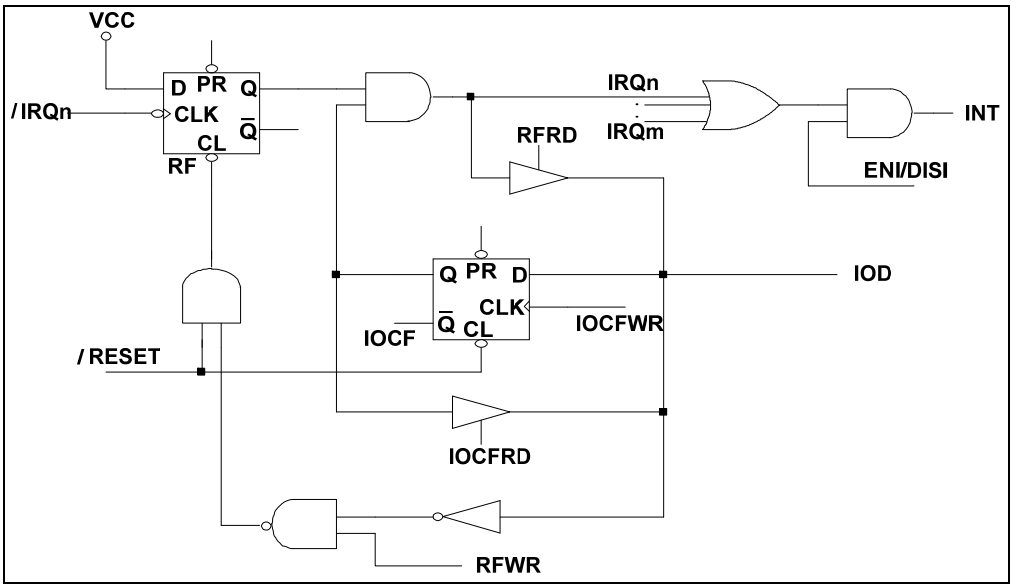


Figure 6-11 Interrupt Input Circuit Diagram

6.7 Oscillator

6.7.1 Oscillator Modes

The EM78P156K can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (XT, HXT1/2), and Low Crystal oscillator mode (LXT1/2). The desired mode can be selected by programming OSC3 ~ OSC0 in the Code Option register. Table 6-4 shows how these four oscillator modes are defined.

Table 6-4 Oscillator Modes Defined by OSC

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); RCOUT is deactivated	0	0	0	0
ERC[1] (External RC oscillator mode); RCOUT is activated	0	0	0	1
IRC[2] (Internal RC oscillator mode); RCOUT is deactivated	0	0	1	0
IRC[2] (Internal RC oscillator mode); RCOUT is activated	0	0	1	1
LXT1[3] (Frequency range of LXT1 mode is 1MHz ~ 100kHz)	0	1	0	0
HXT1[3] (Frequency range of HXT1 mode is 20 MHz ~ 12 MHz)	0	1	0	1
LXT2[3] (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of HXT2 mode is 12 MHz ~ 6 MHz)	0	1	1	1
XT (Frequency range of XT mode is 6 MHz ~ 1 MHz) (default)	1	1	1	1

[1] In ERC mode, ERCin is used as oscillator pin. RCOUT is defined by Code Option Word 1 Bit 4 ~ Bit 1.

[2] In IRC mode, RCOUT is defined by code option Word 1 Bit 4 ~ Bit 1.

[3] In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

The maximum operational frequency of the crystal / resonator under different VDD is listed below.

Table 6-5 Summary of the Maximum Operating Speeds

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.1	4.0
	3.0	8.0
	5.0	20.0

6.7.2 Crystal Oscillator / Ceramic Resonators (Crystal)

The EM78P156K can be driven by an external clock signal through the OSCI pin as shown in the following figure.

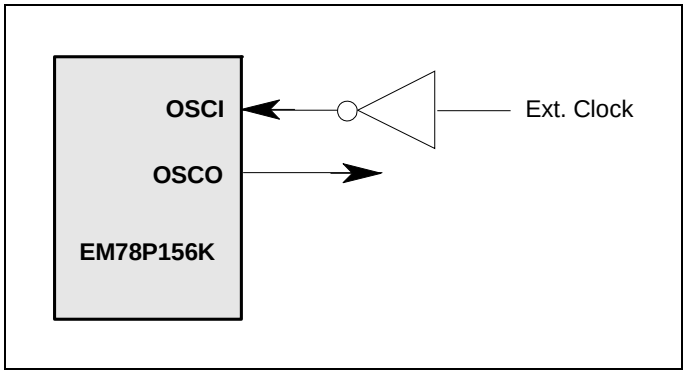


Figure 6-12 Circuit for External Clock Input

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-13 depicts such a circuit. The same thing applies whether it is in the HXT mode or in the LXT mode.

In Figure 6-14, when the connected resonator in OSCI and OSCO is used in applications, the 1 MΩ R1 needs to be shunted with a resonator.

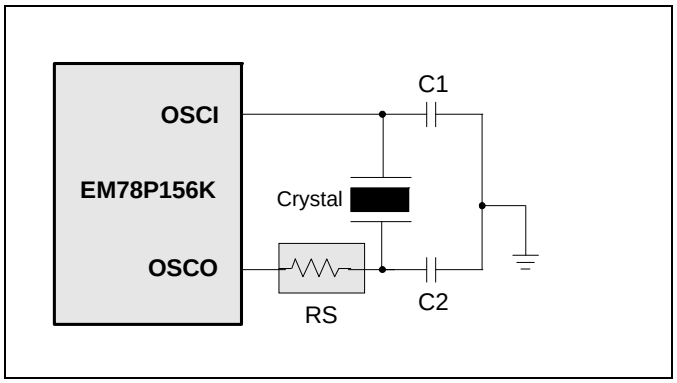


Figure 6-13 Circuit for Crystal / Resonator

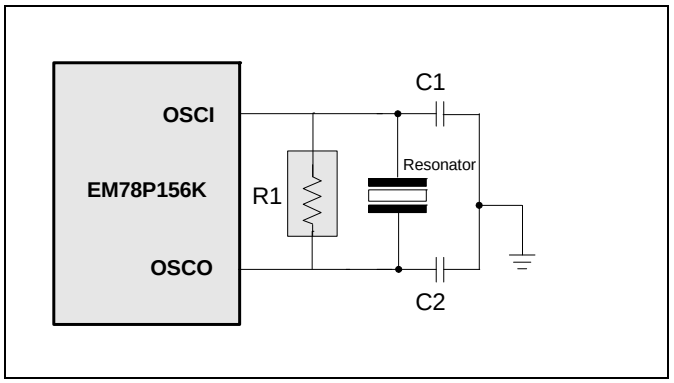


Figure 6-14 Circuit for Crystal / Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. A serial resistor RS, may be necessary for AT strip cut crystal or low frequency mode.

Table 6-6 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100k ~ 1 MHz)	100 kHz	60pF	60pF
		200 kHz	60pF	60pF
		455 kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768 kHz	40pF	40pF
	LXT1 (100k ~ 1 MHz)	100 kHz	60pF	60pF
		200 kHz	60pF	60pF
		455 kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1 ~ 6 MHz)	455 kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT2 (6 ~ 12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		10.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF
	HXT1 (12 ~ 20 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
		20.0 MHz	15pF	15pF

6.7.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-15) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (R_{EXT}), the capacitor (C_{EXT}), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of R_{EXT} should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the R_{EXT} in the RC oscillator is, the faster its frequency will be. On the contrary, for very low R_{EXT} values, for instance, 1 kΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

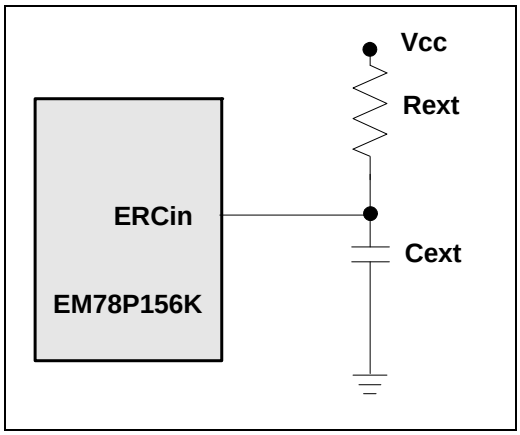


Figure 6-15 External RC Oscillator Mode Circuit

Table 6-7 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20pF	3.3k	2.064 MHz	1.901 MHz
	5.1k	1.403 MHz	1.316 MHz
	10k	750 kHz	719.7 kHz
	100k	81.45 kHz	81.33 kHz
100pF	3.3k	647.3 kHz	615.1 MHz
	5.1k	430.8 kHz	414.3 kHz
	10k	225.8 kHz	219.8 kHz
	100k	23.88 kHz	23.96 kHz
300pF	3.3k	256.6 kHz	245.3 kHz
	5.1k	169.5 kHz	163.0 kHz
	10k	88.53 kHz	86.14 kHz
	100k	9.283 kHz	9.255 kHz

Note: *1: These are measured in DIP packages.*

2. The values are for design reference only.

3. The frequency drift is ± 30%.

6.7.4 Internal RC Oscillator Mode

EM78P156K offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 16 MHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits C0 ~ C4. The table below describes the EM78P156K internal RC drift with variation of voltage, temperature, and process.

Table 6-8 Internal RC Drift Rate (T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V)

Internal RC	Drift Rate			
	Temperature (-40°C ~ 85°C)	Voltage (2.1V ~ 5.5V)	Process	Total
4 MHz	± 1%	± 3% @ 2.1~5.5V	± 2%	± 6%
16 MHz	± 1%	± 1% @ 4.0~5.5V	± 2%	± 4%
8 MHz	± 1%	± 2% @ 3.0~5.5V	± 2%	± 5%
1 MHz	± 1%	± 3% @ 2.1~5.5V	± 2%	± 6%

Note: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.8 Code Option Register

The EM78P156K has a Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

■ **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.8.1 Code Option Register (Word 0)

Word 0											
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2~0
Mnemonic	–	ENWDT	CLKS	LVR1	LVR0	–	–	–	–	–	Protect
1	–	Disable	4 clocks	High	High	–	–	–	–	–	Disable
0	–	Enable	2 clocks	Low	Low	–	–	–	–	–	Enable

Bit 12: Not used. Set to “1” at all time.

Bit 11 (ENWDT): Watchdog timer enable bit

0: Enable

1: Disable

Bit 10 (CLKS): Instruction period option bit.

0: Two oscillator periods

1: Four oscillator periods

Refer to the Instruction Set section.

Bits 9 ~ 8 (LVR1 ~ LVR0): Low Voltage Reset control bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.0V

Bits 7 ~ 3: Not used. Set to "1" at all time.

Bits 2 ~ 0 (Protect): Protect Bits. Each protect status is as follows:

Protect Bits	Protect
0	Enable
1	Disable (Default)

6.8.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	HLP	C4	C3	C2	C1	C0	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	–
1	High	High	High	High	High	High	High	High	High	High	High	High	–
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	–

Bit 12 (HLP): Power consumption mode

0: Low power consumption mode, applies to operating frequency at 400kHz or below 400kHz

1: High power consumption mode, applies to operating frequency above 400kHz (default)

Bits 11 ~ 7 (C4 ~ C0): Internal RC mode Calibration bits. These bits must always be set to "1" only (auto calibration)

Bits 6 ~ 5 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

* Theoretical values, for reference only

Bits 4 ~ 1 (OSC3, ~ OSC0): Oscillator Mode Select bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); RCOUT is deactivated	0	0	0	0
ERC[1] (External RC oscillator mode); RCOUT is activated	0	0	0	1
IRC[2] (Internal RC oscillator mode); RCOUT is deactivated	0	0	1	0
IRC[2] (Internal RC oscillator mode); RCOUT is activated	0	0	1	1
LXT1[3] (Frequency range of LXT1 mode is 1MHz ~ 100kHz)	0	1	0	0
HXT1[3] (Frequency range of HXT1 mode is 20 MHz ~ 12 MHz)	0	1	0	1
LXT2[3] (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of HXT2 mode is 12 MHz ~ 6 MHz)	0	1	1	1
XT (Frequency range of XT mode is 6 MHz ~ 1 MHz) (default)	1	1	1	1

[1] *In ERC mode, ERCin is used as oscillator pin. RCOUT is defined by code option Word 1 Bit 4 ~ Bit 1.*
[2] *In IRC mode, RCOUT is defined by code option Word 1 Bit 4 ~ Bit 1.*
[3] *In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

Bit 0: Not used. Set to "1" at all time.

6.8.3 Customer ID Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 0: Customer's ID code

6.9 Power-on Consideration

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state.

EM78156K POR voltage range is 1.7V ~ 1.9V. Under customer application, when power is OFF, V_{DD} must drop to below 1.8V and remains OFF for 10 µs before power can be switched ON again. This way, the EM78P156K will reset and operate normally. The extra external reset circuit will work well if V_{DD} can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

6.10 External Power-on Reset Circuits

The circuitry in the figure implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time.

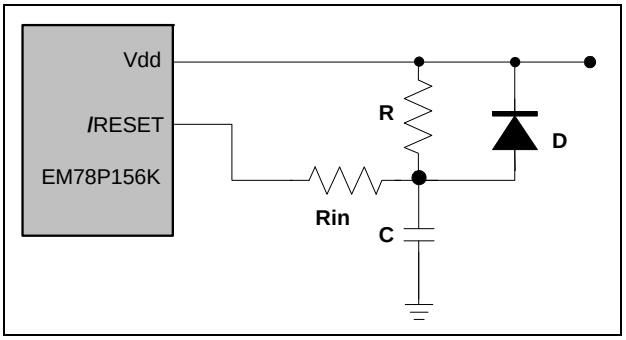


Figure 6-16 External Power-up Reset Circuit

Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40k. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. The current-limited resistor, Rin, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.11 Residue-Voltage Protection

When the battery is replaced, the device power (V_{DD}) is cut off but the residue-voltage remains. The residue-voltage may trip below the minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for the EM78P156K.

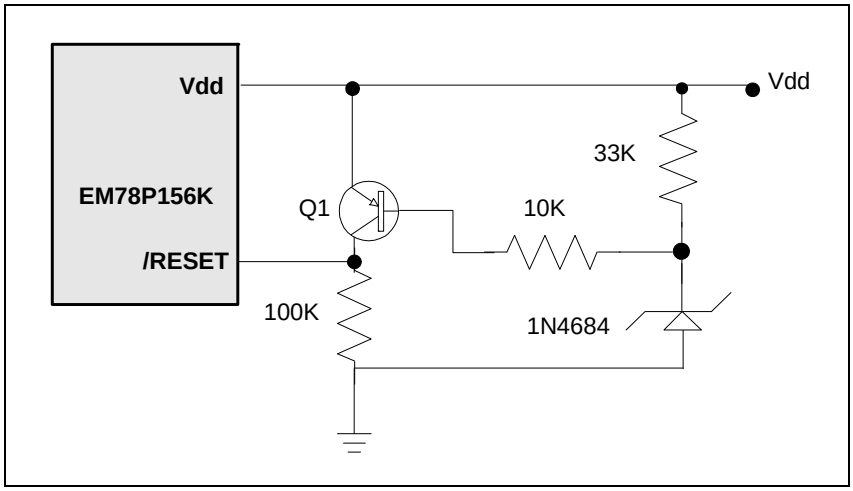


Figure 6-17 Residue Voltage Protection Circuit 1

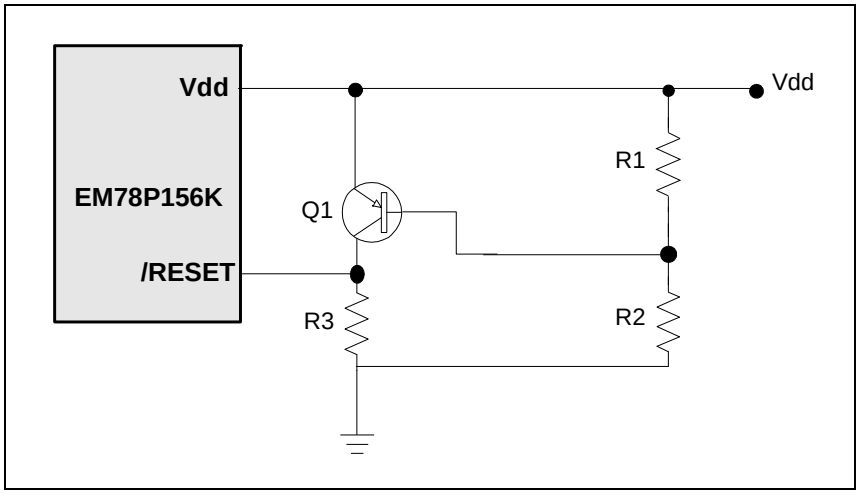


Figure 6-18 Residue Voltage Protection Circuit 2

NOTE

Figure 6-17 and Figure 6-18 should be designed to ensure that the voltage of the /RESET pin is larger than V_{IH} (min)

6.12 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

A) Modify one instruction cycle to consist of four oscillator periods.

B) "JMP", "CALL", "RET", "RETL", "RETI" or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within one instruction cycle. The instructions that are written to the program counter also take one instruction cycle.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low; and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK = F_{OSC} / 4, instead of F_{OSC} / 2.

Moreover, the instruction set has the following features:

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the Instruction Set table:

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b *= Bit field designator that selects the value for the bit located in the register "**R**" and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None [1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None [1]
MOV R, A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A, R	R - A → A	Z, C, DC
SUB R, A	R - A → R	Z, C, DC
DECAR	R - 1 → A	Z
DEC R	R - 1 → R	Z
OR A, R	A ∨ R → A	Z
OR R, A	A ∨ R → R	Z
AND A, R	A & R → A	Z
AND R, A	A & R → R	Z

(Continuation)

Mnemonic	Operation	Status Affected
XOR A, R	A ⊕ R → A	Z
XOR R, A	A ⊕ R → R	Z
ADD A, R	A + R → A	Z, C, DC
ADD R, A	A + R → R	Z, C, DC
MOV A, R	R → A	Z
MOV R, R	R → R	Z
COMAR	/R → A	Z
COM R	/R → R	Z
INCA R	R + 1 → A	Z
INC R	R + 1 → R	Z
DJZA R	R - 1 → A, skip if zero	None
DJZ R	R - 1 → R, skip if zero	None
RRCAR	R(n) → A(n - 1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n - 1), R(0) → C, C → R(7)	C
RLCAR	R(n) → A(n + 1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n + 1), R(7) → C, C → R(0)	C
SWAPAR	R(0-3) → A(4 - 7), R(4-7) → A(0 - 3)	None
SWAPR	R(0-3) ↔ R(4 - 7)	None
JZA R	R + 1 → A, skip if zero	None
JZ R	R + 1 → R, skip if zero	None
BC R, b	0 → R(b)	None 2
BS R, b	1 → R(b)	None 3
JBC R, b	if R(b) = 0, skip	None
JBS R, b	if R(b) = 1, skip	None
CALL k	PC + 1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A, k	k → A	None
OR A, k	A ∨ k → A	Z
AND A, k	A & k → A	Z
XOR A, k	A ⊕ k → A	Z

(Continuation)

Mnemonic	Operation	Status Affected
RETL k	k → A, [Top of Stack] → PC	None
SUB A, k	K - A → A	Z, C,DC
INT	PC + 1 ® [SP], 001H ® PC	None
ADD A, k	K + A → A	Z, C, DC

Note: [1] *This instruction is applicable to IOC5 ~ IOC6, IOCA ~ IOCF only.*
[2] *This instruction is not recommended for interrupt status register operation.*
[3] *This instruction cannot operate under interrupt status register.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	20 MHz

Note: **These parameters are theoretical values and have not been tested.*

8 Electrical Characteristics

8.1 DC Characteristics

T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 2.1V	Two cycles with two clocks	DC	–	4.0	MHz
	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	ERC: VDD to 5V	R: 5kΩ, C: 39pF	F±30%	1500	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	µA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0	–	–	V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6	–	–	0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	2.0	–	–	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	–	–	0.8	V

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	2.5	–	Vdd+0.3	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI	–	–	1.0	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5	–	–	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6	–	–	0. 4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	1.5	–	–	V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	–	–	0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5	–	–	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI	–	–	0.6	V
VOH1	Output High Voltage (Ports 5, Ports 6)	IOH = -12mA	2.4	–	–	V
VOL1	Output Low Voltage (P50 ~ 53 and Port 6) (Schmitt trigger)	IOL = 12mA	–	–	0.4	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	60	75	90	µA
IPD	Pull-down current	Pull-down active, Input pin at VDD	20	35	50	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	–	1	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	10	µA
ICC1	Operating supply current at two clocks (VDD=3V)	/RESET = 'High', F_{OSC}=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	20	µA
ICC2	Operating supply current at two clocks (VDD=3V)	/RESET = 'High', F_{OSC}=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	15	25	µA
ICC3	Operating supply current at two clocks (VDD=5.0V)	/RESET = 'High', F_{OSC}=4 MHz (Crystal type, CLKS="0"), Output pin floating	–	–	1.5	mA
ICC4	Operating supply current at two clocks (VDD=5.0V)	/RESET = 'High', F_{OSC} = 10 MHz (Crystal type, CLKS="0"), Output pin floating	–	–	2.8	mA

Note: **These parameters are theoretical values and have not been tested.*

■ **Internal RC Electrical Characteristics (T_A = 25°C, V_{DD} = 5 V, V_{SS} = 0V)**

Internal RC Selected Band	Drift Rate				
	Temperature	Operating Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.92 MHz	4 MHz	4.08 MHz
16 MHz	25°C	5V	15.68 MHz	16 MHz	16.32 MHz
8 MHz	25°C	5V	7.84 MHz	8 MHz	8.16 MHz
1 MHz	25°C	5V	0.98 MHz	1 MHz	1.02 MHz

■ **Internal RC Electrical Characteristics (Process, Voltage and Temperature Deviation)**

Internal RC Selected Band	Drift Rate (Process & Operating Voltage and Temperature Variation)				
	Temperature	Operating Voltage	Min.	Typ.	Max.
4 MHz	-40 ~ 85°C	2.1V ~ 5.5V	3.76 MHz	4 MHz	4.24 MHz
16 MHz	-40 ~ 85°C	4.0V ~ 5.5V	15.36 MHz	16 MHz	16.64 MHz
8 MHz	-40 ~ 85°C	3.0V ~ 5.5V	7.60 MHz	8 MHz	8.40 MHz
1 MHz	-40 ~ 85°C	2.1V ~ 5.5V	0.94 MHz	1 MHz	1.06 MHz

8.2 AC Characteristics

T_A=25°C, V_{DD}=5V, V_{SS}=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins + 20)/N*	–	–	ns
Tdrh	Device reset hold time	XTAL	16.8 - 30%	16.8	16.8 + 30%	ms
Trst	/RESET pulse width	–	2000	–	–	ns
Twdt	Watchdog timer period	–	16.8 - 30%	16.8	16.8 + 30%	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	C_{LOAD} = 20pF	–	50	–	ns

Note: *These parameters are theoretical values and have not been tested.*

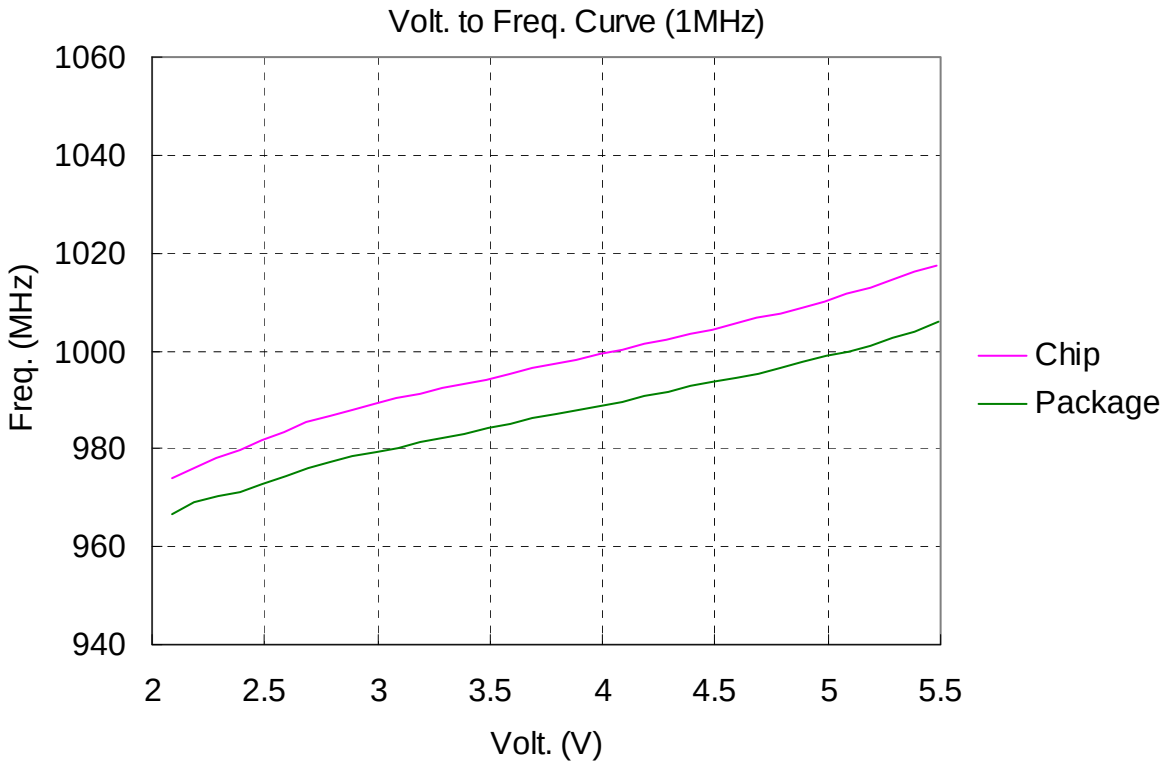
The Watchdog Timer duration is determined by Option Code (Bit 6, Bit 5)

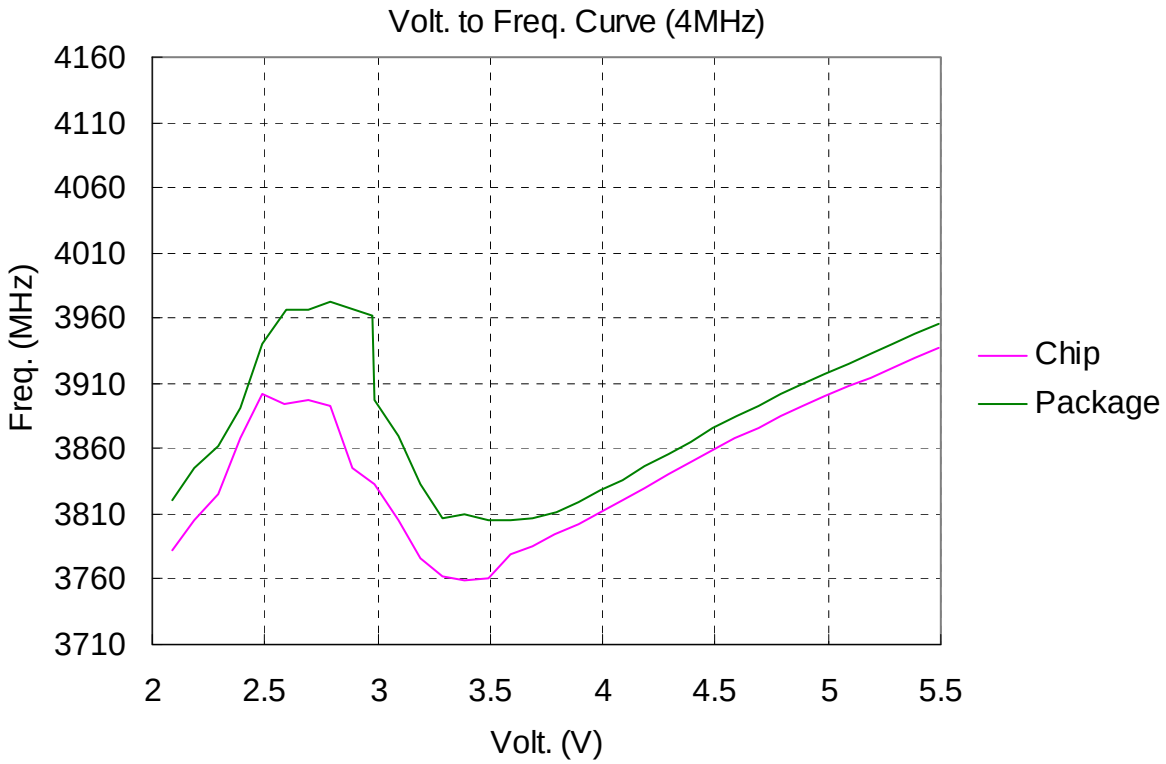
**N = selected prescaler ratio*

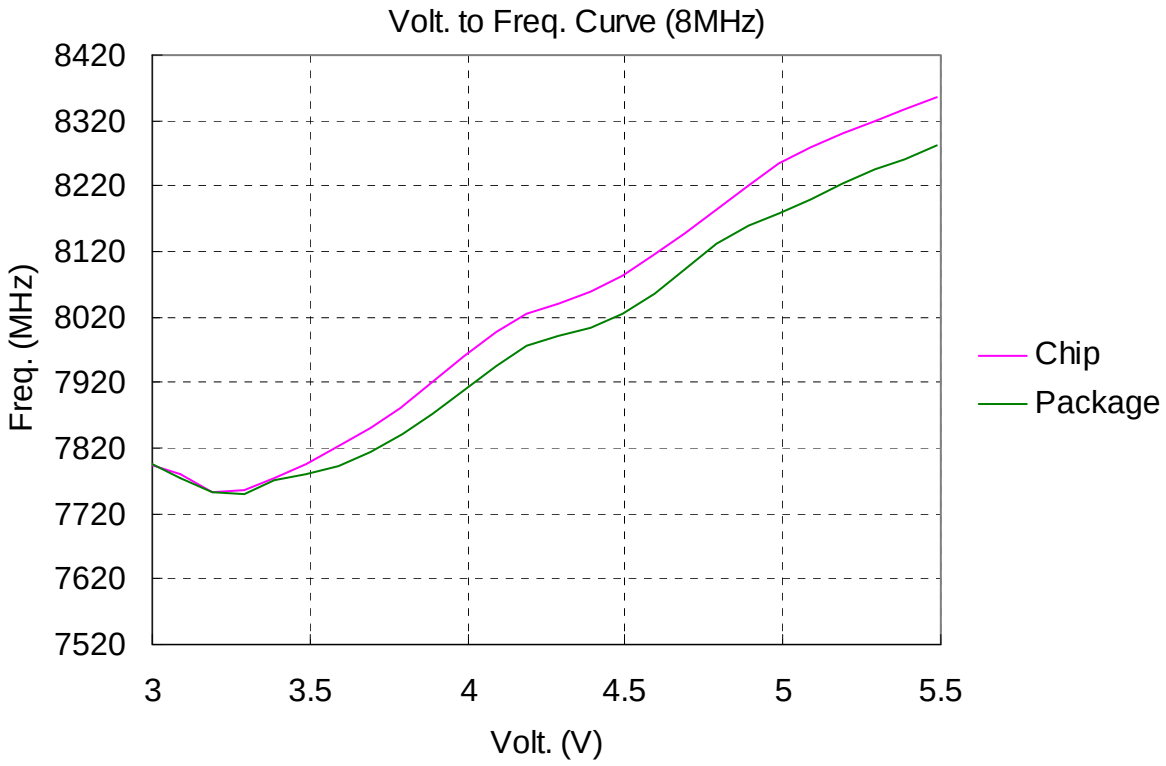
**Twdt: In Crystal mode the WDT time-out length is the same as the set-up time (18 ms).*

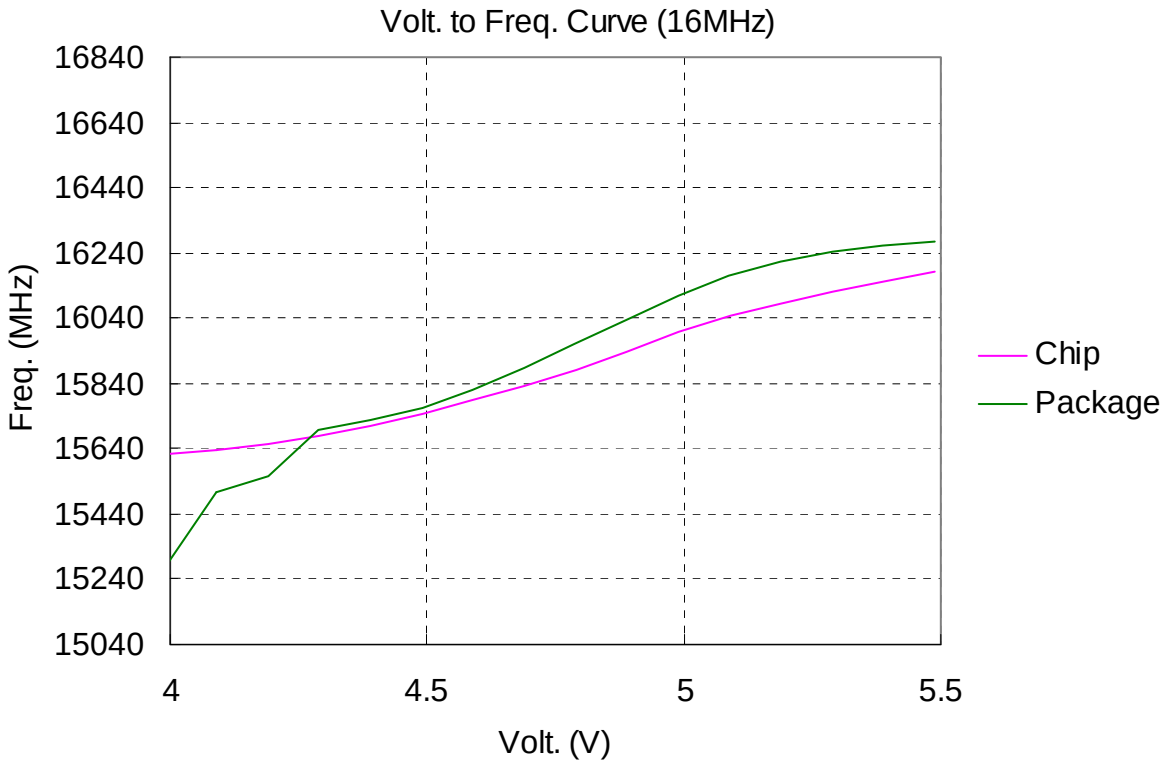
8.3 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphs, the data may be out of the specified warranted operating range.



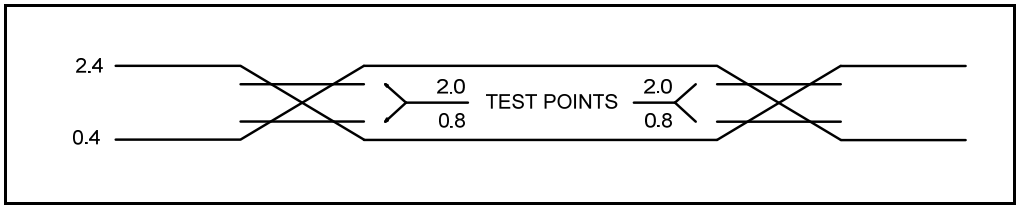

Volt. to Freq. Curve (4MHz)
Freq. (MHz)
4160
4110
4060
4010
3960
3910
3860
3810
3760
3710
2
2.5
3
3.5
4
4.5
5
5.5
Volt. (V)
Chip
Package


Volt. to Freq. Curve (8MHz)
Freq. (MHz)
8420
8320
8220
8120
8020
7920
7820
7720
7620
7520
3
3.5
4
4.5
5
5.5
Volt. (V)
Chip
Package


Volt. to Freq. Curve (16MHz)
16840
16640
16440
16240
16040
15840
15640
15440
15240
15040
Freq. (MHz)
4
4.5
5
5.5
Volt. (V)
Chip
Package

9 Timing Diagrams

AC Test Input / Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**", and 0.4V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**", and 0.8V for logic "**0**"*

Figure 9-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

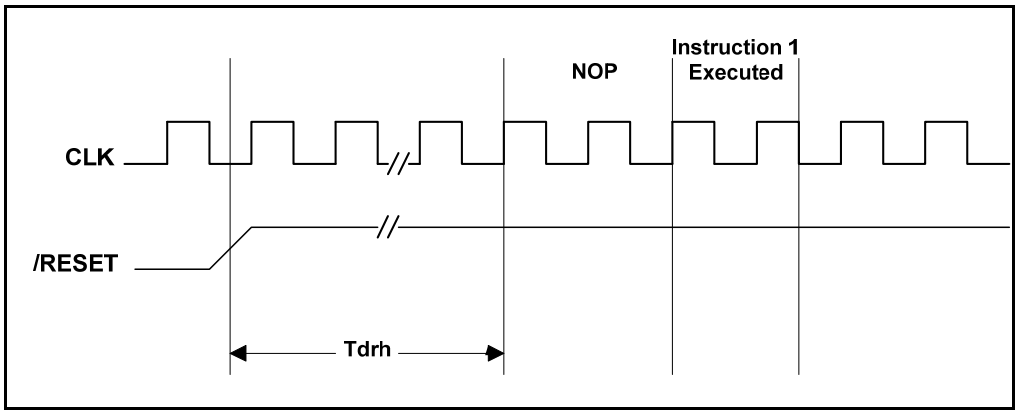


Figure 9-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

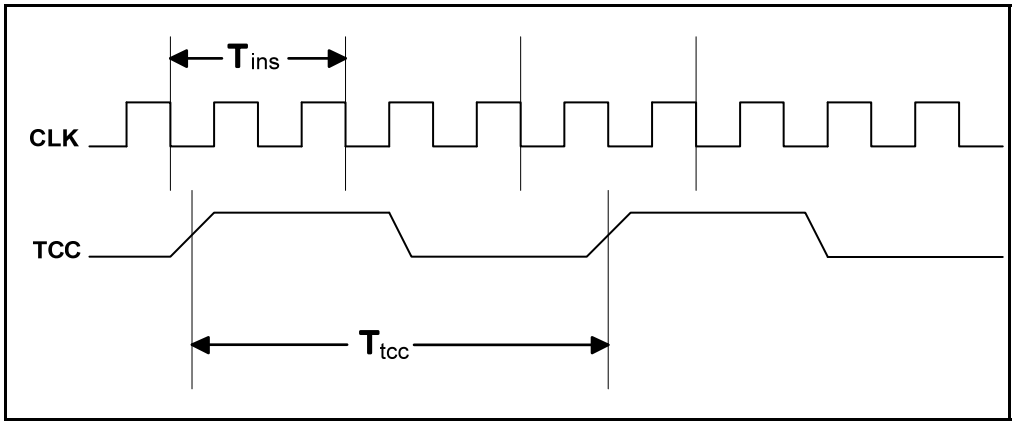
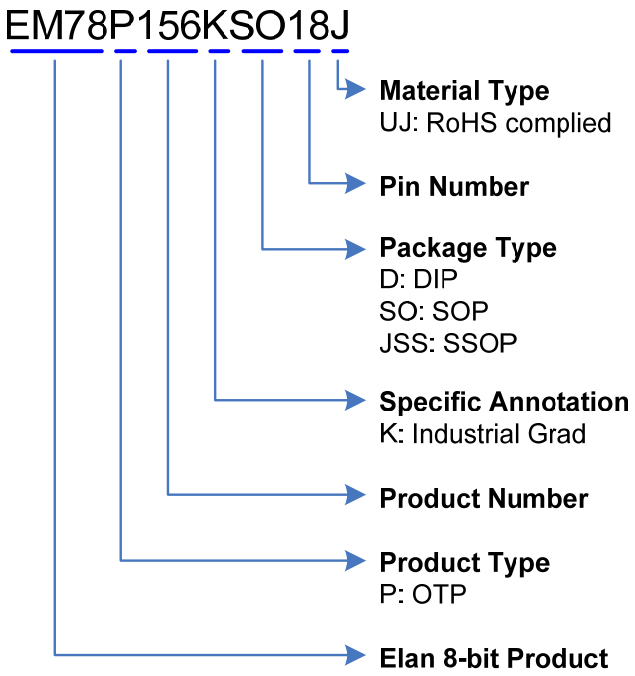


Figure 9-1c TCC Input Timing Diagram

APPENDIX

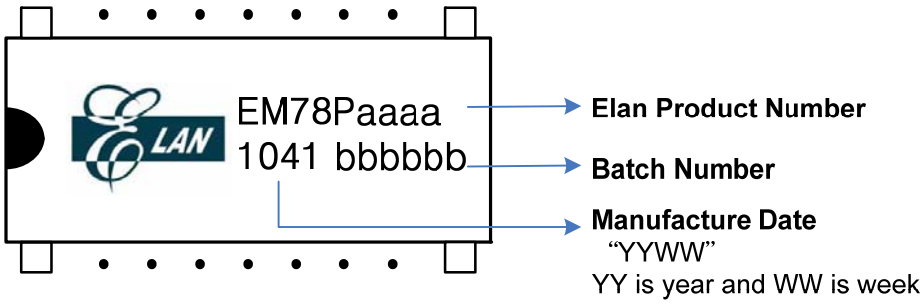
A Ordering and Manufacturing Information



For example:

EM78P156KD18J

is EM78P156K with OTP program memory, industrial grade product, in 18-pin DIP 300mil package with RoHS complied



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P156KD18J	DIP	18	300 mil
EM78P156KSO18J	SOP	18	300 mil
EM78P156KJSS20J	SSOP	20	209 mil

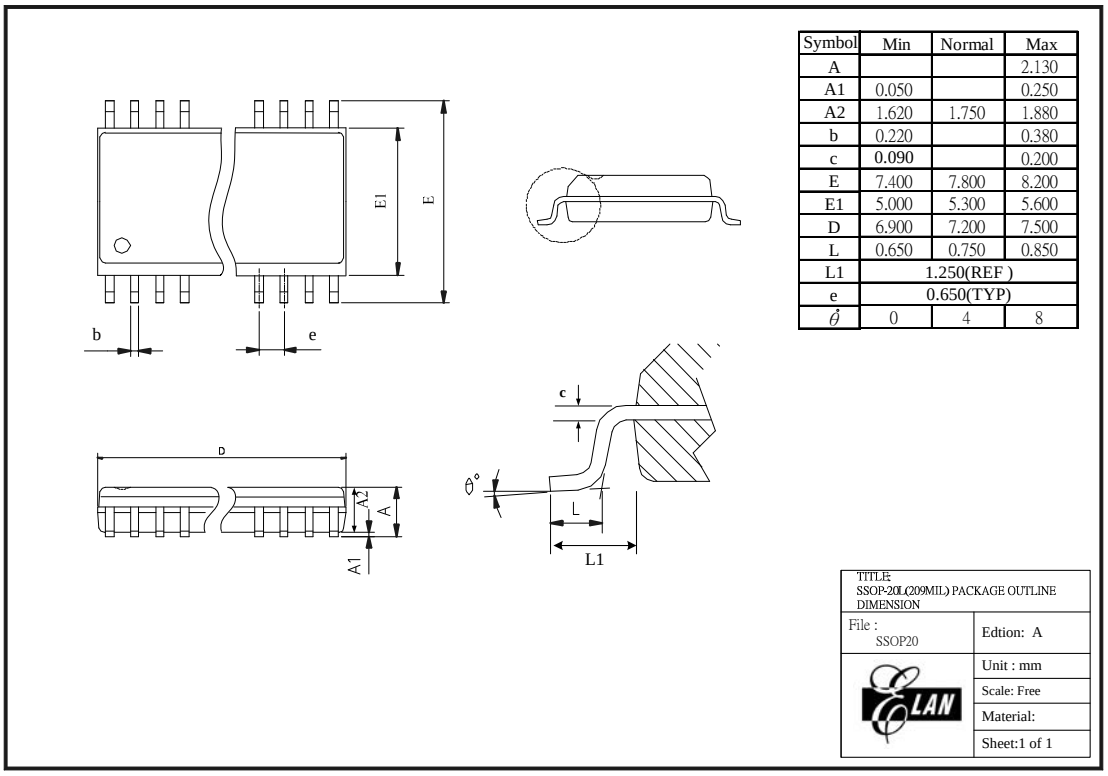
For product code "J".

These are Green products and comply with RoHS specifications

Part No.	EM78P156K
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8 ~ 10
Elongation (%)	> 50%

C Package Information

■ **20-Lead Shrink Small Outline Package (SSOP) — 209 mil**

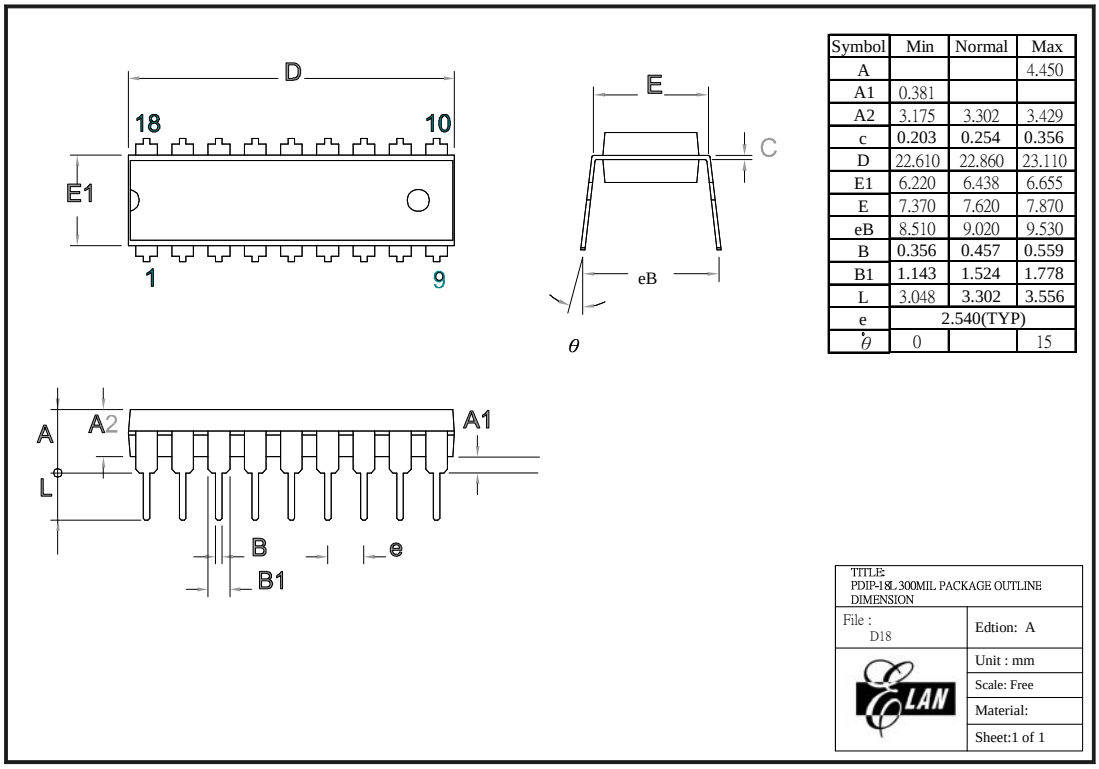


Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ	0	4	8

TITLE: SSOP-20L(209MIL) PACKAGE OUTLINE DIMENSION	
File : SSOP20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1a EM78P156K 20-Lead SSOP Package Type

■ **18-Lead Plastic Dual In–line Package (DIP) — 300 mil**

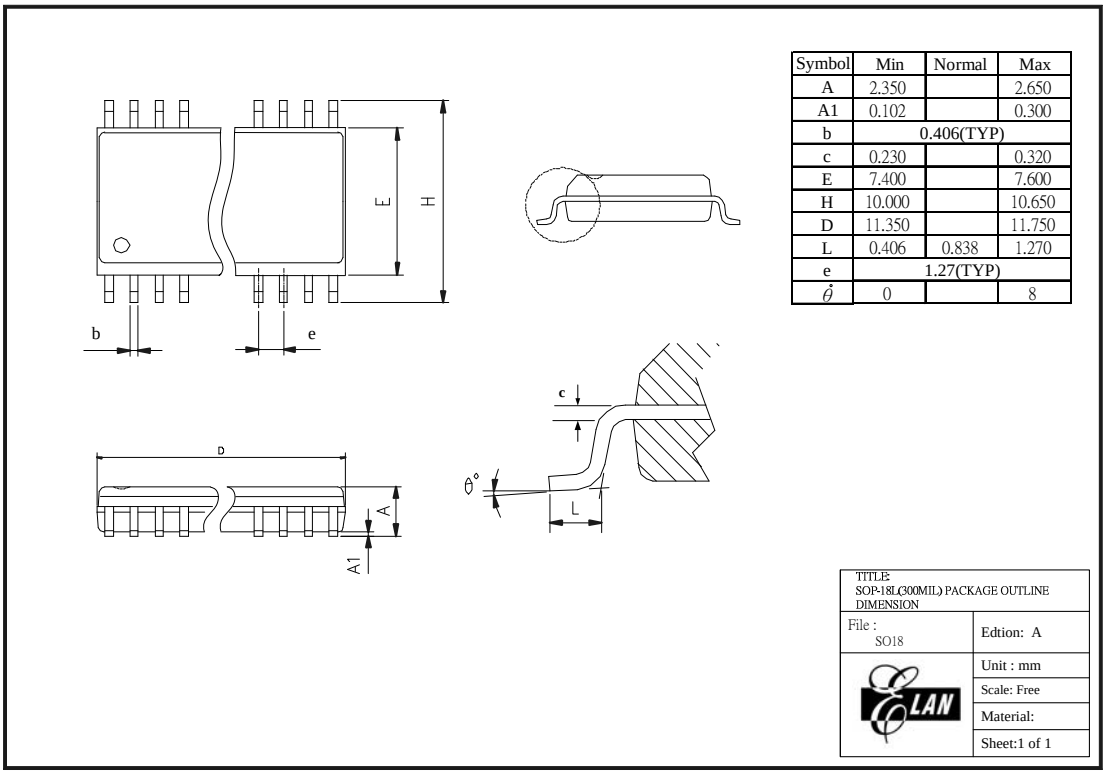


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
File : D18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1c EM78P156K 18-Lead DIP Package Type

■ 18-Lead Small Outline Package (SOP) — 300 mil



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ	0		8

TITLE:
SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO18 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-1d EM78P156K 18-Lead SOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature = 245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min) ~ 150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance) = 24 hrs	
	Step 3: Soak at 30°C / 60%, TD (endurance) = 192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ---- 225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ---- 240 ± 5°C)	
Temperature cycle test	-65°C (15 min) ~ 150°C (15 min), 200 cycles	–
Pressure cooker test	T_A = 121°C, RH = 100%, pressure = 2 atm, TD (endurance) = 96 hrs	–
High temperature / High humidity test	T_A = 85°C , RH = 85%, TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	T_A = 150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	T_A = 125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	T_A = 25°C, VCC = Max. operating voltage, 800mA / 40V	–
ESD (HBM)	T_A = 25°C, ≥ | ± 4kV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	T_A = 25°C, ≥ | ± 400V |	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.