EM78P372N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
Shenzhen Hi-tech Industrial Park
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
ELAN Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5 Bibo Road
Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai,
CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2010/06/21
0.91	Preliminary version	2010/07/19
0.92	Modified the IOCC0 Control Register Modified the Bank 1-RF[3:0] Control Reigster Modified the Bank 0-RA[2:0] Control Reigster	2010/08/06
1.0	Initial Version Modified the Operating frequency range (DC ~ 16 MHz)	2010/12/10
1.1	1. Modified the Electrical Characteristics 2. Modified the Quality Assurance and Reliability section in the Appendix.	2011/05/24
1.2	1. Added the EM78P372NQN16S Package Type 2. Deleted the EM78P372NSS10J/S Package Type. 3. Fixed the number of I/O discription in the Features section. 4. Added Ordering and Manufacturing Information. 5. Modified the instruction table 6. Modified the Part Number 7. Modifed the description about POR and LVR in the Features section	2012/02/09
1.3	1. Added new note items to the existing ones in Section 6.1.9 and Section 6.7.1.3. 2. Reorganized the grouping of the graphs in Section 8.5. 3. Modified the PWM System Block Diagram in Section 6.8.1.	2015/02/09
1.4	1. Modified the package type in Section 2 Features 2. Added User Application Note 3. Modified Appendix A “Ordering and Manufacturing Information” 4. Modified Section 6.7.4 AD Conversion Time. 5. Modified Section 6.8.2 Increment Timer Counter.	2016/03/15

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. The PWM output will not be set, if the duty cycle is “0”.

2. The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to “SLEP” instruction, if the ADWE bit of the RE register is enabled, the TCC will keep on running.

3. During ADC conversion, do not perform output instruction to maintain precision for all of the pins. In order to obtain accurate values, it is necessary to avoid any data transition on I/O pins during AD conversion

4. When using operational amplifier:
   (1) The CMPIE (IOCE0.4), CMPWE (RE.2), and CMPIF (RE.4) bits are invalid.
   (2) The comparator interrupt is invalid.
   (3) The comparator wake-up is invalid.

5. The noise rejection function is turned off in the LXT2 and sleep mode

1 General Description

The EM78P372N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 2K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P372N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip ROM
  - 80×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V/4 MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports: P5, P6, P7
  - 18 I/O pins
  - Wake-up port : P5
  - 8 programmable pull-down I/O pins (P50 ~ P57)
  - 16 programmable pull-high I/O pins (P50 ~ P57) (P60 ~ P67)
  - 8 programmable open-drain I/O pins (P60 ~ P67)
  - 14 programmable high-sink current I/O pins (P51 ~ P54, P56 ~ P57) (P60 ~ P67)
  - External interrupt : P60
- Operating voltage range:
  - 2.1V~5.5V at 0°C~70°C (commercial)
  - 2.3V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (based on 2 clocks):
  - Crystal mode: DC ~ 16 MHz, 4.5V; DC ~ 8 MHz, 3V; DC ~ 4 MHz, 2.1V
  - ERC mode: DC ~ 2 MHz, 2.1V;
  - IRC mode
    Oscillation mode: 16 MHz, 4 MHz, 1 MHz, 8 MHz

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%
16 MHz	±2%	±1% *(4.5~5.5V)	±2%	±5%
8 MHz	±2%	±1% *(3.0~5.5V)	±2%	±5%
1 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%

* Operating voltage range

- All the four main frequencies can be trimmed by programming with six calibrated bits in the ICE300N Simulator. OTP is auto trimmed by ELAN Writer.
- Fast set-up time requires only 0.8ms (VDD: 5V Crystal: 4 MHz, C1/C2: 15pF) in XT mode and 10 μs in IRC mode (VDD: 5V, IRC: 4 MHz)
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 4 programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.2V
  - Power on reset and programmable level voltage reset POR: 1.8V (Default), LVR: 4.0V, 3.5V, 2.7V
  - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - One pair of comparator or OP(offset voltage: smaller than 10mV)
  - Two Pulse Width Modulation (PWM) with 8-bit resolution
- Ten available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - Comparator status change interrupt
  - Low voltage detect (LVD) interrupt
  - PWM1~2 period match interrupt
  - PWM1~2 duty match interrupt
- Special Features:
  - Programmable free running Watchdog Timer (4.5ms : 18ms)
  - Power saving Sleep mode
  - Power-on voltage detector available
  - High EFT immunity (better performance at 4 MHz or below)
- Package Type:
  - 10-pin MSOP 118mil : EM78P372NMS10
  - 14-pin DIP 300mil : EM78P372ND14
  - 14-pin SOP 150mil : EM78P372NSO14
  - 16-pin SOP 150mil : EM78P372NSO16A
  - 18-pin DIP 300mil : EM78P372ND18
  - 18-pin SOP 300mil : EM78P372NSO18
  - 20-pin DIP 300mil : EM78P372ND20
  - 20-pin SOP 300mil : EM78P372NSO20
  - 20-pin SSOP 209mil : EM78P372NSS20
  - 16-pin QFN 3×3×0.8mm : EM78P372NQN16

Note: *These are Green products that do not contain hazardous substances.*

3 Pin Assignment

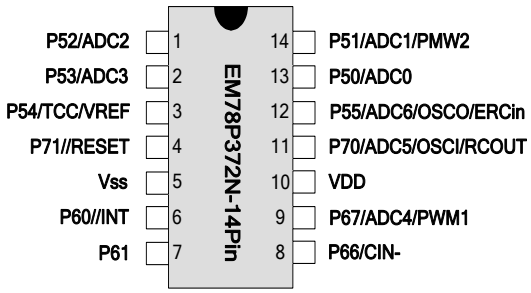


Figure 3-1 EM78P372ND14/SO14

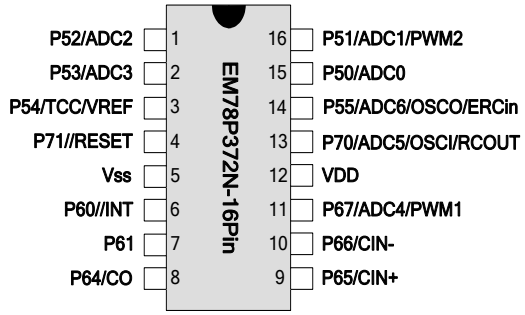


Figure 3-2 EM78P372NSO16A

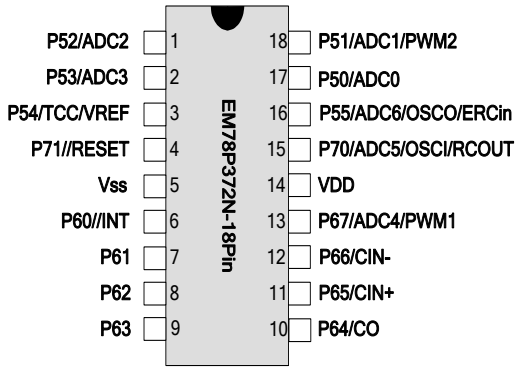


Figure 3-3 EM78P372ND18/SO18

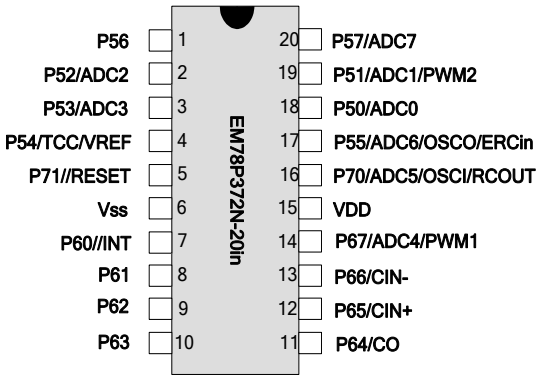


Figure 3-4 EM78P372ND20/SO20/SS20

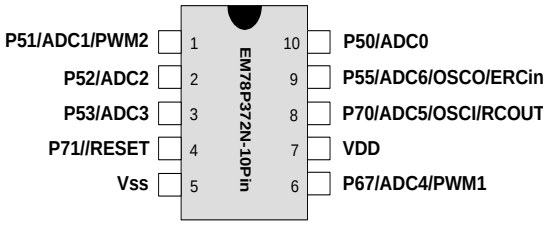


Figure 3-5 EM78P372NMS10

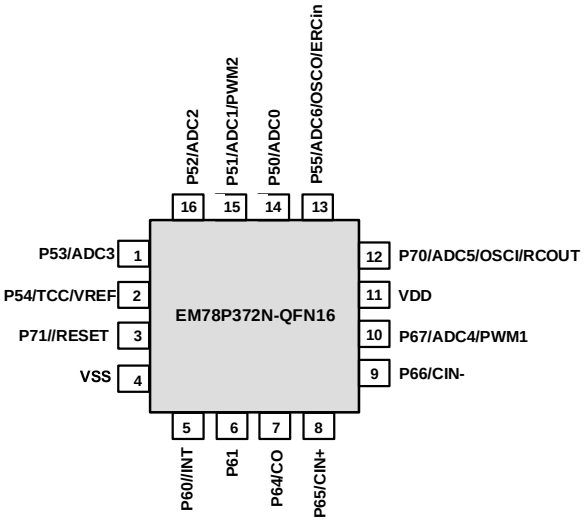


Figure 3-6 EM78P372NQN16

4 Pin Description

Name	Function	Input Type	Output Type	Description
P50	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC0	AN	–	ADC Input 0
P51	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC1	AN	–	ADC Input 1
	PWM2	–	CMOS	PWM2 output
P52	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC2	AN	–	ADC Input 2
P53	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC3	AN	–	ADC Input 3
P54	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	TCC	ST	–	Real Time Clock/Counter clock input
	VREF	AN	–	ADC external voltage reference
P55	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC6	AN	–	ADC Input 6
	OSCO	–	XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN	–	External RC input pin
P56	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
P57	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC7	ST	–	ADC Input 7
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	/INT	ST	–	External interrupt pin

Name	Function	Input Type	Output Type	Description
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
P64/CO	P64	–	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CO	ST	–	Comparator output
P65/CIN+	P65	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CIN+	ST	–	Non-inverting end of comparator
P66/CIN-	P66	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CIN-	ST	–	Inverting end of comparator
P67/ADC4/PWM1	P67	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	ADC4	AN	–	ADC Input 4
	PWM1	–	CMOS	PWM1 output
P70/ADC5/OSCI/ RCOUT	P70	P70	–	Bidirectional I/O pin
	ADC5	AN	–	ADC Input 5
	OSCI	XTAL	–	Clock input of crystal/ resonator oscillator
	ROCUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P71	P71	ST	CMOS	Bidirectional I/O pin (open-drain)
	/RESET	ST	–	System reset pin (should be external pull-high)
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: *ST: Schmitt Trigger input* *AN: analog pin*

XTAL: oscillation pin for crystal/resonator *CMOS: CMOS output*

5 Block Diagram

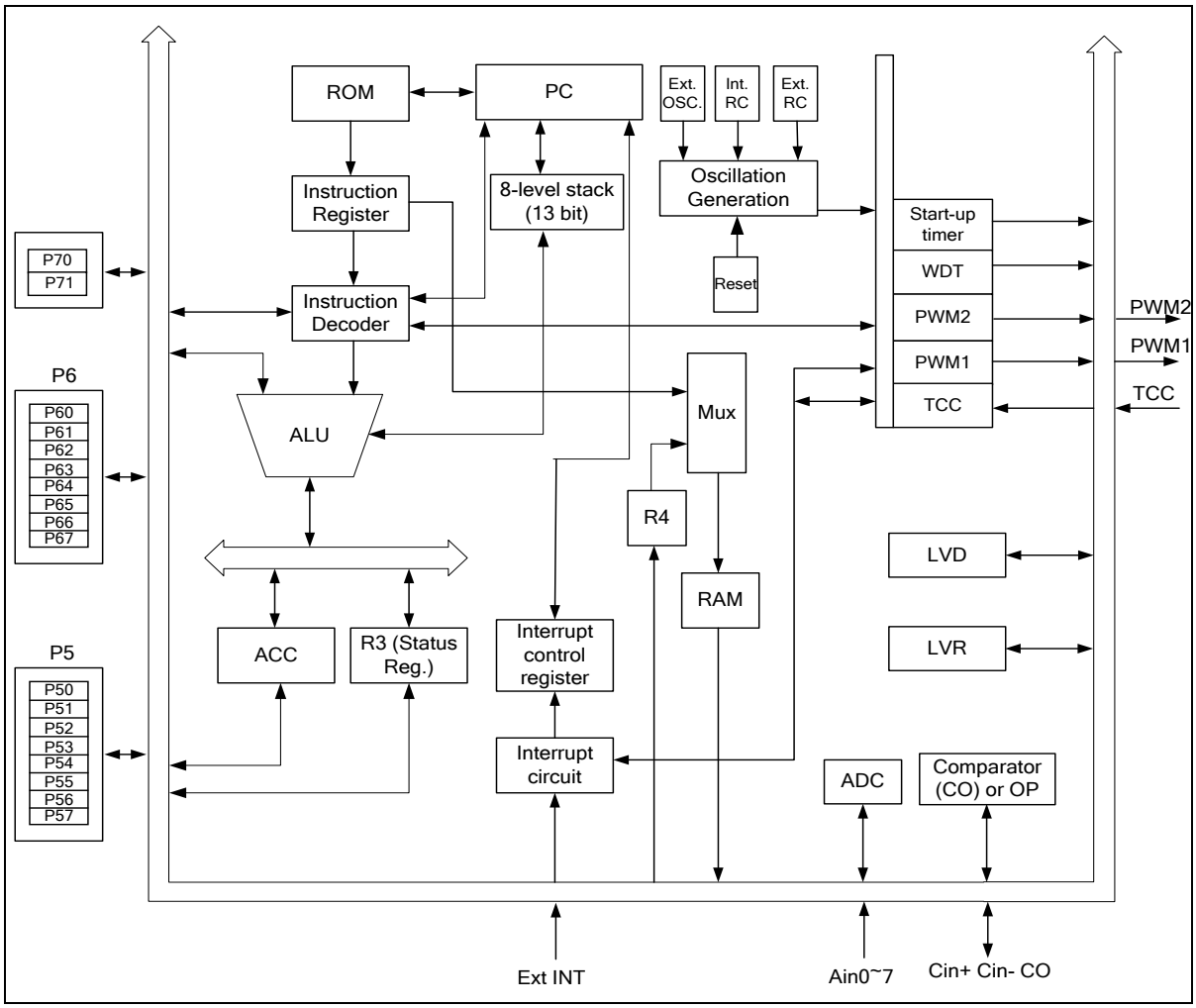


Figure 5-1 EM78P372N Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge which is defined by the TE bit (CONT-5) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- The TCC prescaler counter is assigned to TCC
- The contents of the CONT register is cleared whenever –
  - a value is written to the TCC register
  - a value is written to the TCC prescaler bits (Bits 3, 2, 1, 0 of the CONT register)
  - there's power-on reset, /RESET, or WDT time out reset

6.1.3 R2 (Program Counter) and Stack

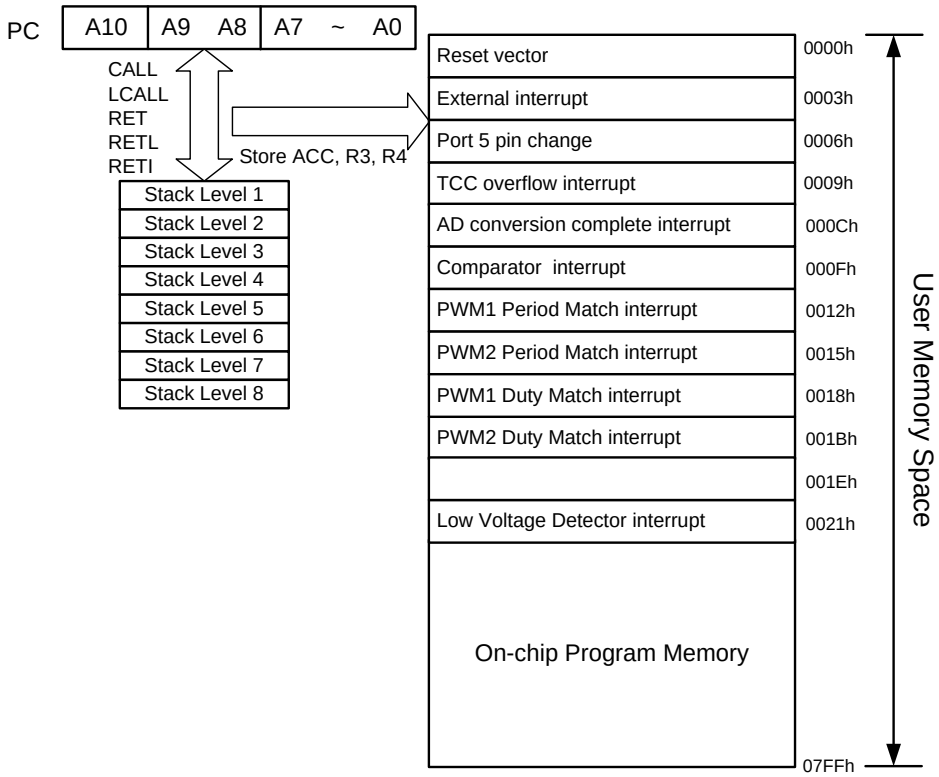


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 11-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration*.
- The configuration structure generates 2K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the program counter bits (A0~A10). Therefore, "LJMP" allows the PC to jump to any location within 2K (2^{11}).
- "LCALL" instruction loads the program counter bits (A0 ~A10), and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11})
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2, A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles.

6.1.3.1 Data Memory Configuration

Address	*Register Bank 0*	*Register Bank 1*	*IOC Page 0*	*IOC Page 1*
00	R0 (Indirect Addressing Register)			
01	R1 (Timer Clock Counter)			
02	R2 (Program Counter)			
03	R3 (Status Register)			
04	R4 (RSR, Bank select)			
05	R5 (Port 5 I/O data)	R5 (TBHP: Table Point Register)	IOC50 (Port 5 I/O control)	IOC51 (HSCR1: High Sink Control Register 1)
06	R6 (Port 6 I/O data)	R6 (TBLP: Table Point Register)	IOC60 (Port 6 I/O control)	IOC61 (HSCR2: High Sink Control Register 2)
07	R7 (Port 7 I/O data)	R7 (PWMCON: PWM Control Register)	IOC70 (Port 7 I/O control)	IOC71 (HDCR1: High Driver Control Register 1)
08	R8 (ADC Input Select Register)	R8 (TMRCON: Timer Control Register)	IOC80 (Comparator Control Register)	IOC81 (HDCR2: High Driver Control Register 2)
09	R9 (ADC Control Register)	R9 (PRD1: PWM1 Time Period)	IOC90 (TMR1: PWM1 Timer)	IOC91 (Reserved)
0A	RA (ADC Offset Calibration Register)	RA (PRD2: PWM2 Time Period)	IOCA0 ((TMR2: PWM2 Timer)	IOCA1 (Reserved)
0B	RB (Converted value AD11~AD4 of ADC)	RB (DT1: PMW1 Duty Cycle)	IOCB0 (Pull-down Control Register)	IOCB1 (Reserved))
0C	RC (Converted value AD11~AD8 of ADC)	RC (DT2: PMW2 Duty Cycle)	IOCC0 (Open-drain Control Register)	IOCC1 (Reserved))
0D	RD (Converted value AD7~AD0 of ADC)	RD (Reserved)	IOCD0 (Pull-high Control Register)	IOCD1 (Reserved)
0E	RE (Interrupt Status 2 and Wake-up Control Register 1)	RE (LVD Control and Wake-up Control Register 2)	IOCE0 (WDT Control Register and Interrupt Mask Register 2)	IOCE1 (Reserved)
0F	RF (Interrupt Status Register 1)	RF (Mode Select and IRC Switch Register)	IOCF0 (Interrupt Mask Register 1)	IOCF1 (Pull-high Control Register)
10 : 1F	16-Byte Common Register			
20 : 3F	Bank 0 32x8	Bank 1 32x8		

Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	–	T	P	Z	DC	C

Bit 7 (RST): Bit of reset type

Set to “1” if wake-up from sleep on pin change, comparator status change, or AD conversion completed. Set to “0” if wake-up from other reset types.

Bit 6 (IOCS): Select the Segment of IO control register

0: Segment 0 (IOC50 ~ IOCF0) selected

1: Segment 1 (IOC51 ~ IOCC1) selected

Bit 5: Not used, set to “0” at all time.

Bit 4 (T): Time-out bit. Set to “1” by the "SLEP" and "WDTC" commands or during power on**,** and reset to “0” by WDT time-out (for more details, see Section 6.5.2, *The T and P Status under Status Register*).

Bit 3 (P): Power-down bit. Set to “1” during power-on or by a "WDTC" command and reset to “0” by a "SLEP" command (see Section 6.5.2, *The T and P Status under Status Register* for more details).

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7 (SBANK): Special Register 0x05~0x0F bank selection bit.

Bit 6 (BANK): Used to select Bank 0 or Bank 1 of the register

Bits 5 ~ 0: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode.

See the table under Section *6.1.3.1 Data Memory Configuration*.

6.1.6 Bank 0 R5 ~ R7 (Port 5 ~ Port 7)

R5 and R6, P70 and P71 are I/O registers.

6.1.7 Bank 0 R8 (AISR: ADC Input Select Register)

The AISR register individually defines the I/O Port as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P57 pin

0: Disable ADC7, P57 functions as I/O pin

1: Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0: Disable ADC6, P55 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0: Disable ADC5, P70 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P67 pin

0: Disable ADC4, P67 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0: Disable ADC3, P53 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0: Disable ADC2, P52 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable ADC1, P51 functions as I/O pin

1: Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable ADC0, P50 functions as I/O pin

1: Enable ADC0 to function as analog input pin

NOTE

The P55/ADC6/OSCO/ERCin pin cannot be applied to OSCO and ADC6 at the same time. If P55/ADC6/OSCO/ERCin functions as OSCO oscillator input pin, then ADE6 bit for R8 must be "0" and ADIS2~0 do not select "110". The P55/ADC6/OSCO/ERCin pin priority is as follows:

:

P55/ADC6/OSCO/ERCin Pin Priority		
High	Medium	Low
OSCO/ERCin	ADC6	P55

The P70/ADC5/OSCI/RCOUT pin cannot be applied to OSCI and ADC5 at the same time. If P70/ADC5/OSCI/RCOUT acts as OSCI oscillator input pin, then ADE5 bit for R8 must be "0" and ADIS2~0 do not select "101". The P70/ADC5/OSCI/RCOUT pin priority is as follows:

P70/ADC5/OSCI/ROCUT Pin Priority		
High	Medium	Low
OSCI/RCOUT	ADC5	P70

The P67/ADC4/PWM1 pin cannot be applied to PWM1 and ADC4 at the same time. If P67/ADC4/PWM1 functions as ADC4 analog input pin, then the P67/ADC4/PWM1 pin priority is as follows:

P67/ADC4/PWM1 Pin Priority		
High	Medium	Low
ADC4	PWM1	P67

The P51/ADC1/PWM2 pin cannot be applied to PWM2 and ADC1 at the same time. If P51/ADC1/PWM2 functions as ADC1 analog input pin, then the P51/ADC1/PWM2 pin priority is as follows:

P51/ADC1/PWM2 Pin Priority		
High	Medium	Low
ADC1	PWM2	P51

The P50/ADC0 pin cannot be applied to ADC0 at the same time. If P50/ADC0 functions as ADC0 analog input pin, then the P50/ADC0 pin priority is as follows:

P50/ADC0 Pin Priority	
High	Low
ADC0	P50

6.1.8 Bank 0 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the VREF/TCC/P54 pin carries out the function of P54 (default)

1: The Vref of the ADC is connected to VREF/TCC/P54

NOTE

- *The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time. If P54/TCC/VREF functions as VREF analog input pin, then CONT Bit 5 "TS" must be "0".*
- *The VREF/TCC/P54 Pin Priority is as follows:*

P54/TCC/VREF Pin Priority		
High	Medium	Low
VREF	TCC	P54

Bit 6 and Bit 5 (CKR1 and CKR0): ADC Clock Rate Select

00 = 1 **:** 16 (default value)

01 = 1 **:** 4

10 = 1 **:** 64

11 = 1 **:** 1

Bit 4 (ADRUN): ADC starts to RUN

0: on completion of the conversion Reset by hardware. This bit cannot be reset through software (default)

1: an A/D conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power

0: ADC is in power down mode (default)

1: ADC is operating normally

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

ADICS	ADIS2	ADIS1	ADIS0	Analog Input Select
0	0	0	0	ADIN0/P50
0	0	0	1	ADIN1/P51
0	0	1	0	ADIN2/P52
0	0	1	1	ADIN3/P53
0	1	0	0	ADIN4/P67
0	1	0	1	ADIN5/P70
0	1	1	0	ADIN6/P55
0	1	1	1	ADIN7/P57
1	0	X	X	OPOUT
1	1	X	X	Internal 1/4 VDD

These bits can only be changed when the ADIF bit and the ADRUN bit are both low. See Section 6.1.13, *RE (Interrupt Status 2 and Wake-up Control Register)*.

6.1.9 Bank 0 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable Calibration (default)

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of the offset voltage

0: Negative voltage (default)

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P372N
0	0	0	0LSB
0	0	1	2LSB
0	1	0	4LSB
0	1	1	6LSB
1	0	0	8LSB
1	0	1	10LSB
1	1	0	12LSB
1	1	1	14LSB

Bit 2 ~ Bit 1 (VREF1 ~ VREF0): ADC internal reference voltage source

VREF1	VREF0	ADC Internal Reference Voltage
0	0	VDD (default)
0	1	4.0V ± 1%
1	0	3.0V ± 1%
1	1	2.0V ± 1%

NOTE

- *If VREF [1:0]=00, the internal reference will not turn on. If VREF[1 :0]≠ 00, the internal reference will turn on automatically. Moreover, the power of the internal reference is irrelevant to ADC.*
- *When using internal voltage reference for the first time, user needs to wait for at least 50 µs to enable and stabilize the voltage reference. Unstable reference will result to inaccurate conversion. On subsequent switching of the voltage reference, user only needs to wait for at least 6µs for stabilization.*
- *If ADC uses internal VREF 2V function, the resulting conversion data will be inaccurate. So user must ensure that the minimum analog reference voltage of AD electrical characteristics is not less than 2.5V.*

Bit 0 (ADICS): ADC Internal Channel Select (select ADC internal 1/4 VDD or OP output pin connected to ADC input)

0: Disable (default)

1: Enable

6.1.10 Bank 0 RB (ADDATA: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.13, Bank 0 *RE (Interrupt Status 2 and Wake-up Control Register)*.

RB is read only.

6.1.11 Bank 0 RC (ADDATA1H: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
“0”	“0”	“0”	“0”	AD11	AD10	AD9	AD8

When AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.13, *Bank 0 RE (Interrupt Status 2 and Wake-up Control Register*).

RC is read only.

6.1.12 Bank 0 RD (ADDATA1L: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.13, *RE (Interrupt Status 2 and Wake-up Control Register*).

RD is read only

6.1.13 Bank 0 RE (Interrupt Status Register 2 and Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE

Note: *1. RE <6, 5, and 4> can be cleared by instruction but cannot be set.*
2. IOCE0 is the interrupt mask register.
3. Reading RE will result to "Logic AND" of the RE and IOCE0.

Bit 7 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected

1: Low voltage is not detected or LVD function is disabled (default)

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag

LVDIF is reset to "0" by software.

Bit 5 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

0: no interrupt occurs (default)

1: interrupt request

Bit 4 (CMPIF): Comparator Interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

0: no interrupt occurs (default)

1: interrupt request

Bit 3 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up (default)

1: Enable ADC wake-up

When AD Conversion enters sleep/idle mode, this bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

0: Disable Comparator wake-up (default)

1: Enable Comparator wake-up

When the Comparator enters sleep/idle mode, this bit must be set to "Enable".

Bit 1 (ICWE): Port 5 input change to wake-up status enable bit

0: Disable Port 5 input change to wake-up status (default)

1: Enable Port 5 input change to wake-up status

When Port 5 change enters sleep/idle mode, this bit must be set to "Enable".

Bit 0 (LVDWE): Low Voltage Detect wake-up enable bit

0: Disable Low Voltage Detect wake-up (default)

1: Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter an interrupt vector or to wake-up the IC from sleep/idle with Low Voltage Detect running, the LVDWE bit must be set to "Enable".

6.1.14 Bank 0 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	ICIF	TCIF

Note: *1. "1" means there is interrupt request, "0"*
2. RF can be cleared by instruction but cannot be set.
3. IOCF0 is the interrupt mask register.
4. Reading RF will result to "logic AND" of the RF and IOCF0

Bit 7: Not used. Set to "0" all the time.

Bit 6 (DT2IF): PWM2 Duty Interrupt flag. Set when PWM2 Duty Match. Reset by software.

Bit 5 (DT1IF): PWM1 Duty Interrupt flag. Set when PWM1 Duty Match. Reset by software.

Bit 4 (PWM2IF): PWM2 Period Interrupt flag. Set when PWM2 period match. Reset by software.

Bit 3 (PWM1IF): PWM1 Period Interrupt flag. Set when PWM1 period match. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.

Bit 1 (ICIF): Port 5 input status change interrupt flag. Set when Port 5 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.15 Bank 1 R5 (TBHP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	RBit10	RBit9	RBit8

Bit 7 (MLB): Chooses the MSB or LSB machine code to move into the register.

The machine code is pointed by TBLP and TBHP register.

Bit 6 ~ Bit 3: Not used. Set to "0" at all time.

Bit 2 ~ Bit 0: Most 3 significant bits of address for program code

6.1.16 Bank 1 R6 (TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bit 7 ~ Bit 0: These are the least 8 significant bits of address for program code.

6.1.17 Bank 1 R7 (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	PWMCAS	PWM2E	PWM1E

Bit 7~ Bit 3: Not used bits. Read as "**0**" all the time

Bit 2 (PWMCAS): PWM Cascade Mode

0: Two Independent 8-bit PWM functions (default value)

1: 16-bit PWM Mode (Cascaded from two 8-bit ones)

Bit 1 (PWM2E): PWM2 enable bit

0: PWM2 is off (default value), and its related pin carries out the P51 function.

1: PWM2 is on, and its related pin is automatically set to output.

Bit 0 (PWM1E): PWM1 enable bit

0: PWM1 is off (default value), and its related pin carries out the P67 function.

1: PWM1 is on, and its related pin is automatically set to output.

6.1.18 Bank 1 R8 (TMRCON: Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

Bit 7 (T2EN): TMR2 enable bit

0: TMR2 is off (default value)

1: TMR2 is on

Bit 6 (T1EN): TMR1 enable bit

0: TMR1 is off (default value)

1: TMR1 is on

Bit 5 ~ Bit 3 (T2P2 ~ T2P0): TMR2 clock prescaler option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.19 Bank 1 R9 (PRD1: PWM1 Time Period)

The content of Bank 1-R9 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

6.1.20 Bank 1 RA (PRD2: PWM2 Time Period)

The content of Bank 1-RA is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

6.1.21 Bank 1 RB (DT1: PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

6.1.22 Bank 1 RC (DT2:PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

6.1.23 Bank 1 RE (LVD Interrupt and Wake-up Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE

Bit 7 (LVDIE): Low voltage detector interrupt enable bit

0: Disable the low voltage detector interrupt (default)

1: Enable the low voltage detector interrupt

NOTE

■ *When the detected low level voltage is used to enter an interrupt vector or enter the next instruction, the LVDIE bit must be set to "Enable".*

Bit 6 (LVDEN): Low voltage detector enable bit

0: Disable the Low voltage detector function (default)

1: Enable the Low voltage detector function

Bit 5 ~ Bit 4: Low voltage detector level bits

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11 **(default)**	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	N/A	1

NOTE

IF Vdd has crossover at LVD voltage in interrupt level as VDD varies, LVD interrupt will occur.

Bit 3 ~ Bit 1: Not used. Set to “0” at all time.

Bit 0 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up (default)

1: Enable External /INT pin wake-up

6.1.24 Bank 1 RF (System Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0

Bit 7: Not used, fixed to "0" all the time.

Bit 6 (TIMERSC): TCC, PWM1, PWM2 clock source select.

0: Fs is used as Fc

1: Fm is used as Fc (default)

Bit 5 (CPUS): CPU Oscillator Source Select

0: Fs : sub frequency for WDT internal RC time base is 16kHz

1: Fm : main oscillator (Fm) (default)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

From SLEP instruction, this bit will determine as to which mode to activate.

0: IDLE = ‘0’ + SLEP instruction → sleep mode (default)

1: IDLE = ‘1’ + SLEP instruction → idle mode

■ CPU Operation Mode

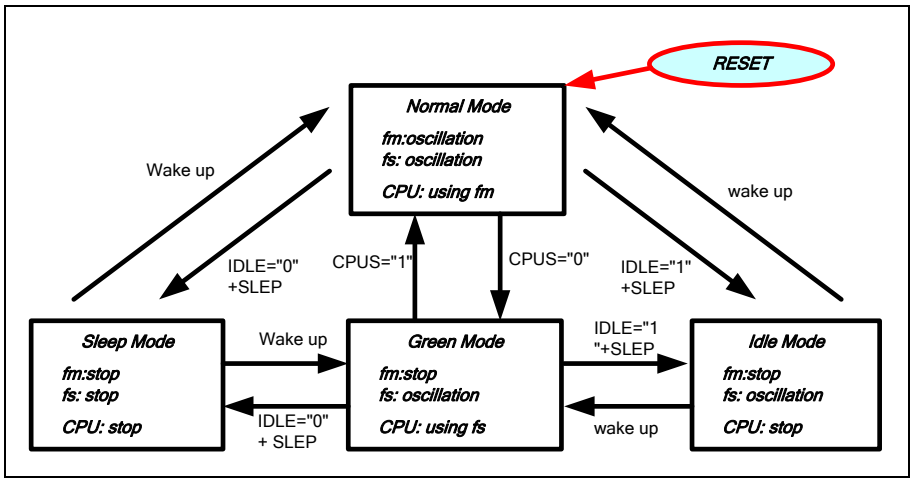


Figure 6-3 CPU Operation Mode Diagram

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S)[1]	Count from Normal/Green (CLK)[2]
Crystal 1M ~ 16 MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	510 CLK
	Green → Normal		510 CLK
	Sleep/Idle → Green	< 100 µs	8 CLK
ERC 2 MHz	Sleep/Idle → Normal	< 5 µs	8 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC 1M, 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	8 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

NOTE

- *[1]The oscillator stable time depends on the oscillator characteristics.*
- *[2]After the oscillator has stabilized, the CPU will count 510/8 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1 : The 4 MHz IRC wakes-up from Sleep mode to Normal mode, the total wake-up time is 2 µs + 8 CLK @ 4 MHz.

Ex 2 : The 4 MHz IRC wakes-up from Sleep mode to Green mode, the total wake-up time is 100 µs + 8 CLK @ 16kHz.

Bit 3 ~ Bit 2 (SHS1 ~ SHS0): Sample and Hold Timing Select
(Recommend at least 4μs, T_{AD}: Period of ADC Operating Clock).

SHS1	SHS0	Sample and Hold Timing(TAD)
0	0	2 x T_{AD}
0	1	4 x T_{AD}
1	0	8 x T_{AD}
1	1	12 x T_{AD} (default)

Bits 1 ~ 0 (RCM1 ~ RCM0): IRC mode select bits.

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

Bank 1 RF<1, 0> will be enabled.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 μs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 μs
16 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 μs
	1	**0**	**16 MHz ± 2%**	4.5V ~ 5.5V	< 1.25 μs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 μs
8 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 μs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	0	**1**	**8 MHz ± 2%**	3.0V ~ 5.5V	< 2.5 μs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 μs
1 MHz	1	1	4 MHz ± 10%	2.1V ~ 5.5V	< 6 μs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	0	**0**	**1 MHz ± 2%**	2.1V ~ 5.5V	< 20 μs

NOTE

- *The initial values of Bank 1 RF<1, 0> will be kept the same as Word 1<6,5>.*
- *If user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

For Example:

1st step When user selects the 4 MHz at the Writer, the initial values of Bank 1 RF<1,0> would be "11", the same as the value of Word 1<6,5> which is "11".

If the MCU is free-running, it will work at 4 MHz ± 2%. Refer to the table below.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 µs

2nd step If it is desired to set Bank 1 RF<1,0> = "10" while the MCU is working at 4 MHz ± 2%, the MCU needs to hold for 1.5 µs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	1	1	4 MHz ± 2%	2.1V ~ 5.5V	< 5 µs
	1	**0**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 µs

3rd step If it is desired to set Bank 1 RF<1,0> = "00" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 24 µs, then it will continue to work at 1 MHz ± 10%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	1	1	4 MHz ± 2%	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	**0**	**1 MHz ± 10%**	2.1V ~ 5.5V	< 24 µs

4th step If it is desired to set Bank 1 RF<1,0> = "11" while the MCU is working at 1 MHz ± 10%, the MCU needs to hold for 5 µs, then it will continue to work at 4 MHz ± 2%.

Writer Trim IRC	Bank 1 RF<1,0>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**1**	**1**	**4 MHz ± 2%**	2.1V ~ 5.5V	< 5 µs
	1	0	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	0	1	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	0	0	1 MHz ± 10%	2.1V ~ 5.5V	< 24 µs

6.1.25 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Note: *The CONT register is both readable and writable. Bit 6 is read only.*

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at the rising edge of the INT pin

1: Interrupt occurs at the falling edge of the INT pin

Bit 6 (INT): Interrupt Enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock. If P54 is used as I/O pin

1: Transition on the TCC pin

Bit 4 (TE): TCC signal edge

0: Increment if the transition from low to high takes place on the TCC pin

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set as Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: Tcc Time-out period [1/FT x prescaler x (256 – Tcc cnt) x 1
Where FT = Fm or Fs, determined by Bank 1 RF TIMERSC bit.

6.2.3 IOC50 ~ IOC70 (I/O Port Control Register)

"**0**" defines the relative I/O pin as output

"**1**" sets the relative I/O pin into high impedance

6.2.4 IOC80 (Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	CMPOUT	COS1	COS0	–	–	–

Note: *Bits 4~0 of the IOC80 register are both readable and writable.*
Bit 5 of the IOC80 register is read only.

Bit 7 and Bit 6: Not used. Set to “0” all the time.

Bit 5 (CMPOUT): Result of the comparator output. This bit is readable only.

Bit 4 and Bit 3 (COS1 and COS0): Comparator/OP Select bits

COS1	COS0	Function Description
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin
0	1	P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	P65 and P66 are Comparator input pins and P64 is Comparator output pin (CO)
1	1	Used as OP and P64 is OP output pin (CO)

Bits 2 ~ 0: Not used. Set to “0” all the time.

6.2.5 IOC90 (TMR1: PWM1 Timer)

6.2.6 IOCA0 (TMR2: PWM2 Timer)

6.2.7 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

The **IOCB0** register is both readable and writable.

Bit 7 (/PD57): Control bit used to enable internal pull-down of the P57 pin.

0: Enable internal pull-down

1: Disable internal pull-down (default)

Bit 6 (/PD56): Control bit used to enable internal pull-down of the P56 pin.

Bit 5 (/PD55): Control bit used to enable internal pull-down of the P55 pin.

Bit 4 (/PD54): Control bit used to enable internal pull-down of the P54 pin.

Bit 3 (/PD53): Control bit used to enable internal pull-down of the P53 pin.

Bit 2 (/PD52): Control bit used to enable internal pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable internal pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable internal pull-down of the P50 pin.

6.2.8 IOCC0 (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

The IOCC0 register is both readable and writable.

Bit 7 (OD67): Control bit used to enable open-drain output of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain output of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain output of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain output of the P64 pin.

Bit 3 (OD63): Control bit used to enable open-drain output of the P63 pin.

Bit 2 (OD62): Control bit used to enable open-drain output of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain output of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin.

6.2.9 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

The **IOCD0** register is both readable and writable.

Bit 7 (/PH57): Control bit used to enable internal pull-high of the P57 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable internal pull-high of the P56 pin.

Bit 5 (/PH55): Control bit used to enable internal pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable internal pull-high of the P54 pin.

Bit 3 (/PH53): Control bit used to enable internal pull-high of the P53 pin.

Bit 2 (/PH52): Control bit used to enable internal pull-high of the P52 pin.

Bit 1 (/PH51): Control bit used to enable internal pull-high of the P51 pin.

Bit 0 (/PH50): Control bit used to enable internal pull-high of the P50 pin.

6.2.10 IOCE0 (WDT Control Register and Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable Watchdog Timer

0: Disable WDT (default)

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC60) must be set to "1".

NOTE

- *When EIS is "0", the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6). Refer to Figure 6-5 (I/O Port and I/O Control Register Circuit for P60 (/INT)) under Section 6.4 (I/O Ports).*
- *EIS is both readable and writable.*

Bit 5 (ADIE): ADIF interrupt enable bit

0: disable ADIF interrupt

1: enable ADIF interrupt

Bit 4 (CMPIE): CMPIF interrupt enable bit

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit, WDT rate is 1:1

1: Prescaler enable bit, WDT rate is set at Bit 2 ~ Bit 0

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	ICIE	TCIE

Note: *The IOCF0 register is both readable and writable.*

Individual interrupt is enabled by setting to "1" its associated control bit in the IOCF0 and in IOCEO Bits 4 and 5.

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-7 Interrupt Input Circuit under Section 6 Interrupt.

Bit 7: Not used. Set to "0" at all time.

Bit 6 (DT2IE): DT2IE interrupt enable bit

0: Disable DT2IF interrupt

1: Enable DT2IF interrupt

Bit 5 (DT1IE): DT1IE interrupt enable bit

0: Disable DT1IF interrupt

1: Enable DT1IF interrupt

Bit 4 (PWM2IE): PWM2IE interrupt enable bit

0: Disable PWM2IF interrupt

1: Enable PWM2IF interrupt

Bit 3 (PWM1IE): PWM1IE interrupt enable bit

0: Disable PWM1IF interrupt

1: Enable PWM1IF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: Disable TCIF interrupt

1: Enable TCIF interrupt

6.2.12 IOC51 (High Sink Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS57	HS56	-	HS54	HS53	HS52	HS51	-

Bit 7 (HS57): Output High Sink current Select for P57.

Bit 6 (HS56): Output High Sink current Select for P56.

Bit 5: Not used.

Bit 4 (HS54): Output High Sink current Select for P54.

Bit 3 (HS53): Output High Sink current Select for P53.

Bit 2 (HS52): Output High Sink current Select for P52.

Bit 1 (HS51): Output High Sink current Select for P51.

Bit 0: Not used.

HSxx	VDD = 5V, Sink Current
0	10 mA (in 0.1VDD)
1	25 mA (in 0.1VDD)

6.2.13 IOC61 (High Sink Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60

Bit 7 (HS67): Output High Sink current Select for P67.

Bit 6 (HS66): Output High Sink current Select for P66.

Bit 5 (HS65): Output High Sink current Select for P65.

Bit 4 (HS64): Output High Sink current Select for P64.

Bit 3 (HS63): Output High Sink current Select for P63.

Bit 2 (HS62): Output High Sink current Select for P62.

Bit 1 (HS61): Output High Sink current Select for P61.

Bit 0 (HS60): Output High Sink current Select for P60.

HSxx	VDD = 5V, Sink Current
0	10 mA (in 0.1VDD)
1	25 mA (in 0.1VDD)

6.2.14 IOC71 (High Driver Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD57	HD56	-	HD54	HD53	HD52	HD51	-

Bit 7 (HD57): Output High Driver current Select for P57.

Bit 6 (HD56): Output High Driver current Select for P56.

Bit 5: Not used.

Bit 4 (HD54): Output High Driver current Select for P54.

Bit 3 (HD53): Output High Driver current Select for P53.

Bit 2 (HD52): Output High Driver current Select for P52.

Bit 1 (HD51): Output High Driver current Select for P51.

Bit 0: Not used.

HDxx	VDD = 5V, Driver Current
0	3.7 mA (in 0.9VDD)
1	10 mA (in 0.9VDD)

6.2.15 IOC81 (High Driver Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60

Bit 7 (HD67): Output High Driver current Select for P67.

Bit 6 (HD66): Output High Driver current Select for P66.

Bit 5 (HD65): Output High Driver current Select for P65.

Bit 4 (HD64): Output High Driver current Select for P64.

Bit 3 (HD63): Output High Driver current Select for P63.

Bit 2 (HD62): Output High Driver current Select for P62.

Bit 1 (HD61): Output High Driver current Select for P61.

Bit 0 (HD60): Output High Driver current Select for P60.

HDxx	VDD = 5V, Driver Current
0	3.7 mA (in 0.9VDD)
1	10 mA (in 0.9VDD)

6.2.16 IOCF1 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Note: *The IOCD0 register is both readable and writable.*

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable internal pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable internal pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable internal pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable internal pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable internal pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable internal pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable internal pull-high of the P60 pin.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2 ~ PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2 ~ PSW0 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Figure 6-3 depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock (Fm/Fs) or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). If TCC signal source is from an external clock, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than Fm clock or Fs clock, determine by Bank 1 RF CPUS bit.

NOTE

The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to “SLEP” instruction, if the ADWE bit of the RE register is enabled, the TCC will keep on running.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode).

During normal operation or in sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. Refer to WDTE bit of IOCE0 register (Section 6.2.10 IOCE0 (WDT Control and Interrupt Mask Registers 2). With no prescaler, the WDT time-out period is approximately 18ms[1] or 4.5ms[2].

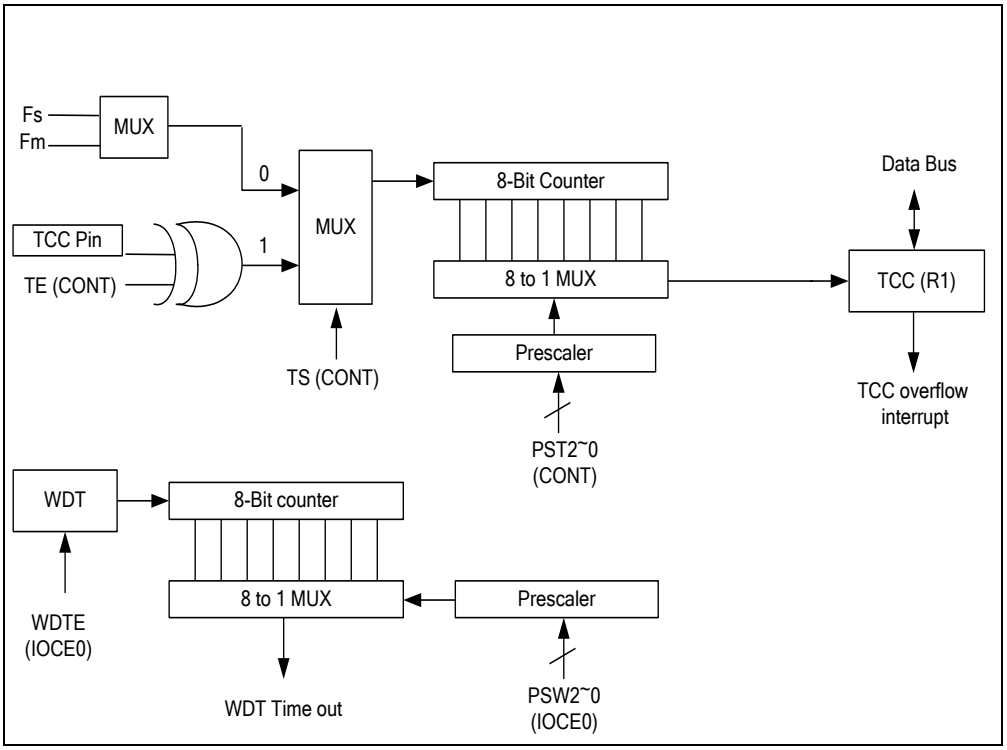


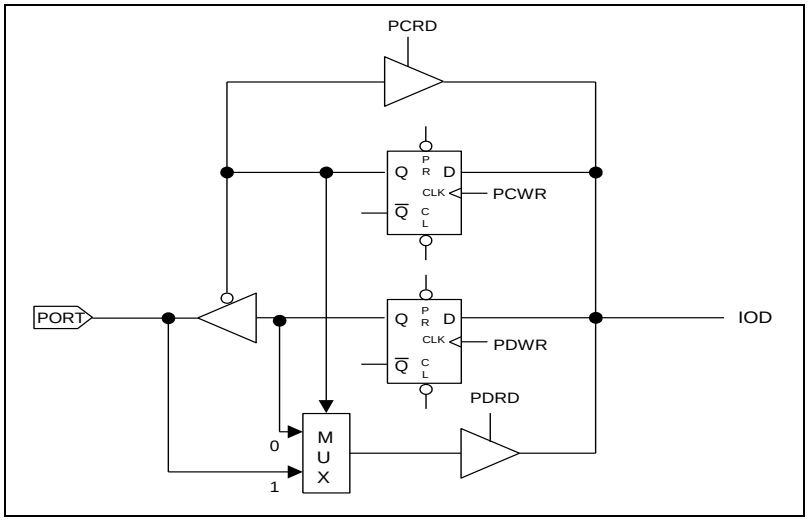
Figure 6-3 TCC and WDT Block Diagram

6.4 I/O Ports

The I/O registers (Port 5, Port 6, and Port 7) are bidirectional tri-state I/O ports. Port 5 is pulled-high and pulled-down internally by software. Likewise, P6 has its open-drain output set through software. Port 5 features an input status changed interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC70). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 6-4, 6-5, 6-6, and 6-7.

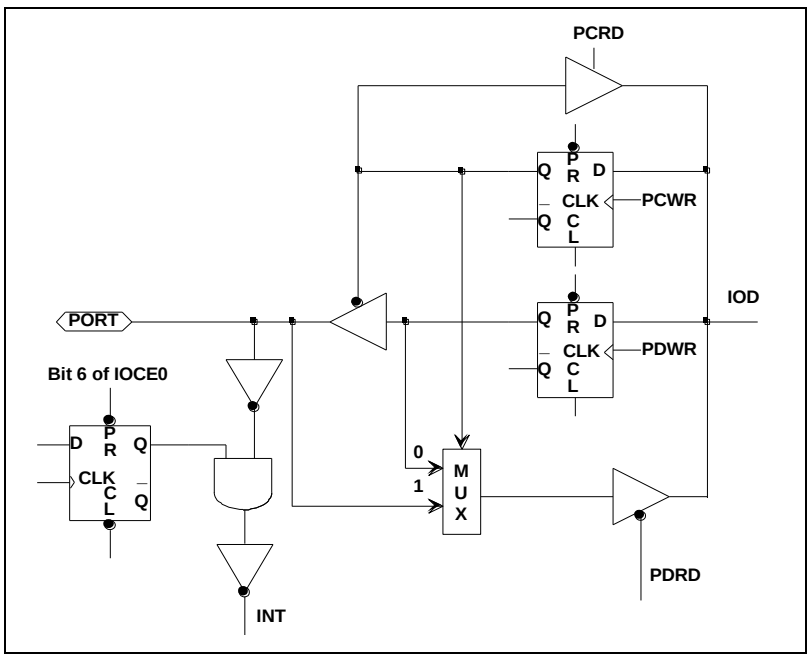
[1] VDD=5V, WDT time-out period = 16.5ms ± 30% at 25°C
VDD=3V, WDT time-out period = 18ms ± 30% at 25°C

[2] VDD=5V, WDT time-out period = 4.2ms ± 30% at 25°C
VDD=3V, WDT time-out period = 4.5ms ± 30% at 25°C



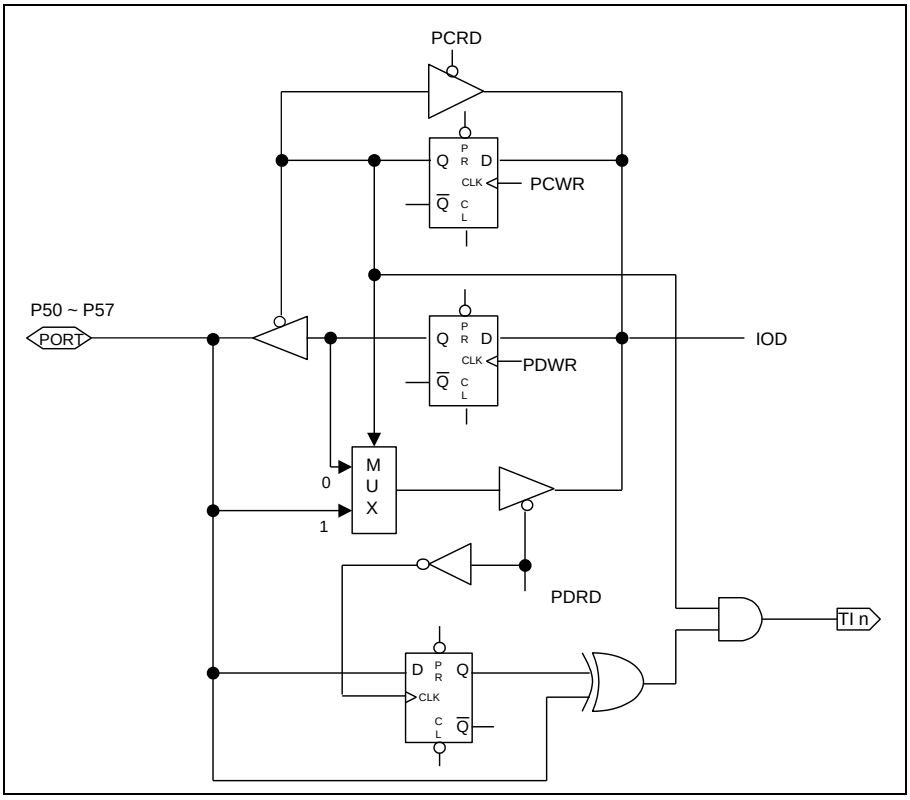
Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-4 I/O Port and I/O Control Register Circuit for Port 6 and Port 7



Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-5 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-6 I/O Port and I/O Control Register Circuit for Ports 50~57

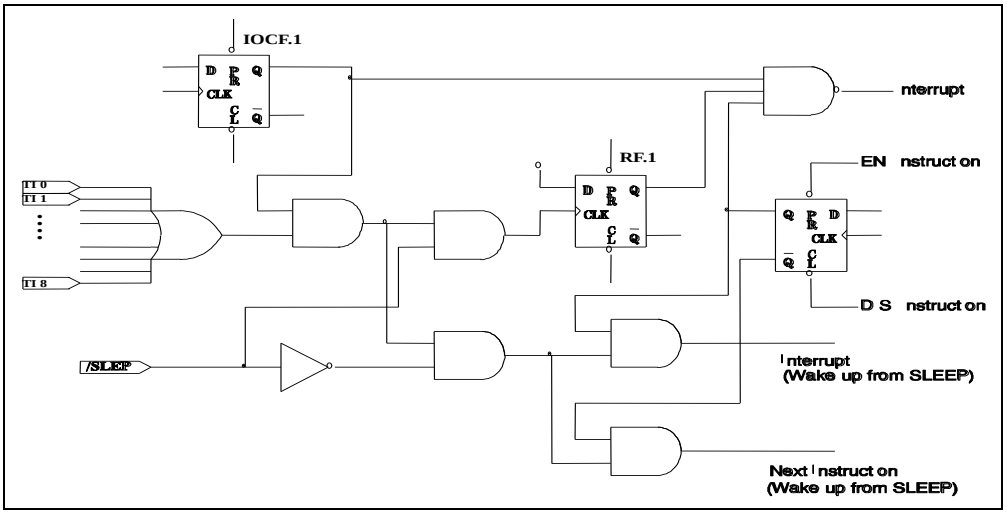


Figure 6-7 Port 5 Block Diagram with Input Change Interrupt / Wake-up

6.4.1 Usage of Port 5 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 5 (MOV R5,R5)	2. Read I/O Port 5 (MOV R5,R5)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt Vector (006H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 5 pin change	
1. Read I/O Port 5 (MOV R5,R5)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF ICIE =1)	
(b) After Port 5 pin changed (interrupt)	
1. IF "ENI" → Interrupt Vector (006H)	
2. IF "DISI" → Next instruction	

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The device is kept in reset condition for a period of approximately 18ms[3] (except in LXT mode) after the reset is detected. When in LXT2 mode, the reset time is 500 ms. Two choices (18ms[3] or 4.5ms[4]) are available for WDT-time out period. Once a reset occurs, the following functions are performed (the initial Address is 000h):

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".

[3] VDD=5V, Setup time period = 16.5 ms ± 30%.
VDD=3V, Setup time period = 18 ms ± 30%.

[4] VDD=5V, Setup time period = 4.2 ms ± 30%.
VDD=3V, Setup time period = 4.5 ms ± 30%.

- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared
- When power is switched on, the upper three bits of R3 is cleared
- The IOCB0 register bits are set to all "1"
- The IOCC0 register bits are set to all "0"
- The IOCD0 register bits are set to all "1"
- Bits 7, 5, and 4 of the IOCE0 register are cleared
- Bits 5 and 4 of the RE register are cleared
- RF and IOCF0 registers are cleared

Executing the “SLEP” instruction will assert the sleep (power down) mode (when IDLE=”0”.). While entering into sleep mode, the Oscillator, TCC, TMR1 and TMR2 are stopped. The WDT (if enabled) is cleared but keeps on running.

During AD conversion, when “SLEP” instruction is set; the Oscillator, TCC, TMR1 and TMR2 keep on running. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 5 input status changes (if ICWE is enabled)

Case 4 Comparator output status changes (if CMPWE is enabled)

Case 5 AD conversion completed (if ADWE is enabled)

Case 6 Low Voltage Detector (if LVDWE is enabled)

The first two cases (1 and 2) will cause the EM78P372N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5 and 6 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x06 (Case 3), 0×0F (Case 4), 0x0C (Case 5) and 0×21 (Case 6) after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up.

Only one of Cases 2 to 6 can be enabled before entering into sleep mode. That is:

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P372N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details.

Case [b] If Port 5 Input Status Change is used to wake up the EM78P372N and the ICWE bit of the RE register is enabled before SLEP, and WDT must be disabled. Hence, the EM78P372N can be awakened only with Case 3. Wake-up time is dependent on the oscillator mode. In RC mode, wake-up time is 10 μs (for stable oscillators). In XT (4 MHz) mode, wake-up time is 800 μs (for stable oscillators), and in LXT2 mode, Wake-up time is 2~3s.

Case [c] If the Comparator output status change is used to wake-up the EM78P372N and the CMPWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P372N can be awakened only with Case 4. Wake-up time is dependent on the oscillator mode. In RC mode, Wake-up time is 10 μs (for stable oscillators). In XT (4 MHz) mode, Wake-up time is 800μs (for stable oscillators), and in LXT2 mode, Wake-up time is 2s~3s.

Case [d] If AD conversion completed is used to wake-up the EM78P372N and ADWE bit of RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P372N can be awakened only with Case 5. The wake-up time is 16 TAD (ADC clock period).

Case[e] If Low voltage detector is used to wake-up the EM78P372N and the LVDWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P372N can be awakened only with Case 6. Wake-up time is dependent on the oscillator mode.

If Port 5 Input Status Change Interrupt is used to wake up the EM78P372N (as in Case [b] above), the following instructions must be executed before SLEP:

```
BC          R3, 6           ; Select Segment 0
MOV         A, @00xx1110b   ; Select WDT prescaler and Disable WDT
IOW         IOCE0
WDTC                        ; Clear WDT and prescaler
MOV         R5, R5          ; Read Port 5
ENI (or DISI)               ; Enable (or disable) global interrupt
MOV         A, @xxxxxx1xb   ; Enable Port 5 input change wake-up bit
MOV         RE
MOV         A, @xxxxxx1xb   ; Enable Port 5 input change interrupt
IOW         IOCF0
SLEP                        ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P372N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BC          R3, 6           ; Select Segment 0
MOV         A, @xxx10XXXb   ; Select a comparator and P64 functions
                            ; as CO pin
IOW         IOC80
MOV         A, @00x11110b   ; Select WDT prescaler and Disable WDT,
                            ; and enable comparator output status
                            ; change interrupt
IOW         IOCE0
WDTC                        ; Clear WDT and prescaler
ENI (or DISI)               ; Enable (or disable) global interrupt
MOV         A, @xxx0x1xxb   ; Enable comparator output status
                            ; change wake-up bit
MOV         RE
SLEP                        ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0 EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0 EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1 EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 5 Pin change	ICWE = 0 ICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWE = 0 ICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1 ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWE = 1 ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion complete	ADWE = 0 ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWE = 0 ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWE = 1 ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWE = 1, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Comparator Interrupt	CMPWE = 0 CMPIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	CMPWE = 0 CMPIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPWE = 1 CMPIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	CMPWE = 1 CMPIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM1 period interrupt	PWM1IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWM1IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM2 period interrupt	PWM2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWM2IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM1 duty interrupt	DT1IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	DT1IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM2 duty interrupt	DT2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	DT2IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWE = 0 LVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid.	
	LVDWE = 0 LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVWE = 1 LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	LVDWE = 1 LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT Timeout	WDTE = 1	Wake up + Reset		Wake up + Reset		Reset		Reset	
Low voltage reset		Wake up + Reset		Wake up + Reset		Reset		Reset	

6.5.1.2 Register Initial Values after Reset

The following summarizes the initialized values for registers.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Type	–	–	–	–	–	–	–	–
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Type	–	–	–	–	–	–	–	–
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	×	×	×	×	×	×	C71	C70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC80	Bit Name	×	×	CMPOUT	COS1	COS0	×	×	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0 (PDCR)	Bit Name	/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC0 (ODCR)	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0 (PHCR1)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0 (WDTCR & IMR2)	Bit Name	WDTC	EIS	ADIE	CMPIE	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCF0 (IMR)	Bit Name	×	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (HSCR1)	Bit Name	HS57	HS56	×	HS54	HS53	HS52	HS51	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 (HSCR2)	Bit Name	HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (HDCR1)	Bit Name	HD57	HD56	×	HD54	HD53	HD52	HD51	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (HDCR2)	Bit Name	HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF1 (PHCR2)	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	1	0	1	1	0	0	0	0
		/RESET and WDT	1	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×02	R2 (PC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x06 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	RST	IOCS	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	1	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	SBANK	BS0	–	–	–	–	–	–
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0×05	Bank 0 R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 0 R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 0 R7	Bit Name	–	–	–	–	–	–	P71	P70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 0 R8 (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0×09	Bank 0 R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
0×0A	Bank 0 RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0B	Bank 0 RB (ADDATA)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 0 RC (ADDATA1H)	Bit Name	×	×	×	×	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	Bank 0 RD (ADDATA1L)	Bit Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 0 RE (ISR2 & WUCR)	Bit Name	/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE
		Power-on	1	0	0	0	0	0	0	0
		/RESET and WDT	1	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 0 RF (ISR2)	Bit Name	×	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 1 R5 (TBHP)	Bit Name	MLB	×	×	×	×	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 1 R6 (TBLP)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 1 R7 (PWMCON)	Bit Name	×	×	×	×	×	PWMCAS	PWM2E	PWM1E
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×08	Bank 1 R8 (TMRCON)	Bit Name	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	Bank 1 R9 (PRD1)	Bit Name	PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	Bank 1 RA (PRD2)	Bit Name	PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	Bank 1 RB (DT1)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 1 RC (DT2)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 1 RE (LVDCR & WUCR)	Bit Name	LVDIE	LVDEN	LVD1	LVD0	×	×	×	EXWE
		Power-on	0	0	1	1	0	0	0	0
		/RESET and WDT	0	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 1 RF (SCR)	Bit Name	-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0
		Power-on	0	1	1	0	1	1	WORD1<6~5>	
		/RESET and WDT	0	1	1	0	1	1	WORD1<6~5>	
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10~0x3F	R10~R3F	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: ***"x"*** *= not used* ***"P"*** *= previous value before reset*
"u" *= unknown or don't care* ***"t"*** *= check "Reset Type" Table in Section 6.5.2*

6.5.1.3 Controller Reset Block Diagram

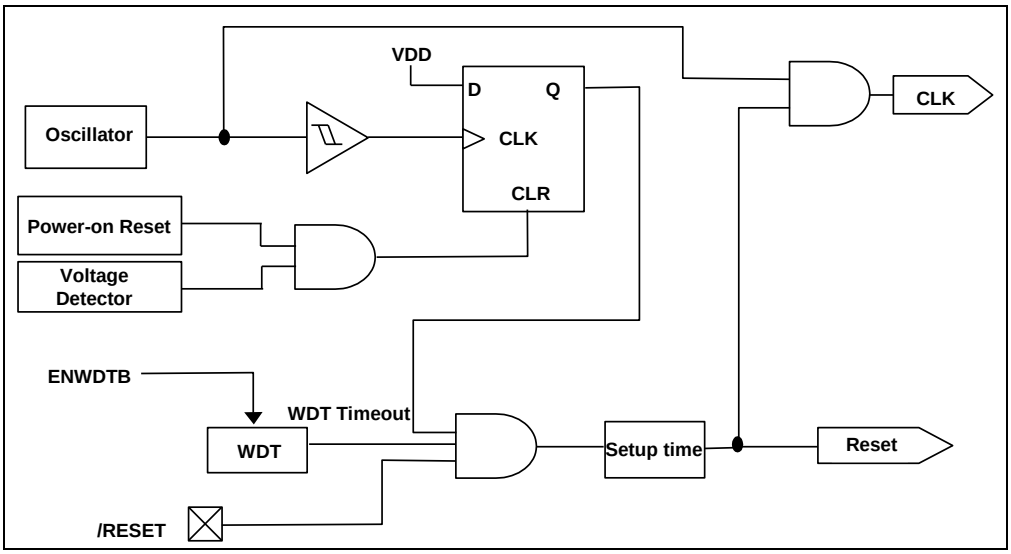


Figure 6-8 Controller Reset Block Diagram

6.5.2 T and P Status under the Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	RST	T	P
Power-on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
LVR during Operating mode	0	*P	*P
LVR wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	1
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

***P:** Previous status before reset

The following shows the events that may affect the status of T and P.

Event	RST	T	P
Power-on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin changed during Sleep mode	1	1	0

*P: Previous value before reset

6.6 Interrupt

The EM78P372N has ten interrupts enumerated below:

1. PWM1~2 period match and duty cycle match overflow interrupt
2. Port 5 Input Status Change Interrupt
3. External interrupt [(P60, /INT) pin]
4. Analog to Digital conversion completed
5. When the comparators status changes
6. Low voltage detector Interrupt

Before the Port 5 Input Status Change Interrupt is enabled, reading Port 5 (e.g. "MOV R5, R5") is necessary. Each Port 5 pin will have this feature if its status changes. The Port 5 Input Status Change Interrupt will wake up the EM78P372N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP instruction. When wake up occurs, the controller will continue to execute program in-line if the global interrupt is disabled. If enabled, the global interrupt will branch out to the Interrupt Vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than system clock time) is eliminated as noise. However, under Low Crystal oscillator (LXT2) mode the noise rejection circuit will be disabled. Edge selection is possible with INTE of CONT. When an interrupt is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H. Refer to Word 1 Bits 9 and 8, Section 6.14.2, Code Option Register (Word 1) for digital noise rejection definition.

RF and RE are the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 and IOCE0 are Interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bits is “Enable”, the flag in the Interrupt Status Register (RF) is set regardless of the ENI execution. Note that the result of RF will be the logic AND of RF and IOCF0 (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from Address 009, 012, 015, 018 and 01BH (PWM1~2 period match and duty match respectively).

When an interrupt generated by AD conversion is completed (if enabled), the next instruction will be fetched from Address 00CH.

When an interrupt is generated by the Comparators (when enabled), the next instruction will be fetched from Address 00FH (Comparator interrupt).

When an interrupt is generated by the Low Voltage Detect (when enabled), the next instruction will be fetched from Address 021H (Low Voltage Detector interrupt).

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers are saved first by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After an interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

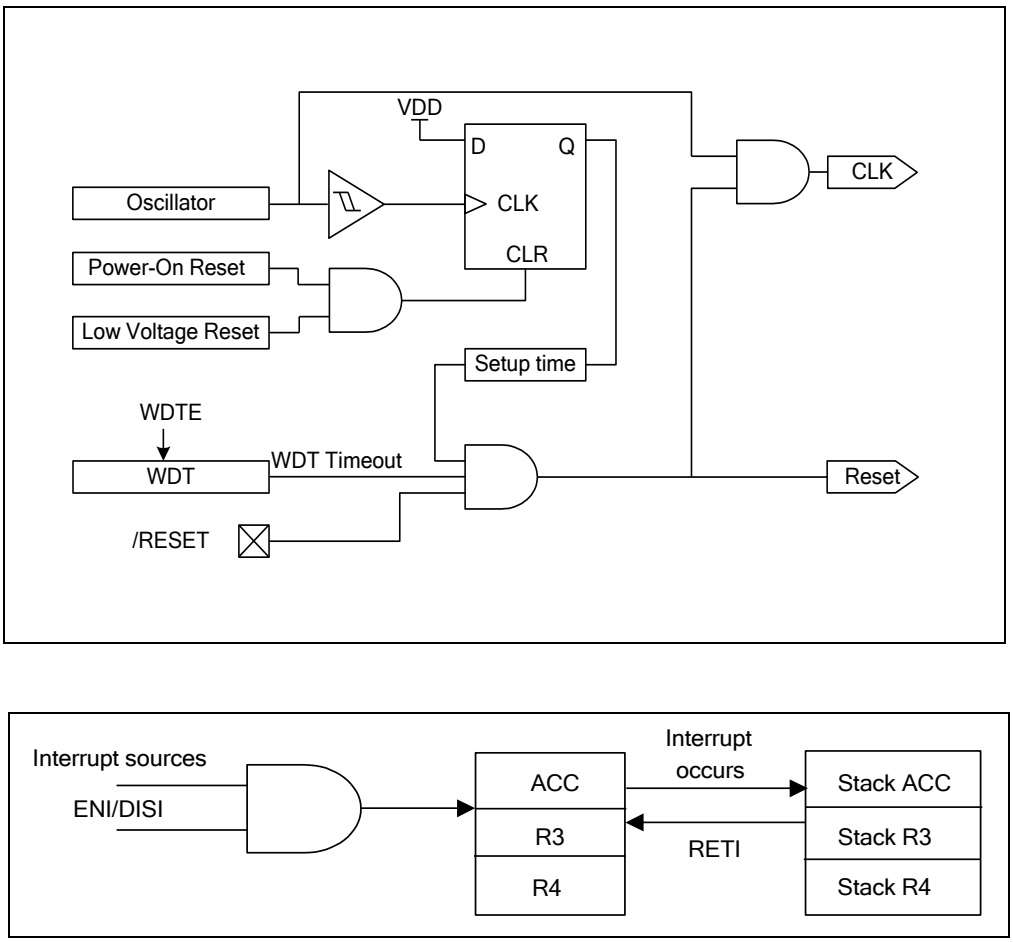


Figure 6-9 Interrupt Back-up Diagram

In EM78P372N, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority *
003H	External interrupt	2
006H	Port 5 pin change	3
009H	TCC overflow interrupt	4
00CH	AD conversion complete interrupt	5
00FH	Comparator interrupt	6
012H	PWM1 period match interrupt	7
015H	PWM2 period match interrupt	8
018H	PWM1 duty match interrupt	9
01BH	PWM2 duty match interrupt	10
021H	Low Voltage Detector interrupt	1

Note: **Priority: 1 = highest ; 10 = lowest priority*

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, & ADOC/RA), three data registers (ADDATA/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins. Connecting to an external VREF is more accurate than connecting to an internal VDD.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H, and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2, ADIS1 and ADIS0.

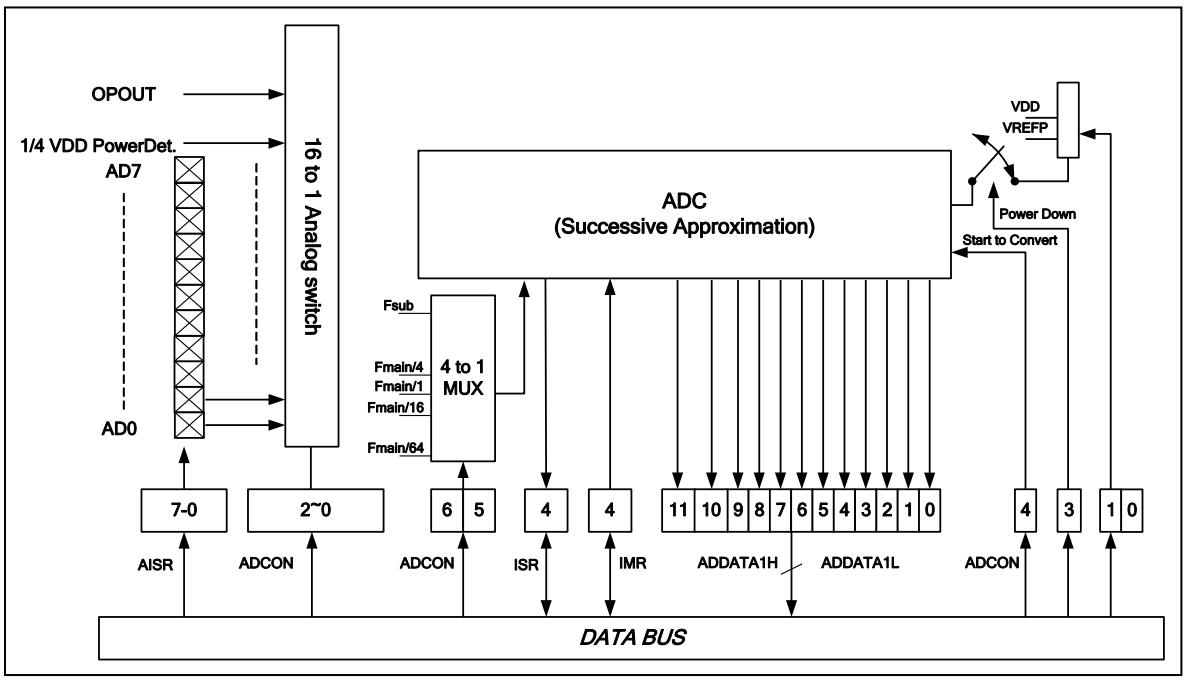


Figure 6-10 Analog-to-Digital Conversion Functional Block Diagram

This is a 12-bit successive approximation register analog to digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFP and VPIS[1:0] bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

6.7.1.1 Bank 0 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The **AISR** register individually defines the P5, P6 and P7 pins as analog inputs or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P57 pin

0: Disable ADC7, P57 functions as I/O pin

1: Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0: Disable ADC6, P55 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0: Disable ADC5, P70 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P67 pin

0: Disable ADC4, P67 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0: Disable ADC3, P53 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0: Disable ADC2, P52 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable ADC1, P51 acts as I/O pin

1: Enable ADC1 acts as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable ADC0, P50 functions as I/O pin

1: Enable ADC0 to function as analog input pin

6.7.1.2 Bank 0 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

The **ADCON** register controls the operation of the AD conversion and determines which pin should be currently active.

Bit 7(VREFS): The input source of the ADC Vref

0: The ADC Vref is connected to Vdd (default value), and the VREF/TCC/P54 pin carries out the P54 function

1: The ADC Vref is connected to VREF/TCC/P54

NOTE

The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time. If P54/TCC/VREF functions as VREF analog input pin, then CONT Bit 5 (TS) must be "0".

The P54/TCC/VREF pin priority is as follows:

P54/TCC/VREF Pin Priority		
High	Medium	Low
VREF	TCC	P54

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of ADC oscillator clock rate

00 = 1: 16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: 1

System Mode	CKR[1:0]	Operating Clock of ADC (F_{AD} = 1 / T_{AD})	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)
Normal Mode	00 (default)	F_{OSC}/16	4 MHz	16 MHz
	01	F_{OSC}/4	1 MHz	4 MHz
	10	F_{OSC}/64	16 MHz	–
	11	F_{OSC}/1	–	1 MHz
Green Mode	xx	–	16k/128kHz	16k/128kHz

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit **cannot** be reset though software.

1: AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to conserve power even while the CPU is operating

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

ADICS	ADIS2	ADIS1	ADIS0	Analog Input Select
0	0	0	0	ADIN0/P50
0	0	0	1	ADIN1/P51
0	0	1	0	ADIN2/P52
0	0	1	1	ADIN3/P53
0	1	0	0	ADIN4/P67
0	1	0	1	ADIN5/P70
0	1	1	0	ADIN6/P55
0	1	1	1	ADIN7/P57
1	0	X	X	OPOUT
1	1	x	x	Internal, 1/4 VDD

These bits can only be changed when the ADIF bit and the ADRUN bit are both Low.

6.7.1.3 RA (ADOC: AD Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P372N
0	0	0	0LSB
0	0	1	2LSB
0	1	0	4LSB
0	1	1	6LSB
1	0	0	8LSB
1	0	1	10LSB
1	1	0	12LSB
1	1	1	14LSB

Bit 2 ~ Bit 1: ADC internal reference voltage source.

VREF1	VREF0	ADC internal Reference Voltage
0	0	VDD
0	1	4.0V ± 1%
1	0	3.0V ± 1%
1	1	2.0V ± 1%

Bit 0 (ADICS): ADC Internal Channel Select (select ADC internal 1/4 VDD or OP output pin connects to ADC input)

0: disable

1: enable

NOTE

- *If VREF [1:0]=00, the internal reference will not turn on. If VREF[1 :0] ≠ 00, the internal reference will turn on automatically. Moreover, the power of the internal reference is irrelevant to ADC.*
- *When using internal voltage reference for the first time, user needs to wait for at least 50 µs to enable and stabilize the voltage reference. Unstable reference will result to inaccurate conversion. On subsequent switching of the voltage reference, user only needs to wait for at least 6µs for stabilization.*
- *If ADC uses internal VREF 2V function, the resulting conversion data will be inaccurate. So user must ensure that the minimum analog reference voltage of AD electrical characteristics is not less than 2.5V.*

6.7.1.4 Bank 1 RF (IRC Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0

Bits 3 ~ 2 (SHS1 ~ SHS0): Select AD sample and hold Timing Select. (Recommend at least 4 μs, T_{AD}: Period of ADC Operating Clock)

SHS1	SHS0	ADC Sample and Hold (TAD)
0	0	2 x T_{AD}
0	1	4 x T_{AD}
1	0	8 x T_{AD}
1	1	12 x T_{AD} (default)

6.7.2 ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)

When the AD conversion is completed, the result is loaded into the ADDATA1H and ADDATA1L. The ADIF is set if ADIE is enabled.

6.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. The maximum recommended impedance for the analog source is 10 kΩ at VDD = 5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

6.7.4 AD Conversion Time

CKR[2:0] select the conversion time (T_{AD}). This allows the MCU to run at maximum frequency without sacrificing the accuracy of the AD conversion. The following tables show the relationship between T_{AD} and the maximum operating frequencies. T_{AD} is 0.5 μs for 3V~5.5V and T_{AD} is 2 μs for 2.5V~3V.

V_{DD} = 3V ~ 5.5V (T_{AD} is 1 μs)

System Mode	CKR[1:0]	Operating Clock of ADC (F_{AD} = 1 / T_{AD})	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)	Conversion Time of One Word (SHS[1:0] = 10*)
Normal Mode	00	F_{Main} / 16	16 MHz	20 μs
	01	F_{Main} / 4	4 MHz	20 μs
	10	F_{Main} / 64	-	-
	11	F_{Main} / 1	1 MHz	20 μs
Green Mode	xx	F_{Sub}	128kHz	157 μs

* *Conversion Time = Sample and Hold (SHS [1:0]=10, 8 × T_{AD}) + 12 × Bit Conversion Time (12 × T_{AD}) + Delay Time between setting ADSTART bit and starting first T_{AD}.*

V_{DD} = 2.5V ~ 3V (T_{AD} is 4 µs)

System Mode	CKR[1:0]	Operating Clock of ADC (F_{AD} = 1 / T_{AD})	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)	Conversion Time of One Word (SHS[1:0] = 10*)
Normal Mode	00	F_{Main} / 16	4 MHz	82 µs
	01	F_{Main} / 4	1 MHz	82 µs
	10	F_{Main} / 64	-	-
	11	F_{Main} / 1	-	-
Green Mode	xx	-	128 kHz	157 µs

*Conversion Time = Sample and Hold (SHS [1:0]=10, 8 × T_{AD}) + 12 × Bit Conversion Time (12 × T_{AD}) + Delay Time between setting ADSTART bit and starting first T_{AD} (0.5 × T_{AD}).

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, PWM1, PMW2 and AD conversion.

The AD Conversion is considered completed as determined by:

1. The ADRUN bit of the R9 register is cleared to “0”.
2. The ADIF bit of the BANK 0 RE register is set to “1”.
3. The ADWE bit of the BANK 0 RE register is set to “1”. Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit of the IOCE0 is enabled and the “DISI” instruction is executed.
5. Wake up and enters into Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.
6. Enters into an Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when the conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.7.6 Programming Process/Considerations

6.7.6.1 Programming Process

Follow these steps to obtain data from the ADC:

1. Write to the eight bits (ADE7: ADE0) on the R8 (AISR) register to define the characteristics of R5 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R9/ADCON register to configure the AD module:
   a) Select the ADC input channel (ADIS2 : ADIS0)
   b) Define the AD conversion clock rate (CKR1 : CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for the ADRUN bit to be cleared to “0” , interrupt flag (ADIF) is set “1,” or ADC interrupt occurs.
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If the ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.7.6.2 Sample Demo Programs

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
PORT6 == 6
R_E== 0XE         ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5      ; Control Register of Port 5
IOC60 == 0X6      ; Control Register of Port 6
IOCE0== 0XE       ; Interrupt Mask Register 2
C_INT== 0XF       ; Interrupt Mask Register
```

C. ADC Control Register

```
ADDATA == 0xB     ; The contents are the results of ADC[11:4]
ADDATA1H == 0xC ; The contents are the results of ADC[11:8]
ADDATA1L == 0xD ; The contents are the results of ADC[7:0]
AISR == 0x08      ; ADC input select register
ADCON == 0x9      ;  7     6    5    4      3    2     1     0
                  ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

D. Define Bits in ADCON

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

E. Program Starts

```
ORG 0             ; Initial address
JMP INITIAL

ORG 0x0C          ; Interrupt vector
JMP CLRRE
;
;(User program section)
;
CLRRE:
MOV A,RE
AND A, @0BXX0XXXXX  ; To clear the ADIF bit, "X" by application
MOV RE,A
BS ADCON, ADRUN     ; To start to execute the next AD conversion
                    ; if necessary
RETI
INITIAL:
MOV A,@0B00000001   ; To define P50 as an analog input
MOV AISR,A
MOV A,@0B00001000   ; To select P50 as an analog input channel, and
                    ; AD power on
MOV ADCON,A         ; To define P50 as an input pin and set the
                    ; clock rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1  ; To define P50 as an input pin, and the others
                    ; are dependent on applications
```

```
IOW PORT5

MOV A, @0BXXXX1XXX  ; Enable the ADWE wake-up function of ADC, "X"
                    ; by application
MOV RE,A
MOV A, @0BXX1XXXXX  ; Enable the ADIE interrupt function of ADC,
                    ; "X" by application
IOW IOCE0
ENI                 ; Enable the interrupt function

BS ADCON, ADRUN     ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

;If Sleep:
SLEP
;
;(User program section)
;

or
;If Polling:
POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously;
JMP POLLING         ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;(User program section)
```

6.8 Dual Sets of PWM (Pulse Width Modulation)

6.8.1 Overview

In PWM mode, PWM1 and PWM2 pins produce 8-bit resolution PWM output (see. the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of PWM is the inverse of the time period. Figure 6-13 *PWM Output Timing* depicts the relation between a time period and a duty cycle.

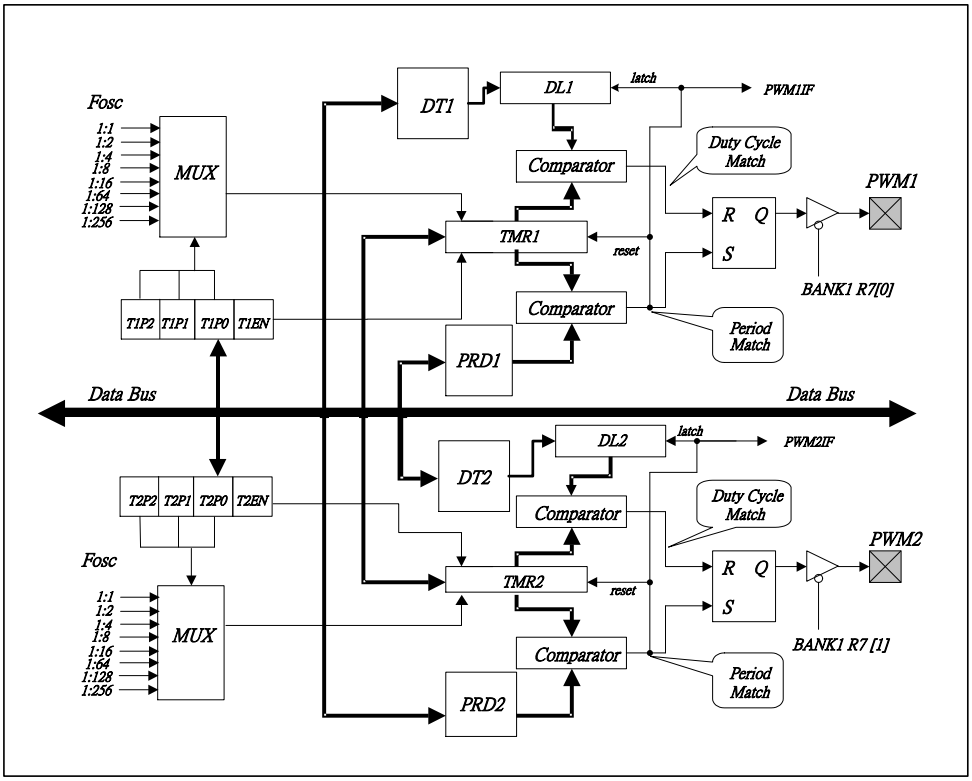


Figure 6-12 PWM System Block Diagram

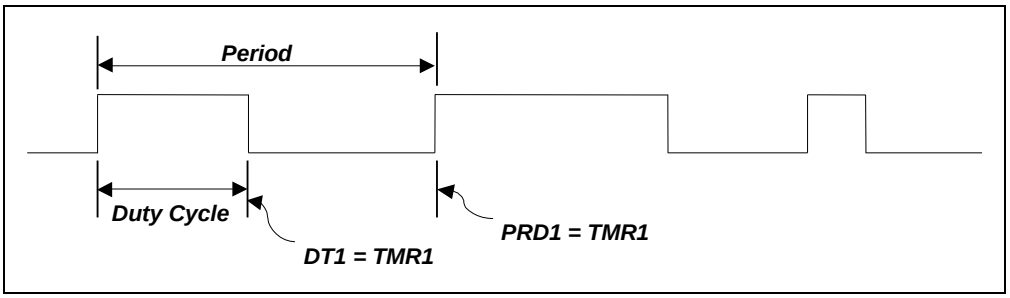


Figure 6-13 PWM Output Timing

6.8.2 Increment Timer Counter (TMRX: TMR1 or TMR2)

TMRX are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. If employed, they can be turned off for power saving by setting the T1EN bit [Bank 1-R8<6>] or T2EN bit [Bank 1-R8<7>] to "**0**".

TMR1 and TMR2 are internal designs and can be read only

6.8.3 PWM Time Period (TMRX: TMR1 or TMR2)

PWM Time Period (PRDX: PRD1 or PRD2). The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMR is cleared
2) The PWMX pin is set to "**1**"
3) The PWMX duty cycle is latched from DT1/DT2 to DL1/DL2

NOTE
*The PWM output will not be set, if the duty cycle is "**0**".*

4) The PWMXIF pin is set to "**1**"

The following formula describes how to calculate the PWM time period:

$$Period = (PRDX + 1) \times \left(\frac{1}{FOSC}\right) \times (TMRX \ \ prescale \ value)$$

Example:

PRDX=49; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,

then $Period = (49+1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5$ **µs**

6.8.4 PWM Duty Cycle (DTX: DT1 or DT2; DLX: DL1 or DL2)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

$$Duty\ Cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times \left(TMRX \quad prescale \quad value \right)$$

Example:

DTX=10; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,

then $Duty\ Cycle = 10 \times \left(\frac{1}{4M}\right) \times 1 = 2.5$ **µs**

6.8.5 Comparator X

Changing the output status while a match occurs will simultaneously set the PWMXIF (TMRXIF) flag.

6.8.6 PWM Programming Process/Steps

1. Load PRDX with the PWM time period.
2. Load DTX with the PWM Duty Cycle.
3. Enable the interrupt function by writing to the IOCF0, if required.
4. Set PWMX pin to be output by writing a desired value to BANK1-R7.
5. Load a desired value to Bank 1-R7 or Bank 1-R8 with TMRX prescaler value and enable both PWMx and TMRX.

6.9 Timer/Counter

6.9.1 Overview

Timer 1 (TMR1) and Timer 2 (TMR2) (TMRX) are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1 and Timer 2 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, the Timer 1 and Timer 2 will keep on running.

6.9.2 Functional Description

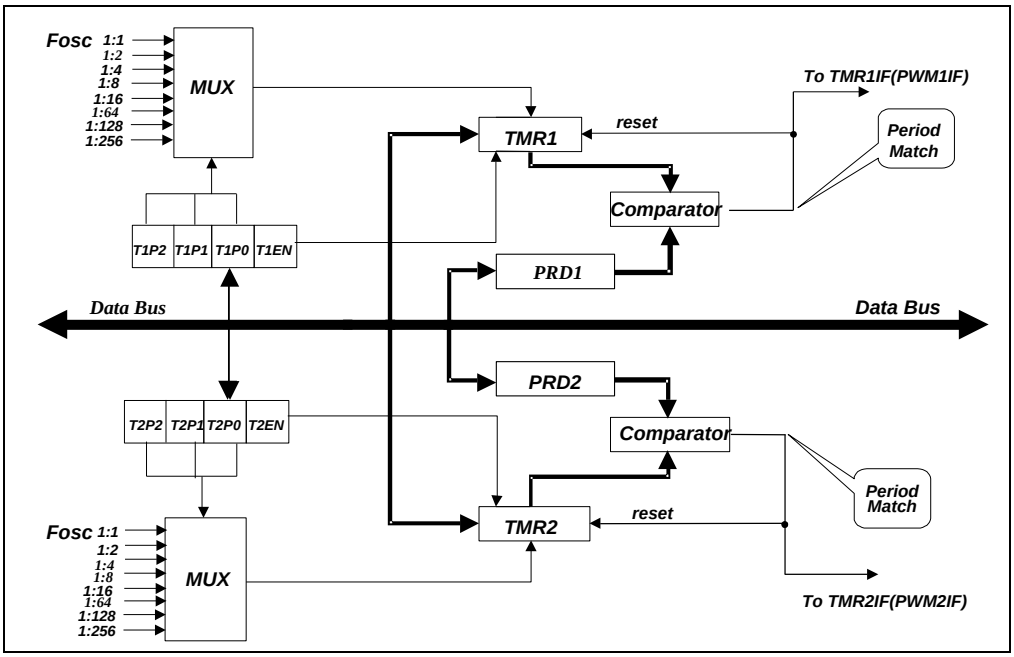


Figure 6-14 Timer Block Diagram

Where:

Fosc: Input clock

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0): The options 1:1, 1:2, 1:4, 1:8, 1:16, 1:64, 1:128, and 1:256 are defined by TMRX. These are cleared when any type of reset occurs.

TMR1 and TMR2: Timer X register. TMRX is increased until it matches with PRDX, and then is reset to "0" (default value).

PRDX (PRD1, PRD2): PWM time period register

Comparator X (Comparator 1 and Comparator 2): Reset TMRX while a match occurs. The TMRXIF (PWMXIF) flag is set at the same time.

6.9.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers as shown in the following table. It must be noted that the PWMX bits must be disabled if their related TMRXs are utilized. That is, Bit 7 ~ Bit 3 of the PWMCON register must be set to "**0**".

■ Related Control Registers of TMR1 and TMR2

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	PWMCON/R7	"0"	"0"	"0"	"0"	"0"	PWMCAS	PWM2E	PWM1E
0x08	TMRCON/R8	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

6.9.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration
2. Enable interrupt function by writing IOCF0, if required
3. Load a desired value for the TMRX prescaler and enable TMRX and disable PWM

6.9.5 PWM Cascade Mode

The PWM Cascade Mode merges two 8-bit PWM function to one 16-bit. In this Mode, the necessary parameters are redefined as shown on the table below:

Parameter / 16-bit PWM	DT (Duty)	PRD (Period)	TMR (Timer)
MSB (15~8)	DT2	PRD2	TMR2
LSB (7~0)	DT1	PRD1	TMR1

The prescaler of this 16-bit PWM uses the prescaler of the TMR1, the MSB of TMR is counted when LSB carry and the PWM1IF bit/PWM1 Pin are redefined as the PWMIF bit/PWM pin for this one.

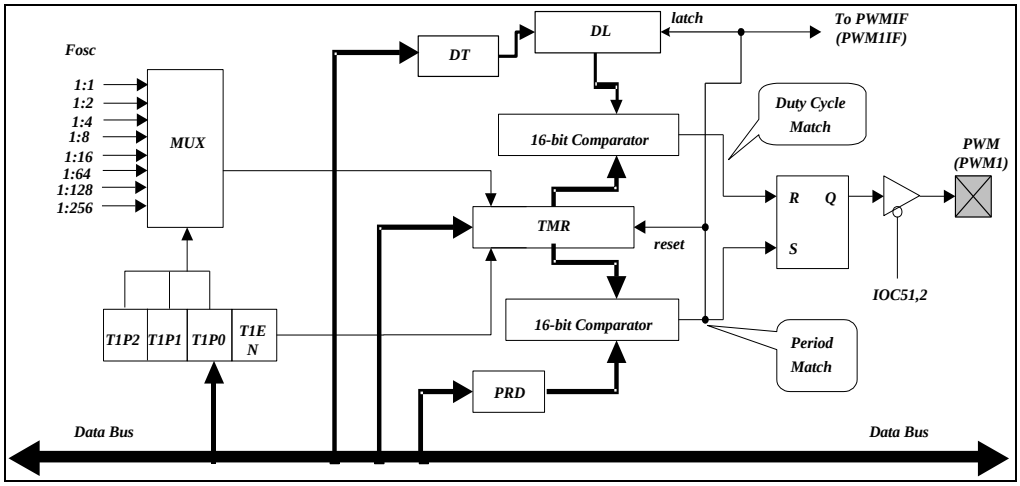


Figure 6-14 Functional Block Diagram of 16-bit PWM (merged from two 8 bits)

6.10 Comparator

The EM78P372N has one comparator which has two analog inputs and one output. The comparator can be employed to wake up the system from sleep/idle mode. The Figure at the right shows the comparator circuit.

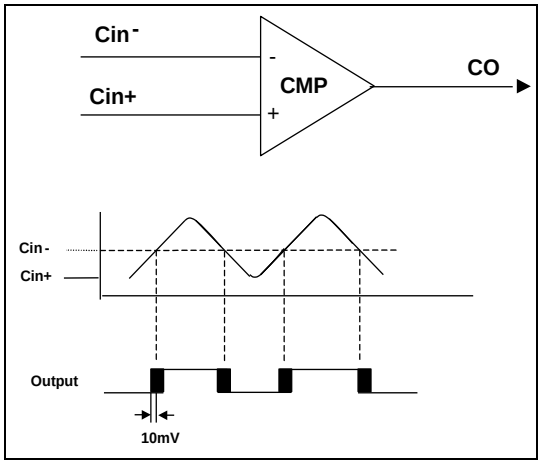


Figure 6-15 Comparator Operating Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.10.2 Comparator Outputs

- The compared result is stored in the CMPOUT of IOC80.
- The comparator outputs are sent to CO (P64) by programming Bit 4 and Bit 3 <COS1, COS0> of the IOC80 register to <1,0>. See the table under Section 6.2.4, IOC80 (Comparator Control Registers) for Comparator/OP select bits Function description.

The following figure shows the Comparator Output block diagram.

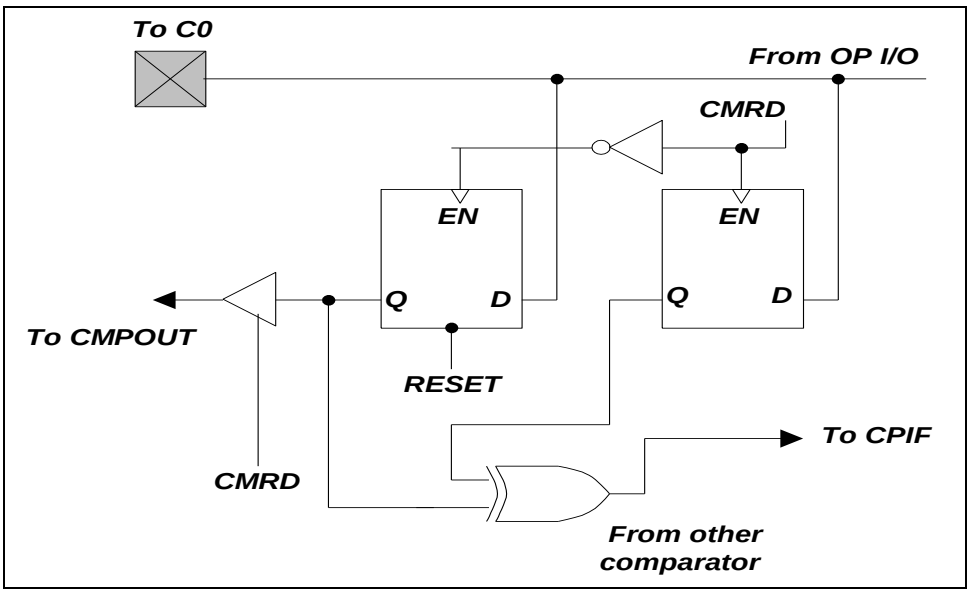


Figure 6-16 Comparator Output Configuration

6.10.3 Using Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output. In this case, the Schmitt trigger function can be disabled for power saving purposes, by setting Bit 4, Bit 3 <COS1, COS0> of the IOC80 register to <1,1>. See the table under Section 6.2.4, IOC80 (Comparator Control Registers) for Comparator/OP select bits function description.

NOTE

Under Operation Amplifier:

- *The CMPIE (IOCE0.4), CMPWE (BANK 0 RE.2), and CMPIF (BANK 0 RE.4) bits are invalid.*
- *The comparator interrupt is invalid.*
- *The comparator wake-up is invalid.*

6.10.4 Comparator Interrupt

- CMPIE (IOCE0.4) must be enabled for the “ENI” instruction to take effect
- Interrupt is triggered whenever a change occurs on the comparator output pin
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOC80<5>.
- CMPIF (Bank 0 RE.4), the comparator interrupt flag, can only be cleared by software

6.10.5 Wake-up from Sleep Mode

- If the CMPWE bit of the Bank 0 RE register is set to “1,” the comparator remains active and the interrupt remains functional, even under Sleep mode.
- If a mismatch occurs, the change will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

The Comparator is considered completed as determined by:

1. COS1 and COS0 bits of IOC80 register setting selects Comparator.
2. CMPIF bit of Bank 0 RE register is set to “1”.
3. CMPWE bit of Bank 0 RE register is set to “1”. Wakes up from Comparator (where it remains in operation during sleep/idle mode).
4. Waking-up and executing the next instruction, if CMPIE bit of IOCE0 is enabled and the “DISI” instruction is executed.
5. Waking-up and entering into Interrupt vector (Address 0x00F), if CMPIE bit of IOCE0 is enabled and the “ENI” instruction is executed.
6. Entering into Interrupt vector (Address 0x00F), if CMPIE bit of IOCE0 is enabled and the “ENI” instruction is executed.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78P372N can be operated in six different oscillator modes, such as Crystal Oscillator Mode (XT), High Crystal Oscillator Mode 1 (HXT1), High Crystal Oscillator Mode 2 (HXT2), Low Crystal Oscillator Mode 1 (LXT1), Low Crystal Oscillator Mode 2 (LXT2), External RC Oscillator Mode (ERC), and RC Oscillator Mode with Internal RC Oscillator Mode (IRC). User can select one of the six modes by programming the OSC3, OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC3, OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P55/ERCin acts as ERCin P70/RCOUT acts as P70	0	0	0	0
ERC[1] (External RC oscillator mode); P55/ERCin acts as ERCin P70/RCOUT acts as RCOUT	0	0	0	1
IRC[2] (Internal RC oscillator mode); P55/ERCin acts as P55 P70/RCOUT acts as P70 (default)	0	0	1	0
IRC[2] (Internal RC oscillator mode); P55/ERCin acts as P55 P70//RCOUT acts as RCOUT	0	0	1	1
LXT1[3] (Frequency range of XT, mode is 100kHz ~ 1 MHz)	0	1	0	0
HXT1[3] (Frequency range of XT mode is 12 MHz ~ 16 MHz)	0	1	0	1
LXT2[3] (Frequency range of XT mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of XT mode is 6 MHz ~ 12 MHz)	0	1	1	1
XT[3] (Frequency range of XT mode is 1 MHz ~ 6 MHz)	1	1	1	1

[1] *In ERC mode, ERCin is used as oscillator pin. RCOUT/P70 is defined by Code Option Word 1 Bit 4 ~ Bit 1.*

[2] *In IRC mode, P55 is normal I/O pin. RCOUT/P70 is defined by Code Option Word 1 Bit4 ~Bit 1.*

[3] *In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

The maximum operating frequency limit of the crystal/resonator at different VDDs are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1V	4
	3.0V	8
	4.5V	16

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P372N can be driven by an external clock signal through the OSCI pin as illustrated below.

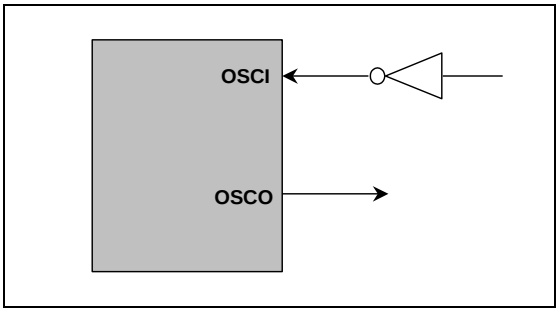


Figure 6-17 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-18 below depicts such a circuit. The same applies to the HXT1 mode, HTX2 mode, LXT1 mode, LXT2 and XT mode.

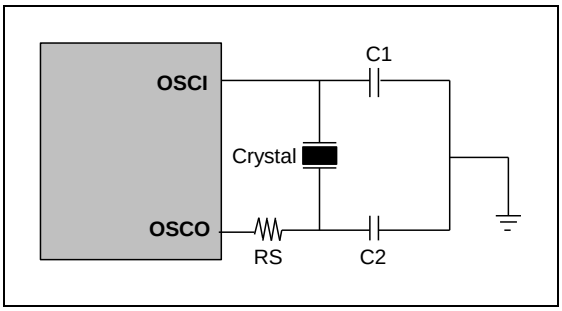


Figure 6-18 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for the appropriate values of C1 and C2. RS, a serial resistor, maybe required for AT strip cut crystal or low frequency mode. Figure 6-21 is a PCB layout suggestion. **When the system works in Crystal mode (16 MHz), a 10 KΩ is connected between OSCI and OSCO.**

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100 K ~ 1 MHz)	100kHz	60 pF	60 pF
		200kHz	60 pF	60 pF
		455kHz	40 pF	40 pF
		1 MHz	30 pF	30 pF
	XT (1 M ~ 6 MHz)	1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	20 pF	20 pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40 pF	40 pF
	LXT1 (100 K ~ 1 MHz)	100kHz	60 pF	60 pF
		200kHz	60 pF	60 pF
		455kHz	40 pF	40 pF
		1 MHz	30 pF	30 pF
	XT (1~6 MHz)	1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	20 pF	20 pF
		6.0 MHz	30 pF	30 pF
	HXT2 (6~12 MHz)	6.0 MHz	30 pF	30 pF
		8.0 MHz	20 pF	20 pF
		12.0 MHz	30 pF	30 pF
	HXT1 (12~20 MHz)	12.0 MHz	30 pF	30 pF
		16.0 MHz	20 pF	20 pF

Circuit diagrams for serial and parallel modes Crystal/Resonator:

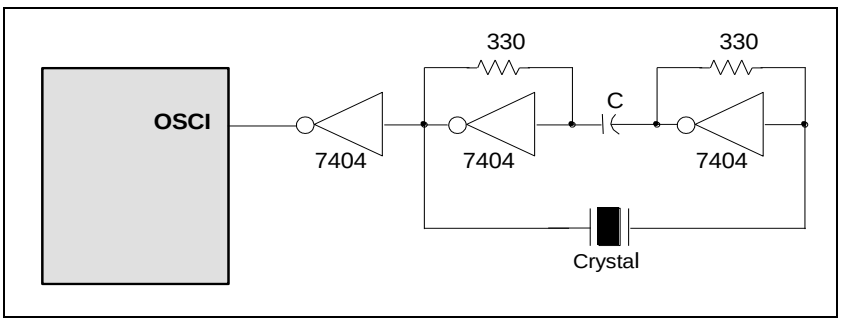


Figure 6-19 Serial Mode Crystal/Resonator Circuit Diagram

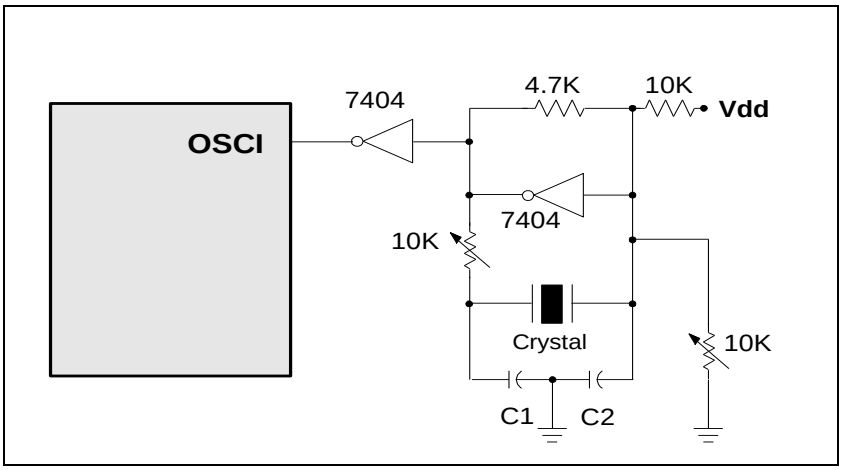


Figure 6-20 Parallel Mode Crystal/Resonator Circuit Diagram

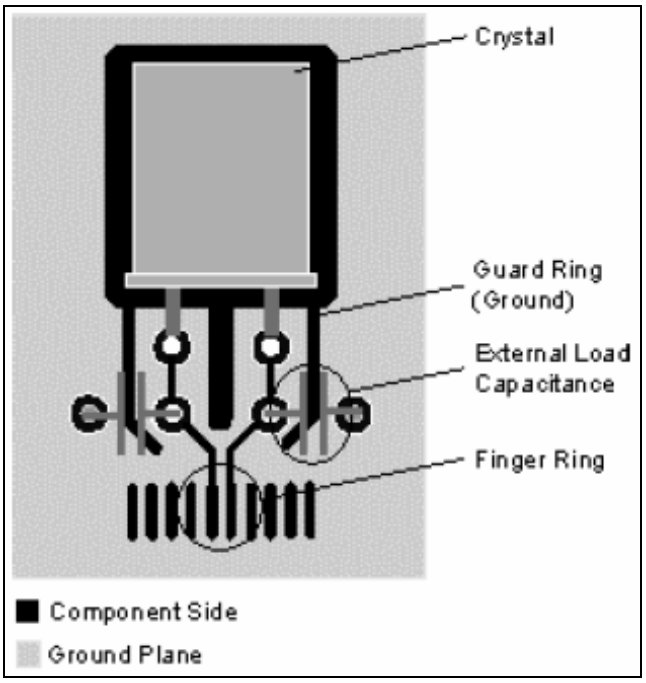


Figure 6-21 Parallel Mode Crystal/Resonator Circuit Diagram

6.11.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-22) could offer an effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

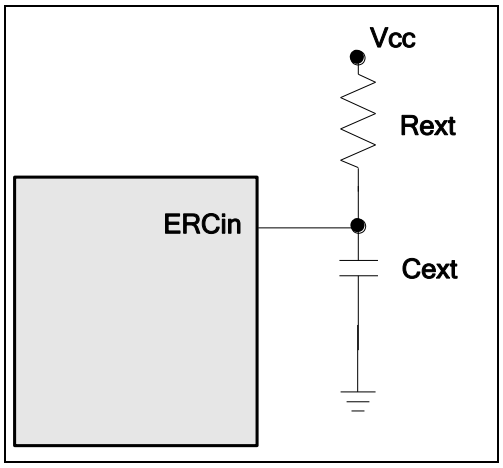


Figure 6-22 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be not lesser than 20 pF, and the value of Rext should not be greater than 1 MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot correctly discharge the capacitance current.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout have certain effects on the system frequency.

The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	2.064 MHz	1.901 MHz
	5.1k	1.403 MHz	1.316 MHz
	10k	750.0kHz	719.0kHz
	100k	81.45kHz	81.33kHz
100 pF	3.3k	647.0kHz	615.0kHz
	5.1k	430.8kHz	414.3kHz
	10k	225.8kHz	219.8kHz
	100k	23.88kHz	23.96kHz
300 pF	3.3k	256.6kHz	245.3kHz
	5.1k	169.5kHz	163.0kHz
	10k	88.53kHz	86.14kHz
	100k	9.283kHz	9.255kHz

Note: *[1]: Measured based on DIP packages.*
[2]: The values are for design reference only.
[3]: The frequency drift is ±30%

6.11.4 Internal RC Oscillator Mode

The EM78P372N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 1 MHz, and 8 MHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P372N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage	Process	Total
4 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%
16 MHz	±2%	±1% *(4.0~5.5V)	±2%	±5%
8 MHz	±2%	±1% *(3.0~5.5V)	±2%	±5%
1 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%

* Operating voltage range

Note: *Theoretical values are for reference only. Actual values may vary depending on the actual process.*

6.12 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes in steady state. The EM78P372N POR voltage range is 1.8V ~ 1.9V. Under customer application, when power is switched OFF, Vdd must drop below 1.8V and remains at OFF state for 10μs before power can be switched ON again. Subsequently, the EM78P372N will reset and work normally. The extra external reset circuit will work well if Vdd rises fast enough (50ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.12.1 Programmable WDT Time-out Period

The Option word (WDTPS) is used to define the WDT time-out period (18ms[5] or 4.5ms[6]). Theoretically, the range is from 4.5ms or 18ms. For most crystal or ceramic resonators, the lower the operation frequency is, the longer is the required set-up time.

[5] VDD=5V, WDT time-out period = 16.5ms ± 30% at 25°C
VDD=3V, WDT time-out period = 18ms ± 30% at 25°C

[6] VDD=5V, WDT time-out period = 4.2ms ± 30% at 25°C
VDD=3V, WDT time-out period = 4.5ms ± 30% at 25°C

6.12.2 External Power-on Reset Circuit

The circuits shown in the following figure implement an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow the Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time.

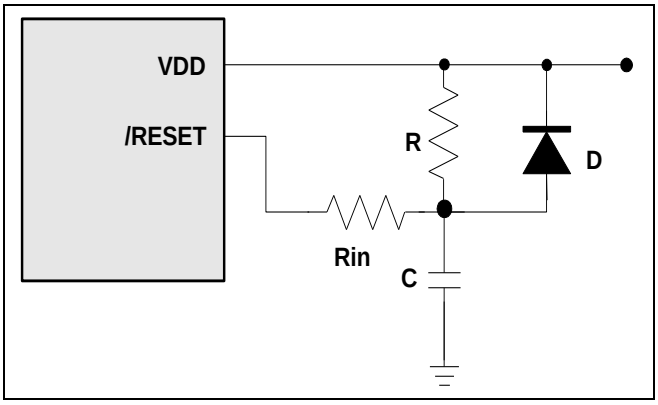


Figure 6-23 External Power-on Reset Circuit

Because the current leakage from the /RESET pin is about ± 5 μA, it is recommended that R should not be greater than 40KΩ. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

6.12.3 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-24 and Figure 6-25 show how to create a protection circuit against residual voltage.

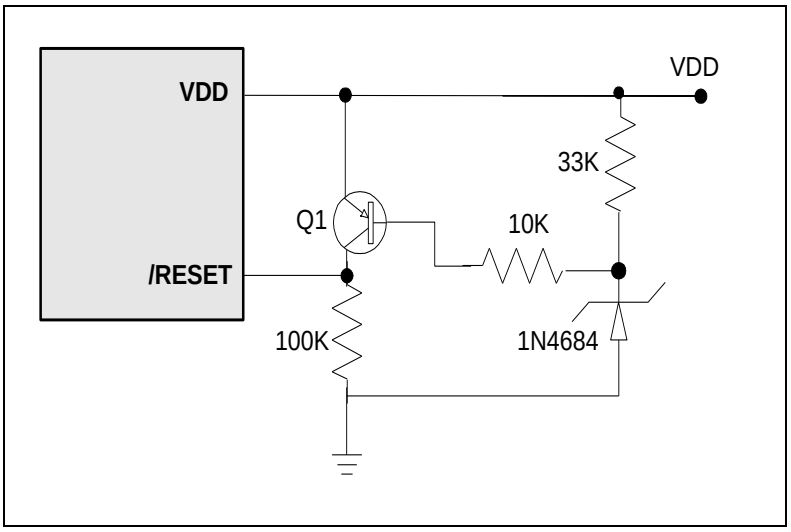


Figure 6-24 Residual Voltage Protection Circuit 1

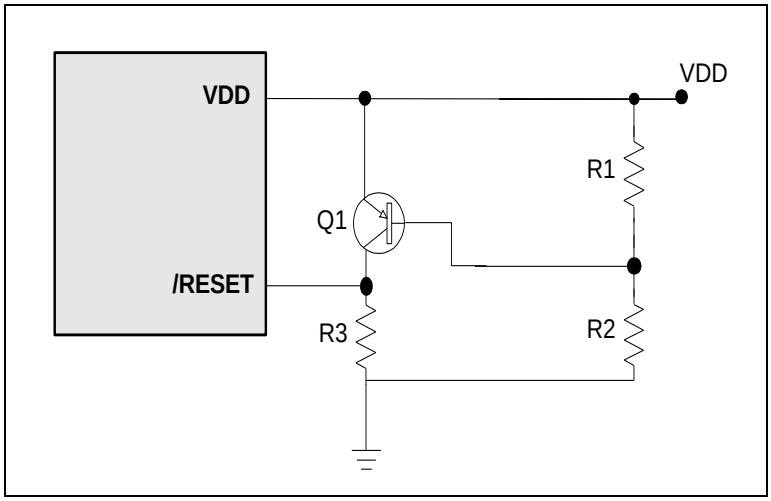


Figure 6-25 Residual Voltage Protection Circuit 2

6.13 Code Option

EM78P372N has two Code Option Words and one Customer ID word that are not part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit12 ~ Bit 0

6.13.1 Code Option Register (Word 0)

Word 0											
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 ~ 0
Mnemonic	TYPE1	TYPE0	WK_CLK	CLKS	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect
1	High	High	8 clock	High	High	High	Disable	Disable	32/fc	Enable	Disable
0	Low	Low	32 clock	Low	Low	Low	Enable	Enable	8/fc	Disable	Enable

Bits 12 ~ 11 (TYPE1 ~ TYPE0): Type selection for EM78P372N (for UWTR)

TYPE 1, TYPE 0	MCU Type	Pin Not Used
00	EM78P372N-10Pin	Port 60 ~ 66 / 54 / 56 / 57 are output low.
01	EM78P372N-14Pin	Port 62 / 63 / 64 / 65 / 56 / 57 are output low.
10	EM78P372N-18Pin	Port 56 / 57 are output low.
11	EM78P372N-20Pin (Default)	X

Bit 10 (WK_CLK): Selecting 8 or 32 clocks wake up from sleep and idle mode (only IRC mode)

0: IRC stable time + 32 clocks

1: IRC stable time + 8 clocks (default)

Bit 9 (CLKS): Instruction period option bit

0: Two oscillator periods

1: Four oscillator periods (default)

Bits 8 ~ 7 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Bit 6 (RESETEN): RESET/P71 Pin Select Bit

0: P71 set to /RESET pin

1: P71 is general purpose input pin or open-drain for output Port (default)

Bit 5 (ENWDT): Watchdog timer enable bit

0: Enable

1: Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulses define bit. The INT pin is falling or rising edge trigger.

0: Pulses equal to 8/fc is regarded as signal

1: Pulses equal to 32/fc is regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 3 (NRE): Noise Rejection Enable

0: Disable noise rejection

1: Enable noise rejection (default), but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bits 2 ~ 0 (Protect): Protect Bit

Protect Bits	Protect
0	Enable
1	Disable (default)

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	C5	C4	C3	C2	C1	C0	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	RCOUT
1	High	High	High	High	High	High	High	High	High	High	High	High	System_clk
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Open_ drain

Bits 12 ~ 7 (C5 ~ C0): Calibrator of internal RC mode C5~C0 must be set to "1" only (auto-calibration).

Bits 6 ~ 5 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (Default)
1	0	16
0	1	8
0	0	1

Bits 4 ~ 1 (OSC3 ~ OSC0): Oscillator Modes Selection bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P55/ERCin acts as ERCin P70/RCOUT acts as P70	0	0	0	0
ERC[1] (External RC oscillator mode); P55/ERCin acts as ERCin P70/RCOUT acts as RCOUT	0	0	0	1
IRC[2] (Internal RC oscillator mode); P55/ERCin acts as P55 P70/RCOUT acts as P70 (default)	0	0	1	0
IRC[2] (Internal RC oscillator mode); P55/ERCin acts as P55 P70/RCOUT acts as RCOUT	0	0	1	1
LXT1[3] (Frequency range of XT, mode is 100kHz ~ 1 MHz)	0	1	0	0
HXT1[3] (Frequency range of XT mode is 12 MHz ~ 16 MHz)	0	1	0	1
LXT2[3] (Frequency range of XT mode is 32.768kHz)	0	1	1	0
HXT2[3] (Frequency range of XT mode is 6MHz ~ 12 MHz)	0	1	1	1
XT[3] (Frequency range of XT mode is 1 MHz ~ 6 MHz)	1	1	1	1

[1] *In ERC mode, ERCin is used as oscillator pin. RCOUT/P70 is defined by code option Word 1 Bit 4 ~ Bit 1.*

[2] *In IRC mode, P55 is normal I/O pin. RCOUT/P70 is defined by code option Word 1 Bit 4 ~ Bit 1.*

[3] *In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

Bit 0 (RCOUT): Instruction clock output enable bit in IRC or ERC mode.

0: RCOUT pin output instruction clock with open drain.

1: RCOUT pin output instruction clock (default)

6.13.3 Customer ID Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	–	–	–	SFS	–	–	–	HLP	–	WDTPS	ID2	ID1	ID0
1	–	–	–	16KHz	–	–	–	High	–	18ms	High	High	High
0	–	–	–	128KHz	–	–	–	Low	–	4.5ms	Low	Low	Low

Bit 12: Not used (reserved). This bit is set to “1” all the time.

Bit 11: Not used, (reserved). This bit is set to “0” all the time.

Bit 10: Not used, (reserved). This bit is set to “1” all the time.

Bit 9 (SFS): Sub-oscillator select for GREEN mode and TCC, PWM1, PWM2 clock source (Non-include WDT time-out and free run setup-up time)

0: 128kHz

1: 16kHz (default)

Bit 8: Not used, (reserved). This bit is set to “0” all the time.

Bit 7: Not used (reserved). This bit is set to “1” all the time.

Bit 6: Not used (reserved). This bit is set to “1” all the time.

Bit 5 (HLP): Power consumption selection

0: Low power consumption mode, applies to operating frequency at 400kHz or below 400kHz

1: High power consumption mode, applies to operating frequency above 400kHz (default)

(User selects LXT1 or LXT2 in crystal mode, HLP function automatically selects low)

Bit 4: Not used, (reserved). This bit is set to “1” all the time.

Bit 3 (WDTPS): WDT Time-out Period

WDTPS	Watchdog Timer*
1	18 ms (Default)
0	4.5 ms

*Theoretical values, for reference only.

Bits 2 ~ 0: Customer’s ID code

6.14 Low Voltage Detector/Low Voltage Reset

The Low Voltage Reset (LVR) and the Low Voltage Detector (LVD) are designed for unstable power situation, such as external power noise interference or in EMS test condition.

When LVR is enabled, the system supply voltage (Vdd) drops below Vdd reset level (V_{RESET}) and remains at 10μs, a system reset will occur and the system will remain in reset status. The system will remain at reset status until Vdd voltage rises above Vdd release level. Refer to Figure 6-26 *LVD/LVR Waveform*.

If Vdd drops below the low voltage detector level, /LVD (Bit 7 of RE) is cleared to "0' to show a low voltage signal when LVD is enabled. This signal can be used for low voltage detection.

6.14.1 Low Voltage Reset

LVR property is set at Bits 8 and 7 of Code Option Word 0. Detailed operation mode is as follows:

Word 0										
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2~Bit 0
TYPE1	TYPE0	WK_CLK	CLKS	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect

Bits 8~7 (LVR1 ~ LVR0): Low Voltage Reset Enable bits.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

6.14.2 Low Voltage Detector

LVD property is set and Register detailed operation mode is as follows:

6.14.2.1 Bank 1 RE (LVD Interrupt and Wake-up Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE

NOTE

- *Bank 1 RE< 6 > register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the Bank 1 RE < 7 > to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 7 (LVDIE): Low voltage Detector interrupt enable bit.

0: Disable Low voltage Detector interrupt

1: Enable Low voltage Detector interrupt

When the detected low level voltage state is used to enter an interrupt vector or enter next instruction, the LVDIE bit must be set to “Enable“.

Bit 6 (LVDEN): Low Voltage Detector Enable bit

0: Disable Low voltage detector

1: Enable Low voltage detector

Bits 5 ~ 4 (LVD1 ~ LVD0): Low Voltage Detector level bits.

LVDEN	LVD1, LVD0	LVD voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	0

6.14.2.2 Bank 0 RE (Interrupt Status 2 and Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE

NOTE

- *Bank 0 RE < 6, 5, 4 > can be cleared by instruction but cannot be set.*
- *Bank 1 RE and IOCE0 is the interrupt mask register.*
- *Reading Bank 0 RE will result to "logic AND" of Bank 1 RE and IOCE0.*

Bit 7 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag

LVDIF is reset to “0” by software or hardware.

Bit 0 (LVDWE): Low Voltage Detect wake-up enable bit.

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

When the Low Voltage Detect is used to enter an interrupt vector or to wake up the IC from Sleep/Idle with Low Voltage Detect running, the LVDWE bit must be set to “Enable”.

6.14.3 Programming Process

Follow these steps to obtain data from the LVD:

1. Write to the two bits (LVD1: LVD0) on the LVDCR register to define the LVD level.
2. Set the LVDWE bit, if the wake-up function is employed.
3. Set the LVDIE bit, if the interrupt function is employed.
4. Write “ENI” instruction, if the interrupt function is employed.
5. Set LVDEN bit to 1
6. Write “SLEP” instruction or Polling /LVD bit.
7. Clear the low voltage detector interrupt flag bit (LVDIF) when Low Voltage Detector interrupt occurred.

The LVD module uses the internal circuit. When LVDEN (Bit 6 of Bank 1-RE) is set to “1”, the LVD module is enabled.

When LVDWE (Bit 0 of RE) is set to “1”, the LVD module will continue to operate during sleep/idle mode. If Vdd drops slowly and crosses the detect point (VLVD), the LVDIF (Bit 6 of RE) will be set to “1”, the /LVD (Bit 7 of RE) will be cleared to “0”, and the system will wake up from Sleep/Idle mode. When a system reset occurs, the LVDIF will be cleared.

When Vdd remains above VLVD, LVDIF is kept at “0” and /LVD is kept at “1”. When Vdd drops below VLVD, LVDIF is set to “1” and /LVD is kept at “0”. If the ENI instruction is executed, LVDIF will be set to “1”, and the next instruction will branch to interrupt Vector 021H. The LVDIF is cleared to “0” by software. Refer to Figure 6-26 below.

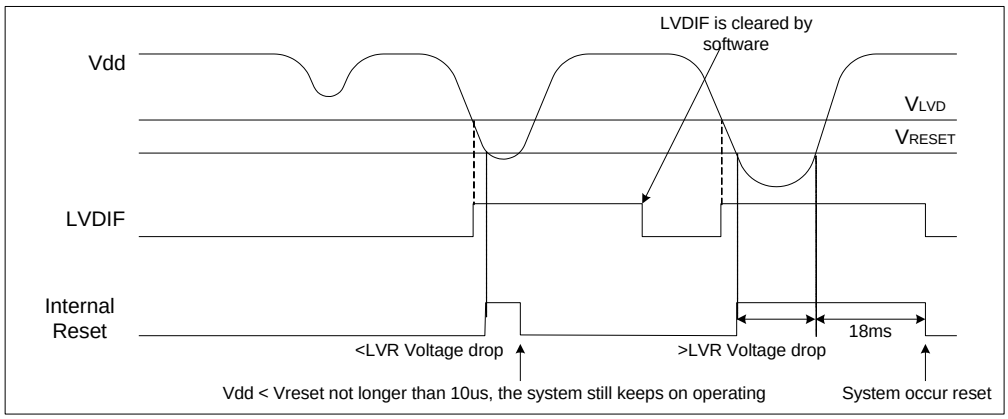


Figure 6-26 LVD/LVR Waveform

6.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.).

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The following symbols are used in the Instruction Set table:

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bits 6 and 7 in R4 determine the selected register bank.

b *= Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ VR → A	Z
OR R,A	A ∨ VR → R	Z

Mnemonic	Operation	Status Affected
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A (7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None [2]
BS R,b	1 → R(b)	None [3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
BANK k	k →R4(6)	None
LCALL k	PC+1→[SP], k→PC	None
LJMP k	k→PC	None
TBRD R	If Bank1 R5.7=0, machine code (7~0) → R Else Bank1 R5.7=1, machine code (12~8) → R(4~0), R(7~5)=(0,0,0)	None

Note: *[1] This instruction is applicable to IOC50~IOCF0, IOC51 ~ IOCF1 only.*
[2] This instruction is not recommended for RF operation.
[3] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768k	4	16	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	760	950	1140	kHz
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	0.7VDD	–	VDD+0.3	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	–	1.8	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	1.1	–	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD+0.3	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = 0.9VDD	–	-3.7	–	mA
IOH2	Output High Voltage (Ports 51~54, 56~57,60~67)			-10		
IOL1	Output Low Voltage (Ports 5, 6, 7)	VOL = 0.1VDD	–	10	–	mA
IOL2	Output Low Voltage (Ports 51~54, 56~57,60~67)			25		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LVR1	Low voltage reset level	Ta= 25°C	2.41	2.7	2.99	V
		Ta= -40~85°C	2.14	2.7	3.25	V
LVR2	Low voltage reset level	Ta= 25°C	3.1	3.5	3.92	V
		Ta= -40~85°C	2.73	3.5	4.25	V
LVR3	Low voltage reset level	Ta= 25°C	3.56	4.0	4.43	V
		Ta= -40~85°C	3.16	4.0	4.81	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–	70	–	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	–	40	–	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	10	μA
ICC1	Operating supply current at two clocks (VDD = 3V)	/RESET= 'High', Fosc=32.768kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	20	μA
ICC2	Operating supply current at two clocks (VDD = 3V)	/RESET= 'High', Fosc=32.768kHz (Crystal type,CLKS="0"), Output pin floating, WDT enabled	–	15	25	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	1.5	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.8	3.0	mA

Note: *1. These parameters are hypothetical (not tested) and are provided for design reference use only.*

2. Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25℃. These data are for design reference only.

Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.92 MHz	4 MHz	4.08 MHz
16 MHz	25°C	5V	15.68 MHz	16 MHz	16.32 MHz
1 MHz	25°C	5V	0.98 MHz	1 MHz	1.02 MHz
8 MHz	25°C	5V	7.84 MHz	8 MHz	8.16 MHz

Internal RC Electrical Characteristics (Ta=-40 ~ 85°C, VDD=2.1 ~ 5.5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40°C ~85°C	2.1V~5.5V	3.80 MHz	4 MHz	4.20 MHz
16 MHz	-40°C ~85°C	2.1V~5.5V	15.2 MHz	16 MHz	16.8 MHz
1 MHz	-40°C ~85°C	2.1V~5.5V	0.95 MHz	1 MHz	1.05 MHz
8 MHz	-40°C ~85°C	2.1V~5.5V	7.60 MHz	8 MHz	8.40 MHz

8.1 AD Converter Characteristics

Vdd=5V, Vss=0V, Ta= 25°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VAREF=VDD=5.0V, VASS=0.0V, FS*1=100kHz, FIN*1=1kHz (VREF is internal VDD)	–	–	1400	µA
	Ivref			–	–	10	µA
IAI2	Ivdd	Analog supply current	VAREF=VDD=5.0V, VASS=0.0V, FS*1=100kHz, FIN*1=1kHz (VREF is external VREF pin)	–	–	900	µA
	IVref			–	–	500	µA
RN		Resolution	–	–	12	–	Bits
INL		Integral Nonlinearity	VAREF=VDD=5.0V VASS=0.0V, FS*1=100kHz, FIN*1=1kHz	–	–	±4	LSB
DNL		Differential nonlinear error	VAREF=VDD=5.0V VASS=0.0V, FS*1=100kHz, FIN*1=1kHz	–	–	±1	LSB
FSE		Full scale error	VAREF=VDD=5.0V VASS=0.0V, FS*1=100kHz	–	–	±8	LSB
OE		Offset error	VAREF= Vdd=5.0V VASS=0.0V, FS*1=100kHz	–	–	±4	LSB
ZAI		External impedance of ADC input channel.	–	–	–	10	KΩ
TAD		Period of ADC clock	VDD=3~5.5V, VASS = 0.0V, FIN*1=1kHz				
			VDD=2.5~3V, VASS = 0.0V, FIN*1=1kHz				
Tsh		Sample and Hold Time	VDD=3~5.5V, V_{ASS} = 0.0V, Ta=25°C	4	–	–	µs
			VDD=2.5~3V, V_{ASS} = 0.0V, Ta=25°C	16	–	–	µs
TCN		AD conversion time (Include S/H Time)	VDD=2.5~5.5V, V_{ASS} = 0.0V	14	–	24	TAD
TADD1		AD delay time between setting "ADRUN" and starting 1st TAD	VDD=2.5~5.5V, VASS=0.0V				
PSRR		Power Supply Rejection	V_{AREF}= 2.5V, VAREF=2.5V, VASS=0V,	–	–	2	LSB

	Ratio	VIN[*1]=0V~2.5V, FS[*1]=25kHz				
$V_{1/4VDD}$	Accuracy for 1/4 VDD		–	±3	–	%

Note:

1. *FS is Sample Rate, that is to say, conversion rate. FIN is freq. of input test sine wave*
2. *The parameters are theoretical values and have not been tested. Such parameters are for design reference only.*
3. *There is no current consumption when ADC is off other than minor leakage current.*
4. *AD conversion result will not decrease with an increase of input voltage and no missing code.*
5. *These parameters are subject to change without further notice.*

8.2 Comparator Characteristics

Vdd = 5.0V, Vss=0V, Ta = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	–	–	–	10	mV
Vcm	Input common-mode voltage range	–	GND	–	VDD	V
ICO	Supply current of comparator	Co=0V, Ta= -40~85C	–	160	–	uA
TRS	Response time	VREF=1.0V, VRL=5V, RL=5.1k, CL=15p (Note[1])	–	1	–	us
TLRS	Large signal response time	VREF=2.5V, VRL = 5V, RL = 5.1k (Note[2])	–	250	–	ns
IOL	Output sink current	Vi(-) = 1V, Vi(+) = 0V, Vo = GND+0.5V (Note[3])	–	12	–	mA
VSAT	Saturation voltage	Vi(-)=1V, Vi(+)=0V, IOL <= 4mA (Note[3])	–	0.2	0.4	V

Note: *1. These parameters are hypothetical (not tested) and provided for design reference use only.*

*2. The response time specified is at 0V~VDD input step with 1/2*VDD overdrive.*

3. The driving ability is determined by the digital output block.

8.3 OP Characteristics

Vdd = 5.0V, Vss=0V, Ta= 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	Vin+=0V	–	–	10	mV
SR	Slew rate	Ta= -40~85°C	–	1.5	–	V/μs
IVR	Input voltage range	–	0	–	5	V
OVS	Output voltage swing	Vip=0V,I_L=1.0mA Ta= -40~85°C	–	123	–	mV
		Vip=5V, I_L=1.0mA Ta= -40~85°C	–	4.68	–	V
IOP	Supply current of OP	Ta= -40~85°C	–	255	–	μA
PSRR	Power supply rejection ratio	Ta= -40~85°C	–	75	–	dB
CMRR	Common mode reject ratio	$0V \leqq V_{CM} \leqq V_{DD}$	–	90	–	dB
GBP	Gain bandwidth product	RL=1Meg, CL=100p	–	2.6	–	MHz

8.4 VREF 2V/3V/4V Characteristics

Vdd = 5.0V, Vss=0V, Ta= -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply	–	2.1	–	5.5	V
I_{VDD}	DC Supply Current	No load	–	–	250	μA
Vref	Accuracy for Vref	2V, 3V, 4V	–	±1	1.75	%
Warn up time	Time ready for voltage reference	VDD=VDD_{min} - 5.5V, Cload = 19.2pf Rload=15.36KΩ	–	30	50	μs
VDD_{min}	Minimum Power Supply	–	–	Vref + 0.2*	–	V

*VDD_{min} : can work at (Vref+0.1V), but will have a poor PSRR.

8.5 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphs, the data maybe out of the specified warranted operating range.

8.5.1 Graphs of P5/P6/P7 Vih/Vil vs. VDD

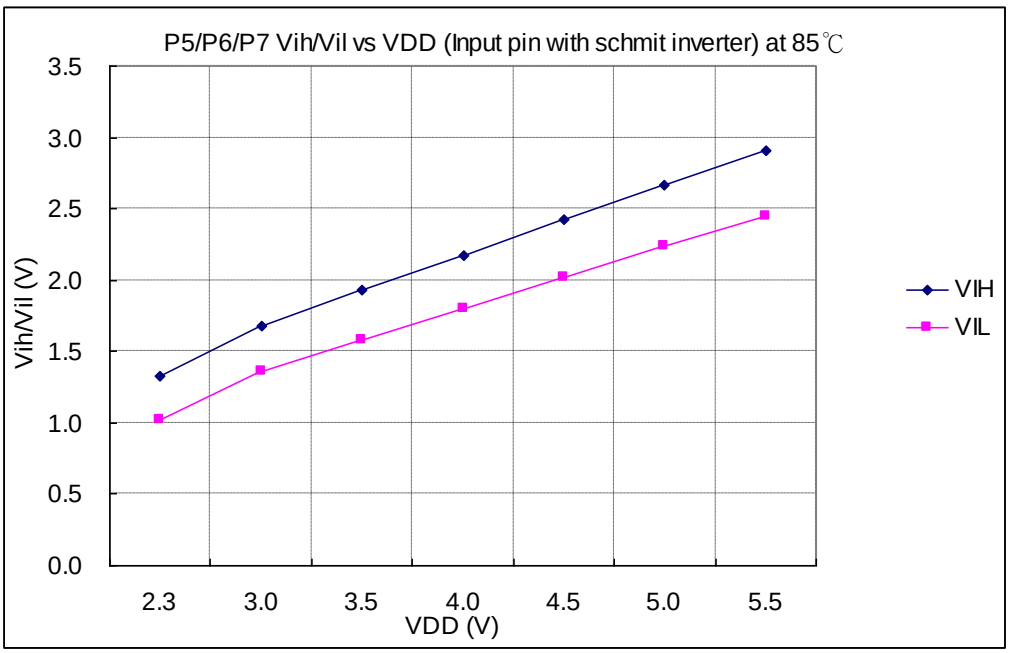


Figure 8-1(a) P5/P6/P7 Vih/Vil vs. VDD @ 85°C

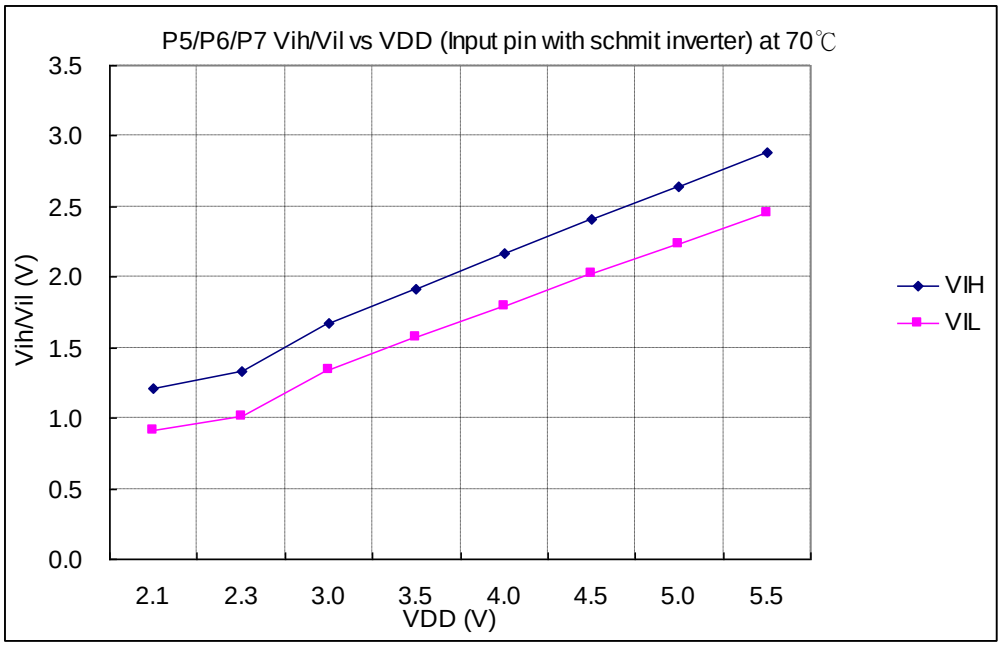


Figure 8-1(b) P5/P6/P7 Vih/Vil vs. VDD @ 70°C

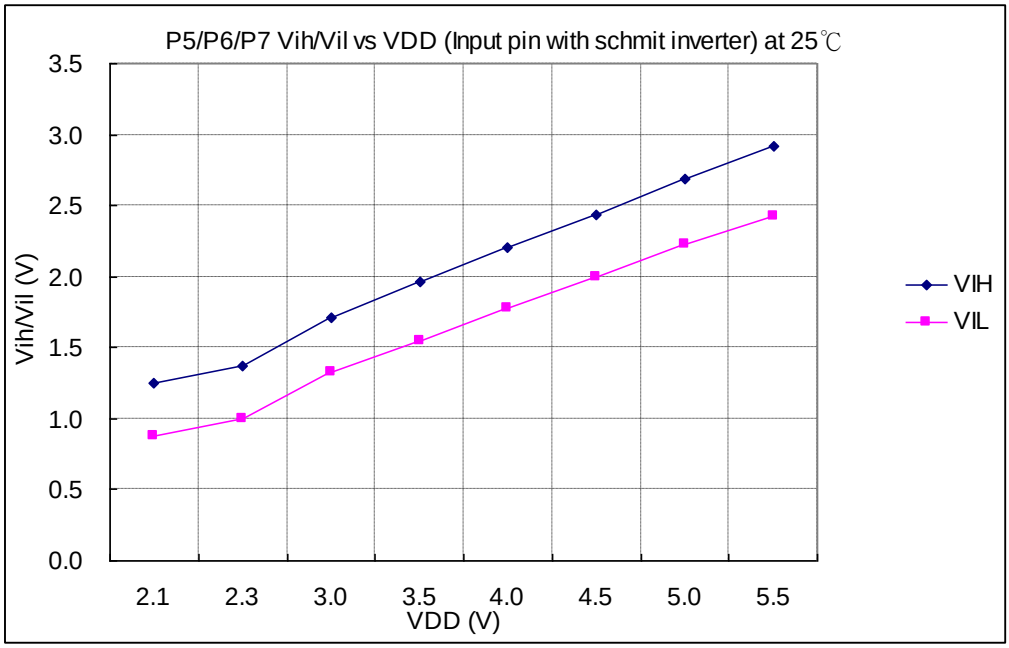


Figure 8-1(c) P5/P6/P7 Vih/Vil vs. VDD @ 25°C

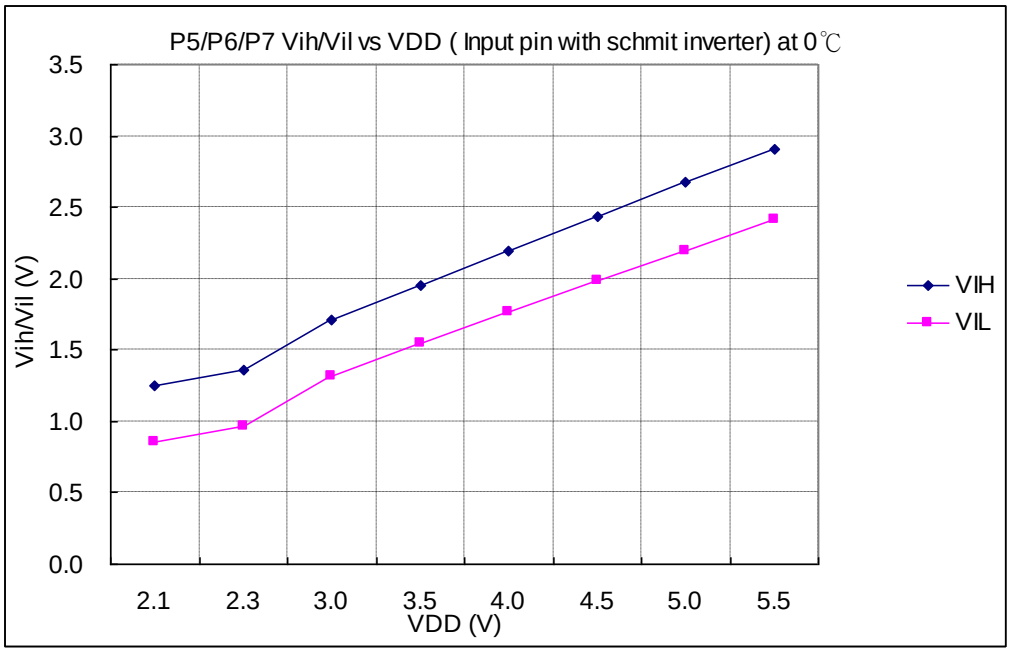


Figure 8-1(d) P5/P6/P7 Vih/Vil vs. VDD @ 0°C

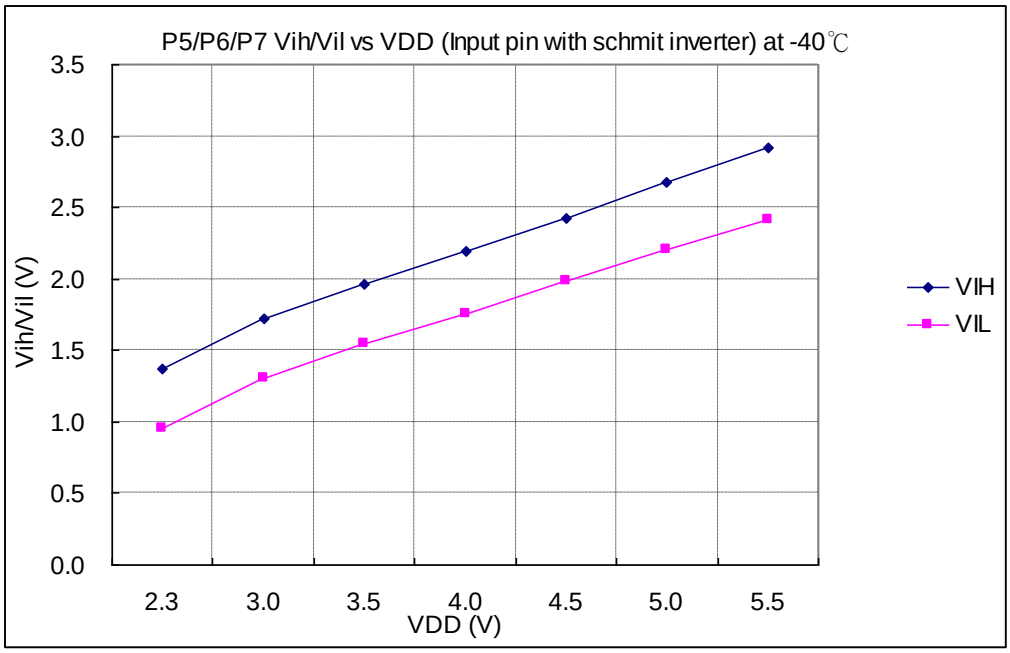


Figure 8-1(e) P5/P6/P7 Vih/Vil vs. VDD @ -40°C

8.5.2 Graphs of P5/P6/P7 Ioh1 vs. Voh

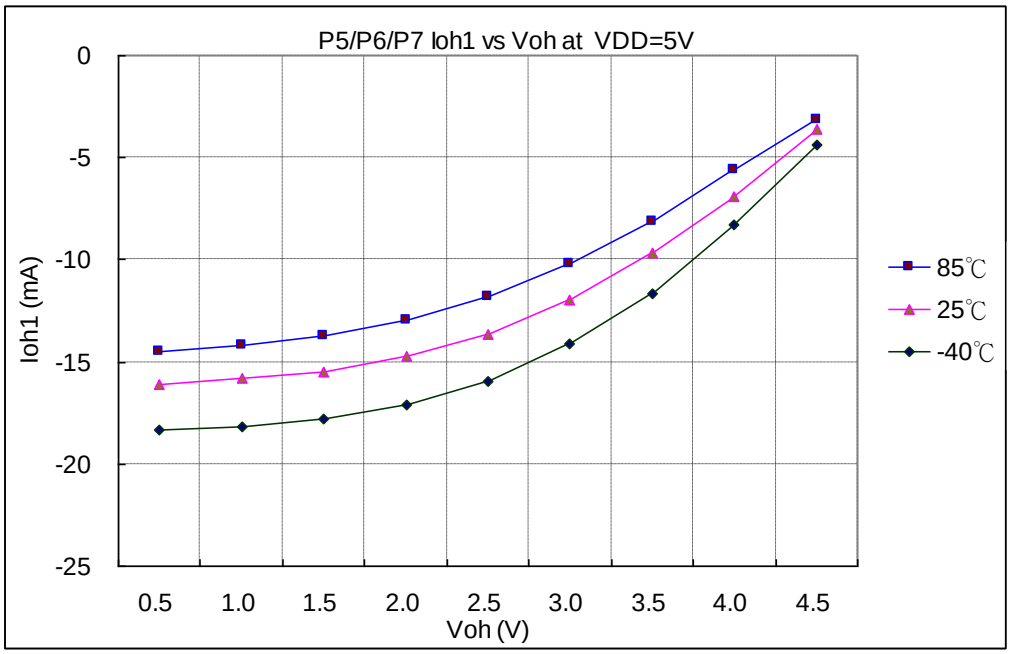


Figure 8-2(a) P5/P6/P7 Ioh1 vs. Voh, VDD=5V

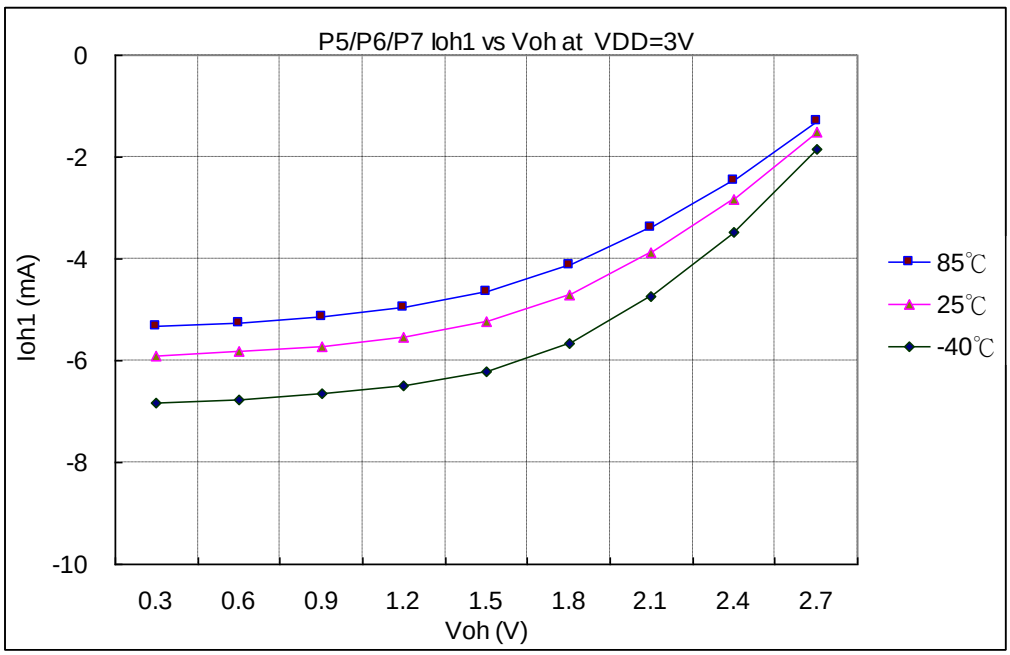


Figure 8-2(b) P5/P6/P7 Ioh1 vs. Voh, VDD=3V

8.5.3 Graphs of P51~P54, P56/P57/P60~P67 Ioh1 vs. Voh

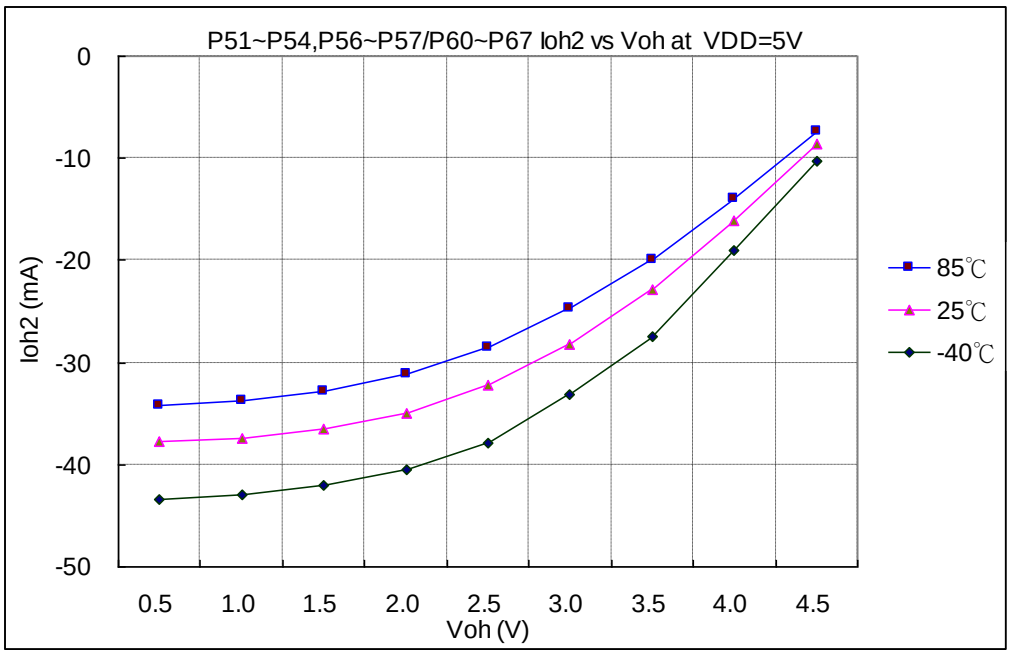


Figure 8-3(a) P51~P54, P56/P57/P60~P67 Ioh2 vs. Voh, VDD=5V

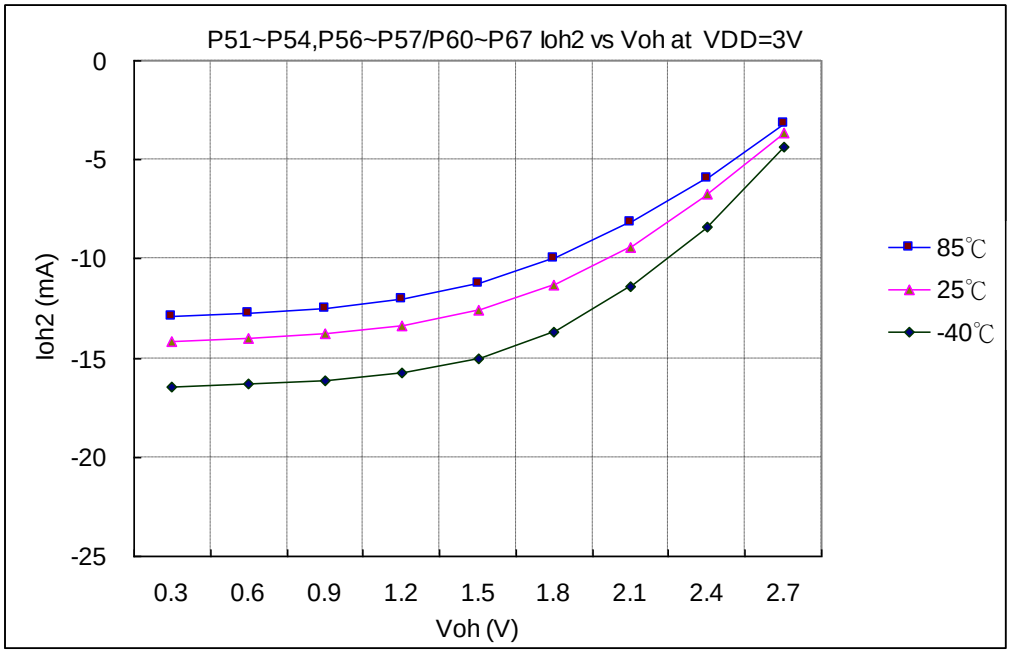


Figure 8-3(b) P51~P54, P56/P57/P60~P67 Ioh2 vs. Voh, VDD=3V

8.5.4 Graphs of P5/P6/P7 Iol1 vs. Vol

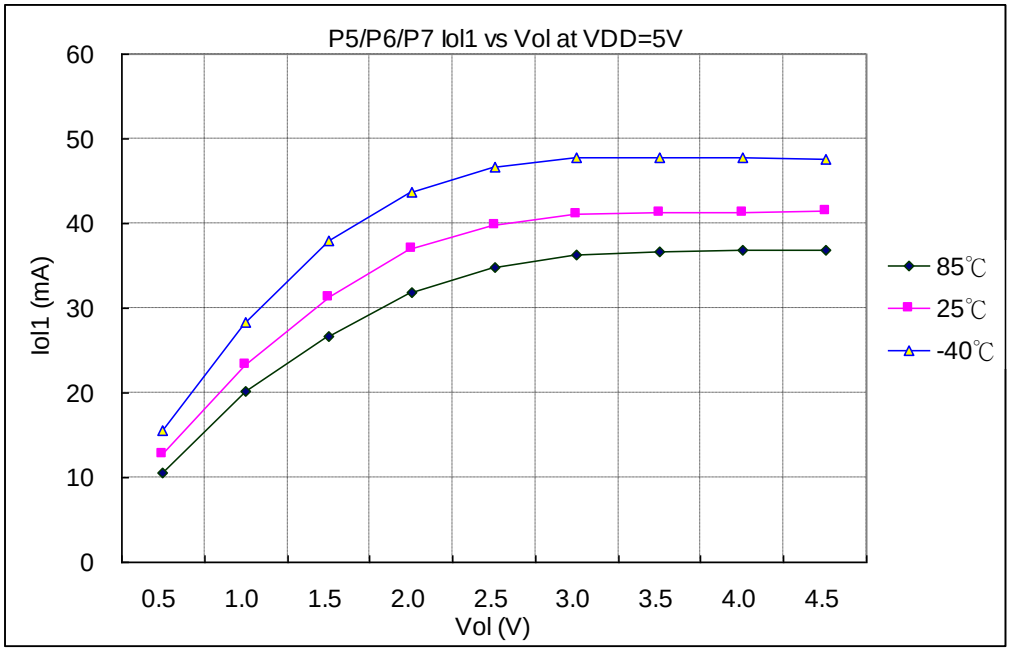


Figure 8-4(a) P5/P6/P7 Iol1 vs. Vol, VDD=5V

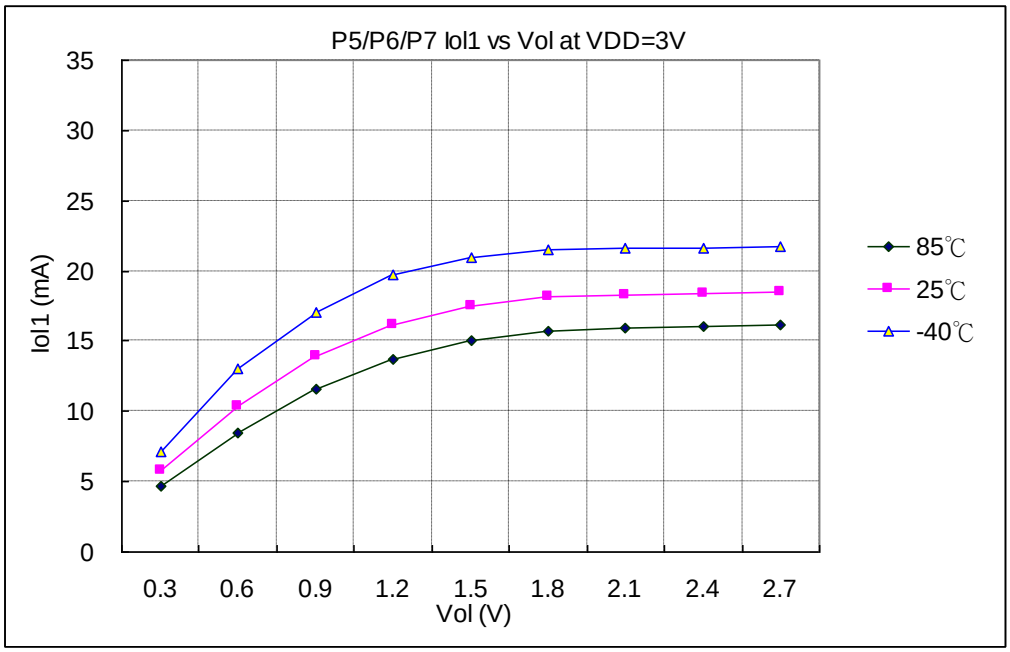


Figure 8-4(b) P5/P6/P7 Iol1 vs. Vol, VDD=3V

8.5.5 Graph of P51~P54, P56/P57/P60~P63 Iol2 vs. Vol

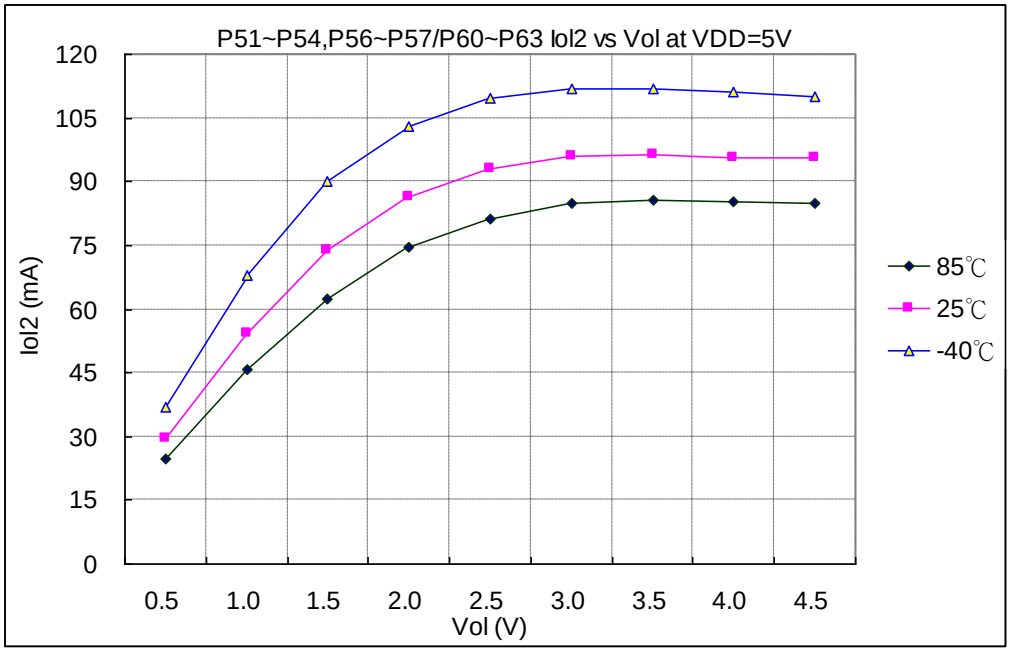


Figure 8-5(a) P51~P54, P56/P57/P60~P63 Iol2 vs. Vol, VDD=5V

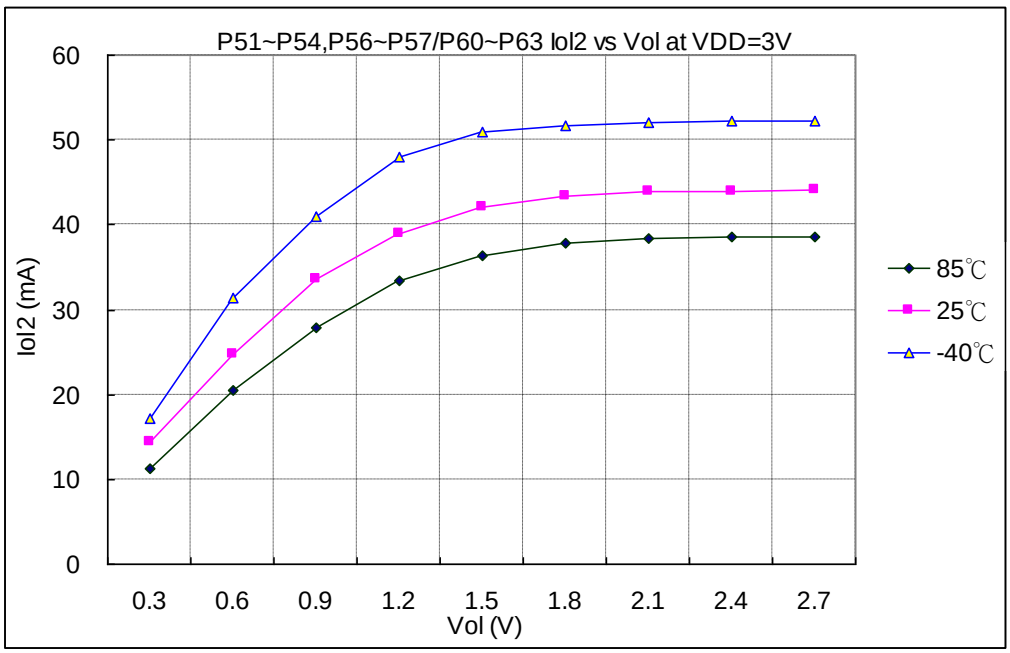


Figure 8-5(b) P51~P54, P56/P57/P60~P63 Iol2 vs. Vol, VDD=3V

8.5.6 Graphs of P5/P6 IPH vs. Temperature at VDD=3V and 5V

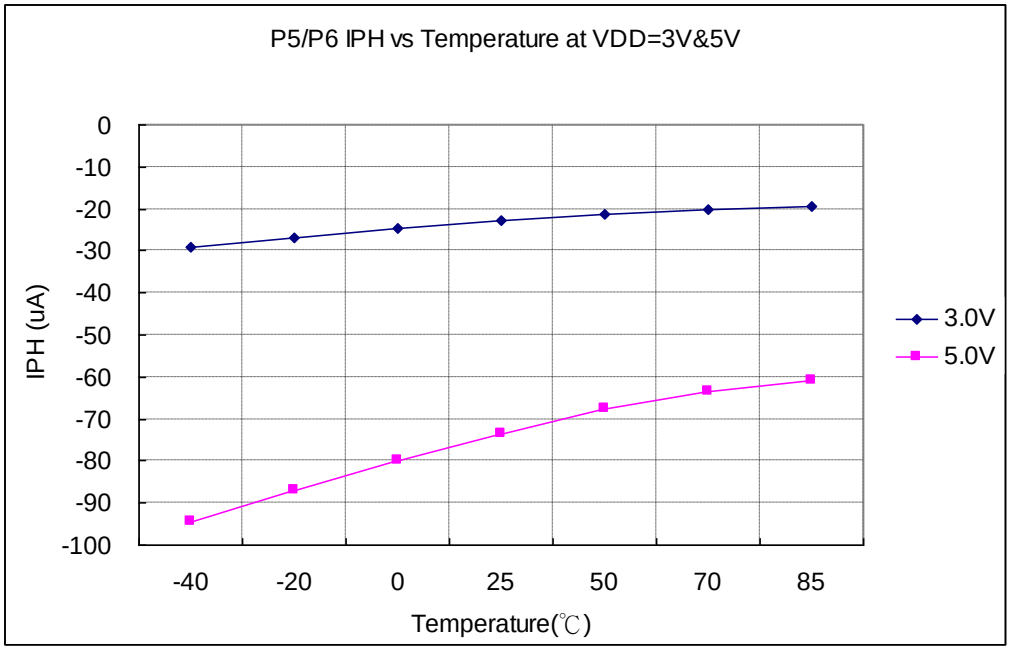


Figure 8-6 P5/P6 IPH vs. Temperature, VDD=3V&5V

8.5.7 Graphs of P5 IPL vs. Temperature at VDD=3V and 5V

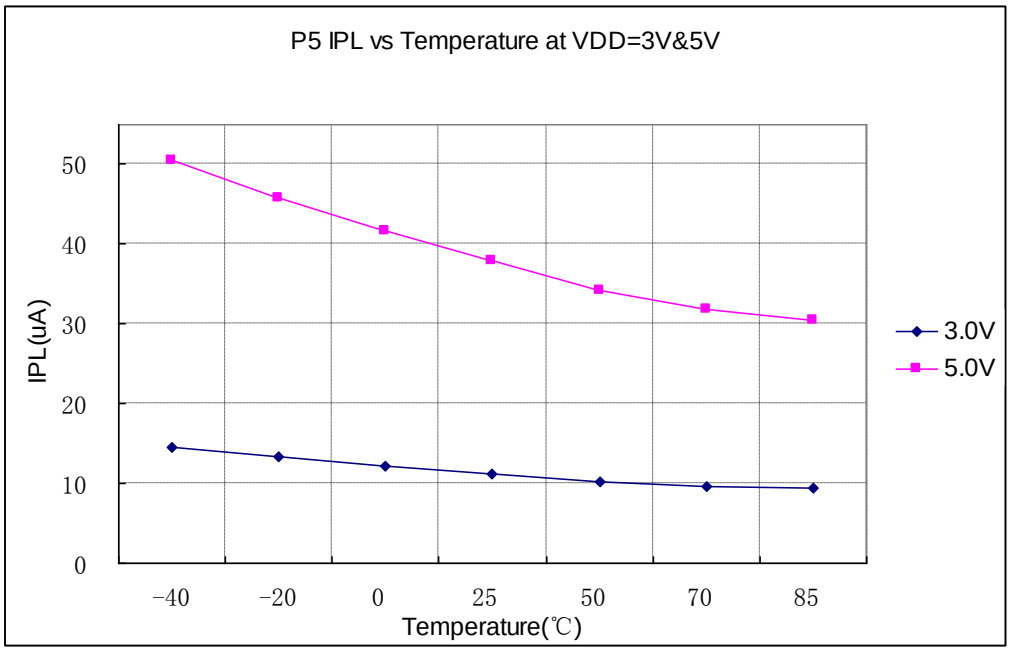


Figure 8-7 P5/P6 IPL vs. Temperature, VDD=3V&5V

8.5.8 Graphs of Typical ICC1 and ICC2 vs. Temperature

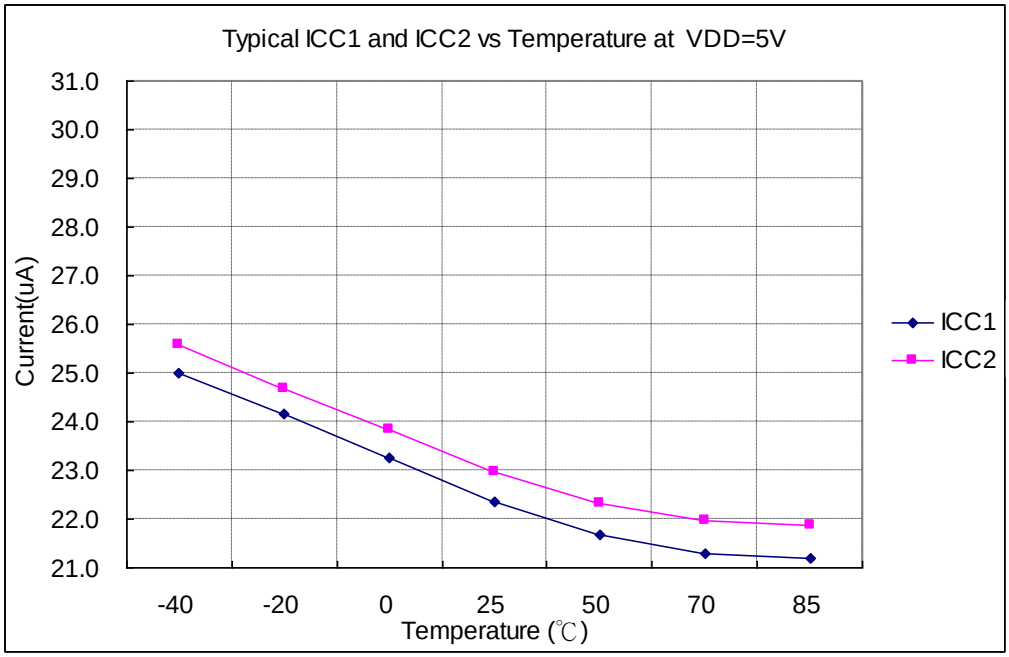


Figure 8-8(a) Typical Operating Current ICC1/ICC2 vs. Temperature, VDD=5V

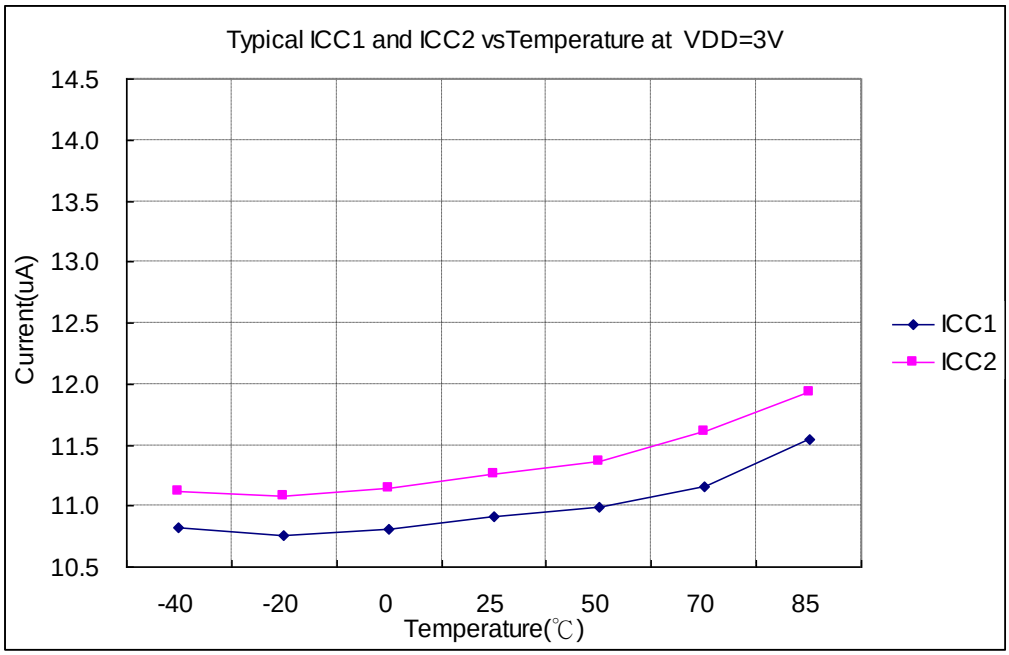


Figure 8-8(b) Typical Operating Current ICC1/ICC2 vs. Temperature, VDD=3V

8.5.9 Graphs of Typical ICC3 and ICC4 vs. Temperature

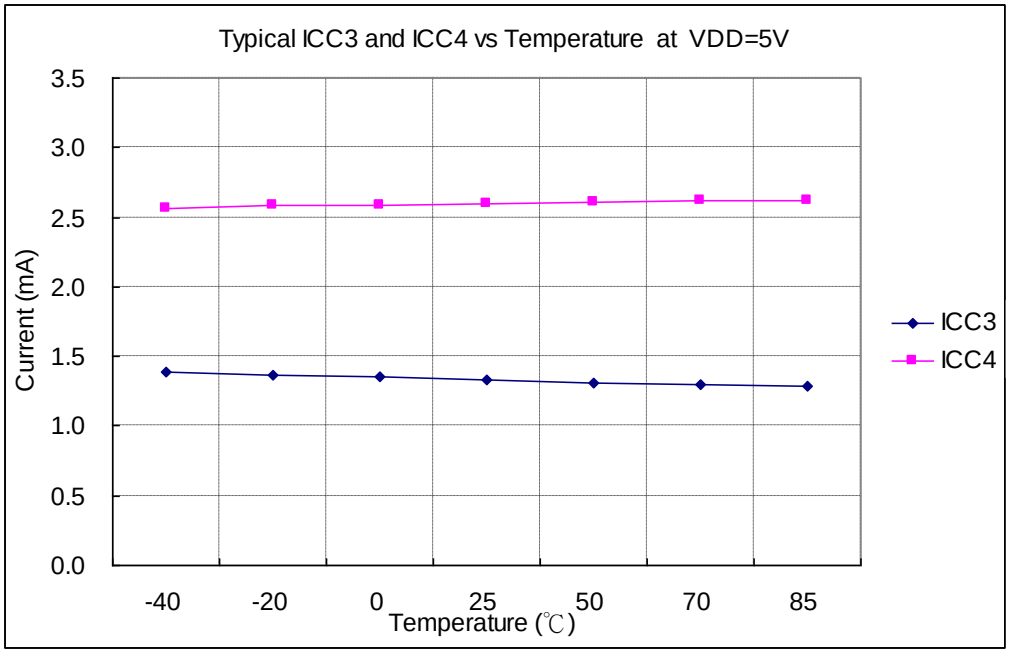


Figure 8-9(a) Typical Operating Current ICC3/ICC4 vs. Temperature, VDD=5V

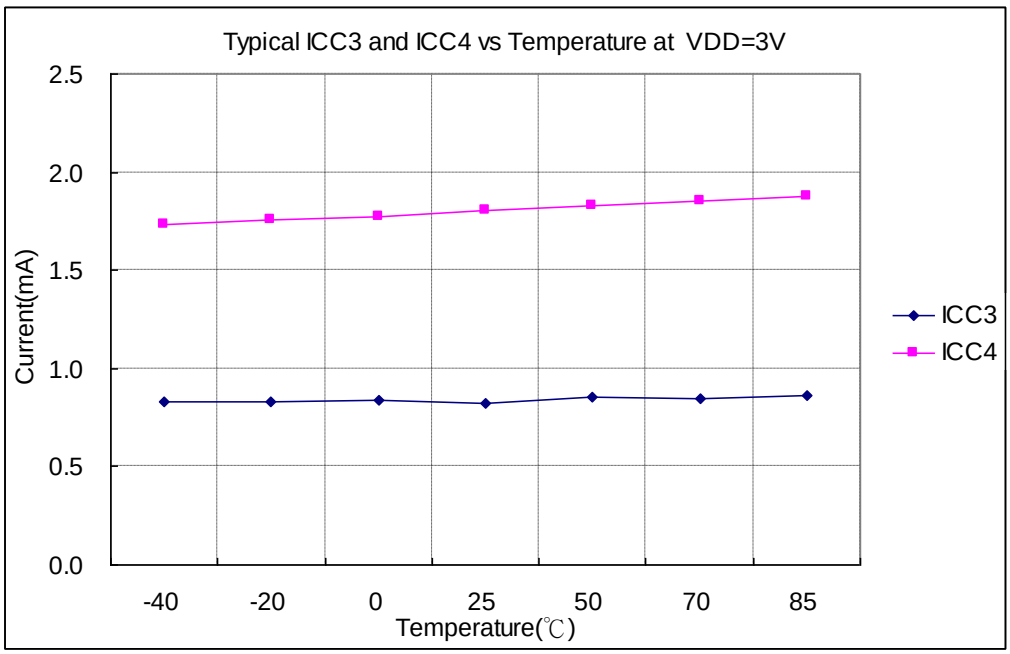


Figure 8-9(b) Typical Operating Current ICC3/ICC4 vs. Temperature, VDD=3V

8.5.10 Graphs of Wake-up Time from Sleep to Normal Mode vs. VDD

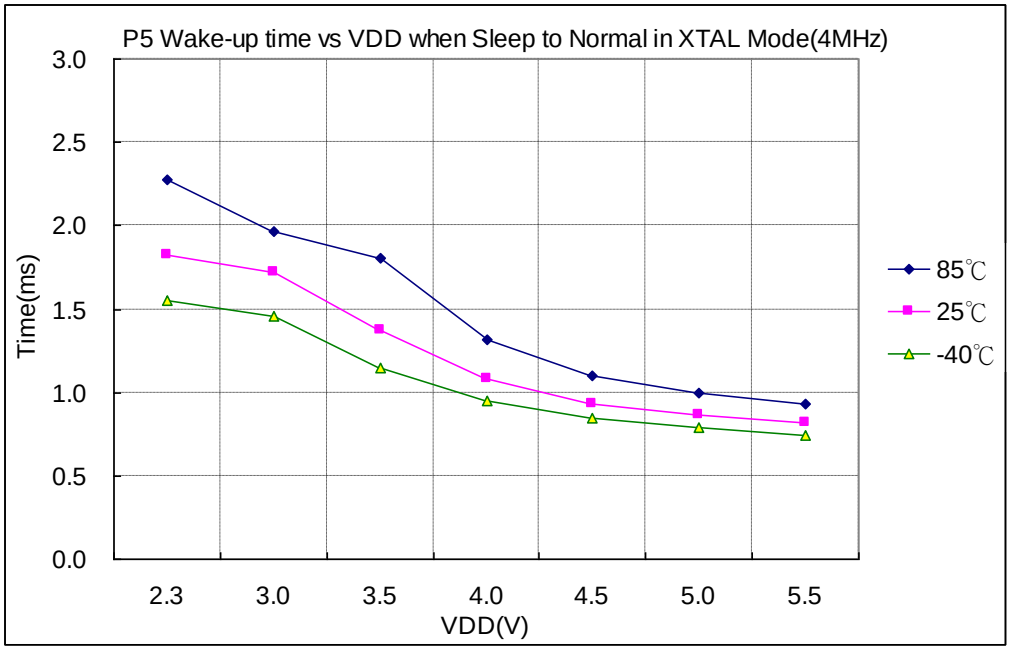


Figure 8-10(a) Wake-up Time from Sleep Mode vs. VDD with XTAL=4MHz

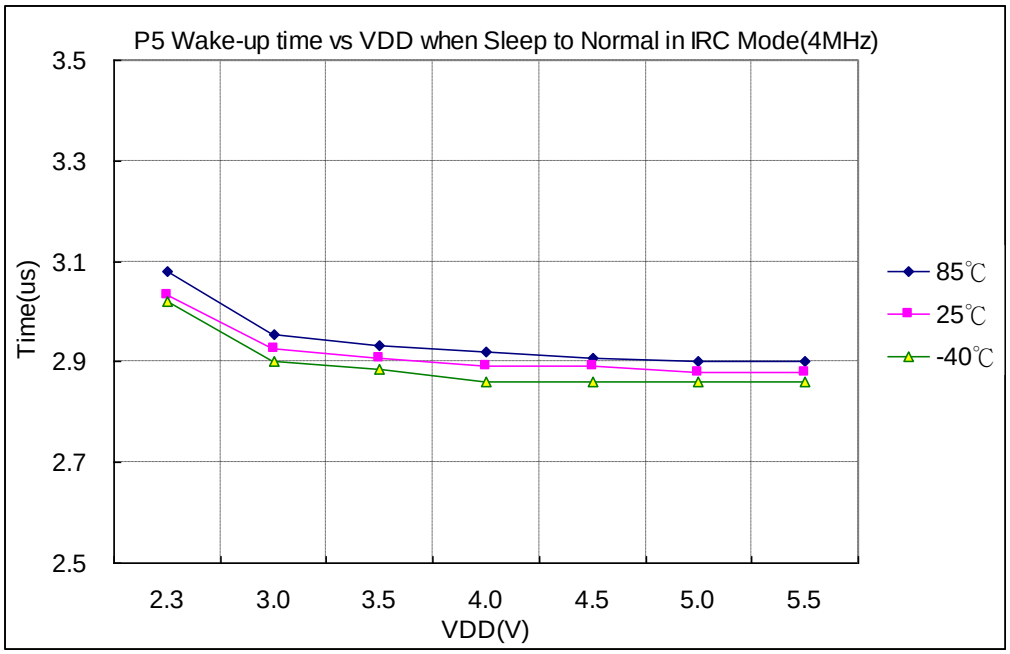


Figure 8-10(b) Wake-up Time from Sleep Mode vs. VDD with IRC=4MHz

8.5.11 Graphs of Wake-up Time from Idle to Normal Mode vs. VDD

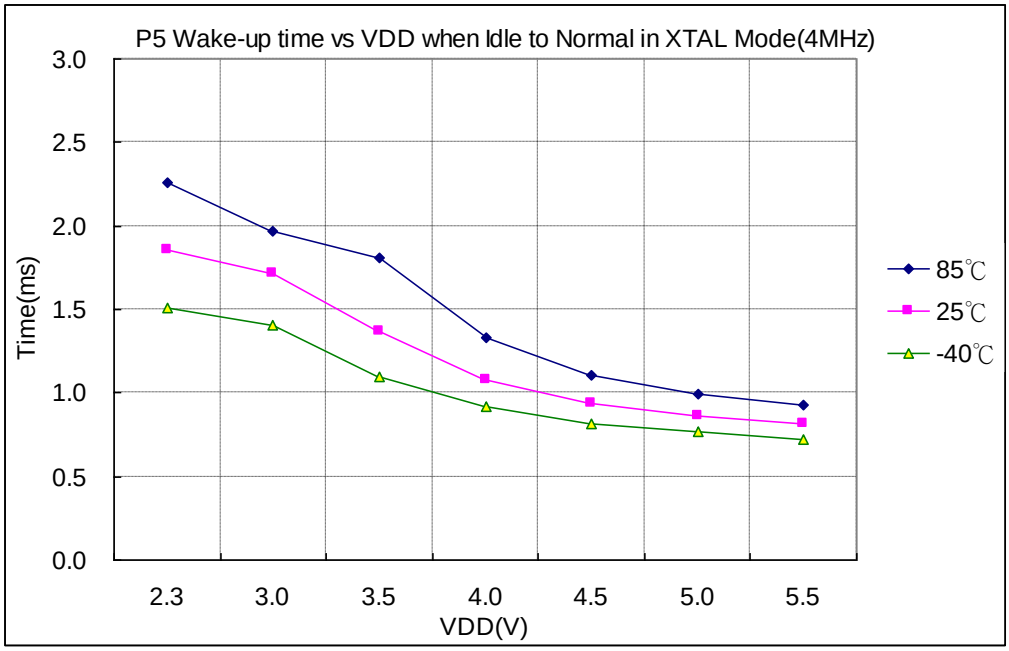


Figure 8-11(a) Wake-up Time from Idle Mode vs. VDD with XTAL=4MHz

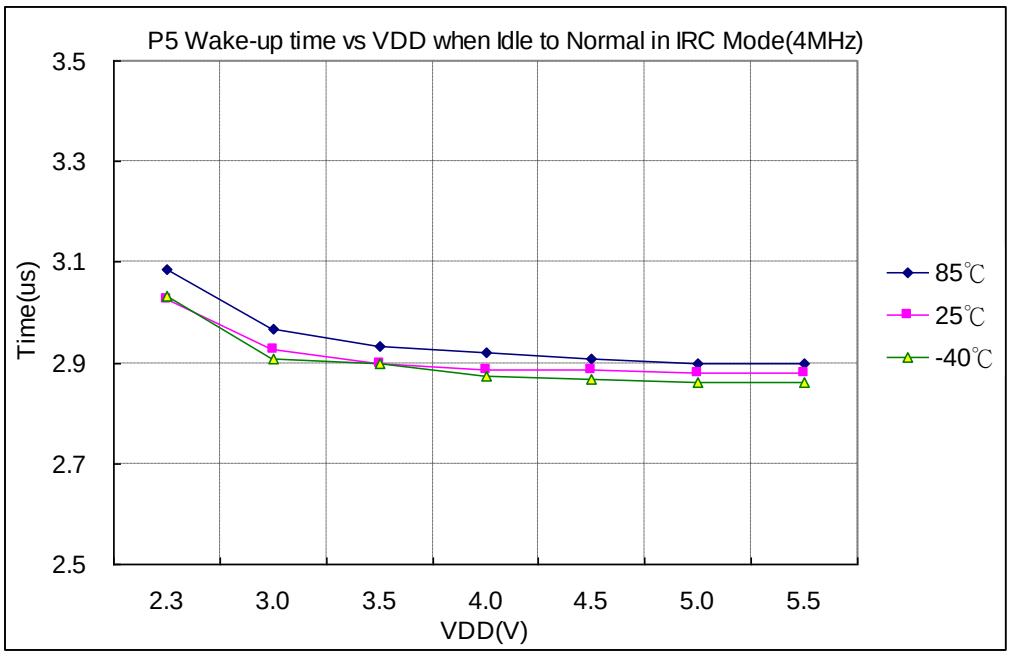


Figure 8-11(b) Wake-up Time from Idle Mode vs. VDD with IRC=4MHz

8.5.12 Graphs of WTD Time Out Period in Normal Mode vs. VDD

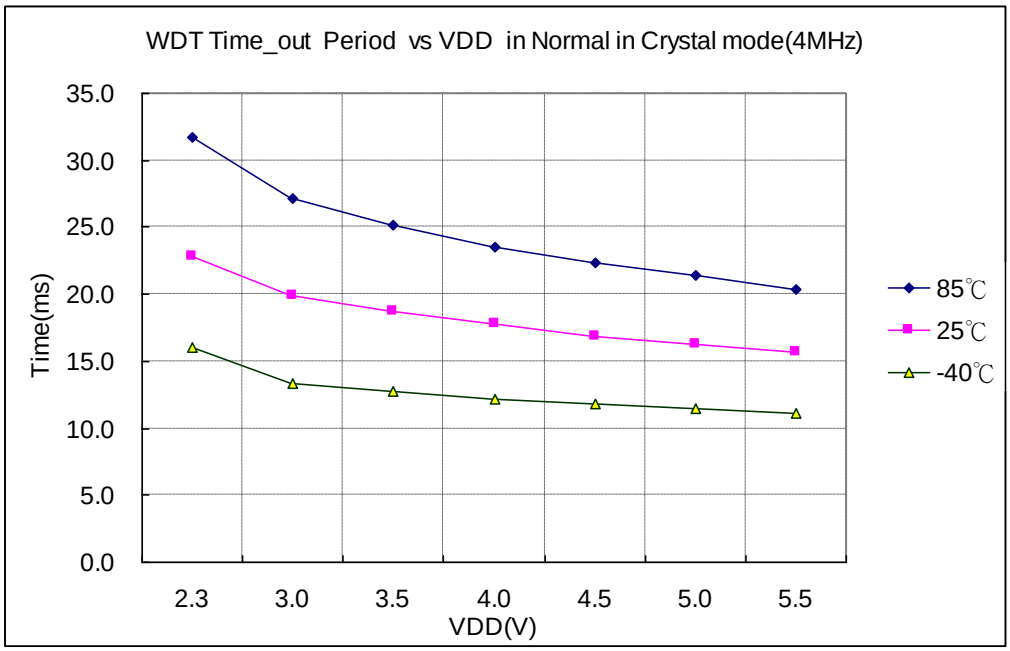


Figure 8-12(a) WDT Time Out Period in Normal Mode vs. VDD with XTAL=4MHz

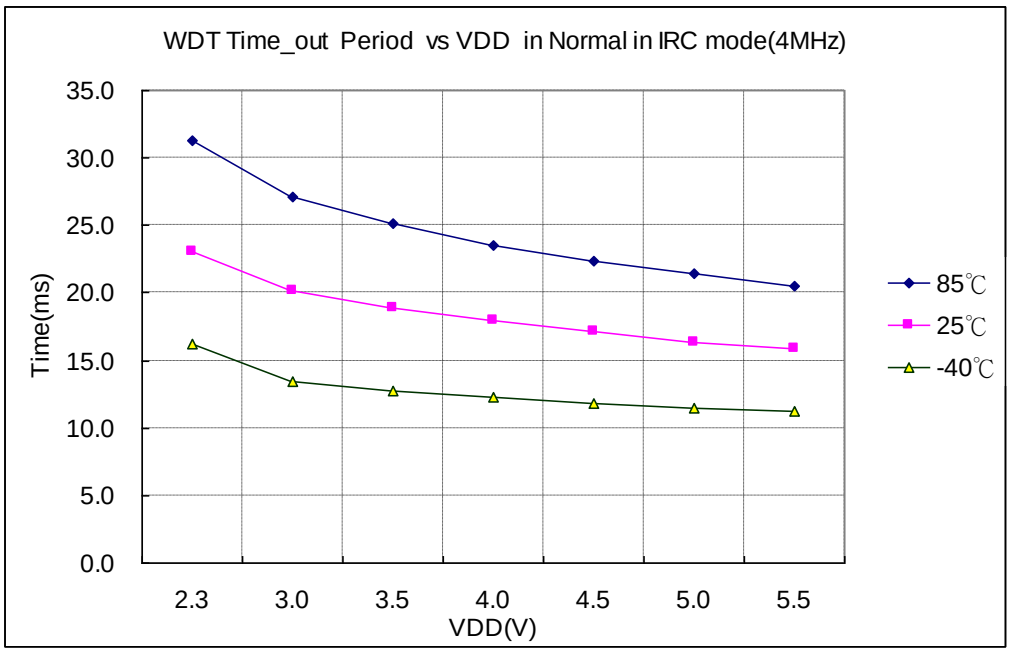


Figure 8-12(b) WDT Time Out Period in Normal Mode vs. VDD with IRC=4MHz

8.5.13 Graphs of Power-on Reset Time in Normal Mode vs. VDD

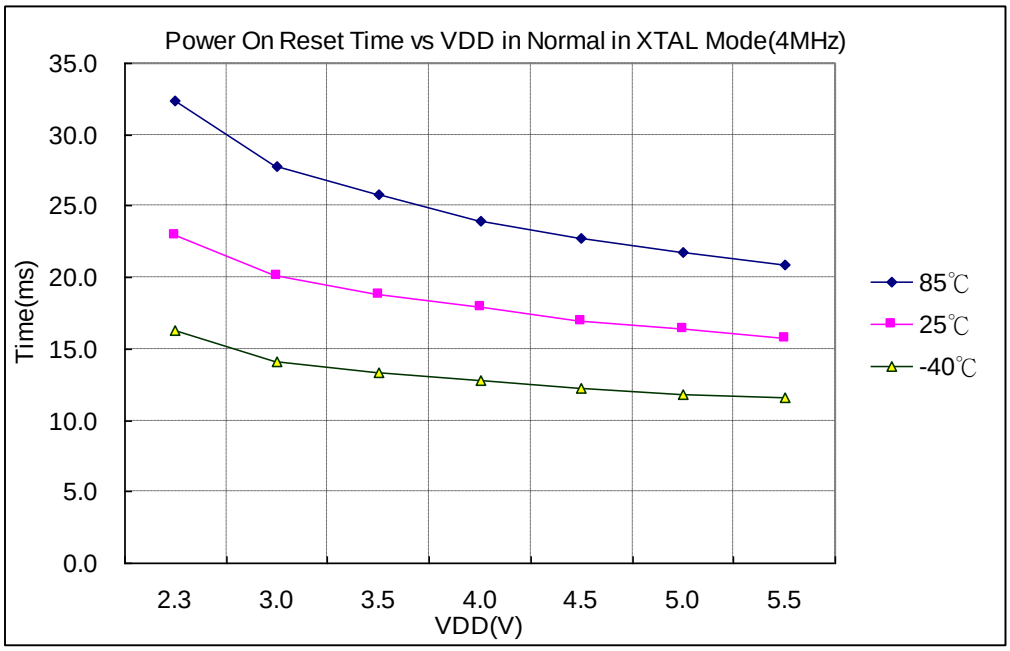


Figure 8-13(a) Power-on Reset Time in Normal Mode vs. VDD with XTAL=4MHz

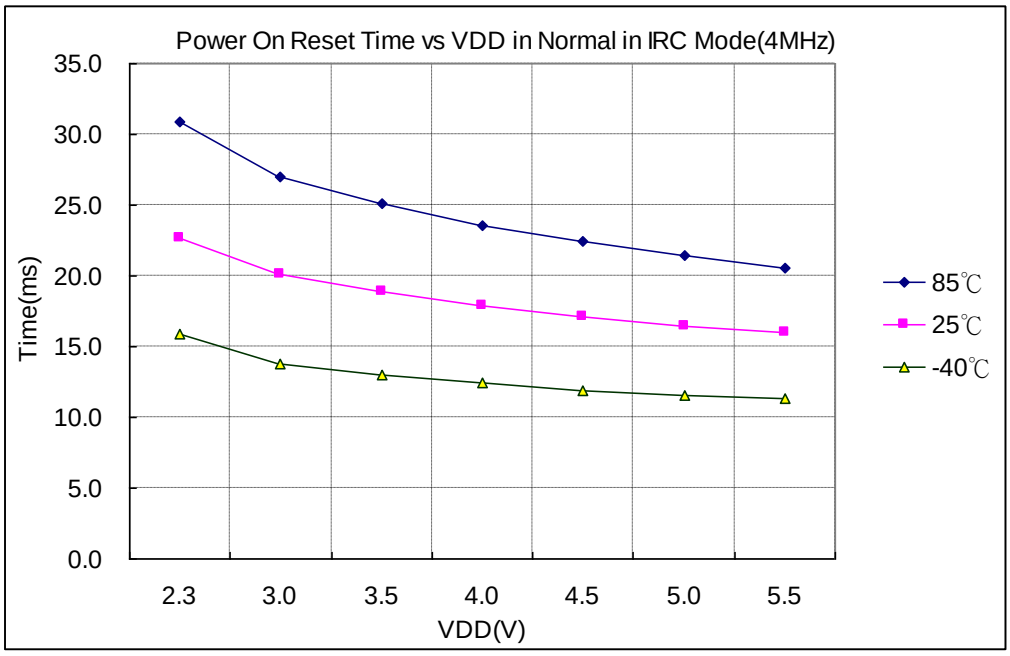


Figure 8-13(b) Power-on Reset Time in Normal Mode vs. VDD with IRC=4MHz

8.5.14 Graphs of Typical ICO vs. Temperature

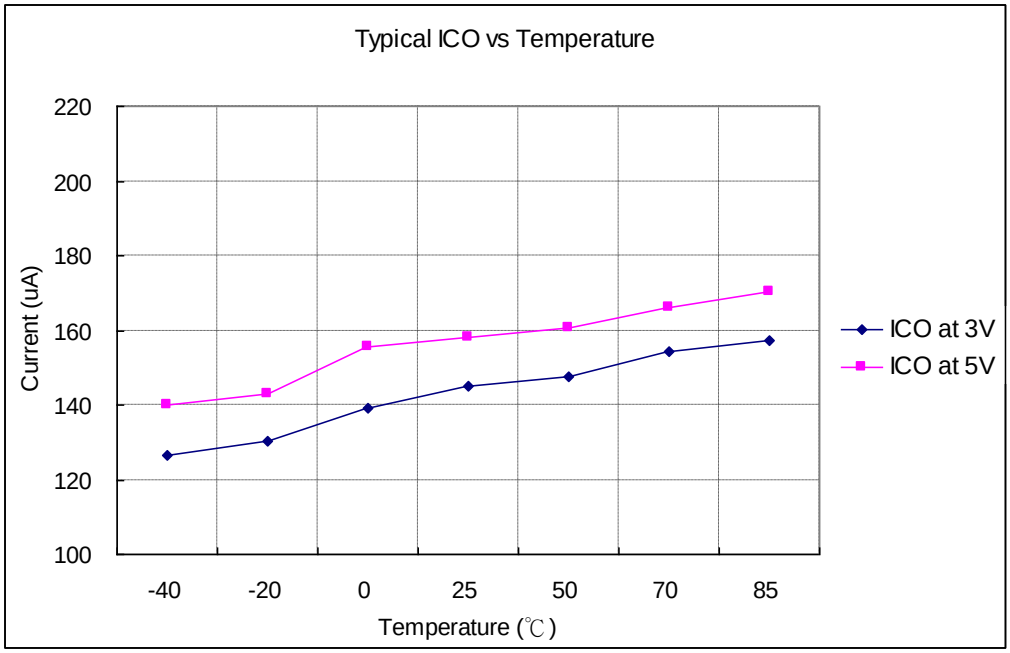


Figure 8-14 Typical Supply Current ICO vs. Temperature

8.5.15 Graphs of Typical IAI1 and IAI2 vs. Temperature

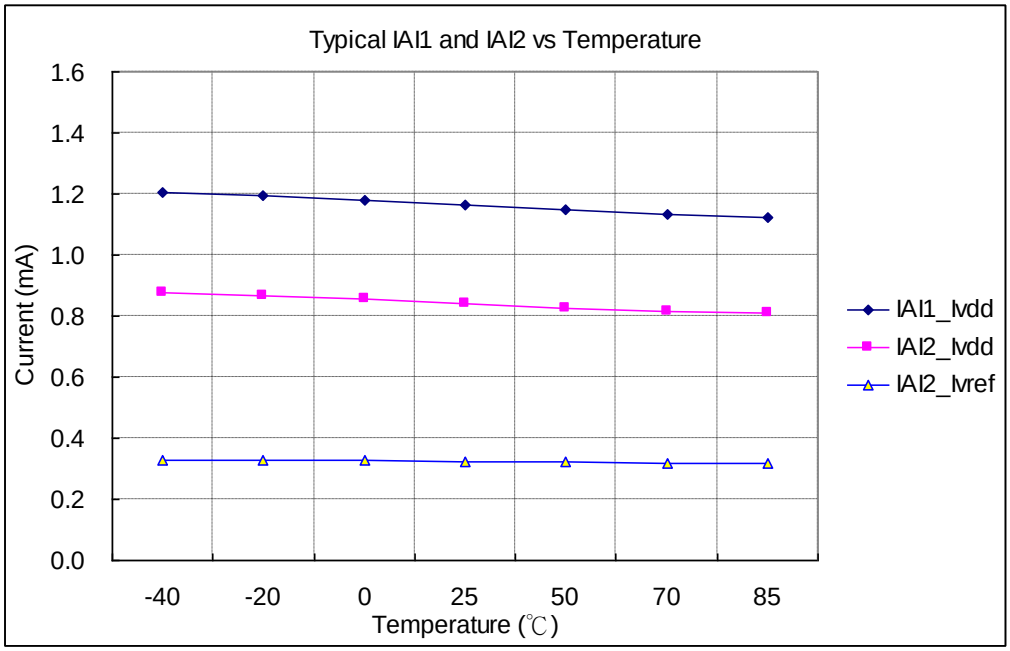


Figure 8-15 Typical AD Current (IAI1 & IAI2) vs. Temperature

8.5.16 Graphs of LVR Level vs. Temperature

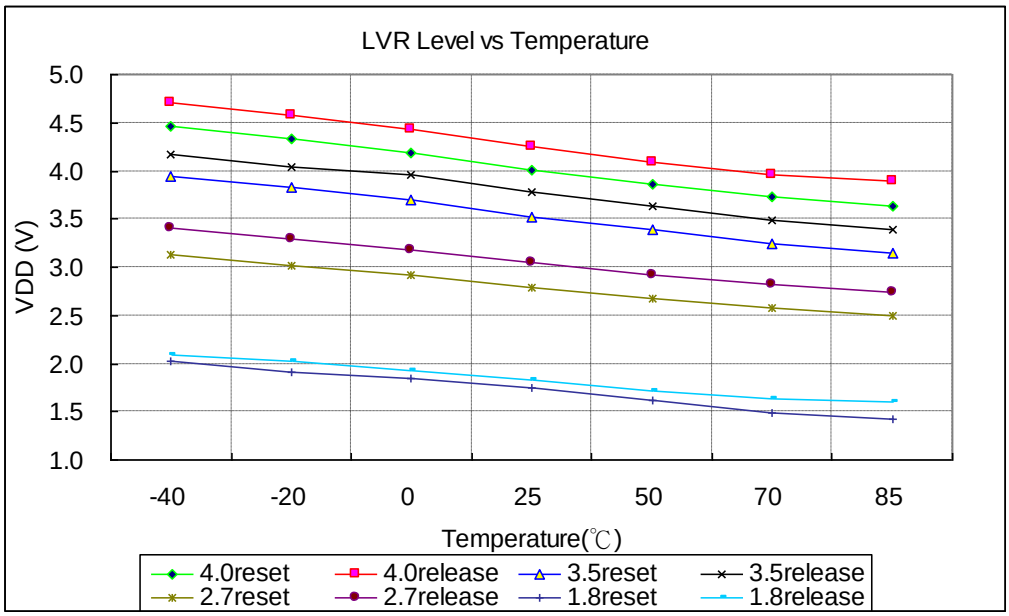


Figure 8-16 LVR Level vs. Temperature

8.5.17 Graphs of Comparator Offset Voltage vs. Temperature

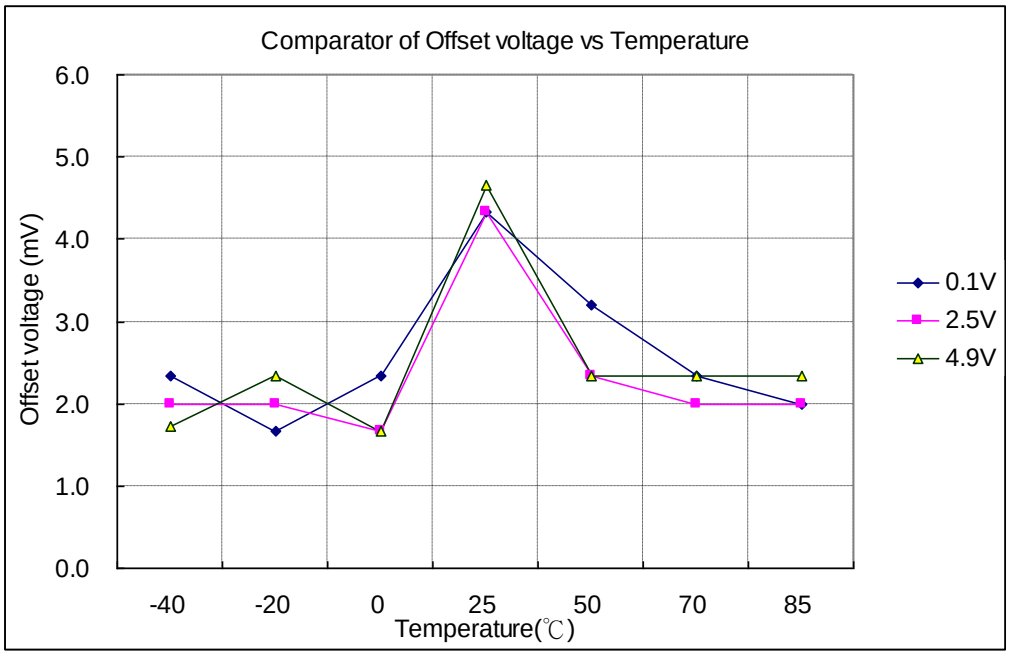


Figure 8-17 CMP Offset Voltage vs. Temperature (V+ is variable)

9 AC Electrical Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	125	–	DC	ns
Tpor	Delay Time after Power-On-Reset release	FSS0=1 (16kHz)	–	16 ± 30%	–	ms
Trstrl	Delay time after /Reset, WDT, and LVR release	Crystal type	–	WSTO + 510/Fm	–	µs
			–	WSTO + 8/Fs	–	µs
		IRC type	–	WSTO + 8/Fm	–	µs
			–	WSTO + 8/Fs	–	µs
Trsth1	Hold Time after /RESET pin reset	–	–	1 µs	–	–
Trsth2	Hold Time after LVR pin reset	–	–	1 µs	–	–
Twdt	Watchdog timer time-out	FSS0=1 (16kHz)	–	16 ± 30%	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20 pF Rload=1MΩ	–	20	–	ns

Note: 1. *WSTO: The waiting time of Start-to-Oscillation*

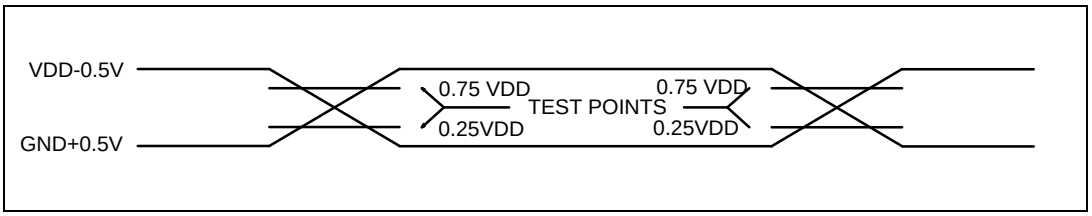
2. *These parameters are hypothetical (not tested) and are provided for design reference only.*

3. *Data under minimum, typical, and maximum (Min., Typ. and Max.) columns are based on hypothetical results at 25℃. These data are for design reference use only.*

****. Tpor** and **Twdt** are **16 ± 30%** ms at **FSS0=1(16kHz)**, Ta=-40°~**85℃**, and VDD=2.1~5.5V*

10 Timing Diagrams

AC Test Input / Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for Logic "**1**", and GND+0.5V for Logic "**0**"*
*Timing measurements are made at 0.75V for Logic "**1**", and 0.25VDD for Logic "**0**"*

Figure 10-1a AC Test Input / Output Waveform Timing Diagram

Reset Timing (CLK = "0")

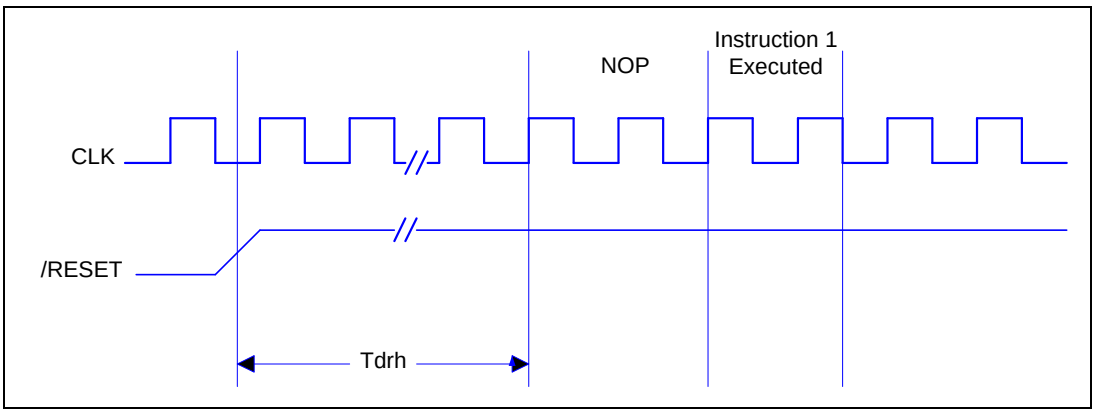


Figure 10-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

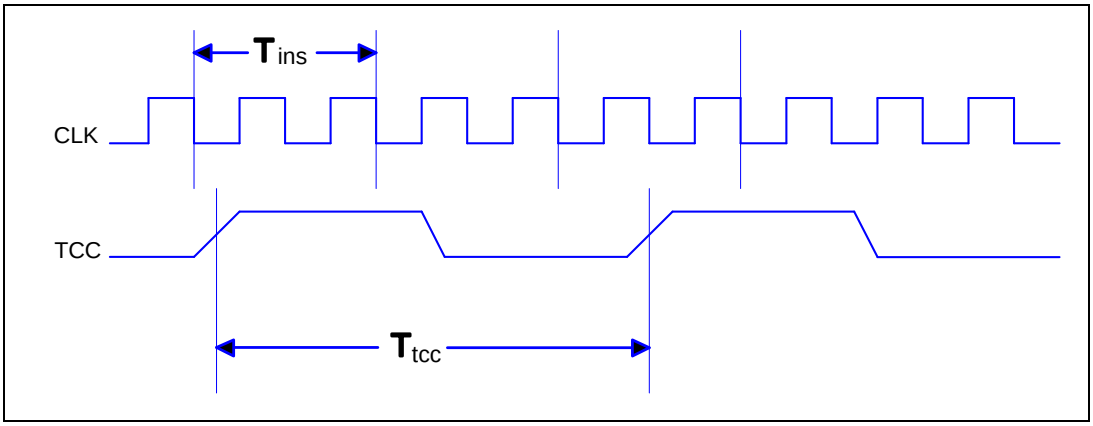
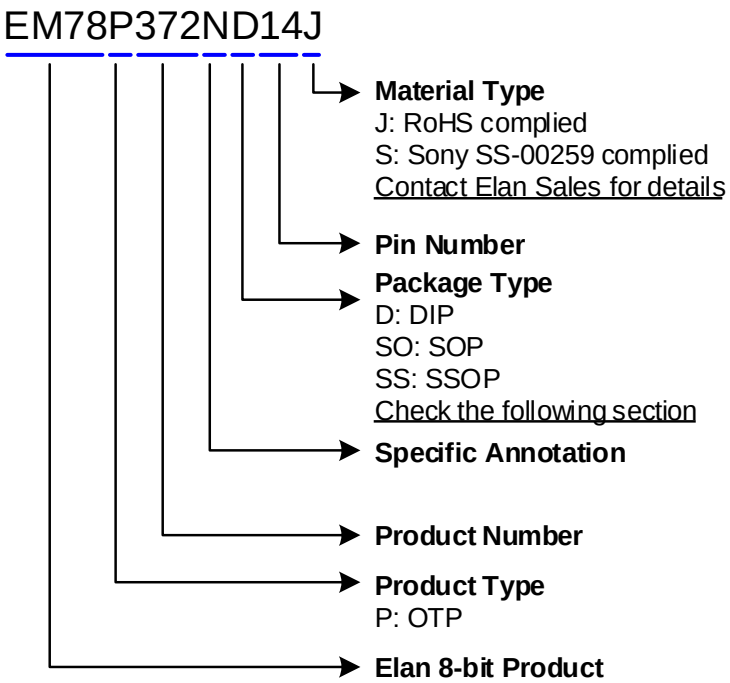


Figure 10-1c TCC Input Timing Diagram

APPENDIX

A Ordering and Manufacturing Information

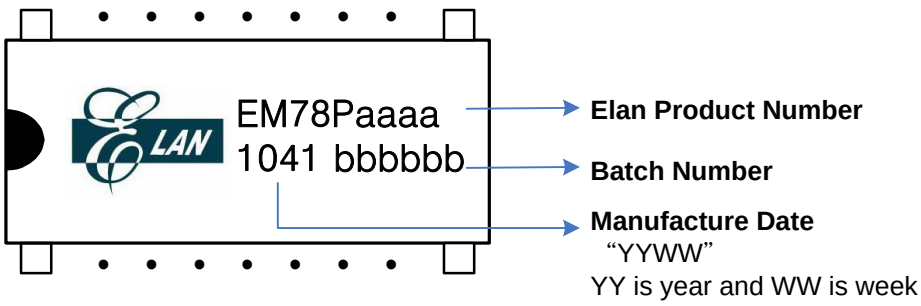


For example:

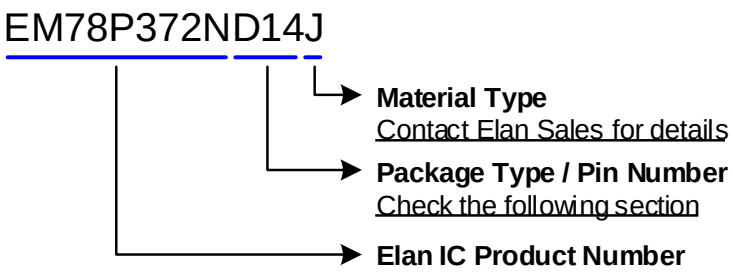
EM78P372NSO14S

is EM78P372N with OTP program memory product,
in 14-pin SOP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P372NMS10	MSOP	10	118 mil
EM78P372ND14	DIP	14	300 mil
EM78P372NSO14	SOP	14	150 mil
EM78P372NSO16A	SOP	16	150 mil
EM78P372ND18	DIP	18	300 mil
EM78P372NSO18	SOP	18	300 mil
EM78P372ND20	DIP	20	300 mil
EM78P372NSO20	SOP	20	300 mil
EM78P372NSS20	SSOP	20	209 mil
EM78P372NQN16	QFN	16	3×3×0.8mm

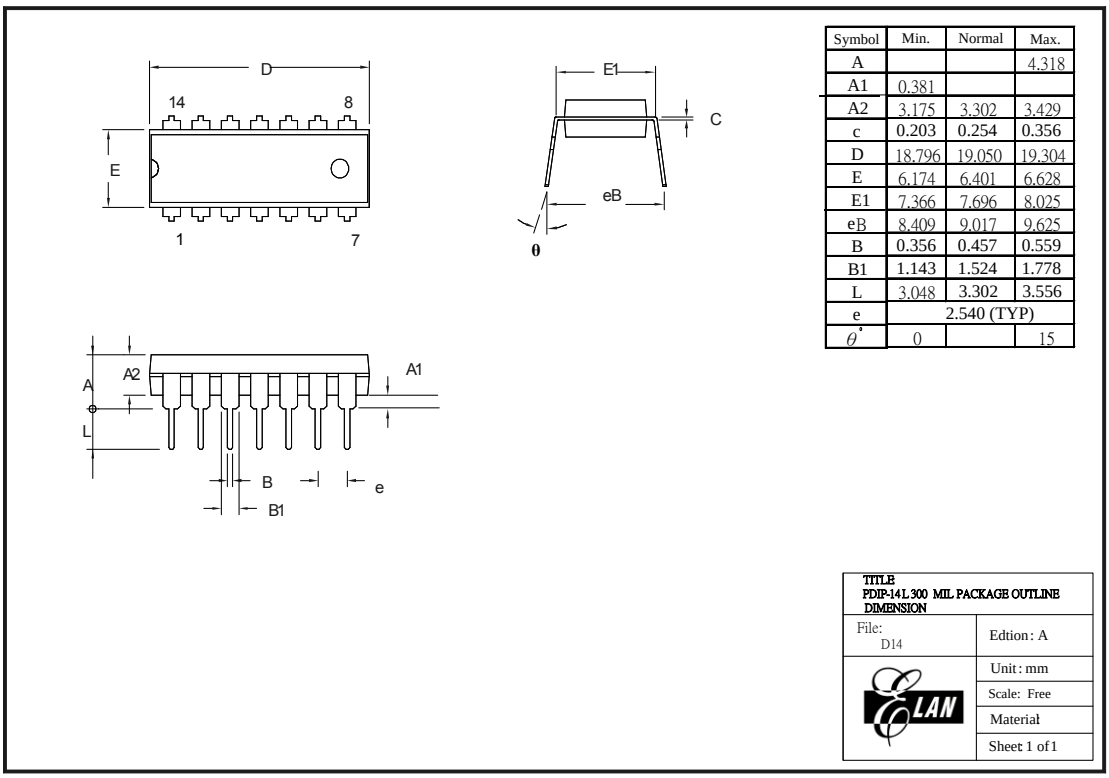
For product code "J".

These are Green products and complies with RoHS specifications

Part No.	EM78P372NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configuration

C.1 EM78P372ND14

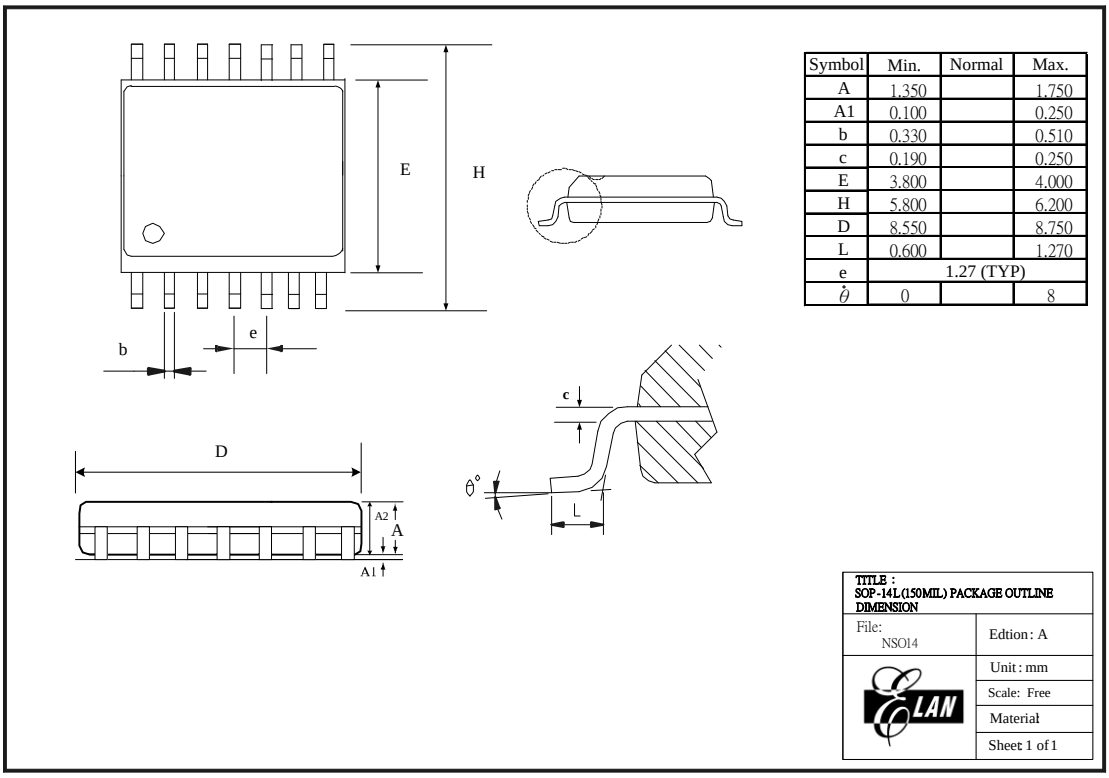


Symbol	Min.	Normal	Max.
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP)		
θ°	0		15

TITLE PDIP-14L 300 MIL PACKAGE OUTLINE DIMENSION	
File: D14	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of 1

Figure C-1 EM78P372N 14-pin PDIP Package Type

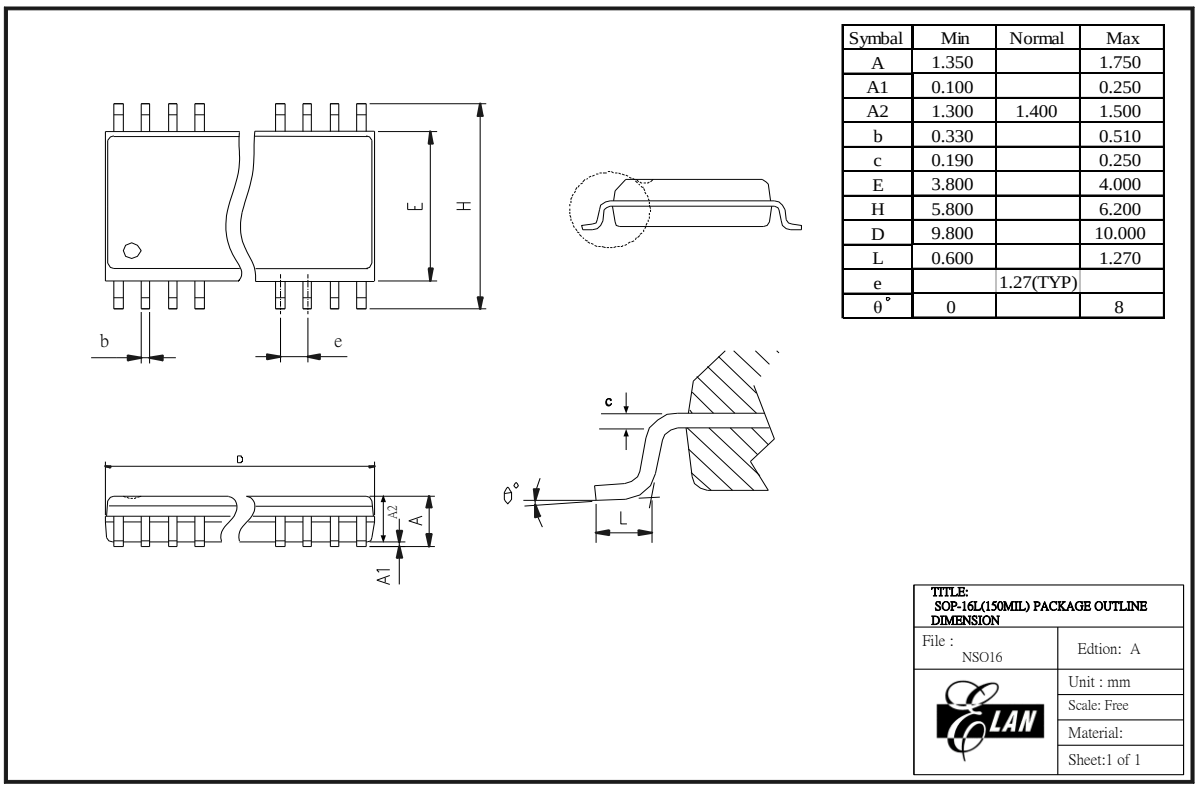
C.2 EM78P372NSO14



Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27 (TYP)		
θ	0		8

Figure C-2 EM78P372N 14-pin SOP Package Type

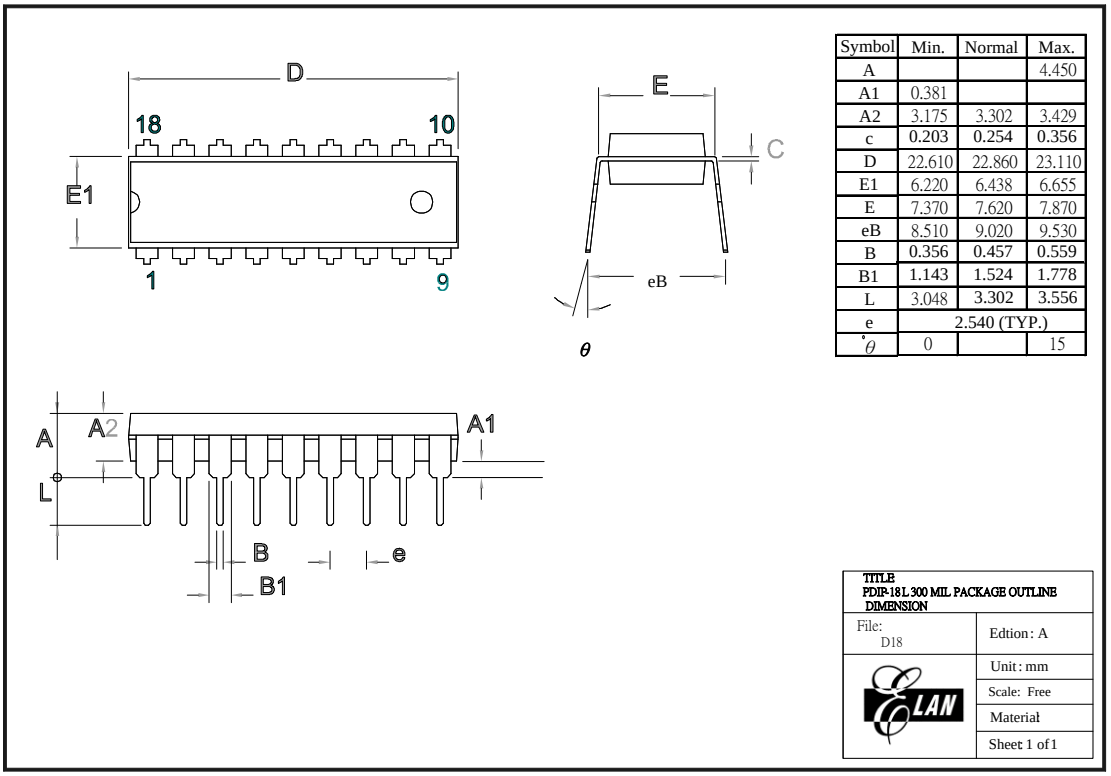
C.3 EM78P372NSO16A



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e		1.27(TYP)	
θ°	0		8

Figure C-3 EM78P372N 16-pin SOP Package Type

C.4 EM78P372ND18

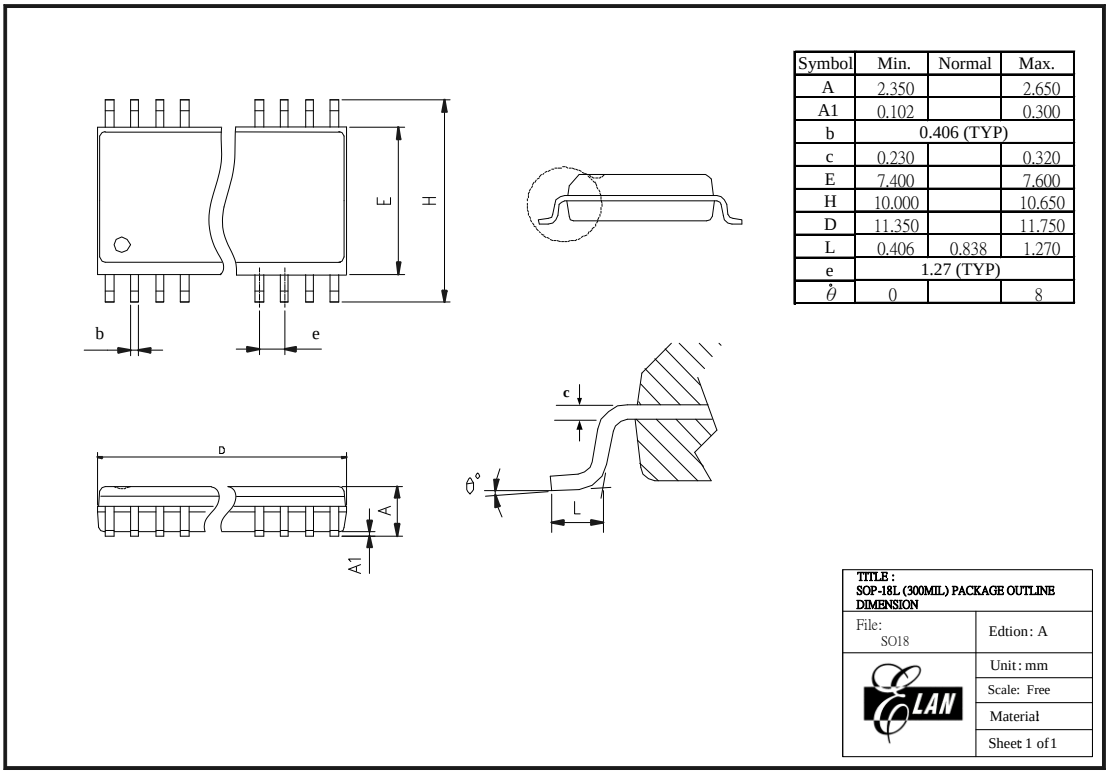


Symbol	Min.	Normal	Max.
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP.)		
θ	0		15

TITLE: PDIP-18L 300 MIL PACKAGE OUTLINE DIMENSION	
File: D18	Edtion : A
	Unit : mm
	Scale: Free
	Material
	Sheet 1 of 1

Figure C-4 EM78P372N 18-pin PDIP Package Type

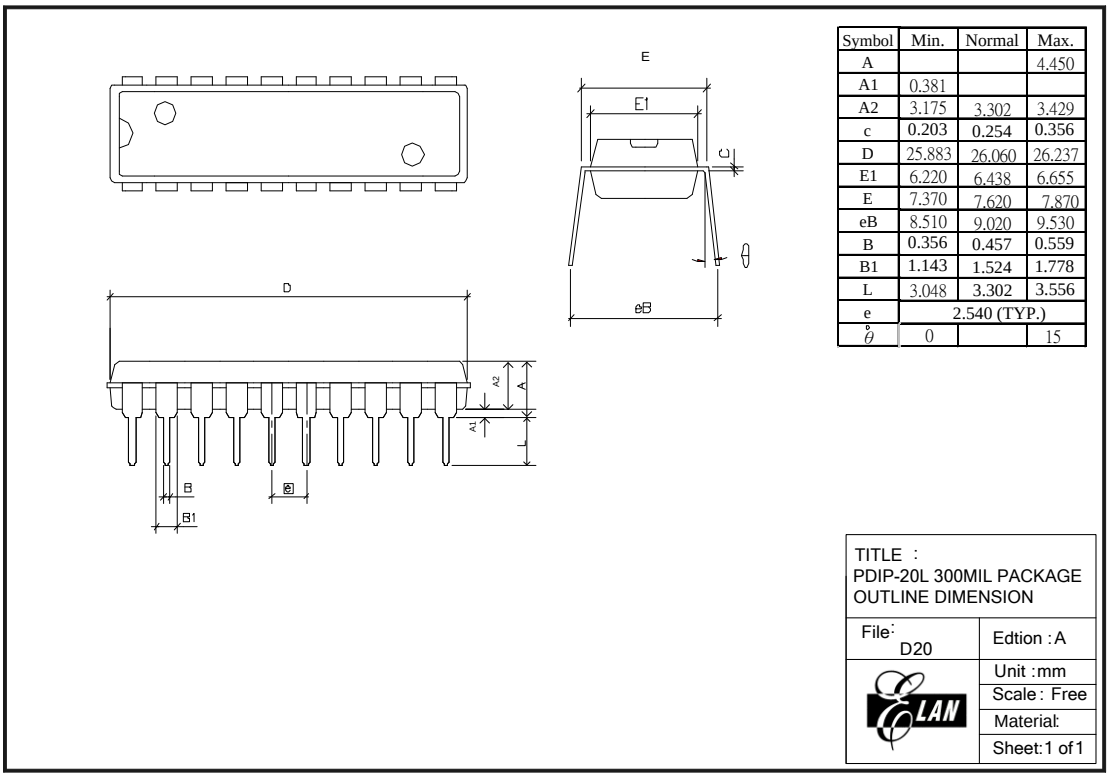
C.5 EM78P372NSO18



Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b	0.406 (TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27 (TYP)		
θ	0		8

Figure C-5 EM78P372N 18-pin SOP Package Type

C.6 EM78P372ND20

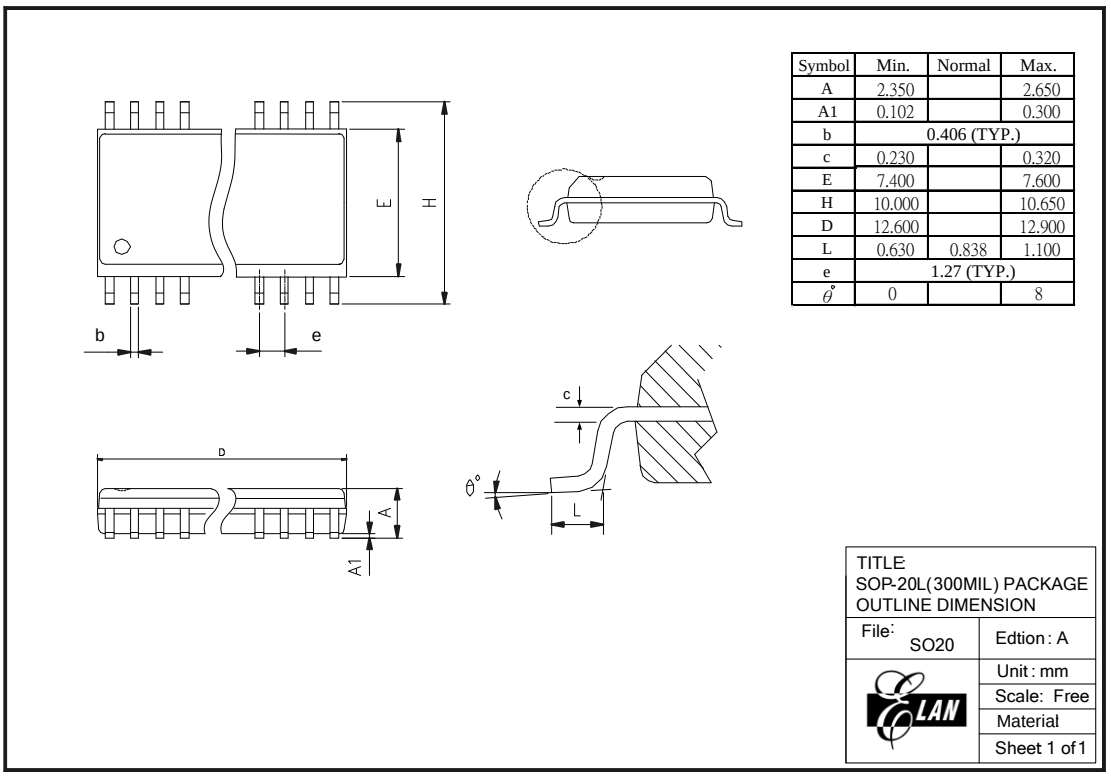


Symbol	Min.	Normal	Max.
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP.)		
θ	0		15

TITLE : PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION	
File: D20	Edtion : A
	Unit : mm
	Scale : Free
	Material:
	Sheet: 1 of 1

Figure C-6 EM78P372N 20-pin PDIP Package Type

C.7 EM78P372NSO20

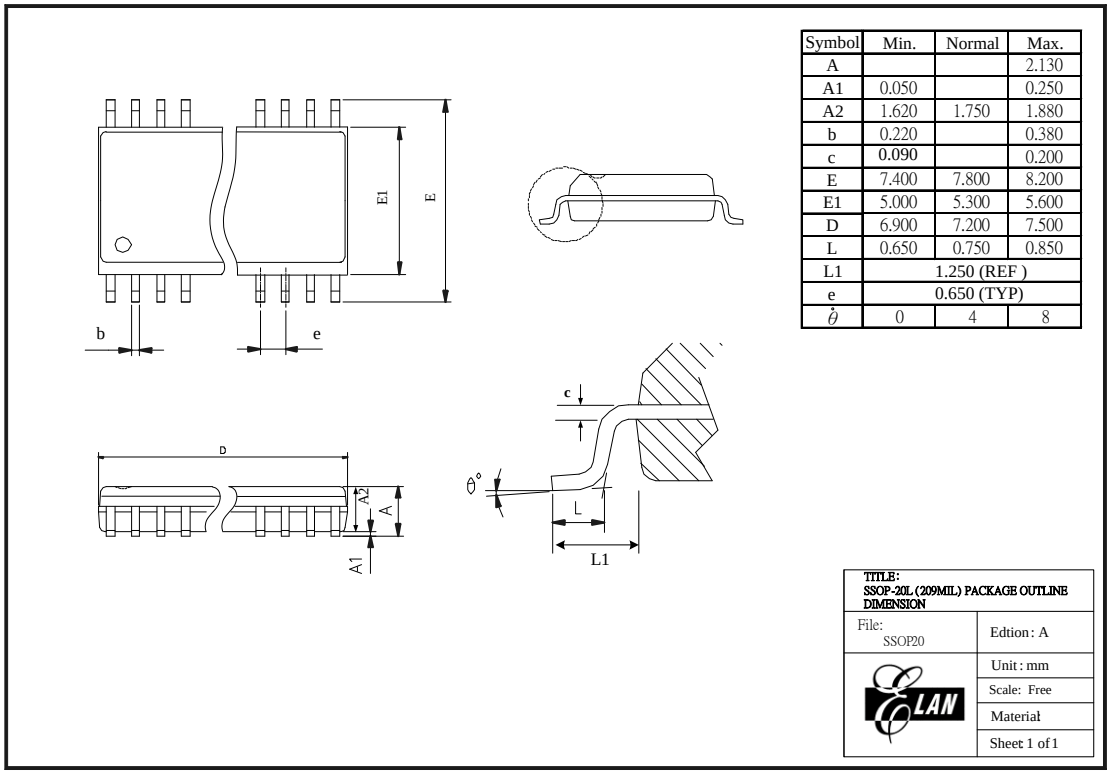


Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b	0.406 (TYP.)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27 (TYP.)		
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File: SO20	Edtion : A
	Unit : mm
	Scale: Free
	Material
	Sheet 1 of 1

Figure C-7 EM78P372N 20-pin SOP Package Type

C.8 EM78P372NSS20



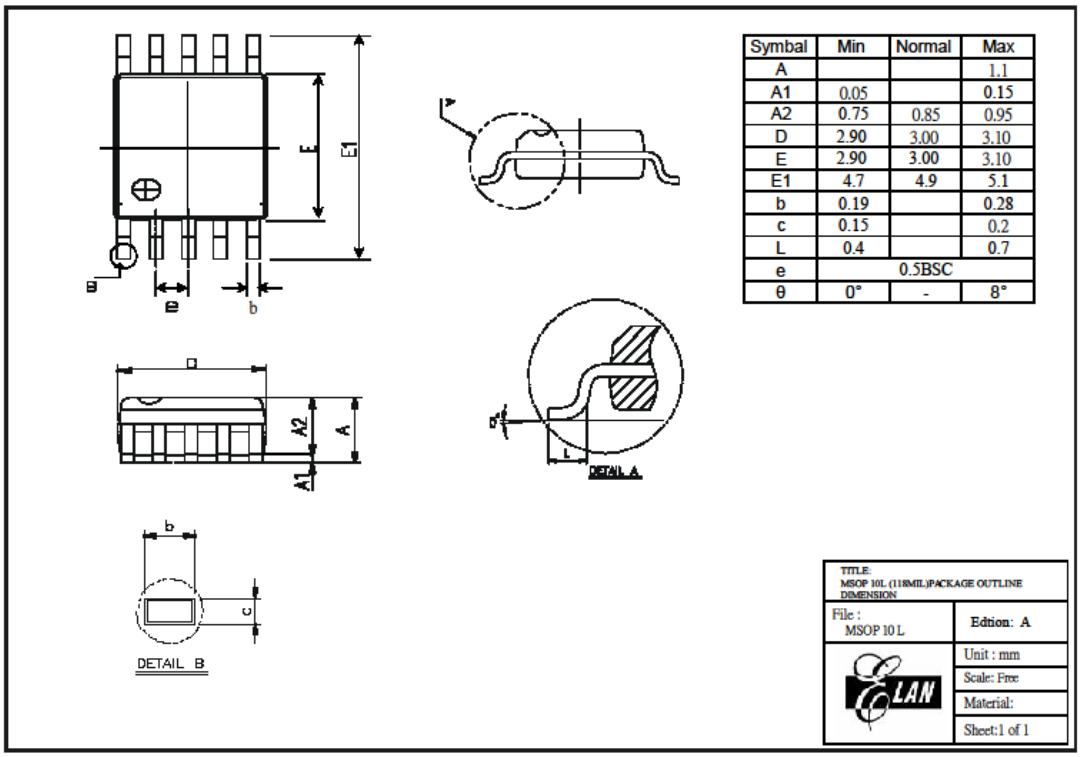
Symbol	Min.	Normal	Max.
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250 (REF)		
e	0.650 (TYP)		
θ	0	4	8

TITLE:
SSOP-20L (209MIL) PACKAGE OUTLINE DIMENSION

File: SSOP20	Edtion : A
	Unit : mm
	Scale: Free
	Material
	Sheet 1 of 1

Figure C-8 EM78P372N 20-pin SSOP Package Type

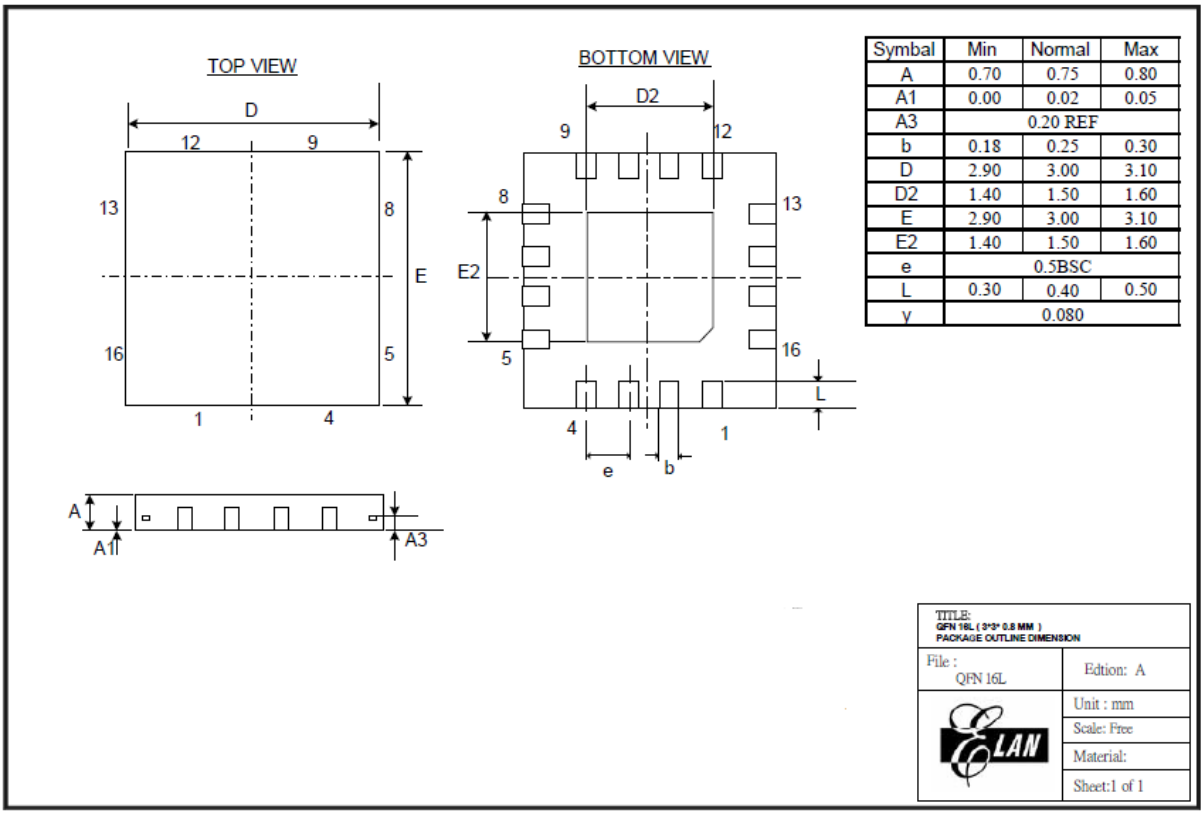
C.9 EM78P372NMS10



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

Figure C-9 EM78P372N 10-pin MSOP Package Type

C.10 EM78P372NQN16



Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e		0.5BSC	
L	0.30	0.40	0.50
y		0.080	

TITLE:
QFN 16L (3*3* 0.8 MM)
PACKAGE OUTLINE DIMENSION

File : QFN 16L | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-10 EM78P372N 16-pin QFN Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (durance)=24 hrs	
	Step 3: Soak at 30°C / 60% , TD (durance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 – 225 ± 5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 – 240 ± 5°C)	
Temperature cycle test	-65° (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (durance) = 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85% , TD (durance)=168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (durance)=500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC=Max. operating voltage, TD (durance) =168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC=Max. operating voltage, 800mA/40V	–
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-)mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.