

82567 GbE Physical Layer Transceiver (PHY)

Datasheet

Product Features

- Reduced power consumption during normal operation and power down modes
- IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab) conformance
- Supports up to 9 kB jumbo frames (full duplex)
- Supports carrier extension (half duplex)
- Auto-negotiation with support for next page
- Smart speed operation, for automatic speed reduction on faulty cable plants
- Automatic MDI crossover capable
- PMA loopback capable (No echo cancel)
- Advanced power management:
 - Low power link up
 - Auto Connect Battery Saver - link disconnect
- Advanced cable diagnostics:
 - TDR
 - Channel frequency response
- Extended configuration load sequence
- Automatic resolution of FDX/HDX mismatch in 10/100 forced configurations
- Dual interconnect between MAC and PHY:
 - LCI for 10/100 Mb/s operation control traffic
 - GLCI for 1000 Mb/s operation
- Three LED outputs
- Multiple voltage regulation modes:
 - External voltage regulation
 - Fully integrated linear regulator (nominal 1.05 V, programmable)
 - Discrete linear voltage regulator (nominal 1.8 V-1.9 V)
- Supported ICH Integrated MAC Features:
 - Linksec (ICH10 only)
 - Manageability: vPro Compatible
 - Performance:
 - RSS Support
 - Checksum offload



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Revision History

| Date | Revision | Description |
|----------------|----------|--|
| Oct 2006 | 0.1 | Initial release (Intel secret) |
| January 2007 | 0.25 | Corrected pin numbers and made minor text corrections (Intel Confidential) |
| February 2007 | 0.26 | Corrected GLAN TX pin numbers; added RSET & DIS_REG1_0 to the signal descriptions; corrected LAN_DISABLE# (active high) to LAN_DISABLE_N (active low); in the Visual Pin Assignment Diagram, pin 37, "LAN Enable" was corrected to "LAN_Disable_N"; removed VHV references. |
| April 2007 | 0.50 | Minor text updates. |
| May 2007 | 0.51 | Updated power consumption target values. |
| August 2007 | 0.75 | Added Low-Power feature information, Recommended Operating Conditions, DC and AC Characteristics, Preliminary LED/TEST/JTAG I/F DC Specifications, Crystal Specification, Voltage Regulator Power Supply Specification, PnP Transistor Specification, and Power Sequencing information. |
| September 2007 | 0.76 | Changed IEEE 802.3ab designation to conformance |
| November 2007 | 1.5 | Updated features list; updated Reference Documents; added SKU information; Updated power rail information (1.8 V-1.9 V, 1.05 V); clarified oscillator placement information; updated power target information; corrected Slope and Operation Range characteristics for 1.8-1.9 V rail; added pointer to reference schematics for regulator information. |
| November 2007 | 1.51 | Deleted "programmable" from 1.8 V-1.9 V power rail listing in the Features list. |
| December 2007 | 1.6 | Corrected 1.05 V power rail tolerance to +7% / -5% (1.0 V min, 1.12 V max) |
| February 2008 | 1.7 | Added XOR test file information; updated SKU and Features table; added information regarding using LAN_PHY_PWR_CTRL ; updated Recommended Operating Conditions; updated DC and AC characteristics; updated crystal/oscillator specifications; updated the measured power consumption values; updated reference schematic link information; updated the 1.8 V-1.9 V rail operational range value; updated the 1.05 V rail operational range value; corrected P _{tot} Min value in PNP specification; |
| March 2008 | 2.0 | Updated Reference Documents list; updated Testability Pins table; updated SKU table; updated Power Consumption tables 7-10; updated power delivery drawing; added Ambient Operating Temperature table. |
| March 2008 | 2.1 | Updated SKU table; Combined Tables 5 and 6 to create new Table 5. |
| April 2008 | 2.2 | Updated Table 2.4 (added pull-up type designation to LAN_DISABLE_N); updated Table 12 (added LAN_DISABLE_N information) |
| July 2008 | 2.3 | Updated WoL information; added System Idle Power Saver information; updated crystal tolerances; updated LED pin table; updated pinout illustration; updated package tolerance values. |
| April 2009 | 2.4 | Updated SKU table; added <i>SPI FLASH Programming Guide</i> and <i>82567 Specification Update</i> to Reference Documents; added note regarding ACBS operation; added WoL power information; added Solution Power information to Power Consumption table; clarified crystal Drive Level specification. |

Note: The revision numbering system changed with the first November 2007 release. At that time, the collateral for this device began synchronizing with platform collateral revision numbering. There were no releases between versions 0.76 and 1.5.

1.0 Introduction

The 82567 is a single port GbE Physical Layer Transceiver (PHY) that connects to its Media Access Controller (MAC) through a dedicated interconnect. The 82567 is based on Intel's GbE PHY technology, and supports operation at data rates of 10/100/1000 Mb/s. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications (802.3, 802.3u, and 802.3ab).

The 82567 operates with the ICH9/9M/10 chipset that incorporates and integrates the MAC, which is referred to as the ICH9/9M/10 LAN.

The 82567 is packaged in a small footprint QFN package. The package size is 8 mm x 8 mm with a pin-to-pin spacing of 0.5 mm, making it attractive for small form-factor platforms.

The 82567 interfaces with its MAC through two interfaces: Gigabit LAN Connect Interface (GLCI) and LAN Connect Interface (LCI). The GLCI is a high-speed proprietary serial interface. The LCI is a low-speed proprietary parallel bus. The 82567 operates using both interfaces; the GLCI for 1000 Mb/s traffic and LCI for all other traffic types.

Figure 1 identifies the major components of the 82567 architecture.

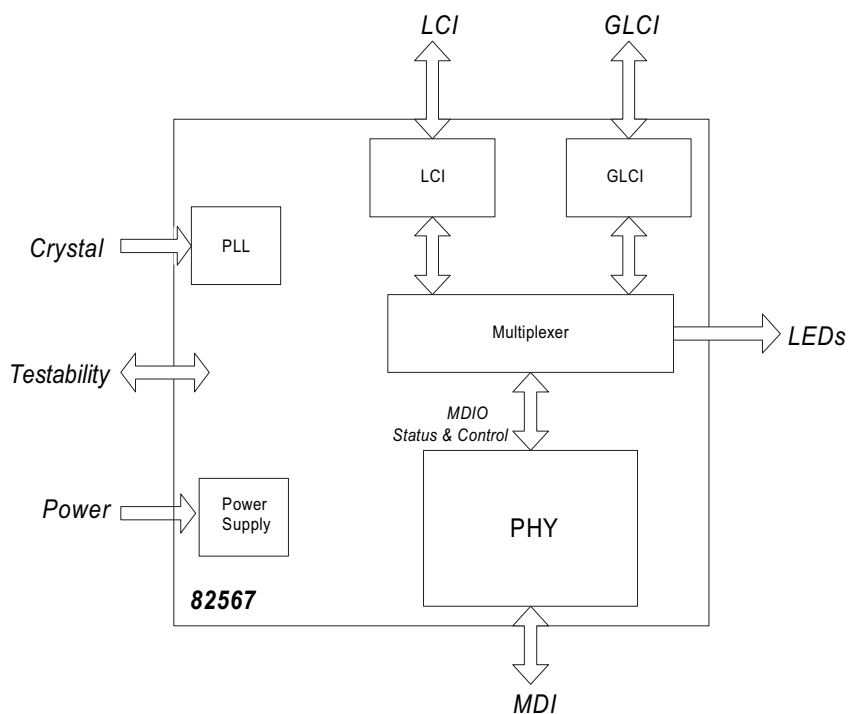


Figure 1. 82567 Block Diagram



1.1 Scope

This document contains datasheet specifications for the 82567, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide application information:

- *IEEE Standard 802.3*, 2002 Edition. Incorporates various IEEE Standards previously published separately. Institute of Electrical and Electronic Engineers (IEEE).
- *I/O Control Hub 9 NVM Map and Programming Information*. Intel Corporation.
- *I/O Control Hub 9M NVM Map and Programming Information*. Intel Corporation.
- *I/O Control Hub 10 NVM Map and Programming Information*. Intel Corporation.
- *ICH9 External Design Specification (EDS)*, Intel Corporation.
- *ICH10 External Design Specification (EDS)*, Intel Corporation.
- *I/O Controller Hub 8/9/10 and 82566/82567/82562V Software Developer's Manual*. Intel Corporation.
- *Information Technology - Telecommunication & Information Exchange Between Systems - LAN/MAN - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer*.
- *Intel® ICH7, ICH8, ICH9 and ICH10 – SPI Family Flash Programming Guide Application Note*. Intel Corporation. Contact your Intel representative to obtain this document.
- *Intel® 82567 Specification Update*, Intel Corporation.

1.3 Product Codes

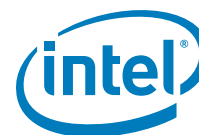
Table 1 lists the product ordering codes for the 82567.

Table 1. Product Ordering Codes¹

Note: For more information regarding the differences between the versions, please contact your Intel field representative.

| Part Number | Product Name | Description |
|-------------|--|---|
| XX82567LM | Intel® 82567 Gigabit Platform LAN Connect Device | Gigabit LAN for high-end Corporate and Workstation designs |
| XX82567LF | Intel® 82567 Gigabit Platform LAN Connect Device | Gigabit LAN for mainstream Corporate and high-end desktop designs |
| XX82567V | Intel® 82567 Gigabit Platform LAN Connect Device | Gigabit LAN for consumer designs |

1. For more information regarding the differences, please contact your Intel field representative.



2.0 Signal Descriptions

2.1 Signal Type Definitions

The signals are defined as follows in the table below:

| Type | Description |
|---------|--|
| In (I) | Standard input-only signal. |
| Out (O) | Totem pole output is a standard active driver. |
| T/s | Tri-state is a bi-directional, tri-state input/output pin. |
| S/st/s | Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/t/s pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/t/s signal any sooner than one clock after the previous owner tri-states it. |
| O/d | Open drain enables multiple devices to share as a wire-OR. |
| A-in | Analog input signal. |
| A-out | Analog output signal. |
| B | Input bias. |
| P | Power |
| PU | Pull-up. |
| PD | Pull-down. |

2.2 GLCI Interface Pins

| Signal Name | Pin | Type | Description |
|----------------------|----------|---------------|--|
| GLAN_RXP GLAN_RXN | 55 56 | A-in | GLCI Serial Data Input This is the differential input for GLCI (MAC to PHY). |
| GLAN_TXN GLAN_TXP | 53 52 | A-out | GLCI Serial Data Output This is the differential output for GLCI (PHY to MAC). |
| XTAL2 XTAL1 | 9 10 | A-out A-in | Crystal Oscillator An external 25 MHz crystal can be connected to these pins to generate a 25 MHz reference clock. A 25 MHz reference clock can also be generated from an external 1.4 V oscillator connected to the XTAL1 input pin. |

2.3 LCI Interface Pins

| Signal Name | Pin | Type | Description |
|-------------------------|----------------|------|---|
| JKCLK | 45 | O | LCI/GLCI Clock The clock is driven by the 82567 according to the operation mode: In 1000 Mb/s mode, JKCLK frequency is 62.5 MHz. In 100 Mb/s mode, JKCLK frequency is 50 MHz. In 10 Mb/s mode and no link, JKCLK frequency is 5 MHz. In power down mode, JKCLK frequency is 0 MHz. |
| JRSTSYNC | 50 | I | Reset/SYNC This pin is driven by the MAC and has two functions: Reset. When this pin is asserted beyond one LCI clock, the 82567 refers to this signal as a reset signal. However, to ensure that the 82567 resets, the reset should remain active for at least 1ms. This functionality is also used to bring the 82567 out of a power-down state. SYNC. When this pin is activated synchronously for one LCI clock only, it is used for synchronization between the MAC and the 82567 on LCI word boundaries. |
| JTXD2 JTXD1 JTXD0 | 44 43 42 | I | LCI Transmit Data These pins are used for receiving real time control and management data transmitted by the ICH9 LAN. These pins are also used to move out of band control from the MAC to the 82567. The pins should be fully synchronous to JKCLK. |
| JRXD2 JRXD1 JRXD0 | 49 48 47 | O | LCI Receive Data These pins are used for transmitting real time control and management data received by the ICH9 LAN. These pins are also used to move out of band control from the 82567 to the MAC. |

2.4 Miscellaneous Pins

| Signal Name | Pin | Type | Description |
|----------------------------|----------|-------|---|
| IEEE_TEST_P IEEE_TEST_N | 12 13 | A-out | Positive side of the high speed differential debug port for the 82567. |
| LAN_DISABLE_N | 37 | I/PU | When this pin is set, the 82567 consumes minimum power and is disabled. |
| RSET | 15 | | This pin should be connected through 4.99 kohm, +-1%, to ground. |
| RESERVED_NC | 51 | | Do not connect. |



2.5 PHY Pins

2.5.1 LED Pins

| Signal Name | Pin | Type | Description |
|-------------|-----|------|--|
| LED0 | 4 | O | LED0 This signal is used for the programmable LED. It is programmed through the Intel® ICH9/ICH10 NVM word 18h. |
| LED1 | 2 | O | LED1 This signal is used for the programmable LED. It is programmed through the Intel® ICH9/ICH10 NVM word 17h. |
| LED2 | 1 | O | LED2 This signal is used for the programmable LED. It is programmed through the Intel® ICH9/ICH10 NVM word 18h. |

Note: Reference the following Application Notes for details regarding the programming of the LEDs and the various modes.

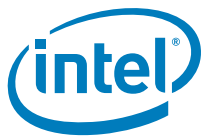
- *I/O Control Hub 9 NVM Map and Programming Information Application Notes*
- *I/O Control Hub 9M NVM Map and Programming Information Application Notes*
- *I/O Control Hub 10 NVM Map and Programming Information Application Notes*

2.5.2 Analog Pins

| Signal Name | Pins | Type | Description |
|--|----------------------|------|--|
| MDI_PLUS[0] MDI_MINUS[0] | 27 26 | A | Media Dependent Interface [0] In MDI configuration, MDI_PLUS[0]+/- is used for the transmit pair and in MDI-X configuration MDI_MINUS[0]+/- is used for the receive pair. |
| MDI_PLUS[1] MDI_MINUS[1] | 23 22 | A | Media Dependent Interface [1] In MDI configuration, MDI_PLUS[1]+/- is used for the receive pair and in MDI-X configuration MDI_MINUS[1]+/- is used for the transmit pair. |
| MDI_PLUS[2] MDI_MINUS[2] MDI_PLUS[3] MDI_MINUS[3] | 21 20 17 16 | A | Media Dependent Interface [2:3] For 1000BASE-T MDI configuration, MDI_PLUS[2:3]+/- is used for the receive pair and in MDI-X configuration MDI_MINUS[2:3]+/- is used for the transmit pair. |

2.5.3 Testability Pins

| Signal Name | Pin | Type | Description |
|-------------|-----|------|------------------|
| JTAG_TCK | 40 | I | JTAG Clock Input |
| JTAG_TDI | 7 | I/PU | JTAG TDI Input |
| JTAG_TDO | 6 | T/s | JTAG TDO Output |



| | | | |
|-----------|----|------|--|
| JTAG_TRST | 35 | I | JTAG Reset |
| JTAG_TMS | 39 | I/PU | JTAG TMS Input |
| TEST_EN | 36 | T/s | Test Mode Enable This signal enables test mode capabilities. It should be strapped to GND for normal operation. |

Note: The 82567 uses the JTAG interface to support XOR files for manufacturing test. BSDL is not supported.

2.6 Power Supply Pins

| Signal Name | Pin | Type | Description |
|-------------|--|------|---|
| VCC3_3 | 3 28 46 | P | 3.3 VDC Supply This is connected to the 82567. |
| VCC1_05 | 5 8 33 38 | P | 1.05 V DC Supply This is connected to the 82567. |
| VCC1_8 | 11 14 18 19 24 25 30 41 32 54 | P | 1.8 V-1.9 V DC Supply This is connected to the 82567. 82567 supports both 1.8 V and 1.9 V for this DC supply. |
| CTRL10 | 31 | Out | 1.05 V Control This is the voltage control signal for the external PNP transistor that generates the 1.05 V supply. |
| CTRL18 | 29 | Out | 1.8 V-1.9 V Control This is the voltage control signal for the external PNP transistor. The default voltage generated from the external PNP is 1.9 V. |
| DIS_REG1_0 | 34 | A | When set to 3.3 V, configured to use external regulator for 1.05 V supply. When set to 0, the internal regulator will be used for 1.05 V supply. A 1 kOhm pull up or 1 kOhm pull down resistor is required, depending on the desired configuration. |



3.0 Features

3.1 Feature Matrix and Product Information

The following matrix shows the features available with the 82567:

| 82567 Sku Platform/Features Information | | | Performance | | | | Extended Power | | Advanced Features*** | | | | | | | | | | | | | | | | | | | | | | | |
|---|---------------------|-----------|-------------------------|---|-----------------|----------------------------|----------------|--------------------|----------------------|---------------|---|--|---|--------------------------|---|-------------------------|---|------------------------|---|-----------------------------|--|----------------|--|------------|--|--------------------------------------|---|-----------------------------------|--|--------------------------------------|---|--|
| Platform | Code Name | Device ID | Jumbo Frames (up to 9k) | | 802.1Q & 802.1p | Receive Side Scaling (RSS) | | 2 Tx & 2 Rx Queues | | Auto MDI/MDIX | | Intel® Auto-Connect Battery Saver (ACBS) | | Link Speed Battery Saver | | Low Power Linkup (LPLU) | | Basic Manageability ** | | Ability to Initiate a Team* | | LinkSec/MACSec | | iSCSI Boot | | Intel® Stable Image Platform program | | Intel® Vpro Processor Technology™ | | Intel® Viiv Processor or Technology™ | | |
| Embedded | ICH8M + 82567V | 1501 | | | | | | | X | | | X | X | | | | | | | | | | | | | | | | | | Intel® 82567V-3 Gigabit Network Connection | |
| High End Desktop/ Workstation | ICH9/9R + 82567LM | 10E5 | X | X | X | X | X | X | X | X | X | X | X | | X | | X | X | | | | | | | | | | | | | Intel® 82567LM-4 Gigabit Network Connection | |
| Mobile | ICH9m+82567LM | 10F5 | X | X | X | X | X | X | X | X | X | X | X | X | X | | | X | X | | | | | | | | | | | | Intel® 82567LM Gigabit Network Connection | |
| | ICH9m+82567LF | 10BF | | X | | | | X | X | X | X | X | X | X | X | | | X | | | | | | | | | | | | | Intel® 82567LF Gigabit Network Connection | |
| | ICH9m+82567V | 10CB | | | | | | X | | X | X | | | | | | | | | | | | | | | | | | | | Intel® 82567V Gigabit Network Connection | |
| Desktop | ICH10/10R+82567LM | 10CC | X | X | X | X | X | X | X | X | X | X | X | X | X | | X | | | | | | | | | | | X | | | Intel® 82567LM-2 Gigabit Network Connection | |
| | ICH10/10R+82567LF | 10CD | | X | | | | X | X | X | X | X | X | X | X | | X | | | | | | | | | | X | | | | Intel® 82567LF-2 Gigabit Network Connection | |
| | ICH10/10R+82567V | 10CE | | | | | | X | | X | X | | | | | | | | | | | | | | | | | X | | | Intel® 82567V-2 Gigabit Network Connection | |
| Desktop | ICH10D/10DO+82567LM | 10DE | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | | | | | | | | | | | Intel® 82567LM-3 Gigabit Network Connection | |
| | ICH10D/10DO+82567LF | 10DF | | X | | | | X | X | X | X | X | X | X | X | | X | X | | | | | | | | | | | | | Intel® 82567LF-3 Gigabit Network Connection | |

* Note: Teaming is supported on Corporate SKU's with no-AMT

** Basic manageability includes ASF & DASH support. For firmware and hardware requirements, please refer to Intel® chipset documentation.

*** For Platform features, other Intel® component skus may be required. Please refer to the relevant Intel® component (chipset/CPU) documentation for sku requirements.

Production information is in the *82567 Specification Update* available from Intel on the Intel Business Link. Contact your Intel representative for more information.

3.2 Power Saving Features

This section provides information about the low power configurations for the 82567.

3.2.1 Intel® Auto Connect Battery Saver (ACBS)

Intel Auto Connect Battery Saver for the 82567 is a hardware-only feature that automatically reduces the PHY to a lower power state when the power cable is disconnected. When the power cable is reconnected, it will renegotiate the line speed following IEEE specs for autonegotiation. By default, autonegotiation starts at 1GHz, then 100 Mb full duplex/half duplex, then 10 Mb full duplex/half duplex.

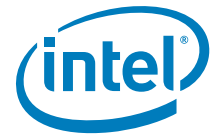
Note: Intel Auto Connect Battery Saver for the 82567 is only supported if autonegotiation is enabled. If link speed is forced and the network cable is disconnected, the 82567 will not enter ACBS, resulting in higher power consumption than specified in section 4.6.

82567 ACBS works in both S0 and Sx states. Unlike the 82566 External ACBS implementation, 82567 ACBS requires no BIOS, software, or external on-board hardware, limiting BOM cost and making implementation easier. When the 82567 PHY is in ACBS mode, the LAN drivers stay loaded and the PHY consumes 37 mW (Solution power is 63 mW). The crystal and LCI/GLCI interface clock still run, but all unneeded internal clocks are gated. Since 82567 ACBS has no driver control, the feature is always enabled, allowing power savings by default. The table below compares 82566 External ACBS implementation and 82567 ACBS implementation:

| | | 82566 ACBS | 82567 ACBS |
|----------------------------------|--------|---|---|
| Implementation (HW/SW/FW) | HW | Needs on board hardware (energy detect circuit, power FET Switch) (BOM Cost ~\$0.2) | No external BOM (\$0) |
| | Driver | Driver controls entry into ACBS. Enabling/Disabling ACBS possible from driver. | No Driver control. Feature always enabled. Enabling/Disabling ACBS is not possible from the driver. |
| | BIOS | Minor changes needed for LAN_PHY_PWR_CTRL (ICH output) configuration. | No BIOS changes needed |
| | FW | NVM Soft Straps and GbE NVM needs to be set up. | NVM does not need to be set up. |
| AC/DC modes | | Supported only in DC mode | Supported in both AC and DC modes. |
| Sx support | | Cannot enter ACBS mode in Sx states. | Can enter ACBS mode in both S0 and Sx states |
| LAN Power Rails | | 3.3/1.8/1.05 V are all turned off in IVRd/IVRi configurations | 3.3/1.8-1.9/1.05 V rails are all left on |
| PHY Power Consumption | | ~7mW | 37 mW PHY power (63 mW solution power) |

3.2.2 Link Speed Battery Saver

Link Speed Battery Saver is a power saving feature that negotiates to the lowest speed possible when a Mobile system operates in DC mode to save power. When in AC mode, where performance is more important than power, it negotiates to the highest speed



possible. The Windows NDIS drivers (Windows XP and later), monitor the AC-to-DC transition on the system to make the PHY negotiate to the lowest connection speed supported by the link partner (usually 10 Mb) when the user unplugs the power cable (switches from AC to DC power). When the AC cable is plugged in, the speed will negotiate back to the fastest LAN speed. This feature can be enabled/disabled directly from DMiX or through the Advanced Settings of the Window's driver.

When transferring packets at 1000/100 Mbps speed, if there is an AC-to-DC transition, the speed will renegotiate to the lower speed. Any packet that was in process will be retransmitted by the protocol layer. If the link partner is hard-set to only advertise a certain speed, then the driver will negotiate to the advertised speed. Since the feature is driver based, it is available in S0 state only.

Link Speed Battery Saver handles duplex mismatches/errors on link seamlessly by re-initiating auto negotiation while changing speed. Link Speed Battery Saver also supports Spanning Tree Protocol.

Note: The packets would get re-transmitted for any protocol other than TCP as well.

3.2.3 System Idle Power Saver (SIPS)

System Idle Power Saver (SIPS) is a software-based power saving feature that is enabled only with Microsoft* Windows* Vista*. This feature is only supported in the S0 state and can be enabled/disabled in the Advanced Tab of the Windows driver or through DMiX. The power savings from this feature is dependent on the link speed of the device. Please refer to Section 4.6 Tables 6-9 for the power dissipated in each link state.

SIPS is designed to save power in mobile systems by negotiating to the lowest possible link speed when both the network is idle and the monitor is turned off due to inactivity. The SIPS feature is activated based on both of the following conditions.

- The Windows* Vista* NDIS driver receives notification from the Operating System (OS) when the monitor is turned "OFF" due to non-activity.
- The LAN driver monitors the current network activity and determines that the network is idle.

Then, with both the monitor "OFF" and the network idle, the LAN negotiates to the lowest possible link speed supported by both the PHY and the link partner (typically 10 Mb). If the link partner is hard-set to only advertise a certain speed, then the LAN will negotiate to the advertised speed. This link speed will be maintained until the LAN driver receives notification from the OS that the monitor is turned "ON," thus exiting SIPS and re-negotiating to the highest possible link speed supported by both the PHY and the link partner. If SIPS is exited when transferring packets, any packet that was being transferred will be re-transmitted by the protocol layer after re-negotiation to the higher link speed.

3.2.4 Low Power Link Up (LPLU)

Low Power Link Up is a firmware/hardware based feature that allows the designer to make the PHY negotiate to the lowest connection speed first and then to the next higher speed and so on. This setting allows users to save power when power is more important than performance.

When speed negotiation starts, the PHY tries to negotiate for a 10 Mb/s link, independent of speed advertisement. If link establishment fails, the PHY tries to negotiate with different speeds. It enables all speeds up to the lowest speed supported by the partner. For example, if the 82567 advertises 10 Mb/s only and the link partner supports 1000/100 Mbps only, a 100Mbps link is established.

LPLU is controlled through the LPLU bit in the PHY Power Management register. The MAC sets and clears the bit according to hardware/software settings. The 82567 auto-negotiates with the updated LPLU setting on the following auto-negotiation operation. The 82567 does not automatically auto-negotiate after a change in the LPLU value. LPLU is not dependent on whether the system is in AC or DC mode. In S0 state, Link Speed Battery Saver overrides the LPLU functionality.

LPLU is enabled for Non-D0a states by GbE NVM image word 17h (bit 10)

- 0b = Low Power Link Up is disabled.
- 1b = Low Power Link Up is enabled in all non-D0a states.

LPLU power consumption depends on what speed it negotiates at. This datasheet includes all of the power numbers for the 82567 in the various speeds; see section 4.6, Tables 1-4.

3.2.5 LAN Disable

82567 has a LAN_DISABLE_N input pin that can be used by the BIOS to disable the PHY. The addition of this feature simplifies the PHY disable feature from the BIOS relative to the LAN Disable sequence used in 82566.

LAN_DISABLE_N is an active low input and when asserted, it loses all functionality other than the ability to power up again. Asserting LAN_DISABLE_N causes:

- GLCI enters electrical idle
- JKCLK is stopped to the MAC
- 25MHz clock remains active
- 82567 tri-states its output buffers
- WOL is not supported

On de-assertion:

- PHY sends JKCLK to MAC; MAC asserts JRSTSYNC
- PHY goes through usual initialization process.

Important Note:

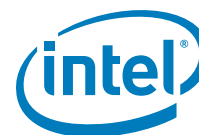
Be sure to check for the latest LAN Disable and LAN_PHY_PWR_CTRL design guidelines. The information in the Specification Updates listed below supercedes the general LAN disable recommendations below.

Depending on which I/O Control Hub you are connecting, the information can be found in the errata section of the following documents:

- *I/O Controller Hub 9 (ICH9) Family Specification Update*
- *I/O Controller Hub 10 (ICH10) Family Specification Update*

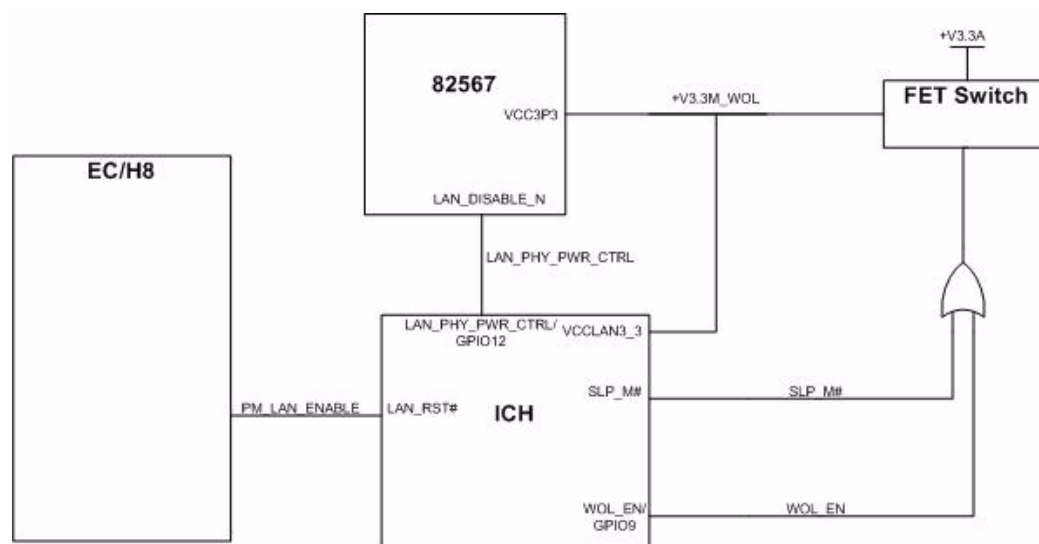
3.2.5.1 General LAN Disable Recommendations

LAN_DISABLE_N needs to be connected to the GPIO12/LAN_PHY_PWR_CTRL output of ICH9, ICH9M, or ICH10. The GPIO12 needs to be configured using ICH soft straps as LAN_PHY_PWR_CTRL (bit [20] of STRP0 register - LAN_PHY_PWR_CTRL/GPIO12 Select (LAN_PHY_PWR_GPIO12_SEL) set to "1." This can be done with the Intel FIT tool by setting LAN_PHY_PWR_CTRL in ICH STRP0 to native mode ("1"). Please refer to ICH9 EDS Section 22.2.5.1 for more details.



In addition, LAN_PHY_PWR_CTRL can also be used to turn the 3.3 V power off to the 82567 when the PHY is disabled. This will also turn the PHY off when in Sx state and WOL is disabled from the OS (through driver settings) for systems that have ME disabled. This capability is called PHY Power Down and can be enabled/disabled through GbE NVM Word 0x13.9.

The figure below shows the power delivery for 82567 and ICH LAN along with the recommended connection for LAN_PHY_PWR_CTRL to LAN_DISABLE_N pin of 82567.



Note: LAN_PHY_PWR_CTRL should be connected directly to LAN_DISABLE_N pin of 82567

Note: LAN_PHY_PWR_CTRL cannot be used to gate the 3.3V power rail to the ICH LAN. Please refer to 82567 Specification Update for more information on LAN_PHY_PWR_CTRL connection.

Figure 2. Recommended Platform Power Delivery for 82567.

4.0 Voltage, Temperature, and Timing Specifications

4.1 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|--------|----------------------------|------|-------|------|
| VCCP | Periphery Voltage Range | 3.0 | 3.6 | V |
| VCC1p8 | Core/Analog Voltage Range | 1.71 | 2.015 | V |
| VCC1p0 | Core Digital Voltage Range | 0.98 | 1.12 | V |

4.2 DC and AC Characteristics

Table 3. DC and AC Characteristics

| Symbol | Parameter | Specification | | | Units |
|--------|-------------------------------------|---------------|---------|---------|-------|
| | | Minimum | Typical | Maximum | |
| V1a | High-threshold for 3.3 V supply | 2.2 | 2.3 | 2.4 | V |
| V2a | Low-threshold for 3.3 V supply | 2.1 | 2.2 | 2.5 | V |
| V1b | High-threshold for 1.05 V supply | 0.65 | 0.7 | 0.75 | V |
| V2b | Low-threshold for 1.05 V supply | 0.55 | 0.6 | 0.65 | V |
| V1c | High-threshold for 1.8-1.9 V supply | 1.15 | 1.2 | 1.25 | V |
| V2c | Low-threshold for 1.8-1.9 V supply | 1.1 | 1.15 | 1.2 | V |

4.3 LED Electrical Specification

Table 4. LED Electrical Specification

| Symbol | Condition | Min | Nom | Max | Units |
|--|----------------------------|-------|-----|------------|-------|
| VDDO | - | 3.0 | 3.3 | 3.6 | V |
| V _{il} | - | -0.65 | | 1.0 | V |
| V _{ih} | - | 2.0 | | VDDO + 0.4 | V |
| Input Leakage | 0 < V _{in} < VDDO | | | 10 | μA |
| I _{ol} @V _{ol} =0.4 V | SR=11 | 12 | | | mA |
| I _{oh} @V _{oh} =VDDO - 0.4 V | SR=11 | 12 | | | mA |
| C _{in} | - | | | 5 | pF |



4.4 Crystal Specifications

Following are the recommended crystal specifications for operation with the 82567.

| Parameter Name | Symbol | Recommended Value | Max/Min Range | Conditions |
|---|----------------------|--------------------|-------------------|------------|
| Frequency | f_o | 25.000 MHz | - | @25 °C |
| Vibration mode | - | Fundamental | - | - |
| Cut | - | AT | - | - |
| Operating/Calibration Mode | - | Parallel | - | - |
| Frequency Tolerance | $\Delta f/f_o$ @25°C | ±30 ppm | Note ¹ | @25 °C |
| Temperature Tolerance | $\Delta f/f_o$ | ±30 ppm | Note ¹ | - |
| Operating Temperature | T_{opr} | -20 to +70 °C | Note ¹ | - |
| Non Operating Temperature | T_{opr} | -40 to +90 °C | - | - |
| Equivalent Series Resistance (ESR) | R_s | 40 Ω | 50 Ω | @25 MHz |
| Load Capacitance | C_{load} | 18 pF (max 24 pF) | Note ¹ | - |
| Shunt Capacitance | C_o | 6 pF | Note ¹ | - |
| Pullability from Nominal Load Capacitance | $\Delta f/C_{load}$ | 15 ppm/pF max | - | - |
| Max Drive Level | D_L | 300 μ W | Note 4 | - |
| Insulation Resistance | IR | 500 M Ω min | | @ 100 VDC |
| Aging | $\Delta f/f_o$ | ±5 ppm per year | ±5 ppm per year | - |
| Differential Board Capacitance | C_D | 2 pF | Note ² | |
| Board Capacitance | C_s | 4 pF | Note ³ | - |
| External Capacitors | C_1, C_2 | 27 pF | Note ¹ | - |
| Board Resistance | R_s | 0.1 Ω | 1 Ω | - |

- When not using values within 1% of the recommended values, the following procedures must be used:
 - On the board with the crystal and the 82567, measure the clock at the output of the receive and transmit lines.
 - Change C_1 and C_2 to meet with the 25 MHz requirement.
 - Ensure the demand on the 25 MHz clock has a deviation of less than 30 ppm (for example, 25 MHz \pm 750 Hz).
 - If the measured frequency is higher than 25.00075 MHz, replace capacitors C_1 and C_2 with larger capacitors.
 - If the measured frequency is lower than 24.99925 MHz, replace capacitors C_1 and C_2 with smaller capacitors.
- Differential board capacitance is the capacitance between Ser_CLK_PLUS and Ser_CLK_MINUS.
- Board capacitance is the differential capacitance between the input and output. This parasitic capacitance must be less than or equal to the specification. This value can change up to 10%. The procedures listed in footnote "1" must be followed to comply with the ppm specification.
- Crystal must meet or exceed the specified drive level (D_L). A crystal with a specified drive level of less than 300 μ W does not meet this requirement.

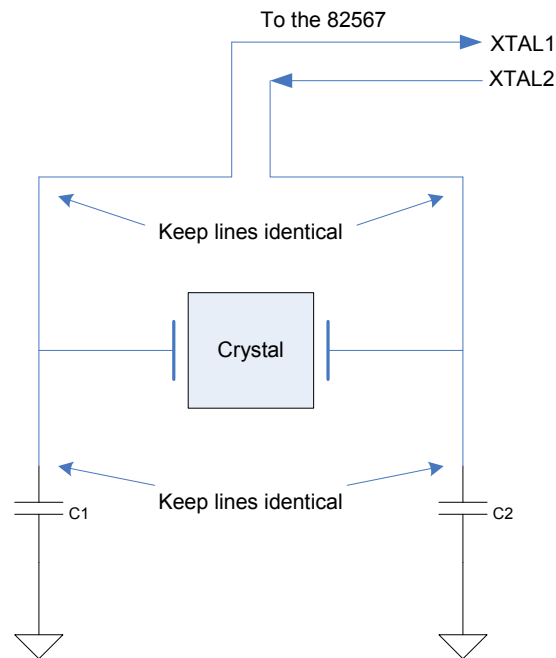


Figure 3. Crystal Connectivity to the 82567

The current from the 82567 does not change regardless of generating the 1.05 V using the on-die transistor or an external pass transistor. The total current demand remains constant, but the power dissipated by the 82567 package changes. The 1.05 V power is either on-die or at the external pass transistor.



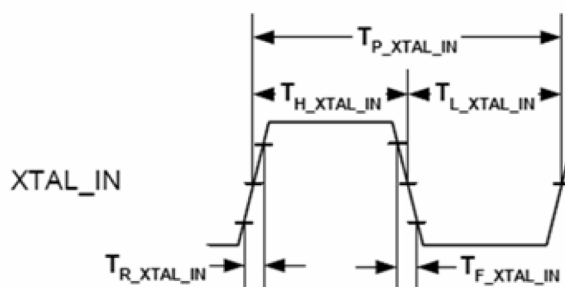
4.5 Oscillator Specifications

Table 5. Oscillator Specifications and Timing Requirements

| Parameter Name | Symbol/ Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|----------------------|---------------|-----|--------------------|------------------|------------|
| Frequency | f | @25 °C] | | 25.0 | | MHz |
| Swing | V_{p-p} | | 3 | 3.3 | 3.6 | V |
| Frequency Tolerance | f/f_0 | -20 to +70 | | ±30 | | ppm |
| Temperature Stability | | 0 °C to 70 °C | | ±30 | | ppm |
| Operating Temperature | T_{opr} | -20 to +70 °C | | | | |
| Aging | f/f_0 | | | ±5 ppm per year | | ppm |
| Coupling capacitor | $C_{coupling}$ | | 12 | 15 | 18 | pF |
| Calibration mode | Parallel | | | | | |
| Oscillator Load Capacitance | | | | 18 | | pF |
| Shunt Capacitance | | | | | 6 | pF |
| Series Resistance, R_s | | | | | 50 | Ω |
| Drive Level | | | | | 300 | μW |
| Insulation Resistance | | @ 100 VDC | 500 | | | M Ω |
| $T_{H_XTAL_IN}$ | XTAL_IN High Time | | 13 | 20 | | ns |
| $T_{L_XTAL_IN}$ | XTAL_IN Low Time | | 13 | 20 | | ns |
| $T_{R_XTAL_IN}$ | XTAL_IN Rise | 10%-90% | | | 5 | ns |
| $T_{F_XTAL_IN}$ | XTAL_IN Fall | 10%-90% | | | 5 | ns |
| $T_{J_XTAL_IN}$ | XTAL_IN Total Jitter | | | | 200 ¹ | ps |

1 Broadband peak-peak=200pS, Broadband rms=3pS, 12 kHz to 20 MHz rms= 1ps

XTAL_IN/XTAL_OUT Timing



4.5.1 Oscillator High Voltage Configuration

This configuration involves capacitor C1, which forms a capacitor divider with Cstray of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

$$V_{in} = V_{DD} * (C1 / (C1 + C_{stray}))$$

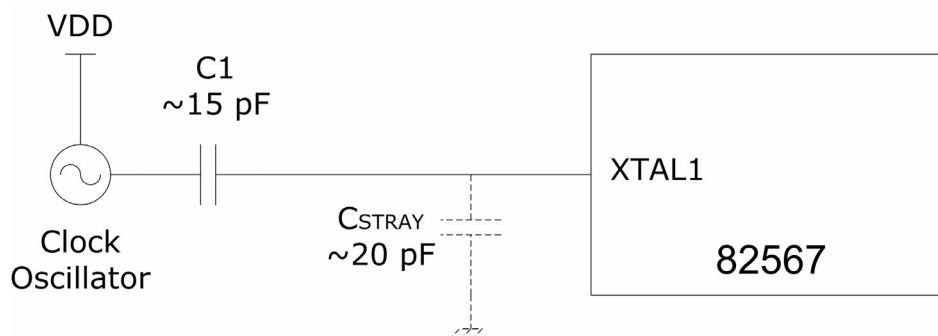
$$V_{in} = 3.3 * (C1 / (C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, $C1$ should be adjusted by tuning the input clock amplitude to approximately 1.2-1.8 V_{ptp}. If C_{stray} equals 20 pF, then $C1$ is 15 pF $\pm 10\%$. A low capacitance, high impedance probe ($C < 1$ pF, $R > 500$ K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation. If jitter performance is poor, a lower jitter clock oscillator can be implemented.

Note: C_{stray} shown in the figure below is not an actual discrete capacitor, but a representation of the board capacitance and is not to be placed in the actual design.

Note: Measure the V_{ptp} at the XTAL1 pin to ensure that it is never over 1.8 V. Overvoltage could lead to a silicon reliability concern.

Note: Keep $C1$ close to the XTAL1 pin of the 82567. This will help make the value of C_{stray} less dependent on the PCB (Total C_{stray} is a combination of C_{stray} of PCB and C_{stray} of silicon).



4.6 Power Consumption

The following table lists the measured values for the 82567's power. The numbers apply to the 82567 power dissipation with External Voltage Regulators (EVRs). Power is reduced according to link speed and link activity.

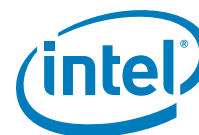


Table 6. Power Consumption—82567 with external Voltage regulator, 1.9V (VCC1P8)

| State | Mode | 3.3 V Current [mA] | 1.9 V Current [mA] | 1.05 V Current [mA] | 82567 Power [mW] | Solution Power [mW] |
|----------|---|--------------------|--------------------|---------------------|------------------|---------------------|
| S0 - Max | 1000Mbps Active, 90°C [Ta] | 22 | 256 | 115 | 680 | 1297 |
| | 1000Mbps Idle, 90°C [Ta] | 22 | 256 | 110 | 675 | 1280 |
| S0 - Typ | 1000Mbps Active | 22 | 254 | 112 | 673 | 1280 |
| | 1000Mbps Idle | 22 | 254 | 106 | 667 | 1261 |
| | 100Mbps Active | 25 | 72 | 18 | 238 | 380 |
| | 100Mbps Idle | 25 | 72 | 18 | 238 | 380 |
| | 10Mbps Active | 4 | 106 | 6 | 221 | 383 |
| | 10Mbps Idle | 4 | 64 | 6 | 141 | 244 |
| | Cable Disconnect (ACBS) | 3 | 12 | 4 | 37 | 63 |
| | Cable Disconnect (82567V only, no ACBS) | 3 | 23 | 7 | 61 | 109 |
| | LAN Disable | 3 | 6 | 3 | 24 | 40 |
| SX | 10Mbps Idle with WOL | 4 | 64 | 6 | 141 | 244 |
| | WOL disabled in driver | 3 | 6 | 3 | 24 | 40 |
| | WOL disabled in BIOS | 3 | 6 | 3 | 24 | 40 |
| | WOL disabled in BIOS w/FET switch‡ | 0 | 0 | 0 | 0 | 0 |

Note: The total solution power is the total amount of power from the 3.3V supply required for the 82567 to operate. In its mathematical form:
solution power = (82567 current) * 3.3 V. The 3.3 V is assumed since this is the normal voltage rail provided to the LAN solution.

‡ Refer to Fig. 2 for details of the implementation of V3.3WOL gated by a FET switch controlled by an OR of WOL_EN and SLP_M#

Table 7. Power Consumption—82567 with internal Voltage regulator, 1.9V (VCC1P8)

| State | Mode | 3.3 V Current [mA] | 1.9 V Current [mA] | 82567 Power [mW] | Solution Power [mW] |
|----------|---|--------------------|--------------------|------------------|---------------------|
| S0 - Max | 1000Mbps Active, 90°C [Ta] | 22 | 377 | 789 | 1317 |
| | 1000Mbps Idle, 90°C [Ta] | 22 | 370 | 776 | 1294 |
| S0 - Typ | 1000Mbps Active | 22 | 372 | 779 | 1300 |
| | 1000Mbps Idle | 22 | 365 | 766 | 1277 |
| | 100Mbps Active | 25 | 88 | 250 | 373 |
| | 100Mbps Idle | 25 | 88 | 250 | 373 |
| | 10Mbps Active | 4 | 113 | 228 | 386 |
| | 10Mbps Idle | 4 | 64 | 135 | 224 |
| | Cable Disconnect (ACBS) | 3 | 16 | 40 | 63 |
| | Cable Disconnect (82567V only, no ACBS) | 3 | 30 | 67 | 109 |
| | LAN Disable | 3 | 9 | 27 | 40 |
| SX | 10Mbps Idle with WOL | 4 | 64 | 135 | 224 |
| | WOL disabled in driver | 3 | 9 | 27 | 40 |
| | WOL disabled in BIOS | 3 | 9 | 27 | 40 |
| | WOL disabled in BIOS w/FET switch‡ | 0 | 0 | 0 | 0 |

Note: The total solution power is the total amount of power from the 3.3V supply required for the 82567 to operate. In its mathematical form:
solution power = (82567 current) * 3.3 V. The 3.3 V is assumed since this is the normal voltage rail provided to the LAN solution.

‡ Refer to Fig. 2 for details of the implementation of V3.3WOL gated by a FET switch controlled by an OR of WOL_EN and SLP_M#

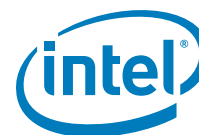


Table 8. Power Consumption—82567 with external Voltage regulator; 1.8 V (VCC1P8)

| State | Mode | 3.3 V Current [mA] | 1.8 V Current [mA] | 1.05 V Current [mA] | 82567 Power [mW] | Solution Power [mW] |
|----------|---|--------------------|--------------------|---------------------|------------------|---------------------|
| S0 - Max | 1000Mbps Active, 90°C [Ta] | 22 | 253 | 115 | 643 | 1287 |
| | 1000Mbps Idle, 90°C [Ta] | 22 | 253 | 110 | 638 | 1270 |
| S0 - Typ | 1000Mbps Active | 22 | 251 | 112 | 636 | 1270 |
| | 1000Mbps Idle | 22 | 251 | 106 | 630 | 1250 |
| | 100Mbps Active | 25 | 71 | 18 | 228 | 376 |
| | 100Mbps Idle | 25 | 71 | 18 | 228 | 376 |
| | 10Mbps Active | 4 | 103 | 6 | 205 | 373 |
| | 10Mbps Idle | 4 | 63 | 6 | 133 | 241 |
| | Cable Disconnect (ACBS) | 3 | 12 | 4 | 36 | 63 |
| | Cable Disconnect (82567V only, no ACBS) | 3 | 23 | 7 | 59 | 109 |
| | LAN Disable | 3 | 6 | 3 | 24 | 40 |
| SX | 10Mbps Idle with WOL | 4 | 63 | 6 | 133 | 241 |
| | WOL disabled in driver | 3 | 6 | 3 | 24 | 40 |
| | WOL disabled in BIOS | 3 | 6 | 3 | 24 | 40 |
| | WOL disabled in BIOS w/FET switch‡ | 0 | 0 | 0 | 0 | 0 |

Note: The total solution power is the total amount of power from the 3.3V supply required for the 82567 to operate. In its mathematical form:
 $\text{solution power} = (82567 \text{ current}) * 3.3 \text{ V}$. The 3.3 V is assumed since this is the normal voltage rail provided to the LAN solution.

‡ Refer to Fig. 2 for details of the implementation of V3.3WOL gated by a FET switch controlled by an OR of WOL_EN and SLP_M#

Table 9. Power Consumption—82567 with internal Voltage regulator, 1.8 V (VCC1P8)

| State | Mode | 3.3 V Current [mA] | 1.8 V Current [mA] | 82567 Power [mW] | Solution Power [mW] |
|----------|---|--------------------|--------------------|------------------|---------------------|
| S0 - Max | 1000Mbps Active, 90 °C [Ta] | 22 | 374 | 746 | 1307 |
| | 1000Mbps Idle, 90 °C [Ta] | 22 | 368 | 735 | 1287 |
| S0 - Typ | 1000Mbps Active | 22 | 369 | 737 | 1290 |
| | 1000Mbps Idle | 22 | 362 | 724 | 1267 |
| | 100Mbps Active | 25 | 86 | 237 | 366 |
| | 100Mbps Idle | 25 | 87 | 239 | 370 |
| | 10Mbps Active | 4 | 113 | 217 | 386 |
| | 10Mbps Idle | 4 | 63 | 127 | 221 |
| | Cable Disconnect (ACBS) | 3 | 14 | 35 | 56 |
| | Cable Disconnect (82567V only, no ACBS) | 3 | 30 | 64 | 109 |
| | LAN Disable | 3 | 9 | 26 | 40 |
| SX | 10Mbps Idle with WOL | 4 | 63 | 127 | 221 |
| | WOL disabled in driver | 3 | 9 | 26 | 40 |
| | WOL disabled in BIOS | 3 | 9 | 26 | 40 |
| | WOL disabled in BIOS w/FET switch† | 0 | 0 | 0 | 0 |

Note: The total solution power is the total amount of power from the 3.3V supply required for the 82567 to operate. In its mathematical form:
solution power = (82567 current) * 3.3 V. The 3.3 V is assumed since this is the normal voltage rail provided to the LAN solution.

† Refer to Fig. 2 for details of the implementation of V3.3WOL gated by a FET switch controlled by an OR of WOL_EN and SLP_M#

4.7 Power Delivery

The 82567 operates from two or three external power rails:

- A 3.3 V power rail for internal power regulation and for periphery.
- A 1.8 V-1.9 V power rail for analog functions. (See the *82567 Specification Update* for more information.)
- An optional 1.05 V power rail. Onboard transistor saved/unused when the on-die LVR is used.

4.7.1 The 1.8 V-1.9 V Rail

The power delivery system supports a load of 300 mA.

The 1.8 V-1.9 V rail is tunable and can be supplied in one of three ways:

- A discrete Switched Voltage Regulator (SVR) solution.
- An external power supply that is not dependent on support from 82567. For example, the platform designer might choose to route a platform-available 1.8 V-1.9 V supply to the 82567.
- A discrete LVR solution where the base current of PnP power transistor is driven by the 82567, while the power transistor is placed externally. 1.9 V is the default value.



4.7.2 The 1.05 V Rail

The 1.05 V power delivery system supports a load of 300 mA.

The 1.05 V rail can be supplied in one of three ways:

- An external power supply that is not dependent on support from the 82567. For example, the platform designer might choose to route a platform-available 1.05 V supply to the 82567.
- A fully integrated on-die LVR solution.
- A discrete LVR solution, where the base current of PNP power transistor is driven by the 82567, while the power transistor is placed externally.
- A discrete Switched Voltage Regulator (SVR) solution.

4.7.3 Voltage Regulator Schematics

Schematics for 82567 power delivery using integrated and discrete LVRs are included in the reference schematics (titled *82567_Gigabit_Ethernet_PHY_Reference_Schematics*)

4.7.4 Voltage Regulator Power Supply Specifications

4.7.4.1 3.3 V Rail

| Title | Description | Min | Max | Units |
|-------------------|---|-----|-------|-------|
| Rise Time | Time from 10% to 90% mark | 1 | 100 | ms |
| Monotonicity | Voltage dip allowed in ramp | | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% | | 28800 | V/s |
| Operational Range | Voltage range for normal operating conditions | 3 | 3.6 | V |
| Ripple | Maximum voltage ripple @ BW = 50MHz | | 70 | mV |
| Overshoot | Maximum voltage allowed | | 4 | V |
| Capacitance | Minimum capacitance | 25 | | uF |

4.7.4.2 1.8 V-1.9 V Rail

| Title | Description | Min | Max | Units |
|--------------------|---|------|-------|-------|
| Rise Time | Time from 10% to 90% mark | 1 | 100 | ms |
| Monotonicity | Voltage dip allowed in ramp | | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% | | 1440 | V/s |
| Operational Range | Voltage range for normal operating condtions | 1.71 | 2.015 | V |
| Ripple | Maximum voltage ripple @ BW = 50MHz | | 50 | mV |
| Overshoot | Maximum voltage allowed | | 2.7 | V |
| Output Capacitance | Capacitance range when using PNP circuit | 20 | 40 | uF |

| Title | Description | Min | Max | Units |
|-------------------|--|-----|-----|-------|
| Input Capacitance | Capacitance range when using PNP circuit | 20 | | μF |
| Capacitance ESR | Equivalent series resistance of output capacitance | 5 | 100 | mΩ |
| Ictrl | Maximum output current rating rating to CTRL18 | | 10 | mA |

Note: Do not use tantalum capacitors.

4.7.4.3 1.05 Rail

| Title | Description | Min | Max | Units |
|--------------------|--|------|------|-------|
| Rise Time | Time from 10% to 90% mark | 1 | 100 | ms |
| Monotonicity | Voltage dip allowed in ramp | | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% | | 800 | V/s |
| Operational Range | Voltage range for normal operating conditions | 0.98 | 1.12 | V |
| Ripple | Maximum voltage ripple @ BW = 50MHz | | 30 | mV |
| Overshoot | Maximum voltage allowed | | 1.5 | V |
| Output Capacitance | Capacitance range when using PNP circuit | 20 | 40 | μF |
| Input Capacitance | Capacitance range when using PNP circuit | 20 | | μF |
| Capacitance ESR | Equivalent series resistance of output capacitance | 5 | 100 | mW |
| Ictrl | Maximum output current rating rating to CTRL10 | | 10 | mA |

4.7.5 PNP Specifications

| Title | Description | Min | Max | Units |
|------------------------|---|-----|-----|-------|
| VCBO | | 20 | | V |
| VCEO | | 20 | | V |
| IC(max) | | 1 | | A |
| IC(peak) | | 1.2 | | A |
| Ptot | Minimum total dissipated power @ 25°C ambient temperature | 1.5 | | W |
| hFE | DC current gain @ Vce=-10V, Ic=500mA | 85 | | |
| hfe | AC current gain @ Ic=50mA VCE=-10V, f=20MH | 2.5 | | |
| Cc | Collector capacitance @ VCB=-5V, f=1MHz | | 50 | pF |
| fT | Transition frequency @ Ic=10mA, VCE=-5V, f=100MHz | 40 | | MHz |
| Recommended Transistor | BCP69 | | | |

Note: Maximum current of 1.8 V-1.9 V is less then 270mA, Maximum current of 1.05 V is less then 139mA. 1.8 V-1.9 V and 1.05 V PnP used is BCP69 (see BCP69 spec).



4.7.6 Power Sequencing

For proper and safe operation, the power supplies must follow the following rule:

$$VDDO (3.3 \text{ V}) \geq AVDD (1.8 \text{ V or } 1.9 \text{ V}) \geq DVDD (1.05 \text{ V})$$

This means that VDDO must start ramping before AVDD and DVDD, but DVDD may reach its nominal operating range before AVDD and VDDO.

Basically, the higher voltages must be greater than or equal to the lower voltages. This is necessary to avoid low impedance paths through clamping diodes and to eliminate back-powering.

The same requirements apply to the power-down sequence.

LAN_RST# must be low throughout the time that the power supplies are ramping. This will guarantee that the MAC and PHY reset cleanly. While LAN_RST# is low, PHYRST# will also be asserted to reset the PHY.

4.8 Timing Parameters

4.8.1 Timing Requirements

The 82567 requires the following start-up and power state transitions.

Table 10. Timing Requirements

| Parameter | Description | Min | Max | Notes |
|-----------------|---|------|---------|-----------------------|
| T_{JRST_min} | Minimum duration of JRSTSYNC pulse | 1 ms | | Per LCI specification |
| T_{c2dud} | Completion of dock/undock configuration following cable connection | | 0.5 sec | |
| T_{r2init} | Completion of PHY configuration following a reset complete indication | | 0.5 sec | |

4.8.2 Timing Guarantees

The 82567 guarantees the following start-up and power state transition related timing parameters.

Table 11. Timing Guarantees

| Parameter | Description | Min | Max | Notes |
|-----------------------------|--|-------|-----------|---|
| T_{PHY_Reset} | Reset de-assertion to PHY reset complete | | 10 ms | PHY configuration should be delayed until PHY completes its reset |
| T_{XTAL} | XTAL frequency stable after platform power ramp up | | 5 ms | |
| T_{POR} | Internal POR trigger after XTAL stable | | 1 μ s | |
| T_{JKCLK} | JKCLK output stable after internal POR | | 3 μ s | |
| $T_{TX_IDLE-TO-DIFF-DATA}$ | Maximum time to transition to valid TX specifications after leaving an electrical idle condition | | 200 ns | Required by GLCI 2.0 specification |
| $T_{RX_IDLE-TO-DIFF-DATA}$ | Maximum time to be ready to accept data after leaving an electrical idle condition | | 200 ns | Required by GLCI 2.0 specification |
| T_{c2an} | Cable connect to start of auto negotiation | 1.2 s | 1.3 s | Per 802.3 specification |

5.0 Package and Pinout Information

The physical characteristics of the 82567 are described in this section. The pin number to signal mapping is indicated in [Section 5.4](#).

5.1 Package Information

The package used for the 82567 is an 56-pin QFN package. The Epad size is option number 4.

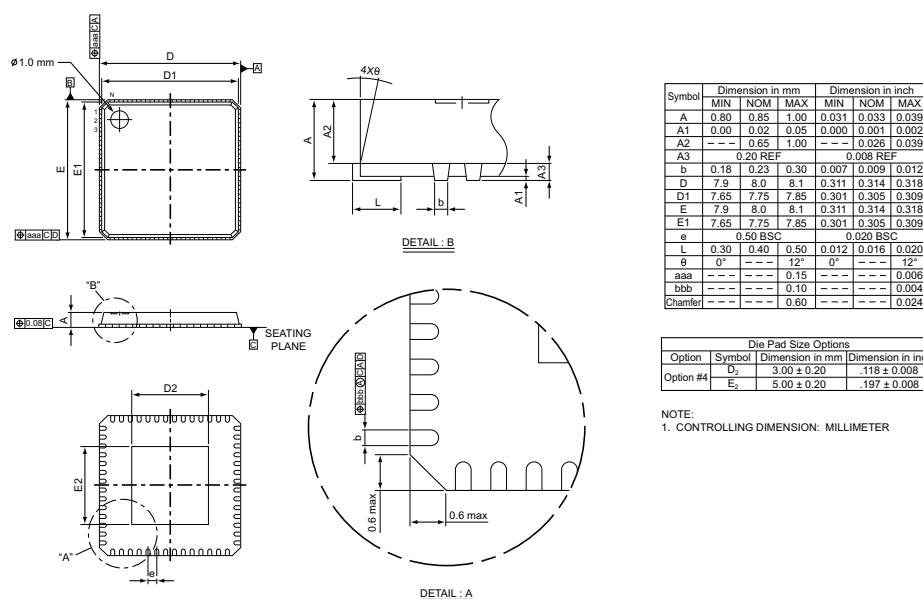


Figure 4. 82567 Mechanical Drawing

5.2 Thermal

The thermal resistance from junction to case, J_C , is 6.1 C/Watt. The thermal resistance from junction to ambient, J_A , is as follows:

| Air Flow (m/s) | Maximum T_J | θ_{ja} (°C/Watt) |
|----------------|---------------|-------------------------|
| 0 | 127.1 | 26.0 |
| 1 | 122.1 | 23.7 |
| 2 | 119.3 | 22.4 |
| 3 | 117.5 | 21.6 |

Note: No heat sink required.

| Operating Ambient Temperature | |
|-------------------------------|---------|
| Minimum | Maximum |
| 0 °C | 85 °C |

5.3 Internal Pull-Up Resistors

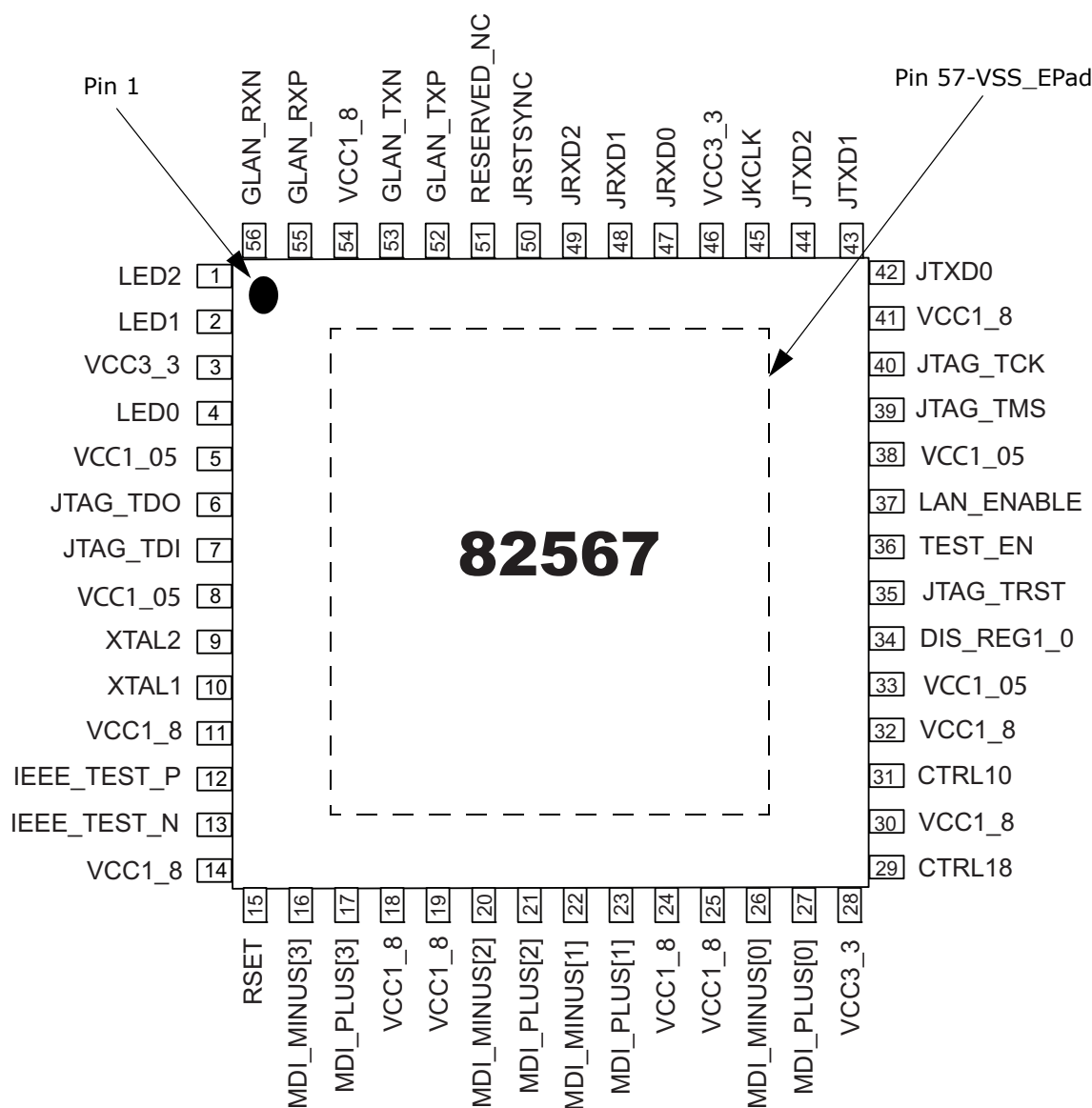
Table 12 lists the internal pull-up resistors and their functionality in different device states. Each internal pull-up resistor has a nominal value of 5 k Ω , ranging from 2.7 k Ω to 8.6 k Ω .

Table 12. Internal Pull-Up Resistors

| Signal Name (Pin Location) | Default State | Power-Down State ¹ |
|----------------------------|---------------|-------------------------------|
| LED0 (4) | Not connected | Connected |
| LED1 (2) | Not connected | Connected |
| LED2 (1) | Not connected | Connected |
| JTAG_TCK (40) | Not connected | Connected |
| JTAG_TDI (7) | Connected | Connected |
| JTAG_TDO (6) | Not connected | Not Connected |
| JTAG_TMS (39) | Connected | Connected |
| JTXD[2:0] (42, 43, 44) | Not Connected | Not Connected |
| JRXD[2:0] (47, 48, 49) | Not Connected | Not Connected |
| LAN_DISABLE_N (37) | Connected | Connected |

1. This column describes the state of the internal pull-up resistors in device power-down mode when the internal voltage regulators are shut down.

5.4 Visual Pin Assignments



Note: VCC1_8 range is 1.71 V to 2.015 V

VCC1_05 range is 0.98 V to 1.12 V

Figure 5. 82567 Pinout (Top View, Pins Down)



Table 13. Pin Mapping

| Pin | Pin Name | Pin | Pin Name |
|-----|--------------|-----|---------------|
| 1 | LED2 | 29 | CTRL18 |
| 2 | LED1 | 30 | VCC1_8 |
| 3 | VCC3_3 | 31 | CTRL10 |
| 4 | LED0 | 32 | VCC1_8 |
| 5 | VCC1_05 | 33 | VCC1_05 |
| 6 | JTAG_TDO | 34 | REG_DIS1_0 |
| 7 | JTAG_TDI | 35 | JTAG_TRST |
| 8 | VCC1_05 | 36 | TEST_EN |
| 9 | XTAL2 | 37 | LAN_DISABLE_N |
| 10 | XTAL1 | 38 | VCC1_05 |
| 11 | VCC1_8 | 39 | JTAG_TMS |
| 12 | IEEE_TEST_P | 40 | JTAG_TCK |
| 13 | IEEE_TEST_N | 41 | VCC1_8 |
| 14 | VCC1_8 | 42 | JTXD0 |
| 15 | RSET | 43 | JTXD1 |
| 16 | MDI_MINUS[3] | 44 | JTXD2 |
| 17 | MDI_PLUS[3] | 45 | JKCLK |
| 18 | VCC1_8 | 46 | VCC3_3 |
| 19 | VCC1_8 | 47 | JRXD0 |
| 20 | MDI_MINUS[2] | 48 | JRXD1 |
| 21 | MDI_PLUS[2] | 49 | JRXD2 |
| 22 | MDI_MINUS[1] | 50 | JRSTSYNC |
| 23 | MDI_PLUS[1] | 51 | RESERVED_NC |
| 24 | VCC1_8 | 52 | GLAN_TXP |
| 25 | VCC1_8 | 53 | GLAN_TXN |
| 26 | MDI_MINUS[0] | 54 | VCC1_8 |
| 27 | MDI_PLUS[0] | 55 | GLAN_RXP |
| 28 | VCC3_3 | 56 | GLAN_RXN |



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