1M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-6, -7 or -8), power consumption (Normal or Low power) , and package type (SOJ, ZIP,DIP) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 1Mx1 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM41C1000D/D-L(5V)
- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	385
-7	358
-8	330

- Refresh cycles

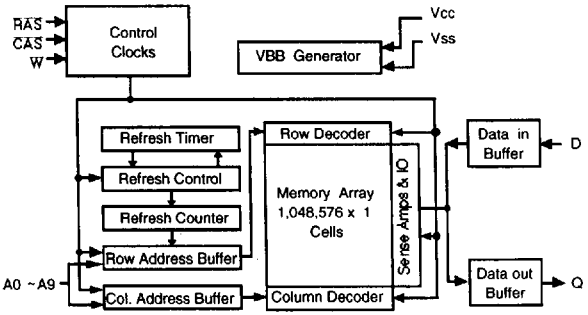
Part No.	Refresh Cycle	Refresh period	
		Normal	L
KM41C1000D	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

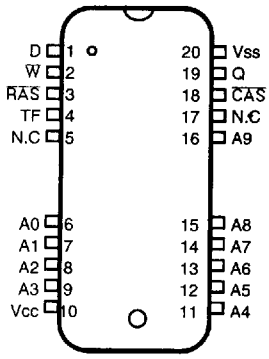
- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL(5V) compatible inputs and outputs
- 256K x 4 fast test mode
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP and DIP packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM

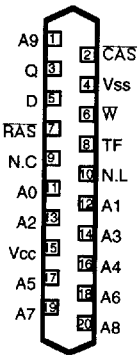


PIN CONFIGURATION (Top Views)

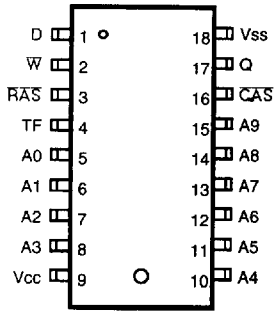
• KM41C1000DJ



• KM41C1000DZ



• KM41C1000DP



Pin Name	Pin Function
A0 - A9	Address Inputs
D	Data In
Q	Data Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
Vcc	Power(+5.0V)
N.C	No Connection
TF	Test Function
NL	No Lead

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	μA
Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM41C1000D	
I_{CC1}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	50 45 40	mA mA mA
I_{CC5}	Normal L	Don't care	1 100	mA μA
I_{CC6}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC7}	L	Don't care	100	μA

I_{CC1}* : Operating current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

D_{IN}=$\overline{W}$=A0 ~ A9 = Vcc-0.2V or 0.2V , T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A9]	C_{IN2}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	130		150		170		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	14
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	14
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	60		60		65		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. Normal operation requires the "TF" pin to be connected to Vss or TTL logic low level or left unconnected on the printed wiring board.
12. When the "TF" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function".
13. In a test mode cycle, the value of tRAC, tCAC, tAA is delayed for 3ns.
14. tAR, tWCR, and tDHR are referenced to $t_{RAD(MAX)}$.