



MC14077B
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**MC14078B, MC14081B,
MC14082B**
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MC14093B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C
Ceramic "L" Package: -12mW/°C from 100°C to 125°C



L SUFFIX
CERAMIC PACKAGE
CASE 632



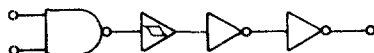
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

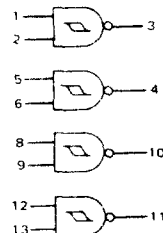
EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V _{in} = 0 or V _{DD}		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
10		9.95	—	9.95	10	—	9.95	—		
15		14.95	—	14.95	15	—	14.95	—		
Output Drive Current (AL Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mA _{dc}
Sink I _{OL}		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}	
10	1.6	—	1.3	2.25	—	0.9	—			
15	4.2	—	3.4	8.8	—	2.4	—			
Output Drive Current (CL/CP Device) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	−2.5	—	−2.1	−4.2	—	−1.7	—	mA _{dc}
Sink I _{OL}		5.0	−0.52	—	−0.44	−0.88	—	−0.36	—	
		10	−1.3	—	−1.1	−2.25	—	−0.9	—	
		15	−3.6	—	−3.0	−8.8	—	−2.4	—	
	5.0	0.52	—	0.44	0.88	—	0.36	—	mA _{dc}	
10	1.3	—	1.1	2.25	—	0.9	—			
15	3.6	—	3.0	8.8	—	2.4	—			
Input Current (AL Device)	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Current (CL/CP Device)	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μA _{dc}
	10	—	0.5	—	0.0010	0.5	—	15		
	15	—	1.0	—	0.0015	1.0	—	30		
Quiescent Current (CL/CP Device) (Per Package)	I _{DD}	5.0	—	1.0	—	0.0005	1.0	—	7.5	μA _{dc}
	10	—	2.0	—	0.0010	2.0	—	15		
	15	—	4.0	—	0.0015	4.0	—	30		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF, on all outputs, all buffers switching)	I _T	5.0	I _T = (1.2 μA/kHz) f + I _{DD}							μA _{dc}
	10	I _T = (2.4 μA/kHz) f + I _{DD}								
	15	I _T = (3.6 μA/kHz) f + I _{DD}								
Hysteresis Voltage (Pins 1, 5, 8 and 12 held high or Pins 2, 6, 9 and 13 held high)	V _H	5.0	0.20	0.62	0.17	0.26	0.6	0.13	0.6	Vdc
	10	0.29	0.85	0.25	0.38	0.8	0.20	0.8		
	15	0.39	1.20	0.33	0.50	1.1	0.27	1.1		
Threshold Voltage (Pins 2, 5, 9, 12 held high or Pins 1, 6, 8, 13 held high) Positive-Going	V _{T+}	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
Negative-Going	V _{T−}	10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	
		15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	
	V _{T−}	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.05	6.08	2.60	6.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

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SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} V_{dc}	Min	Typ. #	Max	Unit
Output Rise Time	t_{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

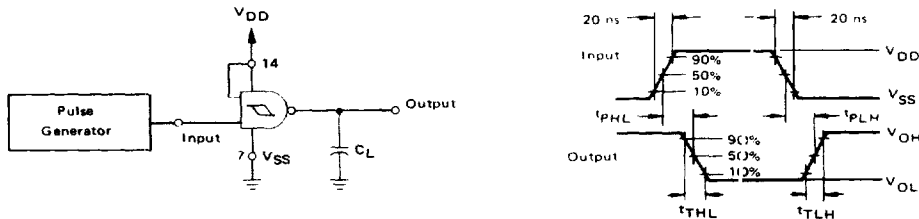
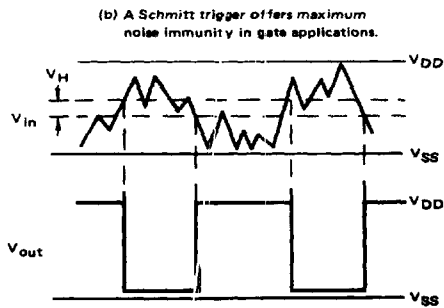
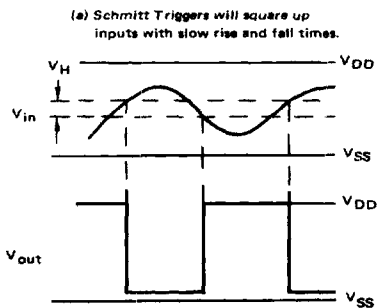
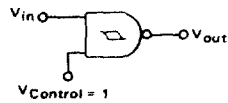


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



MC14093B

FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

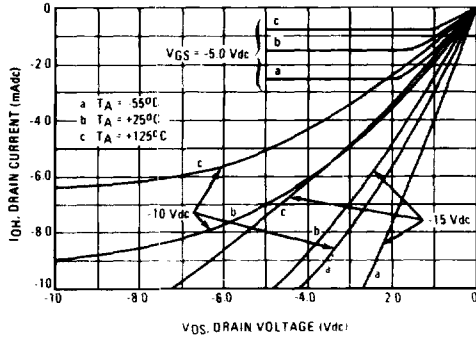
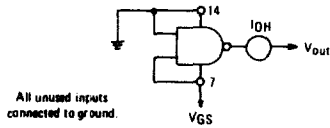


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

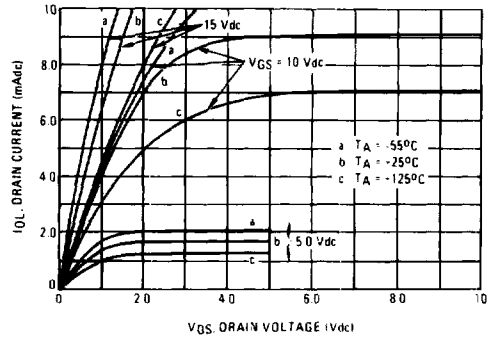
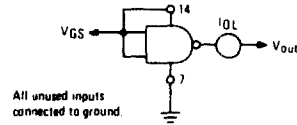
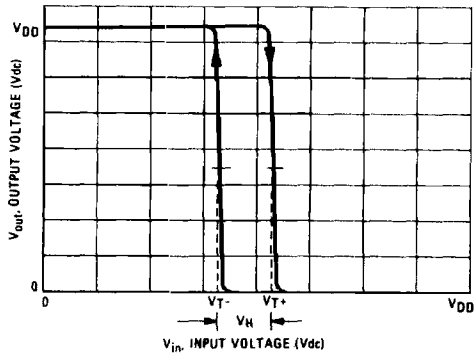


FIGURE 5 – TYPICAL TRANSFER CHARACTERISTICS



PIN ASSIGNMENT

