

HD74HC164

8-bit Parallel-out Shift Register

REJ03D0580-0300

Rev.3.00

Jan 31, 2006

Description

This 8-bit shift register has gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on the input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC164P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74HC164FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B		Q_H
L	X	X	X	L	L		L
H		X	X	Q_{Ao}	Q_{Bo}		Q_{Ho}
H		L	X	L	Q_{An}		Q_{Gn}
H		X	L	L	Q_{An}		Q_{Gn}
H		H	H	H	Q_{An}		Q_{Gn}

Q_{Ao} to Q_{Ho} = Outputs remain unchanged.

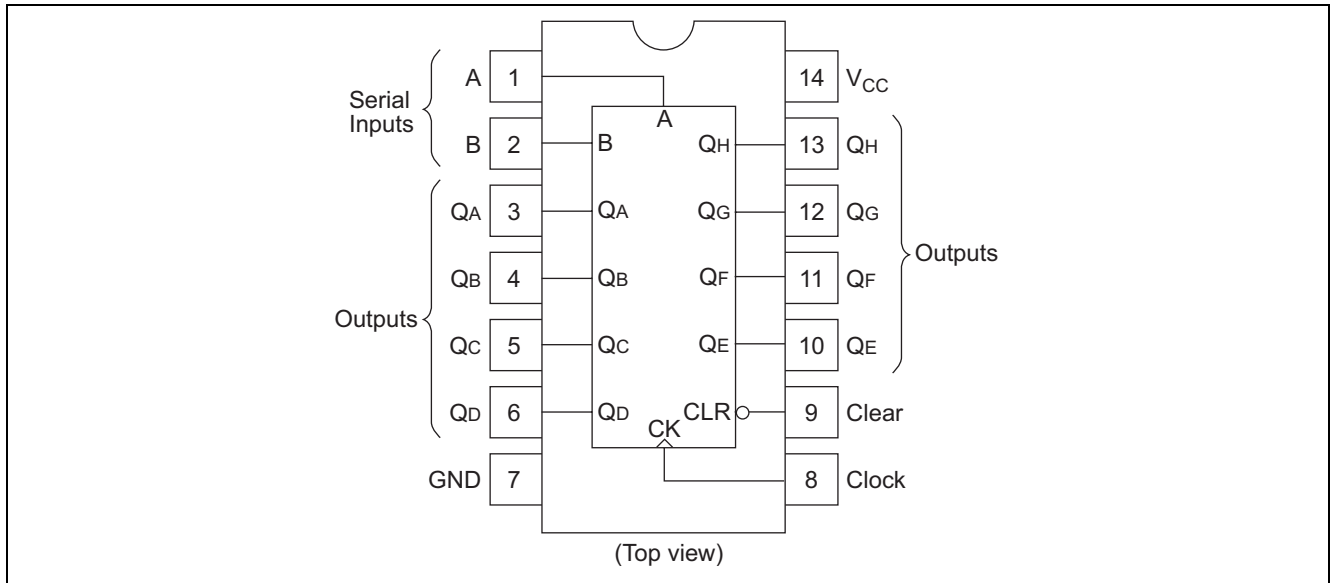
Q_{An} to Q_{Gn} = Data shifted from the previous stage on a positive edge at the clock input.

H : High level

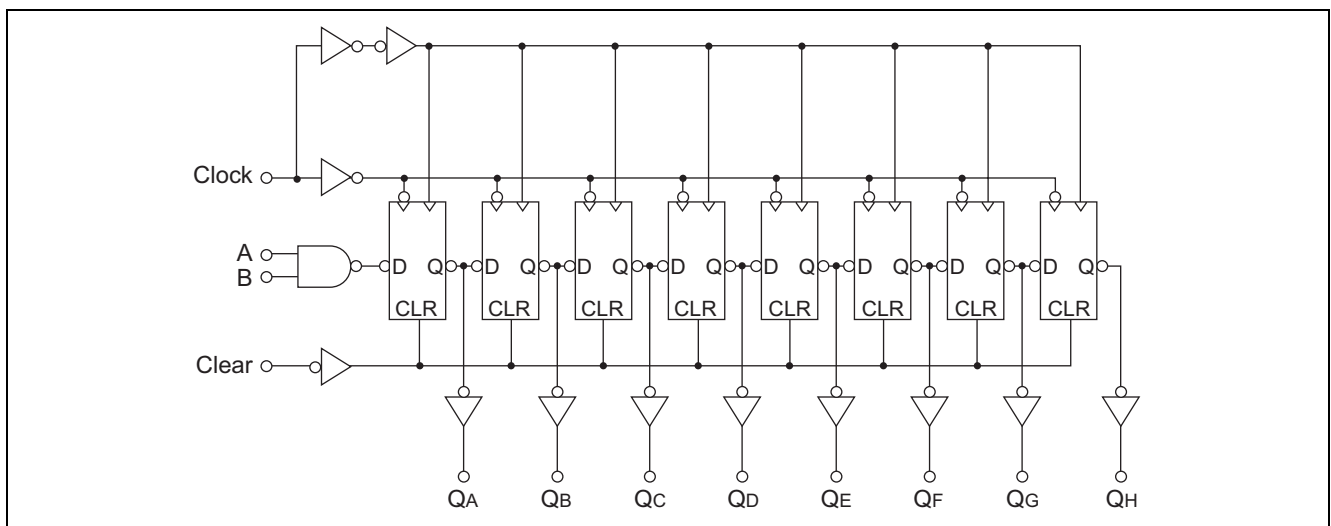
L : Low level

X : Irrelevant

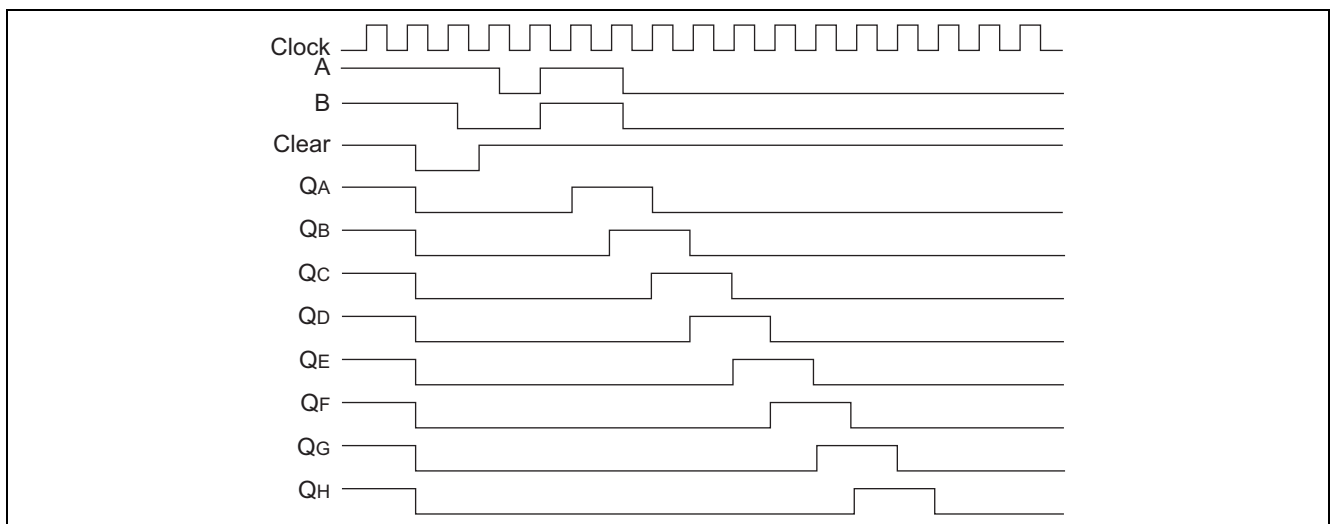
Pin Arrangement



Logic Diagram



Timing Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

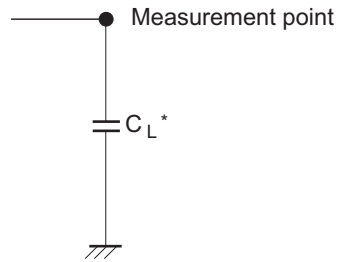
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			$I_{OH} = -4 \text{ mA}$
		6.0	5.68	—	—	5.63	—			$I_{OH} = -5.2 \text{ mA}$
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4 \text{ mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2 \text{ mA}$
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC} \text{ or GND}$	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC} \text{ or GND}, I_{out} = 0 \mu\text{A}$	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

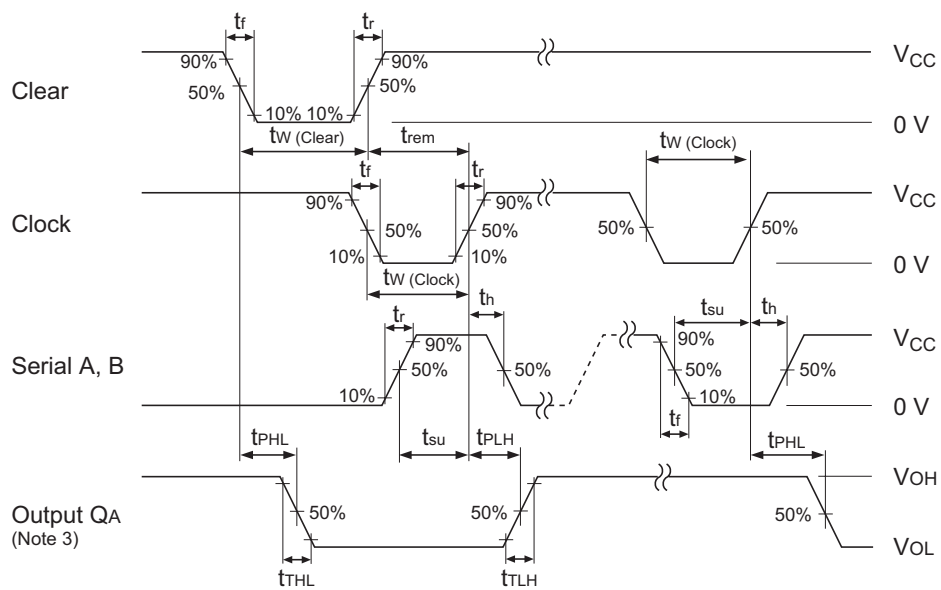
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t _{PHL}	2.0	—	—	160	—	200	ns	Clock to Q
		4.5	—	14	32	—	40		
		6.0	—	—	27	—	34		
	t _{PLH}	2.0	—	—	160	—	200	ns	
		4.5	—	15	32	—	40		
		6.0	—	—	27	—	34		
	t _{PHL}	2.0	—	—	175	—	220	ns	Clear to Q
		4.5	—	17	35	—	44		
		6.0	—	—	30	—	37		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	A, B to Clock
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t _h	2.0	5	—	—	5	—	ns	Clock to A, B
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t _{rem}	2.0	5	—	—	5	—	ns	Clear to Clock
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	Clock
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
		2.0	80	—	—	100	—	ns	Clear
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH} , t _{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

Test Circuit



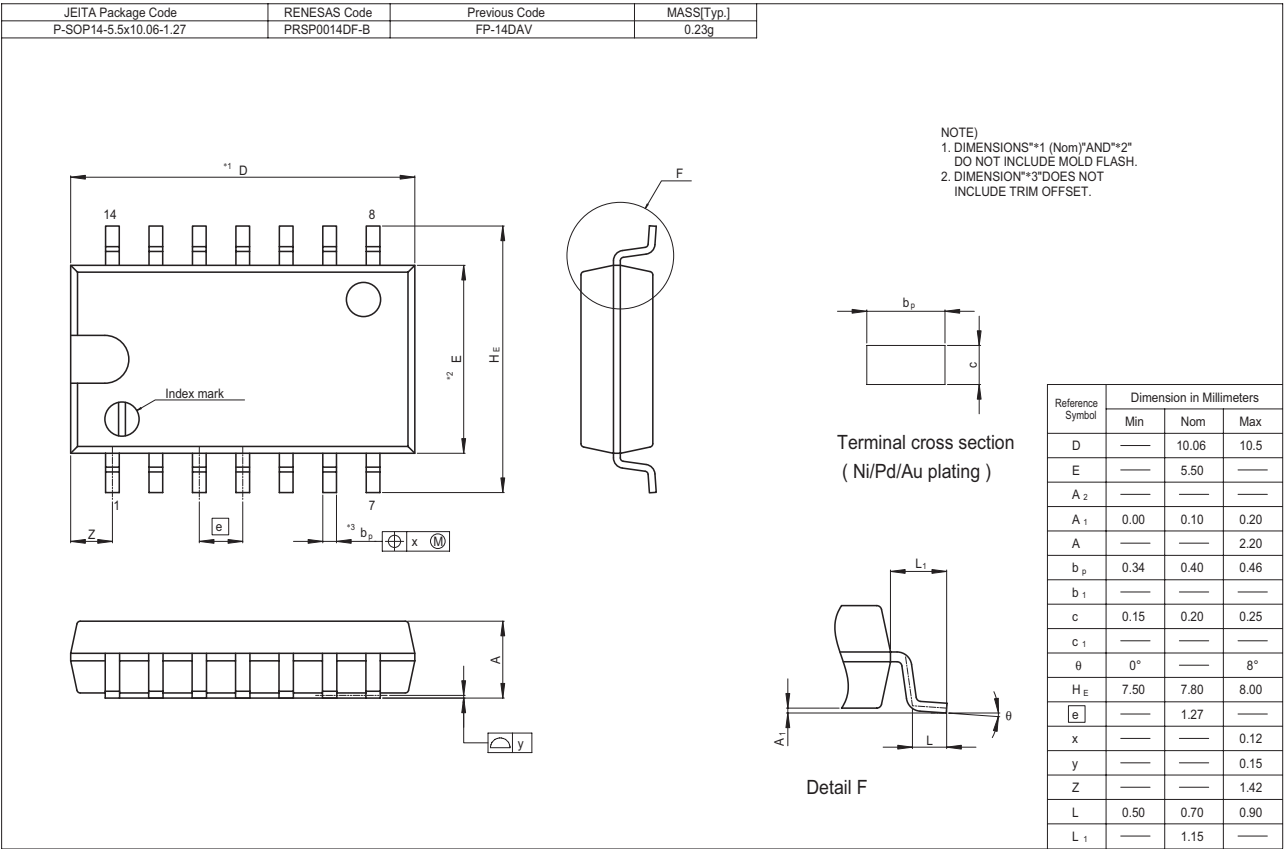
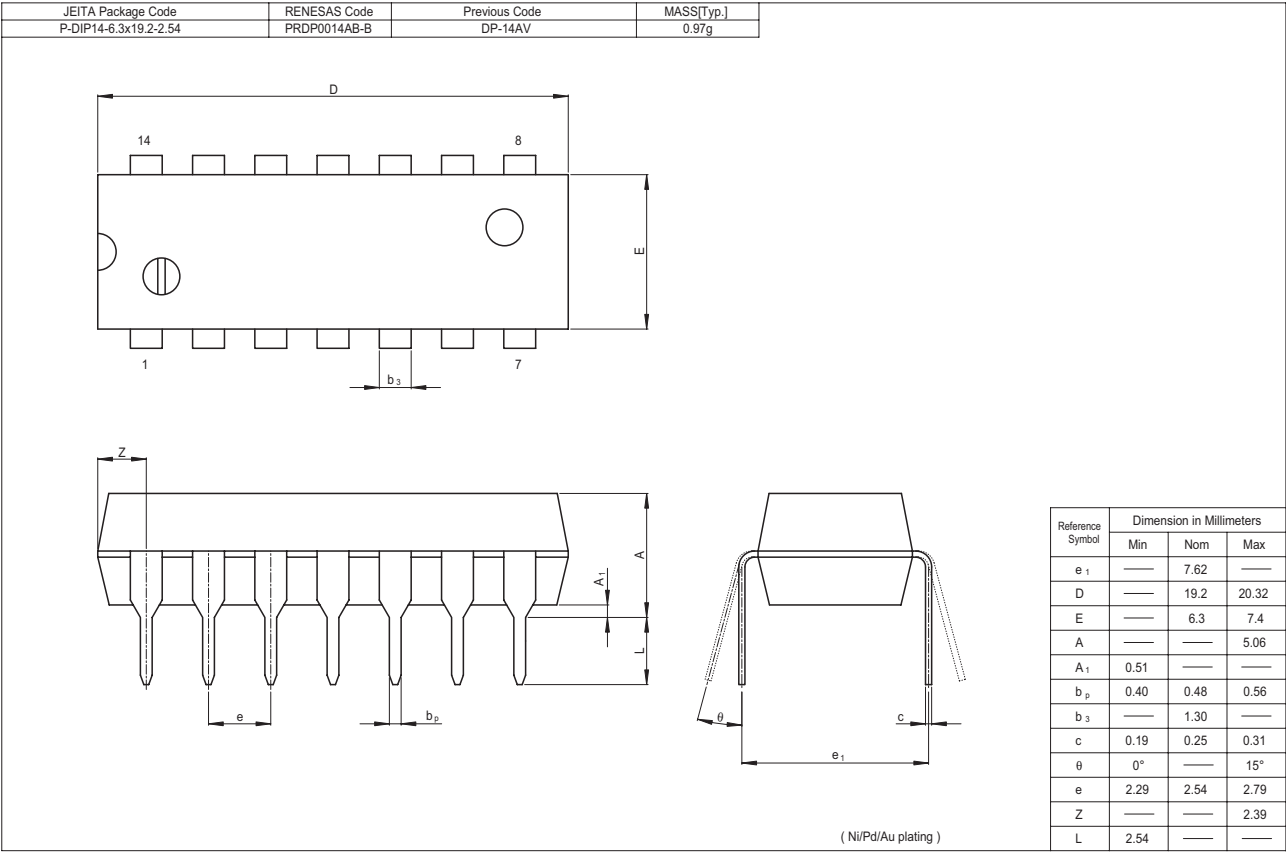
Note: C_L includes the probe and fix capacitance.

Waveforms



- Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.
 3. See function table for Q_B to Q_H outputs.

Package Dimensions



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