



Low Power Schottky Logic – 74LS164

8-Bit Serial-Input / Parallel-Output Shift Register in bare die form

Rev 1.0
24/11/17

Description

The 74LS164 is fabricated on a 2µm 40V Bipolar process. The device consists of x2 serial data inputs, A and B, provided so that one input can be used as a data enable. Data is entered on each rising edge of the clock. A LOW on the master reset input ($\overline{\text{CLR}}$) clears the register, forcing all outputs LOW, independent of other inputs. All inputs are equipped with Schottky clamp diodes to limit termination effects & achieve high speed. These input circuits also protect against static discharge & transient excess voltage.

Features:

- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Direct drop-in replacement for obsolete components in long term programs.
- Industrial temperature range.

Ordering Information

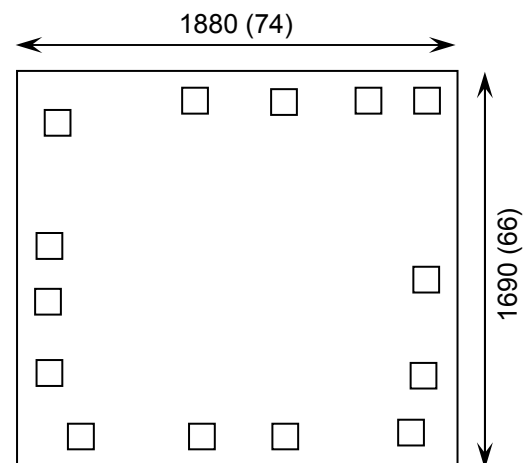
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54LS164](#)

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness $\leftrightarrow$ 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1060 x 1690 74 x 67	µm mils
Minimum Bond Pad Size	110 x 110 4.33 x 4.33	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	



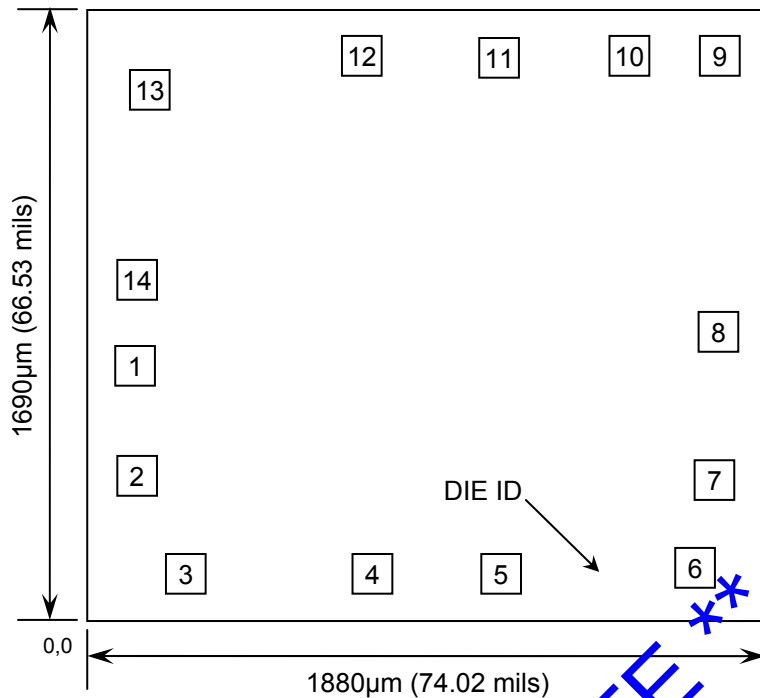


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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.075	0.647
2	B	0.077	0.342
3	Q _A	0.203	0.075
4	Q _B	0.725	0.075
5	Q _C	1.091	0.075
6	Q _D	1.625	0.083
7	GND	1.691	0.331
8	CLK	1.693	0.745
9	CLR	1.691	1.504
10	Q _E	1.449	1.505
11	Q _F	1.091	1.503
12	Q _G	0.697	1.505
13	Q _H	0.085	1.412
14	V _{CC}	0.077	0.885
CONNECT CHIP BACK TO GND OR FLOAT			

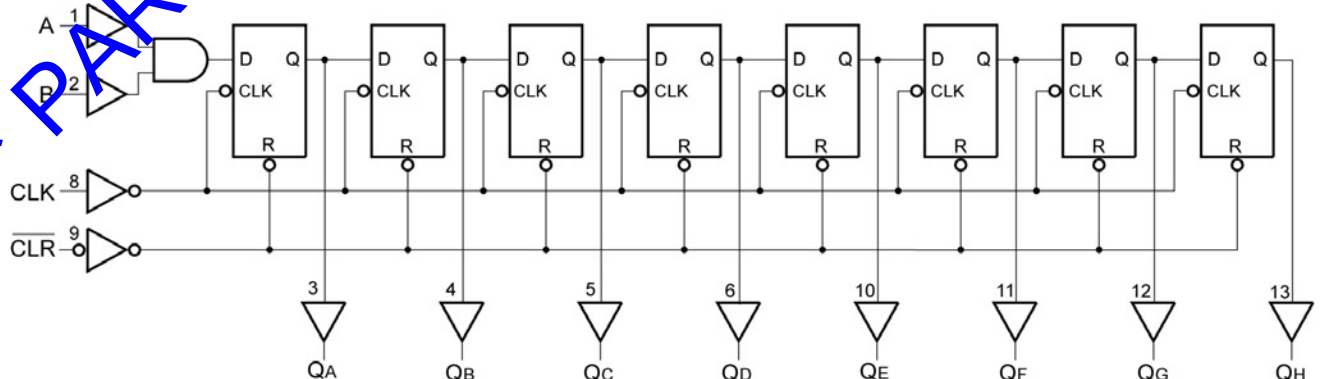
Function Table

INPUTS				OUTPUTS		
CLR	CLK	A	B	Q _A	Q _B	...
L	X	X	X	L	L	L
H	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	↑	H	H	H	Q _{AN}	Q _{GN}
H	↑	L	X	L	Q _{AN}	Q _{GN}
H	↑	X	L	L	Q _{AN}	Q _{GN}

Logic Diagram

D = Data Input

Q_{An} - Q_{Gn} = Data shift from preceding register on rising edge clock input





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.25	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
High-Level Output Current	I_{OH}	-	0.4	mA
Low-Level Output Current	I_{OL}	-	8	mA
Clock Frequency	f_{clock}	0	25	MHz
Pulse Width – Clock or Clear	t_w	20	-	ns
Setup time – A or B to Clock	t_{su}	15	-	ns
Recovery Time	t_{rec}	5	-	ns
Operating Temperature Range	T_J	-40	+85	°C

DC Electrical Characteristics² $T_J = -40^{\circ}\text{C}$ to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	V_{IK}	$V_{CC} = \text{MIN}$ $I_{IN} = -18\text{mA}$	-	-	-1.5	V
Output Voltage High	V_{OH}	$V_{CC} = \text{MIN}$, $I_{OH} = -0.4\text{mA}$ $V_{IH} = 2\text{V}$, $V_{IL} = \text{MAX}$	2.7	3.5	-	V
Output Voltage Low	V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{V}$, $V_{IL} = \text{MAX}$	-	0.35	0.5	V

2. All typical values @ $V_{CC} = 5\text{V}$, $T_J = 25^{\circ}\text{C}$.





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DC Electrical Characteristics continued ² $T_J = -40^{\circ}\text{C}$ to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input High Current	I_{IH}	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	-	-	20	μA
		$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$	-	-	0.1	mA
Input Low Current	I_{IL}	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	-	-	-0.4	mA
Short Circuit Current ³	I_{OS}	$V_{CC} = \text{MAX}$	-20	-	-100	mA
Power Supply Current	I_{CC}	$V_{CC} = \text{MAX}$	-	6	27	mA

3. Not more than one output should be shorted at a time, nor for more than 1 second.

AC Electrical Characteristics⁴ $T_J = 25^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, Clock to Q	t_{PLH}	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	-	-	27	ns
Propagation Delay, Clock to Q	t_{PHL}	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	-	-	32	ns
Propagation Delay, Reset to Q	t_{PHL}	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	-	-	36	ns

Timing Requirements⁵ $T_J = 25^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Setup Time, A or B to CLK	t_{su}	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	15	-	-	ns
Hold Time, CLK to A or B	t_h	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	5	-	-	ns
Pulse Width, Clock or Reset	t_w	$V_{CC} = 5\text{V}, C_L = 15\text{pF}, R_L = 2\text{k}\Omega, t_r = 15\text{ns}, t_f = 6\text{ns}$	20	-	-	ns

4. Not production tested in die form, characterized by chip design and tested in package.





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Switching Waveforms

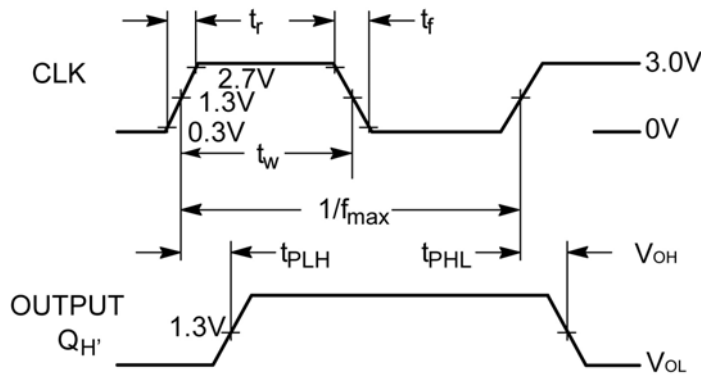


Figure 1 – Clock Propagation Delay & Output Timing

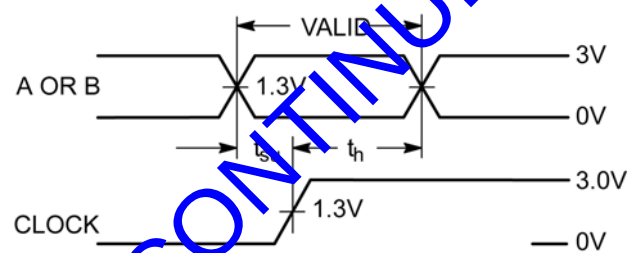


Figure 2 – Data Transition Timing, Serial Input & Clock

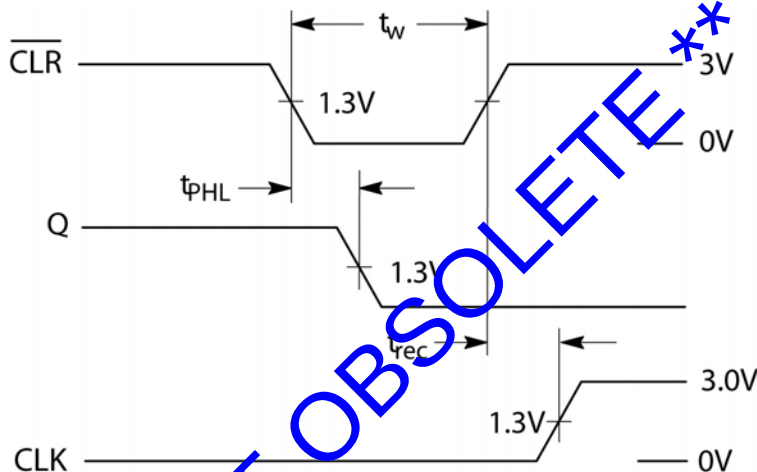


Figure 3 – Reset to Output Propagation Delay & Timing

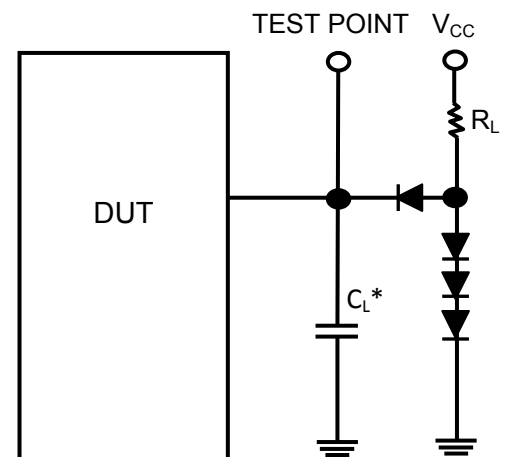


Figure 4 – Test Setup

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