



# PCA9306

Dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator

Rev. 02 — 21 February 2007

Product data sheet

## 1. General description

The PCA9306 is a dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.1 V to 3.6 V ( $V_{\text{ref}(1)}$ ) and 2.3 V to 5.5 V ( $V_{\text{bias(ref)}(2)}$ ).

The PCA9306 allows bidirectional voltage translations between 1.2 V and 5 V without the use of a direction pin. The low ON-state resistance ( $R_{\text{on}}$ ) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

In I<sup>2</sup>C-bus applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9306 enables the system designer to isolate two halves of a bus, thus more I<sup>2</sup>C-bus devices or longer trace length can be accommodated by using the enable pin. The PCA9306 is not a bus buffer like the PCA9509 or PCA9517 that provides level translation and physically isolates the capacitance to either side of the bus even when both sides are connected.

The PCA9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage ( $V_{\text{pu(D)}}$ ) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

## 2. Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I<sup>2</sup>C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I<sup>2</sup>C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard mode and Fast mode I<sup>2</sup>C-bus devices and multiple masters
- Allows voltage level translation between:
  - ◆ 1.0 V  $V_{\text{ref}(1)}$  and 1.8 V, 2.5 V, 3.3 V or 5 V  $V_{\text{bias(ref)}(2)}$
  - ◆ 1.2 V  $V_{\text{ref}(1)}$  and 2.5 V, 3.3 V or 5 V  $V_{\text{bias(ref)}(2)}$
  - ◆ 1.8 V  $V_{\text{ref}(1)}$  and 3.3 V or 5 V  $V_{\text{bias(ref)}(2)}$
  - ◆ 2.5 V  $V_{\text{ref}(1)}$  and 5 V  $V_{\text{bias(ref)}(2)}$
  - ◆ 3.3 V  $V_{\text{ref}(1)}$  and 5 V  $V_{\text{bias(ref)}(2)}$
- Provides bidirectional voltage translation with no direction pin
- Low 3.5  $\Omega$  ON-state connection between input and output ports provides less signal distortion
- Open-drain I<sup>2</sup>C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I<sup>2</sup>C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation for isolation when EN = LOW
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Packages offered: SO8, TSSOP8, VSSOP8, XQFN8

3. Ordering information

Table 1. Ordering information  
*T<sub>amb</sub>* = −40 °C to +85 °C.

| Type number               | Topside mark       | Package               |                                                                                          |          |
|---------------------------|--------------------|-----------------------|------------------------------------------------------------------------------------------|----------|
|                           |                    | Name                  | Description                                                                              | Version  |
| PCA9306D                  | PCA9306            | SO8                   | plastic small outline package; 8 leads; body width 3.9 mm                                | SOT96-1  |
| PCA9306DP                 | 306P               | TSSOP8 <sup>[1]</sup> | plastic thin shrink small outline package; 8 leads; body width 3 mm                      | SOT505-1 |
| PCA9306DC                 | 306C               | VSSOP8                | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm               | SOT765-1 |
| PCA9306DP1 <sup>[2]</sup> | 306T               | TSSOP8                | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm  | SOT505-2 |
| PCA9306DC1 <sup>[3]</sup> | 306U               | VSSOP8                | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm               | SOT765-1 |
| PCA9306GM                 | P6X <sup>[4]</sup> | XQFN8                 | plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm | SOT902-1 |

- [1] Also known as MSOP8.
- [2] Same footprint and pinout as the Texas Instruments PCA9306DCT.
- [3] Same footprint and pinout as the Texas Instruments PCA9306DCU.
- [4] 'X' will change based on date code.

4. Functional diagram

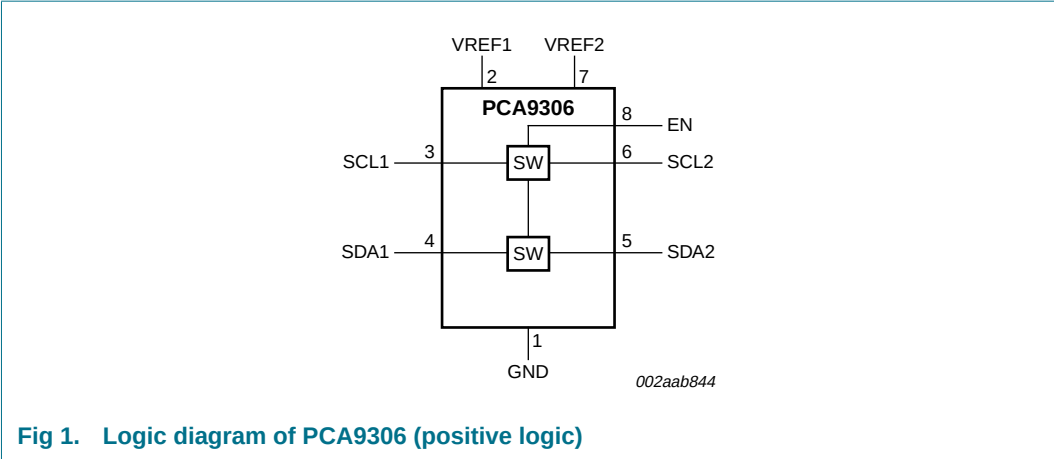
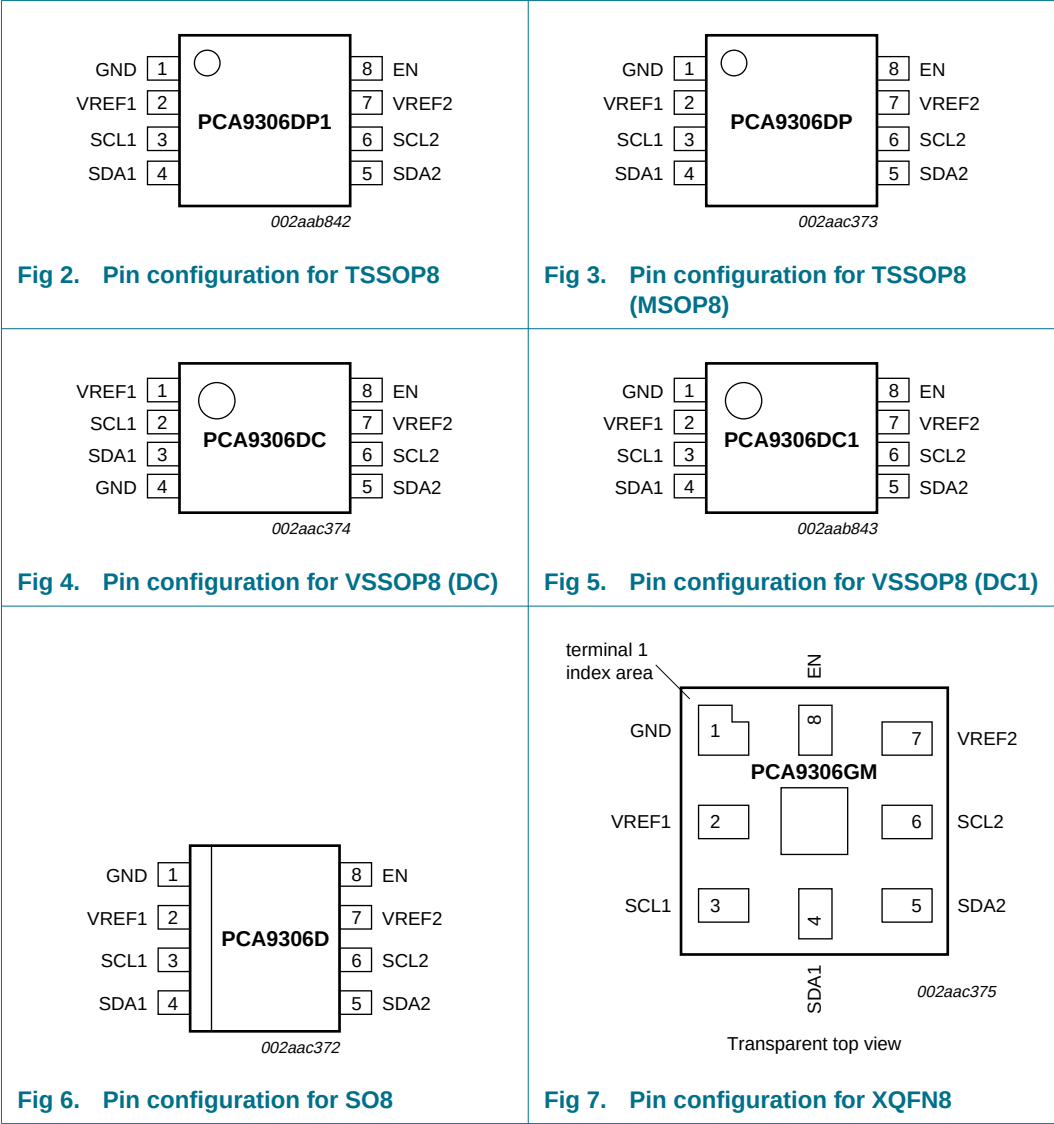


Fig 1. Logic diagram of PCA9306 (positive logic)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin                                                          |             | Description                                                                  |
|--------|--------------------------------------------------------------|-------------|------------------------------------------------------------------------------|
|        | SO8,<br>TSSOP8 (MSOP8),<br>TSSOP8,<br>VSSOP8 (DC1),<br>XQFN8 | VSSOP8 (DC) |                                                                              |
| GND    | 1                                                            | 4           | ground (0 V)                                                                 |
| VREF1  | 2                                                            | 1           | low-voltage side reference supply voltage for SCL1 and SDA1                  |
| SCL1   | 3                                                            | 2           | serial clock, low-voltage side; connect to VREF1 through a pull-up resistor  |
| SDA1   | 4                                                            | 3           | serial data, low-voltage side; connect to VREF1 through a pull-up resistor   |
| SDA2   | 5                                                            | 5           | serial data, high-voltage side; connect to VREF2 through a pull-up resistor  |
| SCL2   | 6                                                            | 6           | serial clock, high-voltage side; connect to VREF2 through a pull-up resistor |
| VREF2  | 7                                                            | 7           | high-voltage side reference supply voltage for SCL2 and SDA2                 |
| EN     | 8                                                            | 8           | switch enable input; connect to VREF2 and pull-up through a high resistor    |

6. Functional description

Refer to [Figure 1 “Logic diagram of PCA9306 \(positive logic\)”](#).

6.1 Function table

Table 3. Function selection (example)  
H = HIGH level; L = LOW level.

| Input EN <sup>[1]</sup> | Function                 |
|-------------------------|--------------------------|
| H                       | SCL1 = SCL2; SDA1 = SDA2 |
| L                       | disconnect               |

[1] EN is controlled by the V<sub>bias(ref)(2)</sub> logic levels and should be at least 1 V higher than V<sub>ref(1)</sub> for best translator operation.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).  
Over operating free-air temperature range.*

| Symbol                    | Parameter                      | Conditions           | Min                 | Max  | Unit |
|---------------------------|--------------------------------|----------------------|---------------------|------|------|
| V <sub>ref(1)</sub>       | reference voltage (1)          |                      | −0.5                | +6   | V    |
| V <sub>bias(ref)(2)</sub> | reference bias voltage (2)     |                      | −0.5                | +6   | V    |
| V <sub>I</sub>            | input voltage                  |                      | −0.5 <sup>[1]</sup> | +6   | V    |
| V <sub>I/O</sub>          | voltage on an input/output pin |                      | −0.5 <sup>[1]</sup> | +6   | V    |
| I <sub>ch</sub>           | channel current (DC)           |                      | -                   | 128  | mA   |
| I <sub>IK</sub>           | input clamping current         | V <sub>I</sub> < 0 V | -                   | −50  | mA   |
| T <sub>stg</sub>          | storage temperature            |                      | −65                 | +150 | °C   |

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol                                   | Parameter                      | Conditions                | Min | Typ | Max | Unit |
|------------------------------------------|--------------------------------|---------------------------|-----|-----|-----|------|
| V <sub>I/O</sub>                         | voltage on an input/output pin | SCL1, SDA1,<br>SCL2, SDA2 | 0   | -   | 5   | V    |
| V <sub>ref(1)</sub> <sup>[1]</sup>       | reference voltage (1)          | VREF1                     | 0   | -   | 5   | V    |
| V <sub>bias(ref)(2)</sub> <sup>[1]</sup> | reference bias voltage (2)     | VREF2                     | 0   | -   | 5   | V    |
| V <sub>I(EN)</sub>                       | input voltage on pin EN        |                           | 0   | -   | 5   | V    |
| I <sub>sw(pass)</sub>                    | pass switch current            |                           | -   | -   | 64  | mA   |
| T <sub>amb</sub>                         | ambient temperature            | operating in<br>free-air  | −40 | -   | +85 | °C   |

[1] V<sub>ref(1)</sub> ≤ V<sub>bias(ref)(2)</sub> − 1 V for best results in level shifting applications.

## 9. Static characteristics

**Table 6. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol        | Parameter                          | Conditions                                                                   | Min            | Typ <sup>[1]</sup> | Max  | Unit          |
|---------------|------------------------------------|------------------------------------------------------------------------------|----------------|--------------------|------|---------------|
| $V_{IK}$      | input clamping voltage             | $I_I = -18\text{ mA}$ ; $V_{I(EN)} = 0\text{ V}$                             | -              | -                  | -1.2 | V             |
| $I_{IH}$      | HIGH-level input current           | $V_I = 5\text{ V}$ ; $V_{I(EN)} = 0\text{ V}$                                | -              | -                  | 5    | $\mu\text{A}$ |
| $C_{I(EN)}$   | input capacitance on pin EN        | $V_I = 3\text{ V}$ or $0\text{ V}$                                           | -              | 7.1                | -    | pF            |
| $C_{io(off)}$ | off-state input/output capacitance | SCLn, SDAn;<br>$V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{I(EN)} = 0\text{ V}$ | -              | 4                  | 6    | pF            |
| $C_{io(on)}$  | on-state input/output capacitance  | SCLn, SDAn;<br>$V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{I(EN)} = 3\text{ V}$ | -              | 9.3                | 12.5 | pF            |
| $R_{on}$      | ON-state resistance <sup>[2]</sup> | SCLn, SDAn;<br>$V_I = 0\text{ V}$ ; $I_O = 64\text{ mA}$                     | <sup>[3]</sup> |                    |      |               |
|               |                                    | $V_{I(EN)} = 4.5\text{ V}$                                                   | -              | 2.4                | 5.0  | $\Omega$      |
|               |                                    | $V_{I(EN)} = 3\text{ V}$                                                     | -              | 3.0                | 6.0  | $\Omega$      |
|               |                                    | $V_{I(EN)} = 2.3\text{ V}$                                                   | -              | 3.8                | 8.0  | $\Omega$      |
|               |                                    | $V_{I(EN)} = 1.5\text{ V}$                                                   | -              | 9.0                | 20   | $\Omega$      |
|               |                                    | $V_I = 2.4\text{ V}$ ; $I_O = 15\text{ mA}$                                  |                |                    |      |               |
|               |                                    | $V_{I(EN)} = 4.5\text{ V}$                                                   | -              | 4.8                | 7.5  | $\Omega$      |
|               |                                    | $V_{I(EN)} = 3\text{ V}$                                                     | -              | 46                 | 80   | $\Omega$      |
|               |                                    | $V_I = 1.7\text{ V}$ ; $I_O = 15\text{ mA}$                                  |                |                    |      |               |
|               |                                    | $V_{I(EN)} = 2.3\text{ V}$                                                   | -              | 40                 | 80   | $\Omega$      |

[1] All typical values are at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

[3] Guaranteed by design.

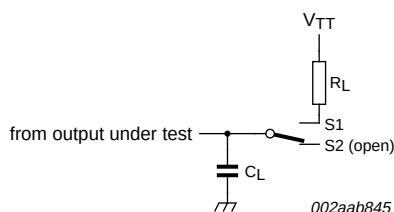
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics (translating down)**
 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise specified. Values guaranteed by design.

| Symbol                                                                                                                              | Parameter                     | Conditions                                         | C <sub>L</sub> = 50 pF |     | C <sub>L</sub> = 30 pF |     | C <sub>L</sub> = 15 pF |      | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|----------------------------------------------------|------------------------|-----|------------------------|-----|------------------------|------|------|
|                                                                                                                                     |                               |                                                    | Min                    | Max | Min                    | Max | Min                    | Max  |      |
| V <sub>I(EN)</sub> = 3.3 V; V <sub>IH</sub> = 3.3 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 1.15 V (see <a href="#">Figure 8</a> ) |                               |                                                    |                        |     |                        |     |                        |      |      |
| t <sub>PLH</sub>                                                                                                                    | LOW-to-HIGH propagation delay | from (input) SCL2 or SDA2 to (output) SCL1 or SDA1 | 0                      | 2.0 | 0                      | 1.2 | 0                      | 0.6  | ns   |
| t <sub>PHL</sub>                                                                                                                    | HIGH-to-LOW propagation delay | from (input) SCL2 or SDA2 to (output) SCL1 or SDA1 | 0                      | 2.0 | 0                      | 1.5 | 0                      | 0.75 | ns   |
| V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 2.5 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 0.75 V (see <a href="#">Figure 8</a> ) |                               |                                                    |                        |     |                        |     |                        |      |      |
| t <sub>PLH</sub>                                                                                                                    | LOW-to-HIGH propagation delay | from (input) SCL2 or SDA2 to (output) SCL1 or SDA1 | 0                      | 2.0 | 0                      | 1.2 | 0                      | 0.6  | ns   |
| t <sub>PHL</sub>                                                                                                                    | HIGH-to-LOW propagation delay | from (input) SCL2 or SDA2 to (output) SCL1 or SDA1 | 0                      | 2.5 | 0                      | 1.5 | 0                      | 0.75 | ns   |

**Table 8. Dynamic characteristics (translating up)**
 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise specified. Values guaranteed by design.

| Symbol                                                                                                                                                                               | Parameter                     | Conditions                                         | C <sub>L</sub> = 50 pF |      | C <sub>L</sub> = 30 pF |      | C <sub>L</sub> = 15 pF |     | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|----------------------------------------------------|------------------------|------|------------------------|------|------------------------|-----|------|
|                                                                                                                                                                                      |                               |                                                    | Min                    | Max  | Min                    | Max  | Min                    | Max |      |
| V <sub>I(EN)</sub> = 3.3 V; V <sub>IH</sub> = 2.3 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 3.3 V; V <sub>M</sub> = 1.15 V; R <sub>L</sub> = 300 Ω (see <a href="#">Figure 8</a> ) |                               |                                                    |                        |      |                        |      |                        |     |      |
| t <sub>PLH</sub>                                                                                                                                                                     | LOW-to-HIGH propagation delay | from (input) SCL1 or SDA1 to (output) SCL2 or SDA2 | 0                      | 1.75 | 0                      | 1.0  | 0                      | 0.5 | ns   |
| t <sub>PHL</sub>                                                                                                                                                                     | HIGH-to-LOW propagation delay | from (input) SCL1 or SDA1 to (output) SCL2 or SDA2 | 0                      | 2.75 | 0                      | 1.65 | 0                      | 0.8 | ns   |
| V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 1.5 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 2.5 V; V <sub>M</sub> = 0.75 V; R <sub>L</sub> = 300 Ω (see <a href="#">Figure 8</a> ) |                               |                                                    |                        |      |                        |      |                        |     |      |
| t <sub>PLH</sub>                                                                                                                                                                     | LOW-to-HIGH propagation delay | from (input) SCL1 or SDA1 to (output) SCL2 or SDA2 | 0                      | 1.75 | 0                      | 1.0  | 0                      | 0.5 | ns   |
| t <sub>PHL</sub>                                                                                                                                                                     | HIGH-to-LOW propagation delay | from (input) SCL1 or SDA1 to (output) SCL2 or SDA2 | 0                      | 3.3  | 0                      | 2.0  | 0                      | 1.0 | ns   |

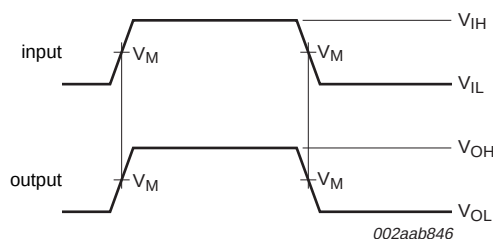

**a. Load circuit**

S1 = translating up; S2 = translating down.

$C_L$  includes probe and jig capacitance.

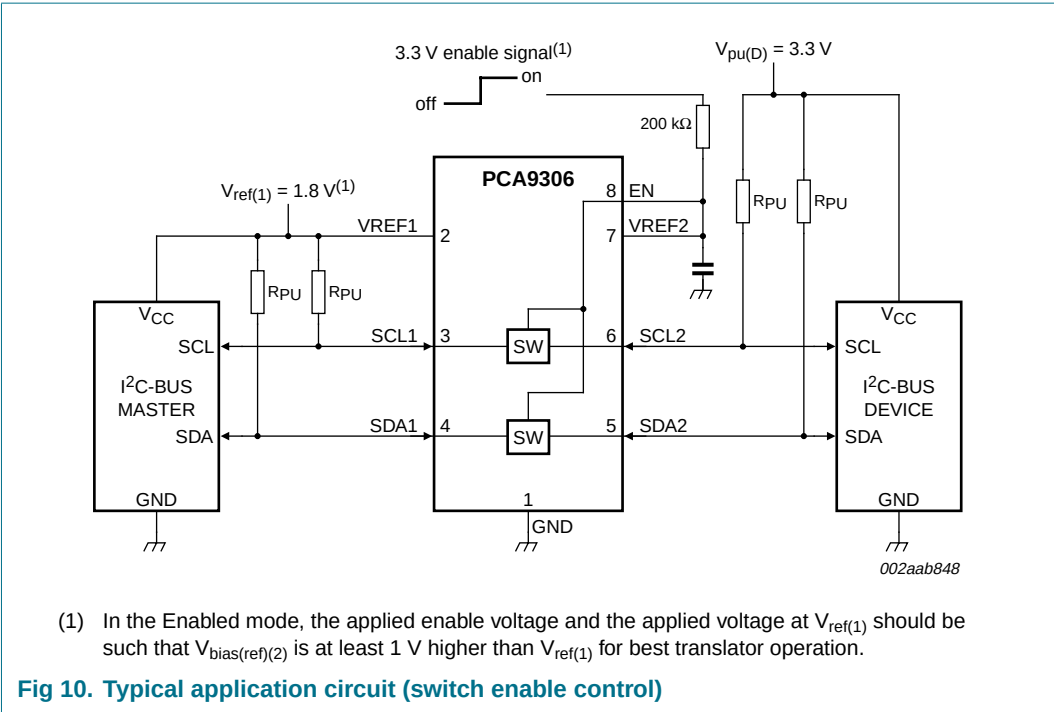
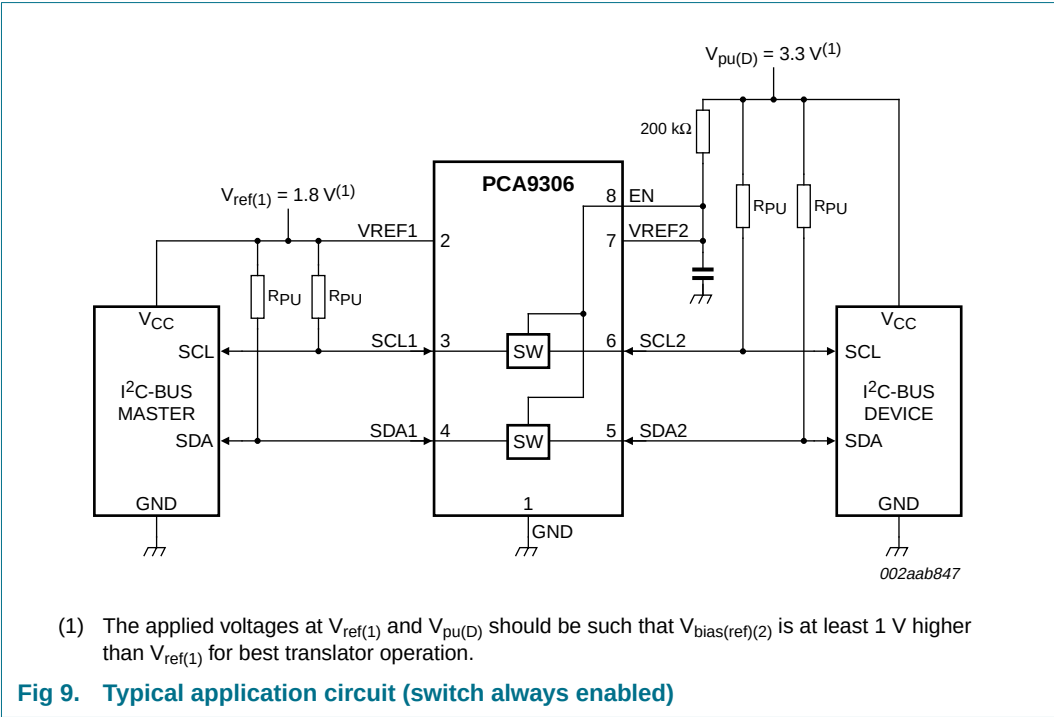
All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ;  $Z_0 = 50\text{ }\Omega$ ;  $t_r \leq 2\text{ ns}$ ;  $t_f \leq 2\text{ ns}$ .

The outputs are measured one at a time, with one transition per measurement.


**b. Timing diagram**
**Fig 8. Load circuit for outputs**



11. Application information



### 11.1 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side  $V_{pu(D)}$  through a pull-up resistor (typically 200 k $\Omega$ ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I<sup>2</sup>C-bus master output can be totem-pole or open-drain (pull-up resistors may be required) and the I<sup>2</sup>C-bus device output can be totem-pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to  $V_{pu(D)}$ ). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ( $V_{ref(1)}$ ) is connected to the processor core power supply voltage. When VREF2 is connected through a 200 k $\Omega$  resistor to a 3.3 V to 5.5 V  $V_{pu(D)}$  power supply, and  $V_{ref(1)}$  is set between 1.0 V and ( $V_{pu(D)} - 1$  V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to  $V_{pu(D)}$ .

**Table 9. Application operating conditions**

Refer to [Figure 9](#).

| Symbol             | Parameter                  | Conditions            | Min                | Typ <sup>[1]</sup> | Max | Unit         |
|--------------------|----------------------------|-----------------------|--------------------|--------------------|-----|--------------|
| $V_{bias(ref)(2)}$ | reference bias voltage (2) |                       | $V_{ref(1)} + 0.6$ | 2.1                | 5   | V            |
| $V_{I(EN)}$        | input voltage on pin EN    |                       | $V_{ref(1)} + 0.6$ | 2.1                | 5   | V            |
| $V_{ref(1)}$       | reference voltage (1)      |                       | 0                  | 1.5                | 4.4 | V            |
| $I_{sw(pass)}$     | pass switch current        |                       | -                  | 14                 | -   | mA           |
| $I_{ref}$          | reference current          | transistor            | -                  | 5                  | -   | $\mu$ A      |
| $T_{amb}$          | ambient temperature        | operating in free-air | -40                | -                  | +85 | $^{\circ}$ C |

[1] All typical values are at  $T_{amb} = 25$   $^{\circ}$ C.

### 11.2 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{pu(D)} - 0.35 \text{ V}}{0.015 \text{ A}}$$

[Table 10](#) summarizes resistor reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor values shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306 device at 0.175 V, although the 15 mA only applies to current flowing through the PCA9306 device.

**Table 10. Pull-up resistor values**

Calculated for  $V_{OL} = 0.35\text{ V}$ ; assumes output driver  $V_{OL} = 0.175\text{ V}$  at stated current.

| $V_{pu(D)}$ | Pull-up resistor value ( $\Omega$ ) |                      |         |                      |         |                      |
|-------------|-------------------------------------|----------------------|---------|----------------------|---------|----------------------|
|             | 15 mA                               |                      | 10 mA   |                      | 3 mA    |                      |
|             | Nominal                             | +10 % <sup>[1]</sup> | Nominal | +10 % <sup>[1]</sup> | Nominal | +10 % <sup>[1]</sup> |
| 5 V         | 310                                 | 341                  | 465     | 512                  | 1550    | 1705                 |
| 3.3 V       | 197                                 | 217                  | 295     | 325                  | 983     | 1082                 |
| 2.5 V       | 143                                 | 158                  | 215     | 237                  | 717     | 788                  |
| 1.8 V       | 97                                  | 106                  | 145     | 160                  | 483     | 532                  |
| 1.5 V       | 77                                  | 85                   | 115     | 127                  | 383     | 422                  |
| 1.2 V       | 57                                  | 63                   | 85      | 94                   | 283     | 312                  |

[1] +10 % to compensate for  $V_{CC}$  range and resistor tolerance.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1

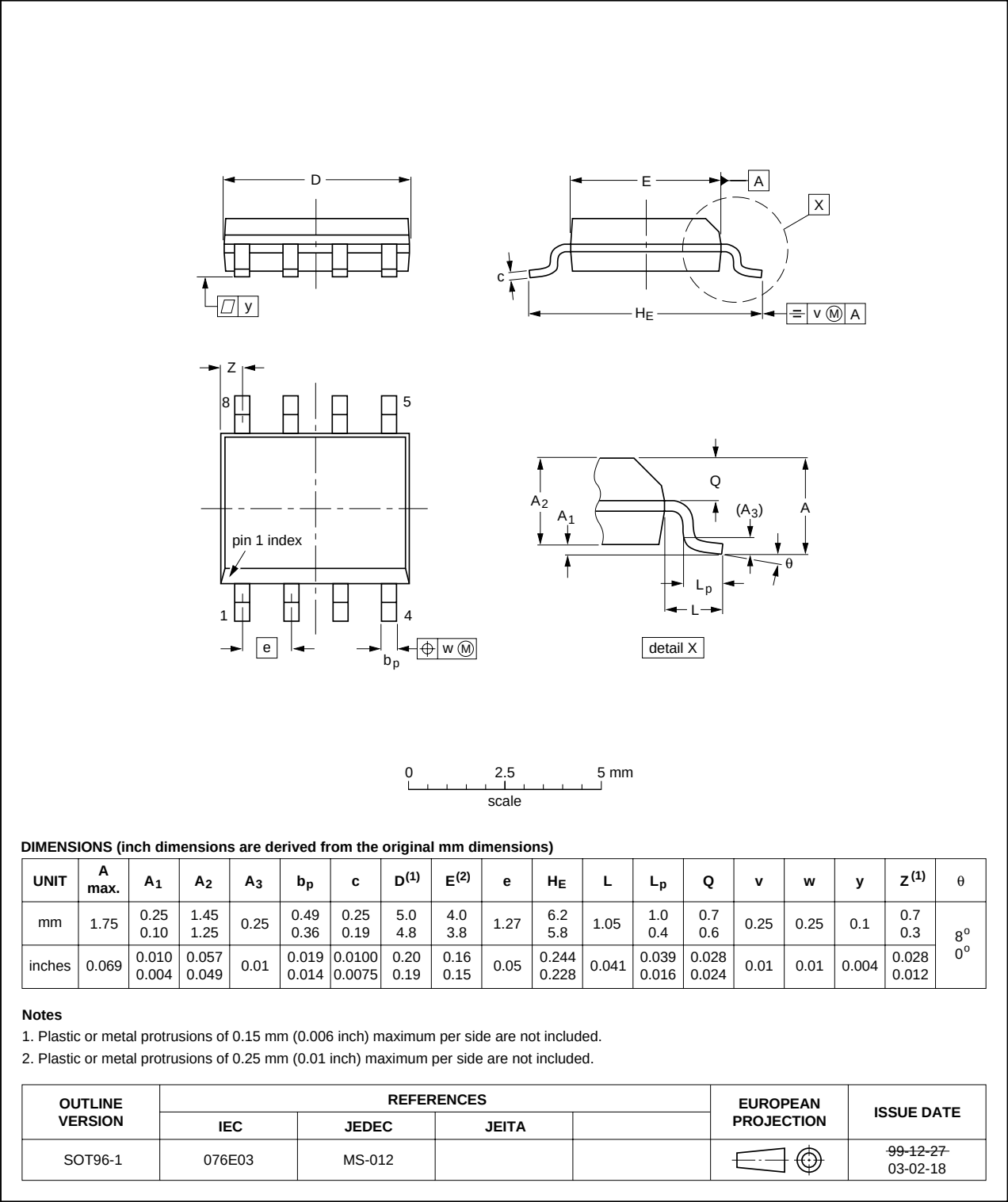


Fig 11. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

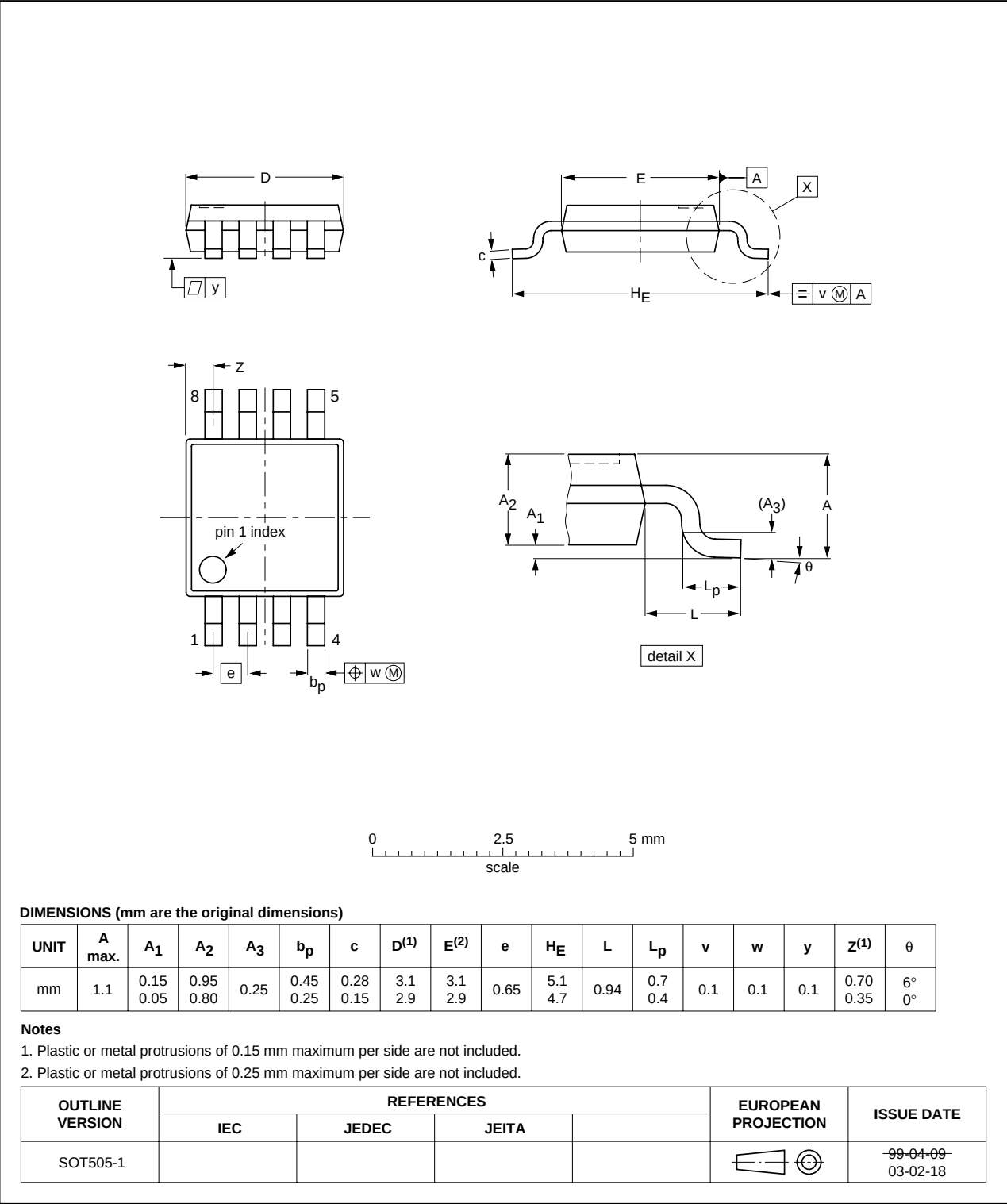


Fig 12. Package outline SOT505-1 (TSSOP8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm    SOT505-2

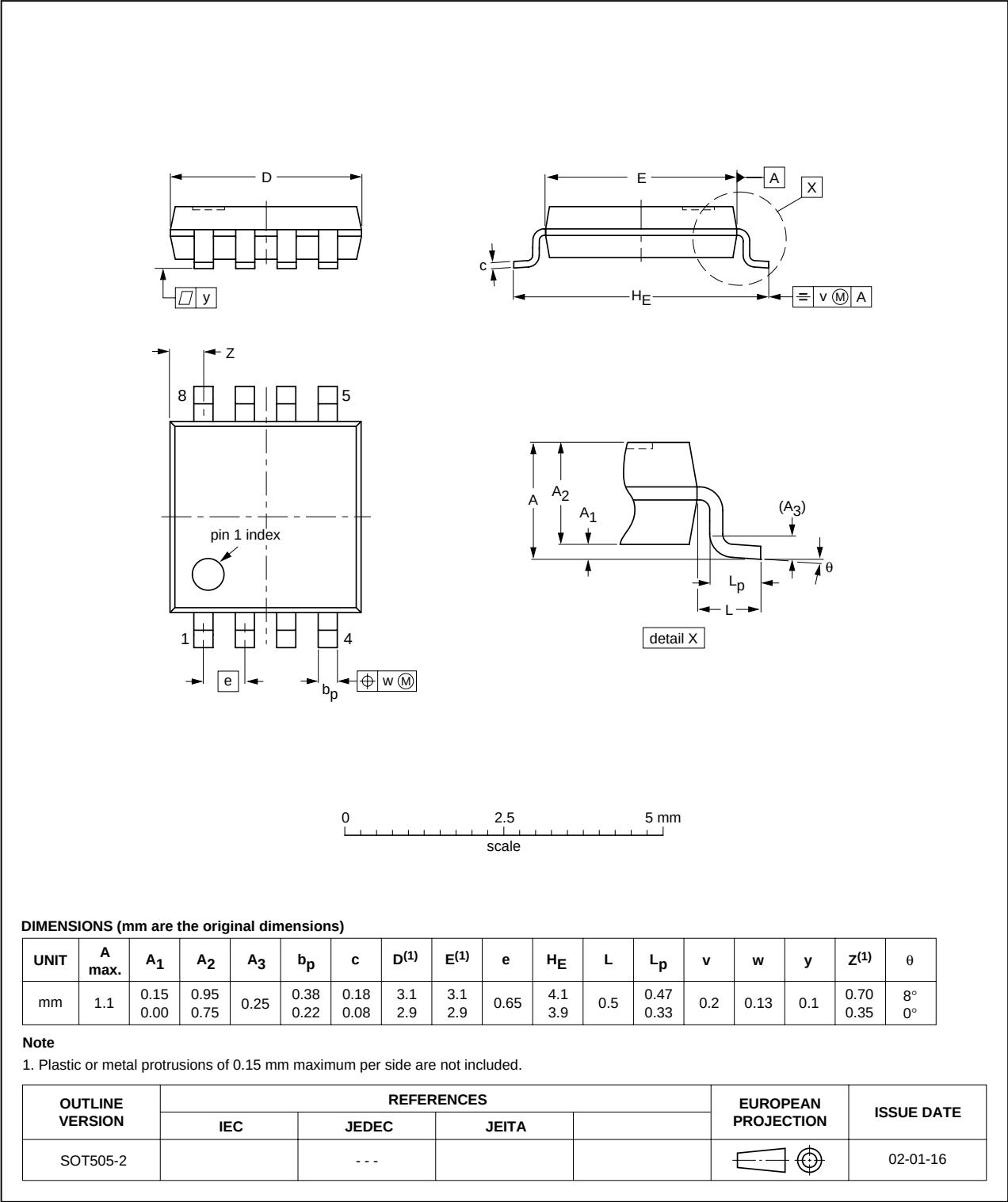


Fig 13. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

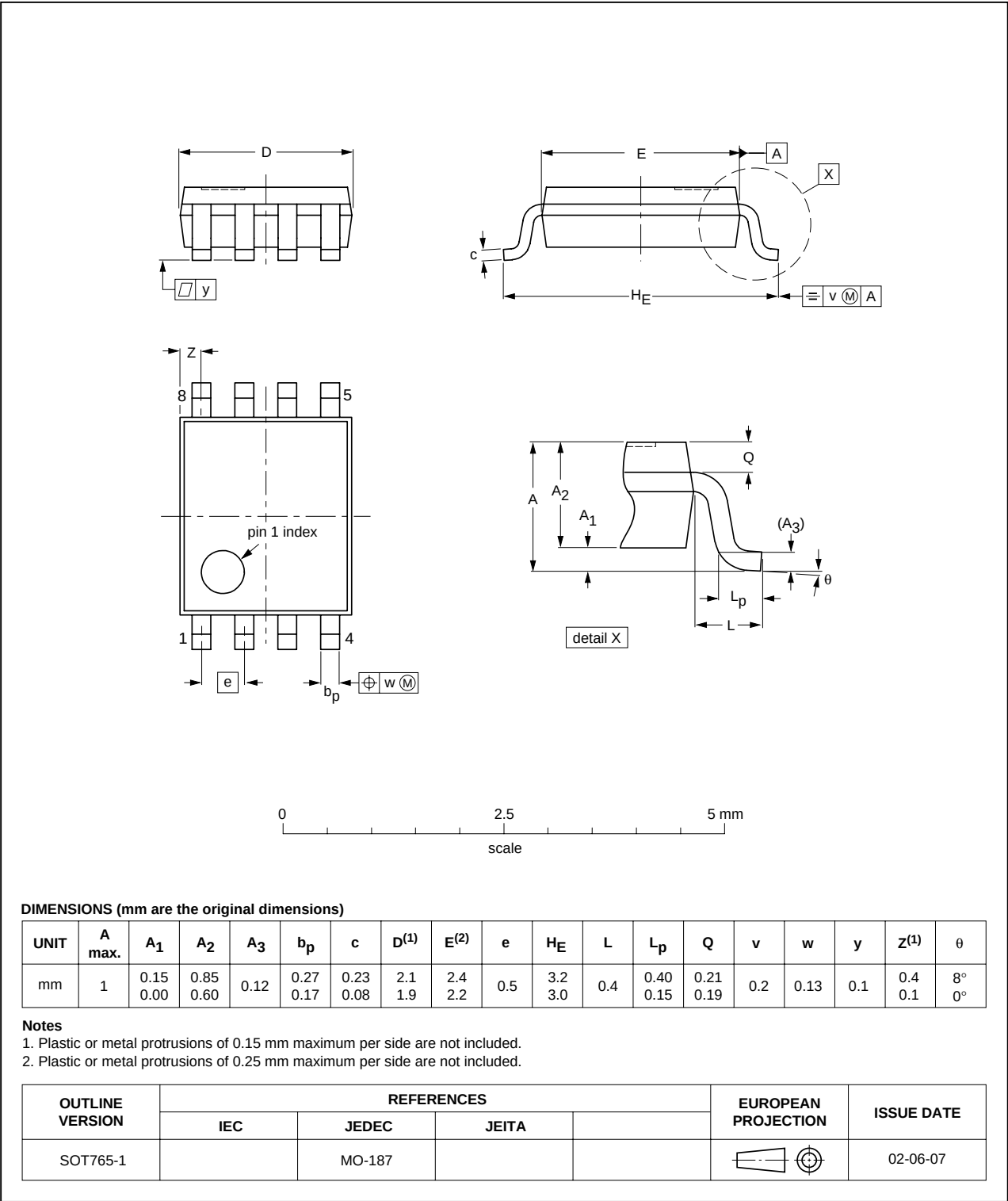


Fig 14. Package outline SOT765-1 (VSSOP8)

XQFN8: plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-1

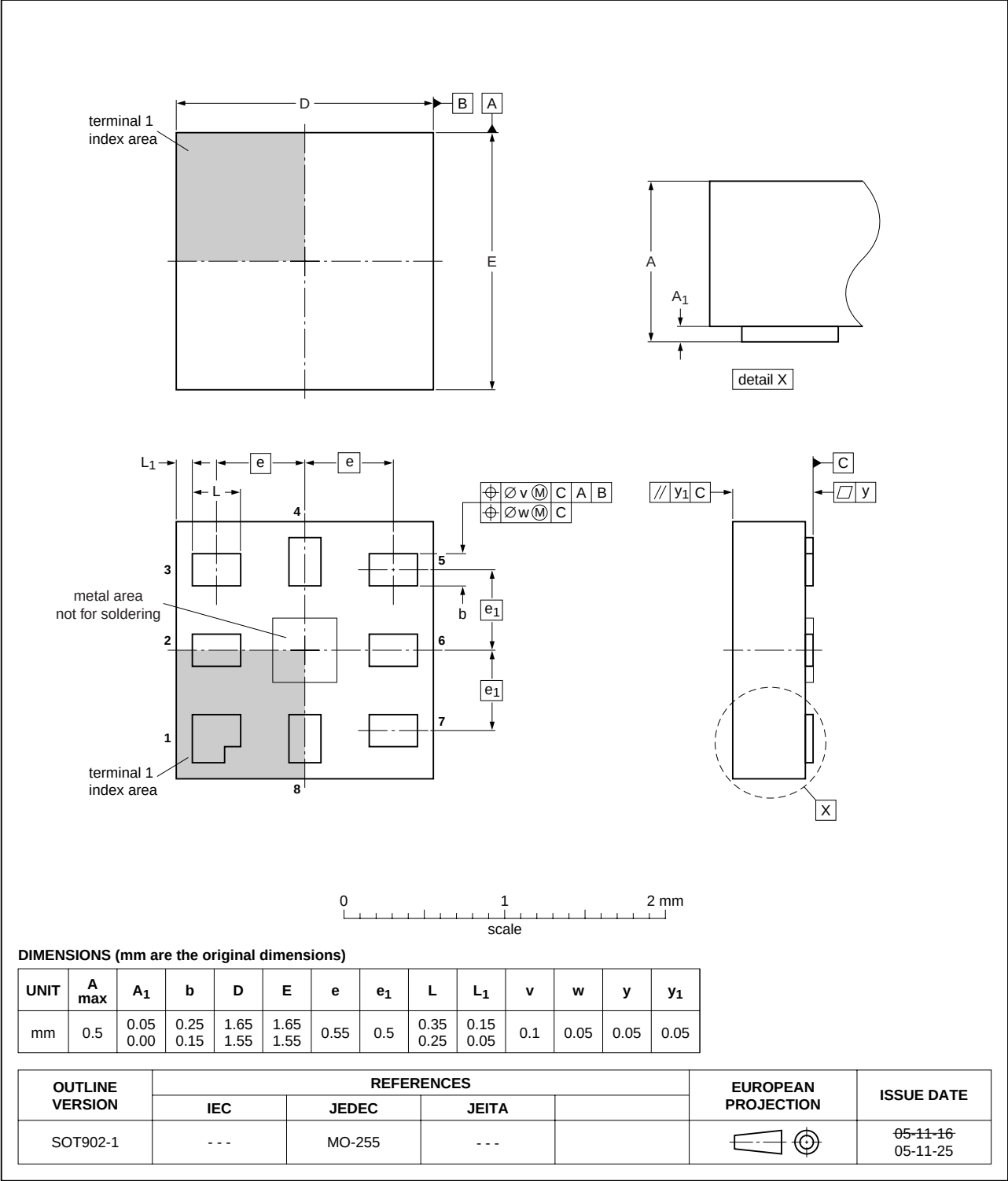


Fig 15. Package outline SOT902-1 (XQFN8)



## 13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 16](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 11](#) and [12](#)

**Table 11. SnPb eutectic process (from J-STD-020C)**

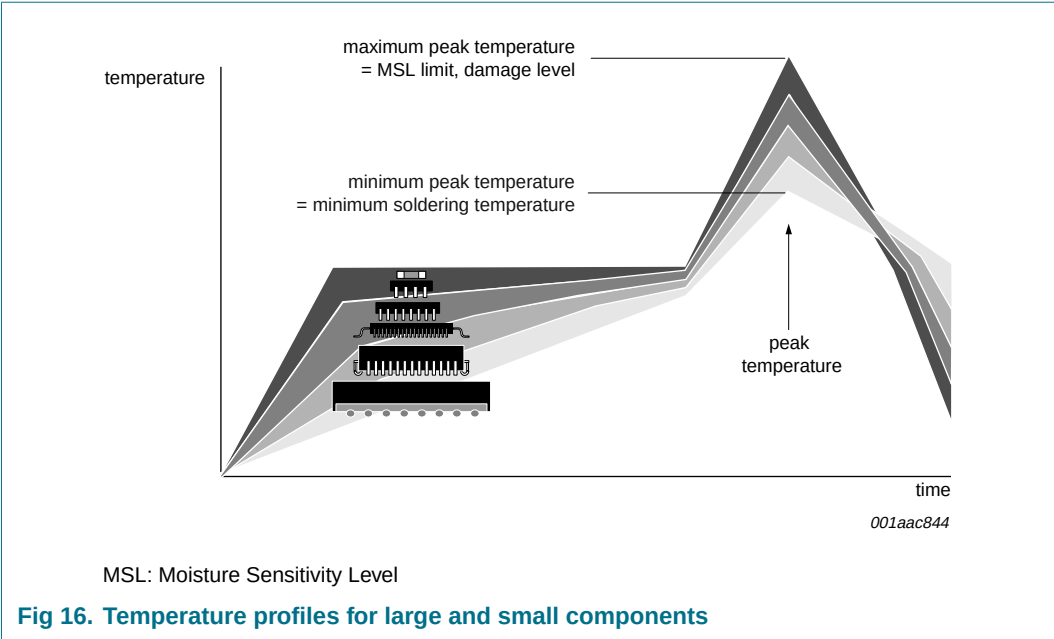
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 12. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 16](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

14. Abbreviations

Table 13. Abbreviations

| Acronym              | Description                  |
|----------------------|------------------------------|
| CDM                  | Charged Device Model         |
| ESD                  | ElectroStatic Discharge      |
| HBM                  | Human Body Model             |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus |
| I/O                  | Input/Output                 |
| MM                   | Machine Model                |
| PRR                  | Pulse Repetition Rate        |
| SMBus                | System Management Bus        |

15. Revision history

Table 14. Revision history

| Document ID                                                          | Release date | Data sheet status  | Change notice | Supersedes |
|----------------------------------------------------------------------|--------------|--------------------|---------------|------------|
| PCA9306_2                                                            | 20070221     | Product data sheet | -             | PCA9306_1  |
| Modifications:                                                       |              |                    |               |            |
| • <a href="#">Table 1 “Ordering information”</a> :                   |              |                    |               |            |
| – changed topside mark for type number PCA9306GM from “P06” to “P6X” |              |                    |               |            |
| – added <a href="#">Table note 4</a>                                 |              |                    |               |            |
| PCA9306_1                                                            | 20061020     | Product data sheet | -             | -          |

## 16. Legal information

### 16.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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