

MC14094B

8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

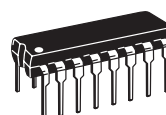


ON Semiconductor

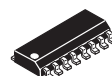
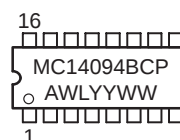
Formerly a Division of Motorola

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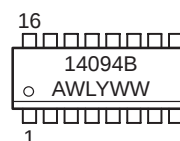
MARKING DIAGRAMS



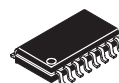
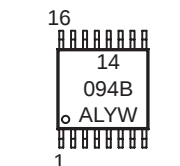
PDIP-16
P SUFFIX
CASE 648



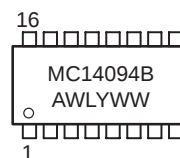
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14094BCP	PDIP-16	2000/Box
MC14094BD	SOIC-16	48/Rail
MC14094BDR2	SOIC-16	2500/Tape & Reel
MC14094BDT	TSSOP-16	96/Rail
MC14094BDTR2	TSSOP-16	2500/Tape & Reel
MC14094BF	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14094B

PIN ASSIGNMENT

STROBE	1	●	16	V _{DD}
DATA	2		15	OUTPUT ENABLE
CLOCK	3		14	Q ₅
Q ₁	4		13	Q ₆
Q ₂	5		12	Q ₇
Q ₃	6		11	Q ₈
Q ₄	7		10	Q' _S
V _{SS}	8		9	Q _S

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q ₁	Q _N	Q _S *	Q' _S
	0	X	X	Z	Z	Q ₇	No Chg.
	0	X	X	Z	Z	No Chg.	Q ₇
	1	0	X	No Chg.	No Chg.	Q ₇	No Chg.
	1	1	0	0	Q _{N-1}	Q ₇	No Chg.
	1	1	1	1	Q _{N-1}	Q ₇	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q ₇

Z = High Impedance X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q₈ and Q_S.

MC14094B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (4.1 μA/kHz) f + I _{DD} I _T = (14 μA/kHz) f + I _{DD} I _T = (140 μA/kHz) f + I _{DD}							μAdc
3–State Output Leakage Current	I _{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μA

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14094B

SWITCHING CHARACTERISTICS ^(7.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

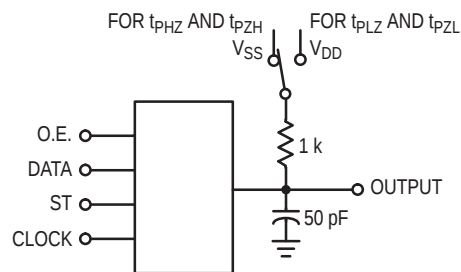
Characteristic	Symbol	V _{DD} Vdc	Min	Typ ⁽⁸⁾	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.35 ns/pF) C _L + 33 ns t _{TLH} , t _{THL} = (0.6 ns/pF) C _L + 20 ns t _{TLH} , t _{THL} = (0.4 ns/pF) C _L + 20 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Serial out QS t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 305 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 107 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 82 ns Clock to Serial out Q'S t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 350 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 149 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 62 ns Clock to Parallel out t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 375 ns t _{PLH} , t _{PHL} = (0.35 ns/pF) C _L + 177 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 122 ns Strobe to Parallel out t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 245 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 127 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 87 ns	t _{PLH} , t _{PHL}	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — — — — —	350 125 95 230 110 75 420 195 135 290 145 100	600 250 190 460 220 150 840 390 270 580 290 200	ns
Output Enable to Output t _{PHZ} , t _{PZL} = (0.90 ns/pF) C _L + 95 ns t _{PHZ} , t _{PZL} = (0.36 ns/pF) C _L + 57 ns t _{PHZ} , t _{PZL} = (0.26 ns/pF) C _L + 42 ns t _{PLZ} , t _{PZH} = (0.90 ns/pF) C _L + 180 ns t _{PLZ} , t _{PZH} = (0.36 ns/pF) C _L + 77 ns t _{PLZ} , t _{PZH} = (0.26 ns/pF) C _L + 57 ns	t _{PHZ} , t _{PZL} t _{PLZ} , t _{PZH}	5.0 10 15 5.0 10 15	— — — — — —	140 75 55 225 95 70	280 150 110 450 190 140	
Setup Time Data in to Clock	t _{su}	5.0 10 15	125 55 35	60 30 20	— — —	ns
Hold Time Clock to Data	t _h	5.0 10 15	0 20 20	– 40 – 10 0	— — —	ns
Clock Pulse Width, High	t _{WH}	5.0 10 15	200 100 83	100 50 40	— — —	ns
Clock Rise and Fall Time	t _{r(cl)} t _{f(cl)}	5 10 15	— — —	— — —	15 5.0 4.0	μs
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	2.5 5.0 6.0	1.25 2.5 3.0	MHz
Strobe Pulse Width	t _{WL}	5.0 10 15	200 80 70	100 40 35	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

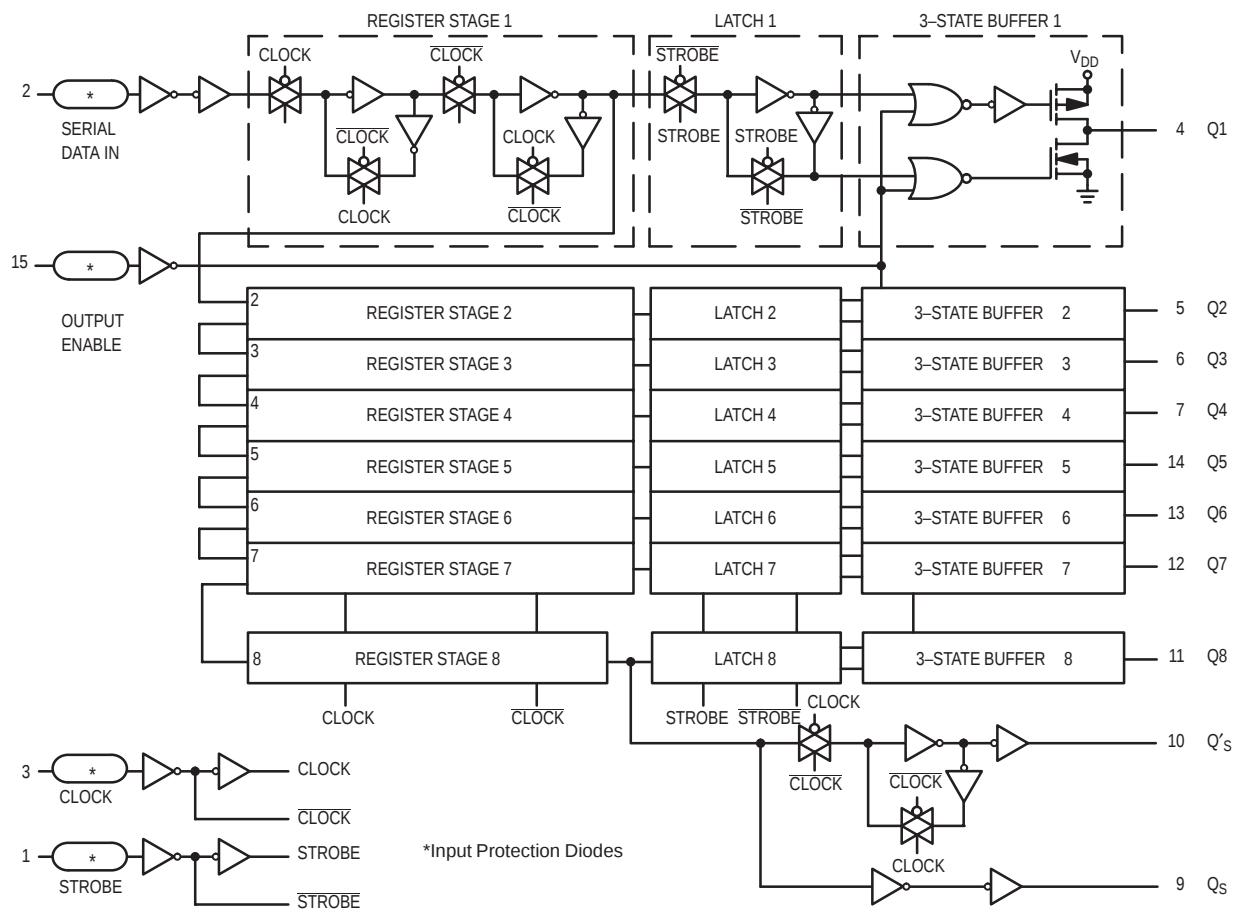
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14094B

3-STATE TEST CIRCUIT

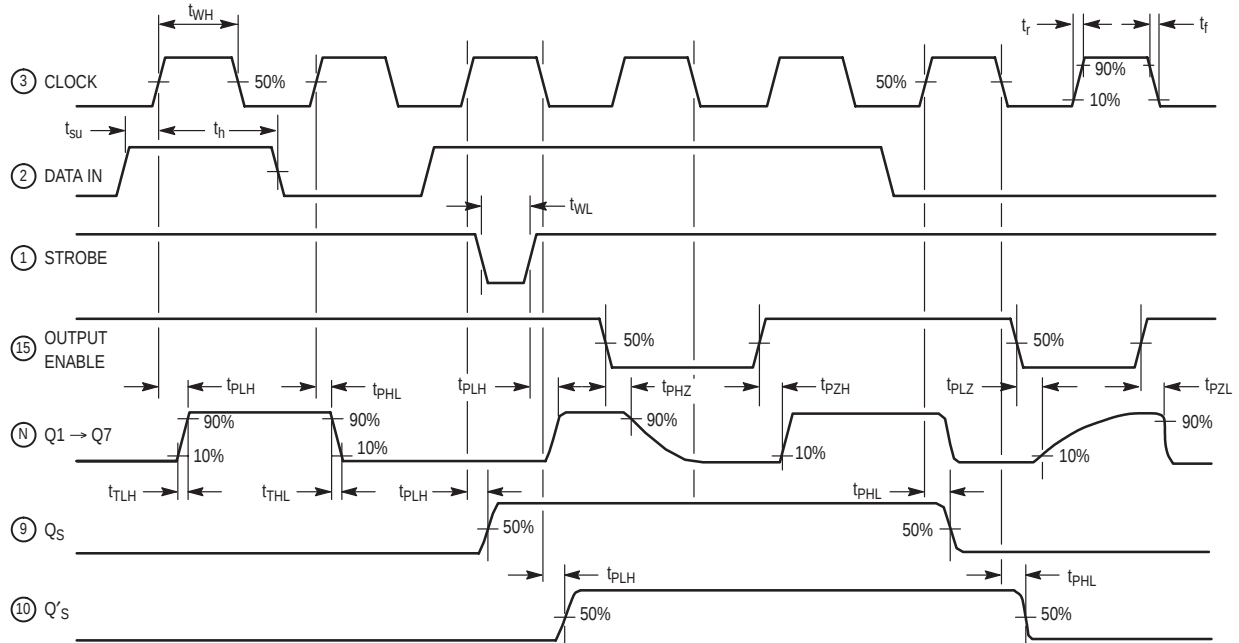


BLOCK DIAGRAM



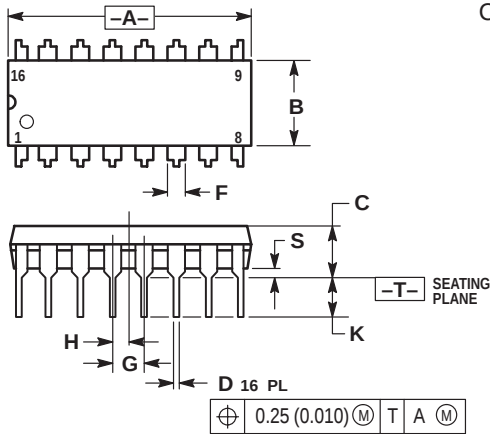
MC14094B

DYNAMIC TIMING DIAGRAM



PACKAGE DIMENSIONS

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



NOTES:

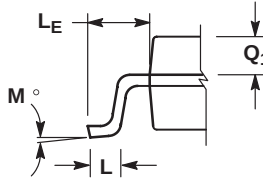
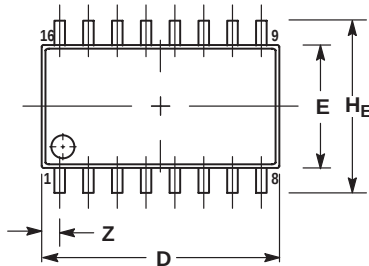
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

MC14094B

PACKAGE DIMENSIONS

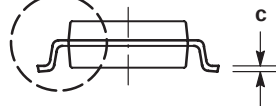
SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



DETAIL P



VIEW P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

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JAPAN: ON Semiconductor, Japan Customer Focus Center

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Email: r14525@onsemi.com

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