

BCD Rate Multiplier

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	− 65 to + 150	°C
T _L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

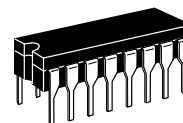
Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

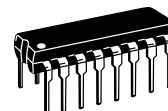
TRUTH TABLE (X = Don't Care, *D = Most Significant Bit)

Inputs										Output			
										Logic Level		Number of Pulses	
D*	C	B	A	No. of Clock Pulses	E _{in}	Strobe	Cascade	Clear	Set	Out	Out	E _{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	—	—	—	—
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

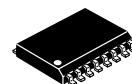
MC14527B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



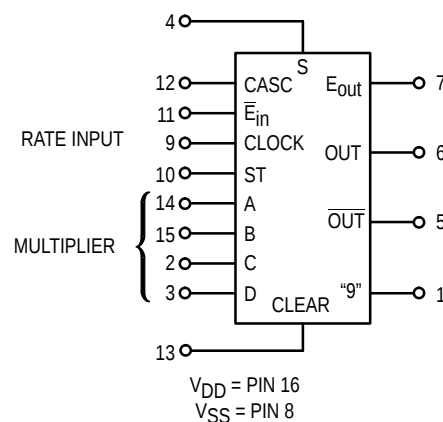
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = − 55° to 125°C for all packages.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

[illegible]

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_I) = I_T(50 \text{ pF}) + (C_I - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.0012$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

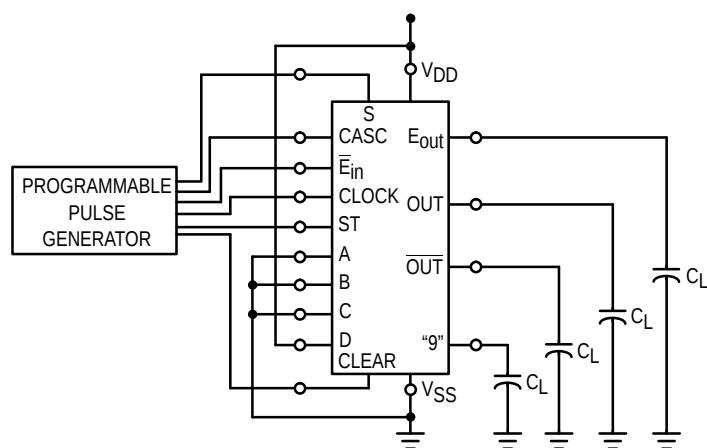
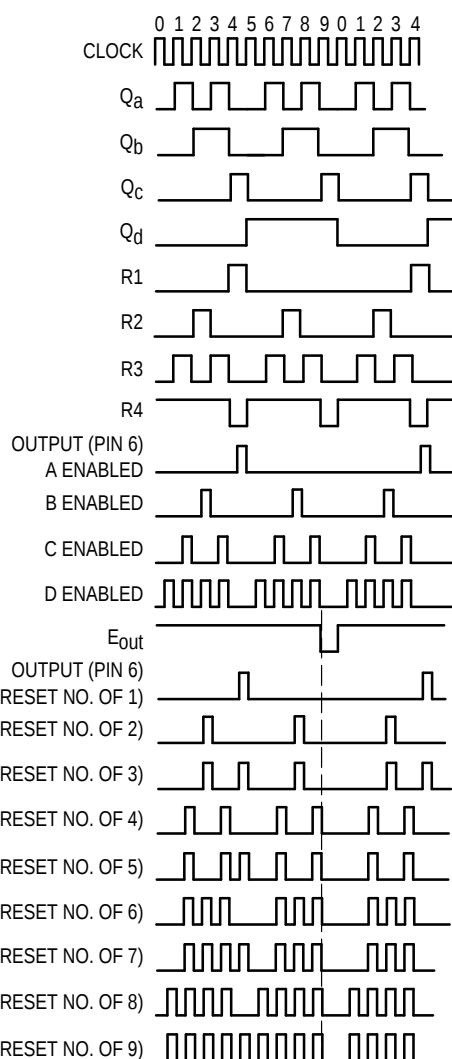
"9"	1	16	V _{DD}
C	2	15	B
D	3	14	A
S	4	13	CLEAR
$\overline{\text{OUT}}$	5	12	CASC
OUT	6	11	$\bar{E}_{in}$
E _{out}	7	10	ST
V _{SS}	8	9	CLOCK

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$	$t_{PHL},$ t_{PHL}	5.0 10 15	— — —	200 100 70	400 200 140	ns
Clock to $\overline{\text{Out}}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 40 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	125 65 45	250 130 90	ns
Clock to E _{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 210 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	295 130 85	590 260 170	ns
Clock to “g” $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	400 155 110	800 310 220	ns
Set or Clear to Out $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 295 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	380 165 110	760 330 220	ns
Cascade to Out $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 40 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	125 65 45	250 130 90	ns
Strobe to Out $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 145 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 72 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	230 105 70	260 210 140	ns
Clock Pulse Width	t_{WH}	5.0 10 15	500 200 150	250 110 80	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.0 4.5 6.0	1.2 2.5 3.5	MHz
Clock Pulse Rise and Fall Time	$t_{TLH},$ t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Set or Clear Pulse Width	t_{WH}	5.0 10 15	240 100 75	80 35 30	— — —	ns
Set Removal Time	t_{rem}	5.0 10 15	0 0 0	– 20 – 10 – 7.5	— — —	ns
Enable In Setup Time	t_{su}	5.0 10 15	400 150 120	175 60 45	— — —	ns

* The formulas given are for the typical characteristics only at 25°C.

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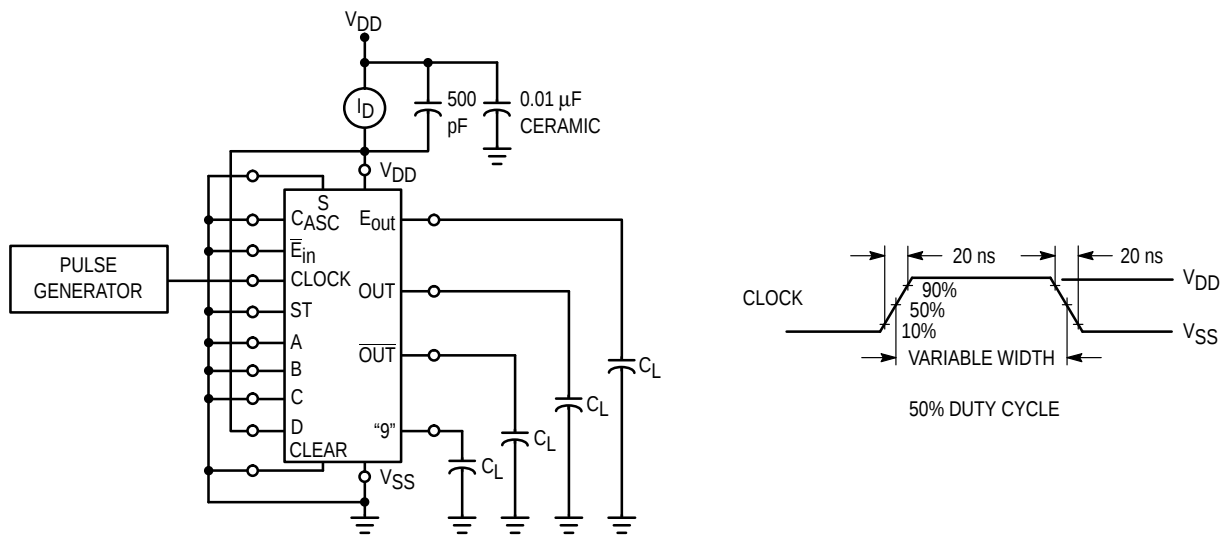
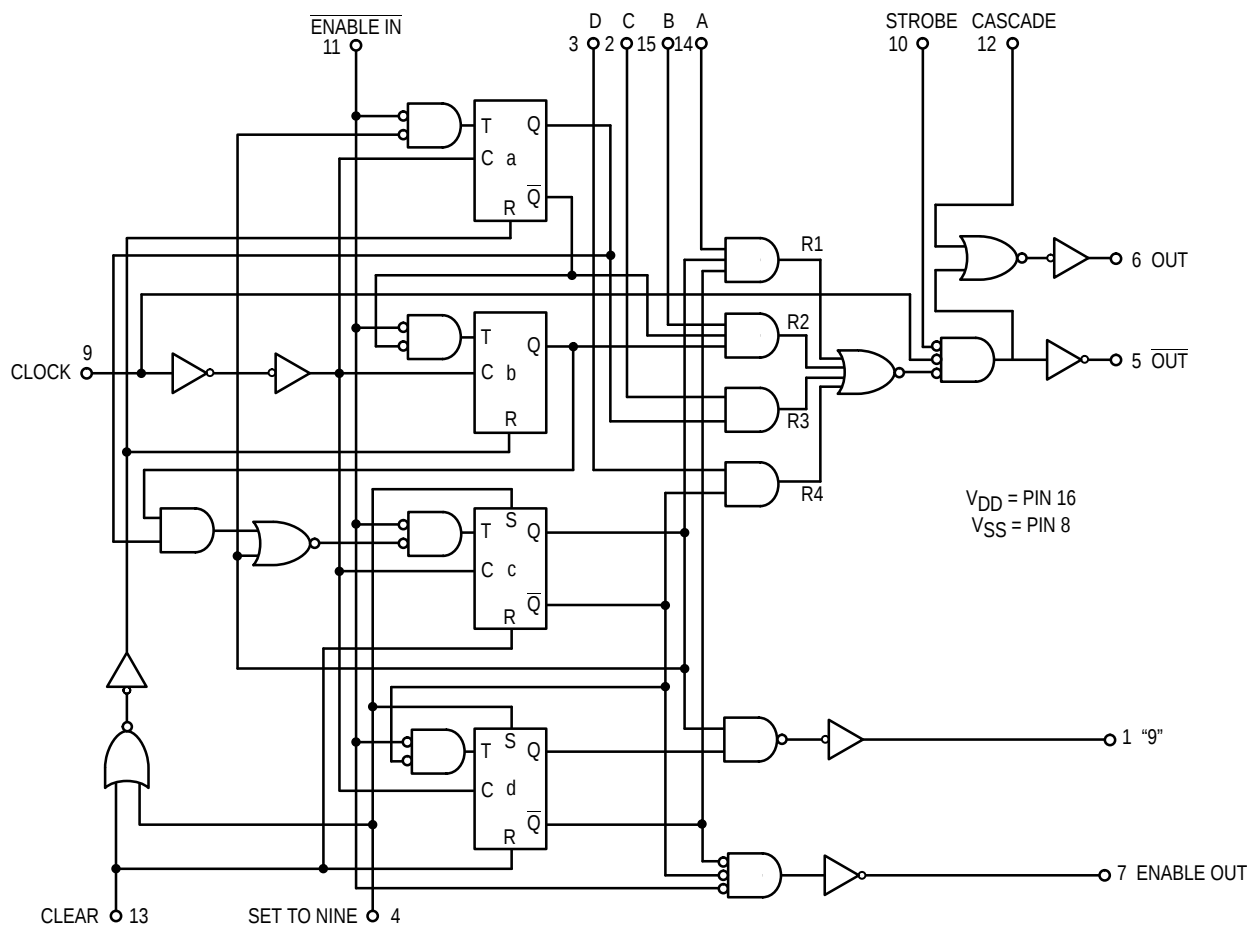


Figure 3. Power Dissipation Test Circuit and Waveform

LOGIC DIAGRAM



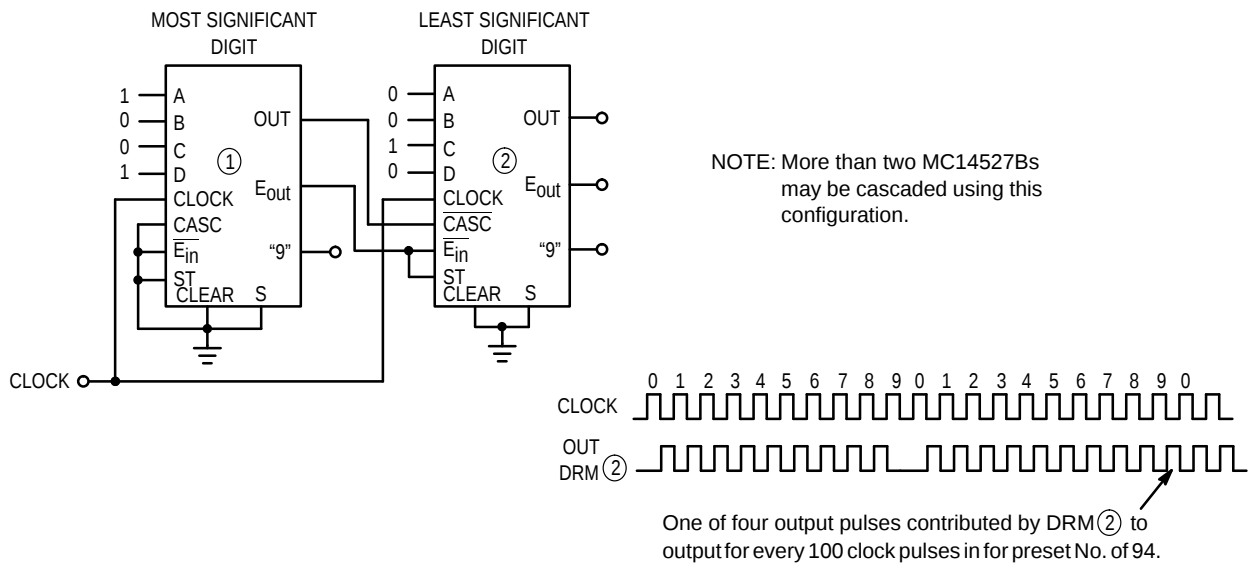
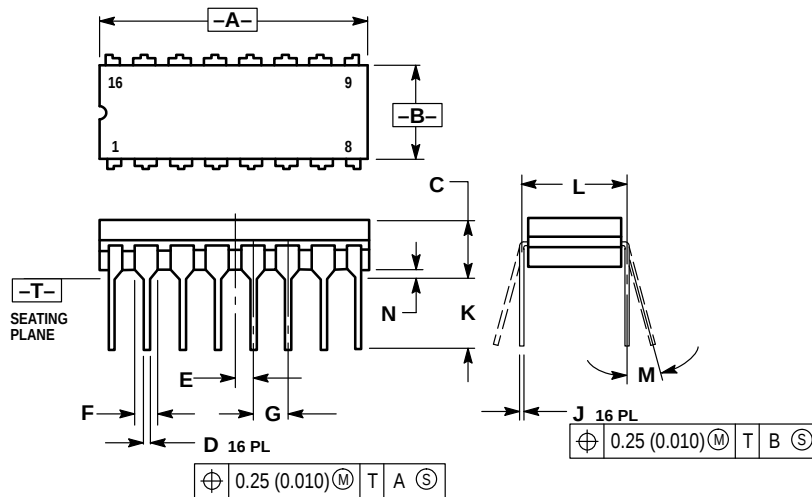


Figure 4. Two MC14527Bs in Cascade with Preset No. of 94

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

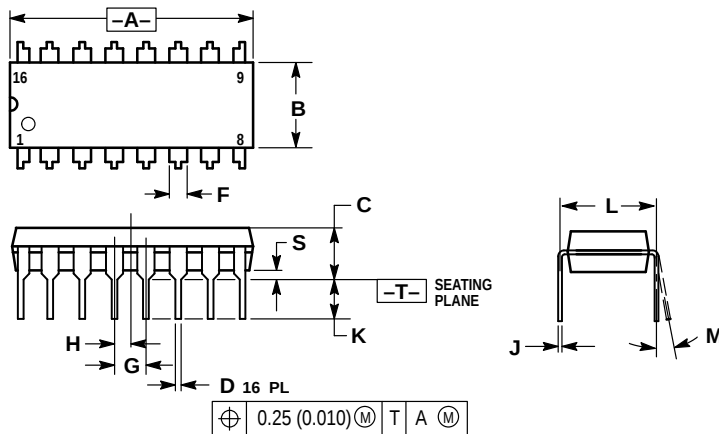


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

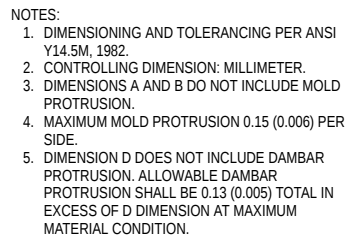


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G-02
ISSUE A



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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