

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE01H10D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

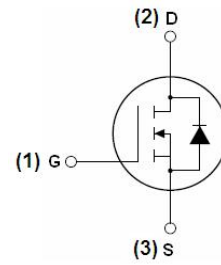
- $V_{DS} = 100V, I_D = 100A$
 $R_{DS(ON)} < 12m\Omega @ V_{GS}=10V$ (Typ:9.9m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE01H10D	NCE01H10D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	100	A
$I_D(100^\circ C)$	Drain Current-Continuous($T_C=100^\circ C$)	80	A
I_{DM}	Pulsed Drain Current	380	A
P_D	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/ $^\circ C$
E_{AS}	Single pulse avalanche energy ^(Note 5)	720	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	0.75	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

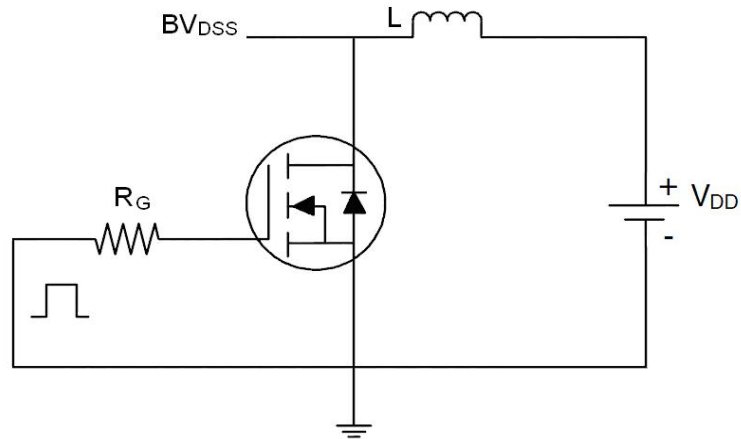
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$	-	9.9	12	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=20V, I_D=40A$	-	71	-	S
Dynamic Characteristics ^(Note 4)						
C_{iss}	Input Capacitance	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4820	-	PF
C_{oss}	Output Capacitance		-	244	-	PF
C_{riss}	Reverse Transfer Capacitance		-	197	-	PF
Switching Characteristics ^(Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, I_D=40A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	15	-	nS
t_r	Turn-on Rise Time		-	50	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	40	-	nS
t_f	Turn-Off Fall Time		-	55	-	nS
Q_g	Total Gate Charge	$V_{DS}=50V, I_D=40A,$ $V_{GS}=10V$	-	123	-	nC
Q_{gs}	Gate-Source Charge		-	27	-	nC
Q_{gd}	Gate-Drain Charge		-	44	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage ^(Note 3)	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
I_S	Diode Forward Current ^(Note 2)	-	-	-	100	A
t_{rr}	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_F = 40A$ $di/dt = 100A/\mu s$ (Note 3)	-	38	80	nS
Q_{rr}	Reverse Recovery Charge		-	53	100	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

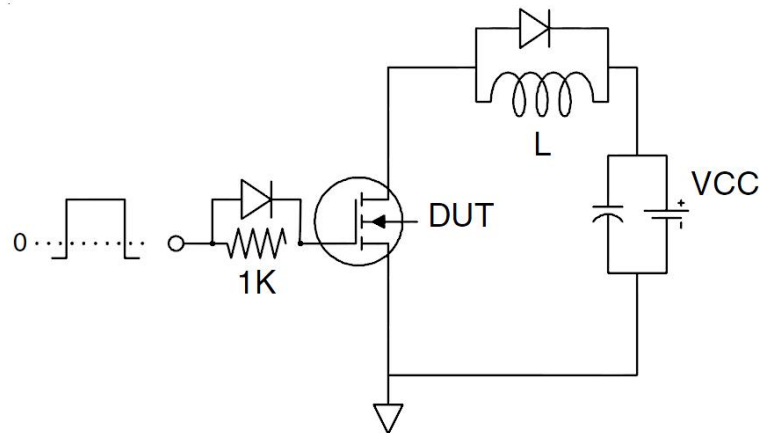
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

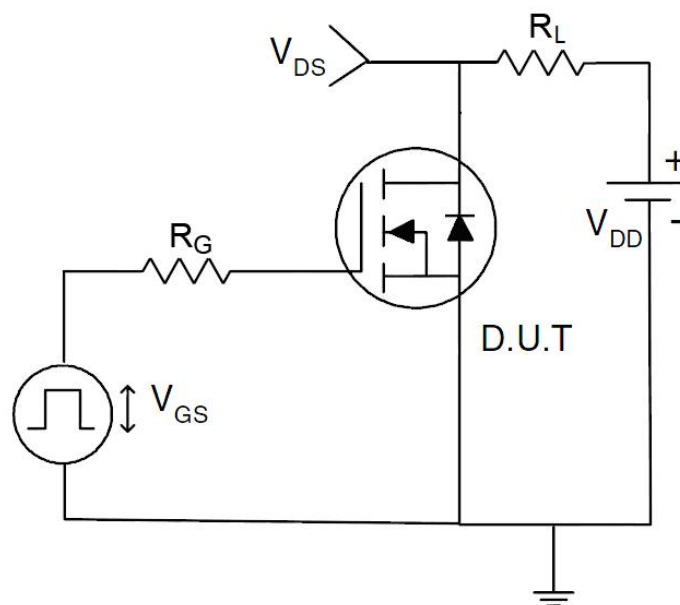
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

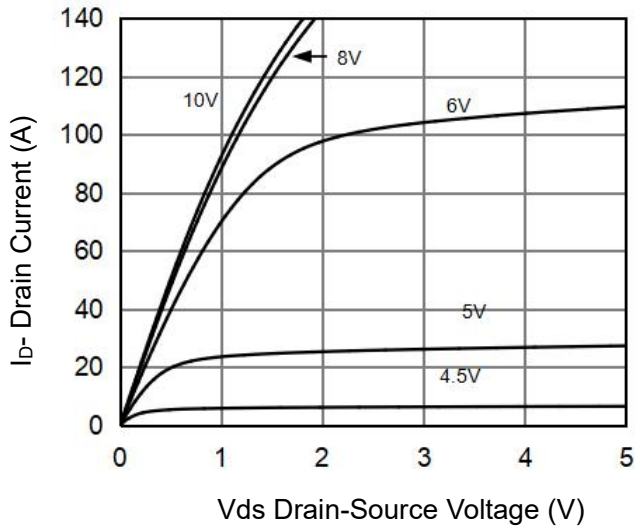


Figure 1 Output Characteristics

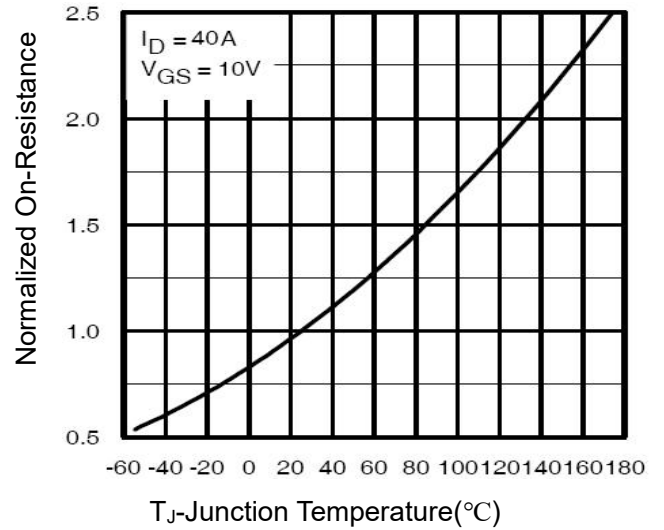


Figure 4 Rdson-Junction Temperature

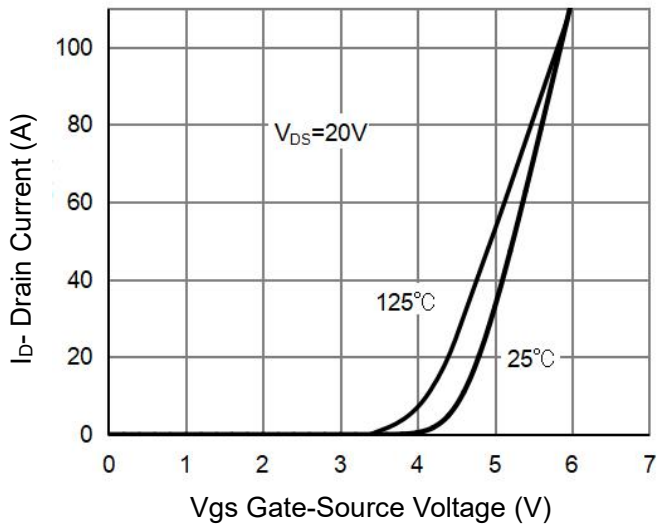


Figure 2 Transfer Characteristics

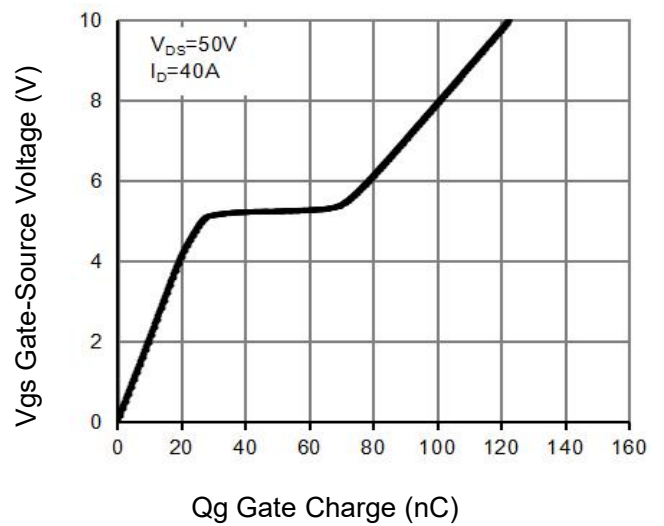


Figure 5 Gate Charge

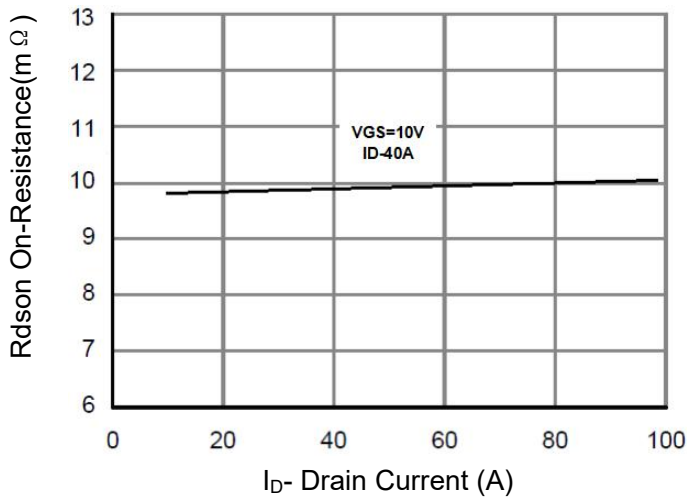


Figure 3 Rdson- Drain Current

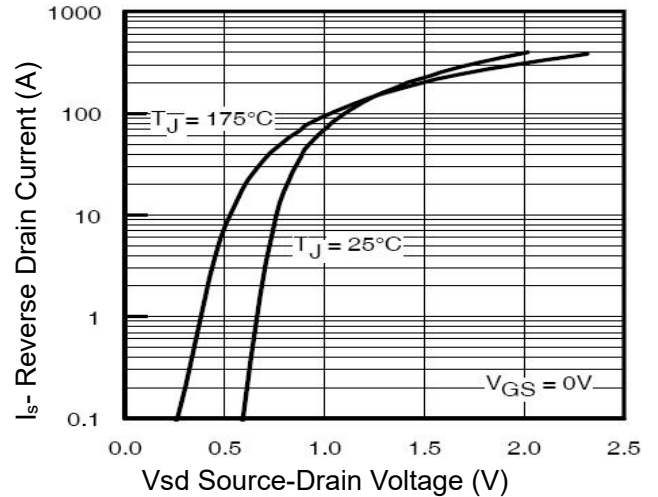
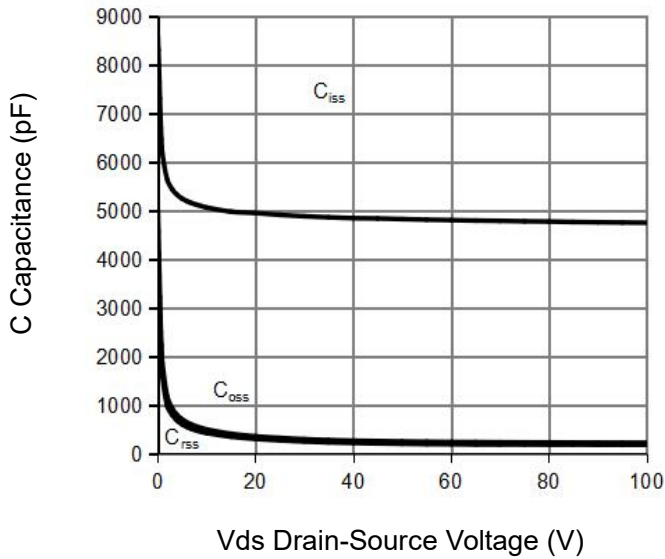
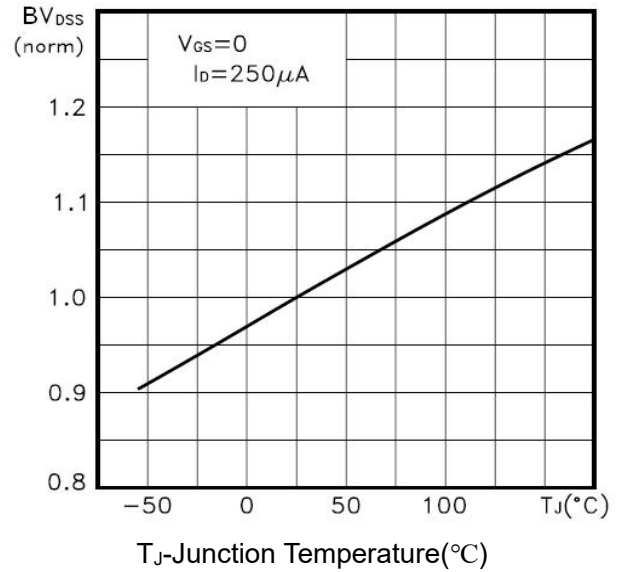


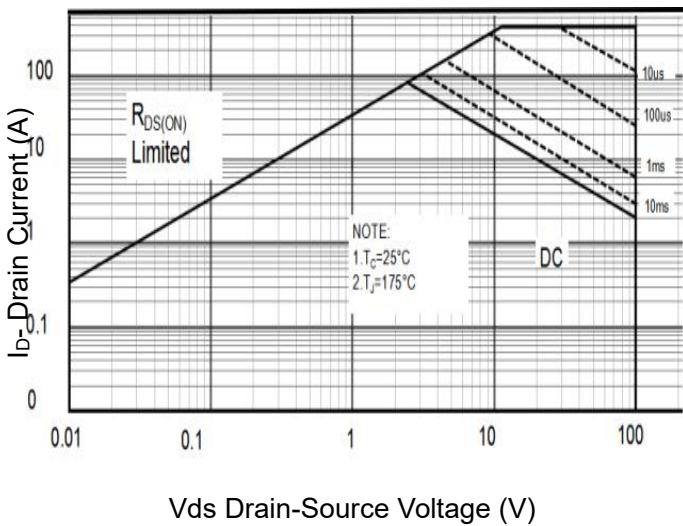
Figure 6 Source- Drain Diode Forward



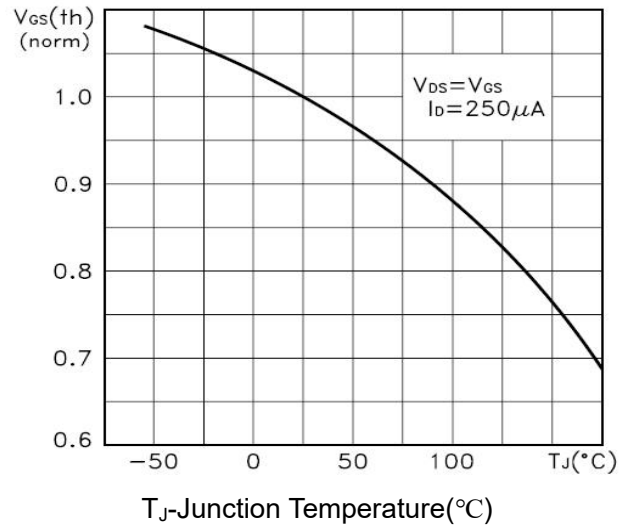
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

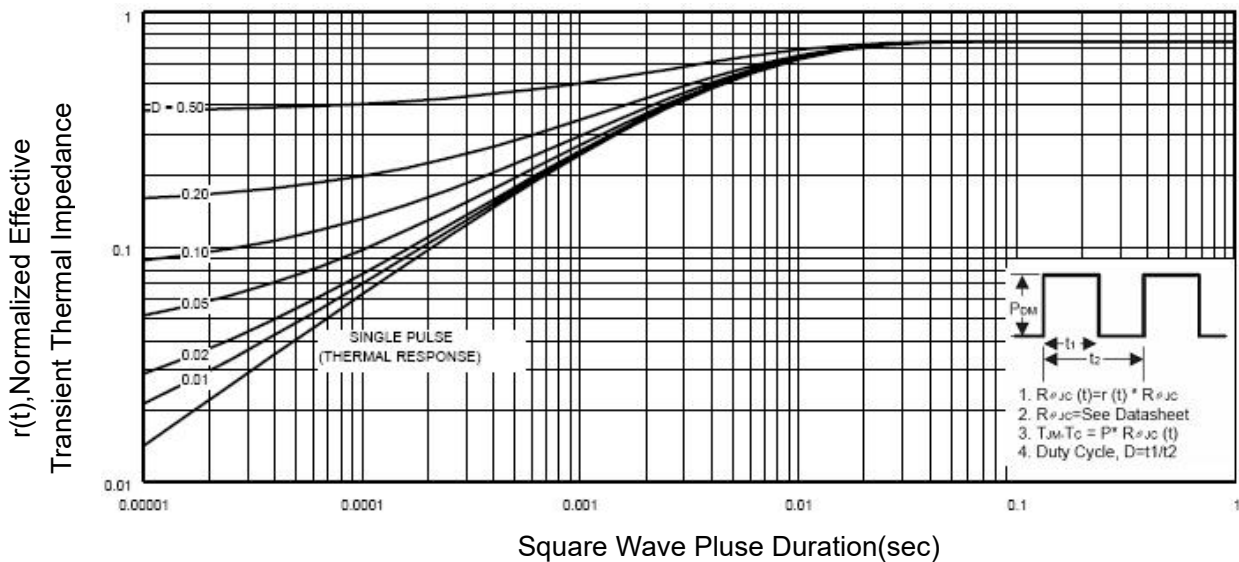
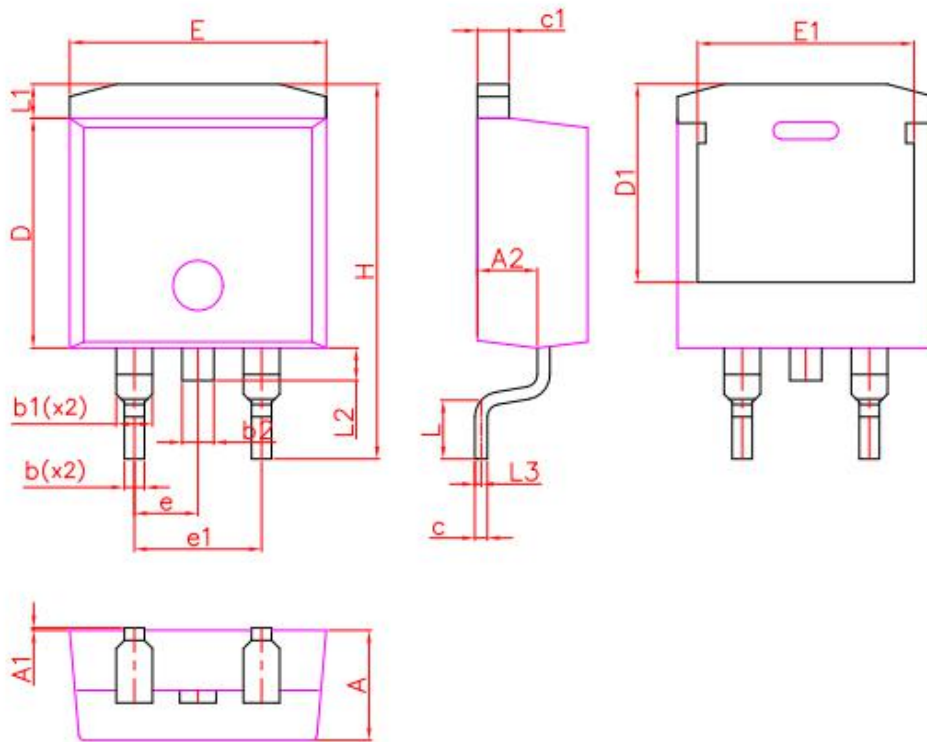


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



T0263			
DIM.	MIN.	NOM.	MAX.
A	4.20	4.40	4.60
A1	0.00	0.10	0.25
A2	2.20	2.40	2.60
b	0.70	0.80	0.90
b1	1.20	1.45	1.75
b2	1.17	1.27	1.37
c	0.40	0.50	0.60
c1	1.15	1.27	1.40
D	9.10	9.20	9.30
D1	7.63	7.93	8.23
E	10.05	10.25	10.45
E1	8.35	8.65	8.95
e	2.54BSC		
e1	5.08BSC		
H	14.61	15.00	15.88
L	1.78	2.35	2.79
L1	1.36REF		
L2	1.3REF		
L3	0.25REF		
All dimensions in millimeters			

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