

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP4060EQ uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification. It is ESD protected.

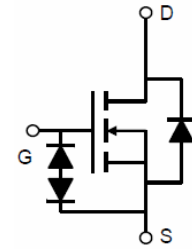
General Features

- $V_{DS} = 40V, I_D = 60A$
 $R_{DS(ON)} = 3.1m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 4.1m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested
- ESD protection : HBM Class 2

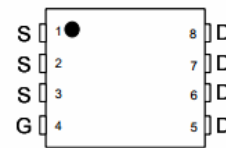
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

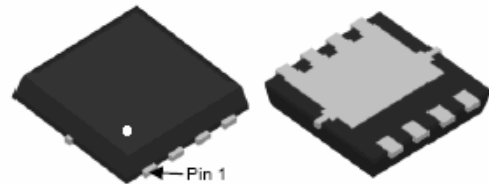
100% UIS TESTED!
100% ΔV_d s TESTED!



Schematic Diagram



Top View and Pin Assignment



Top View

Bottom View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP4060EQ	NCEP4060EQ	DFN3.3X3.3-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	60	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	42.3	A
Pulsed Drain Current (Package Limited)	I_{DM}	260	A
Maximum Power Dissipation	P_D	48	W
Derating factor		0.38	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	288	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.6	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	3.1	3.4	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	4.1	4.4	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$		40	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	2100	2600	PF
Output Capacitance	C_{oss}		-	639	800	PF
Reverse Transfer Capacitance	C_{rss}		-	23.6	29	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=20A$ $V_{GS}=10V, R_G=1.6\Omega$	-	7.5	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	26	-	nS
Turn-Off Fall Time	t_f		-	3.3	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	34.3	47	nC
Gate-Source Charge	Q_{gs}		-	7.1		nC
Gate-Drain Charge	Q_{gd}		-	3.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=60A$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	60	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 500A/\mu s$ ^(Note 3)	-	19	-	nS
Reverse Recovery Charge	Q_{rr}		-	40	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}C, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

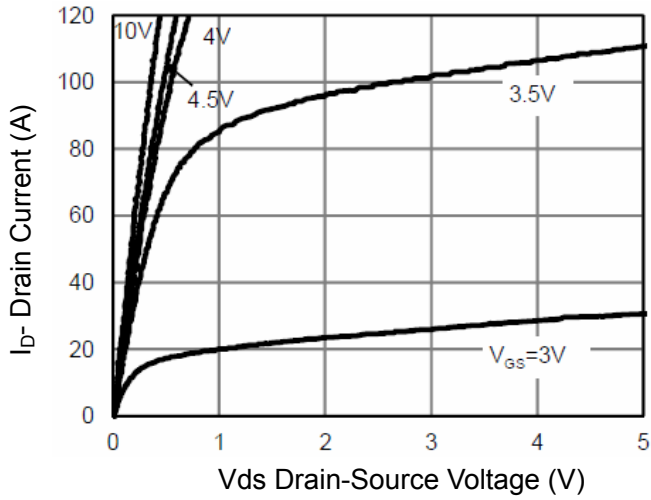


Figure 1 Output Characteristics

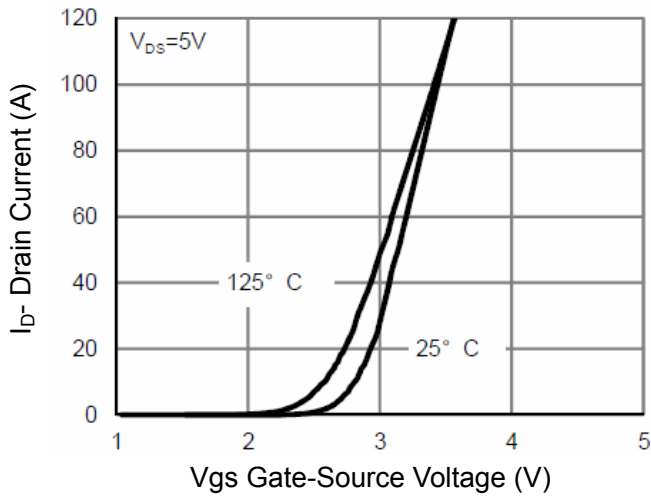


Figure 2 Transfer Characteristics

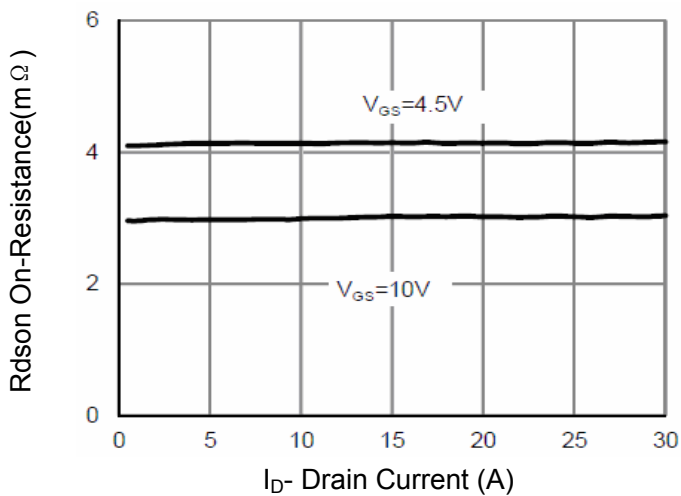


Figure 3 Rdson- Drain Current

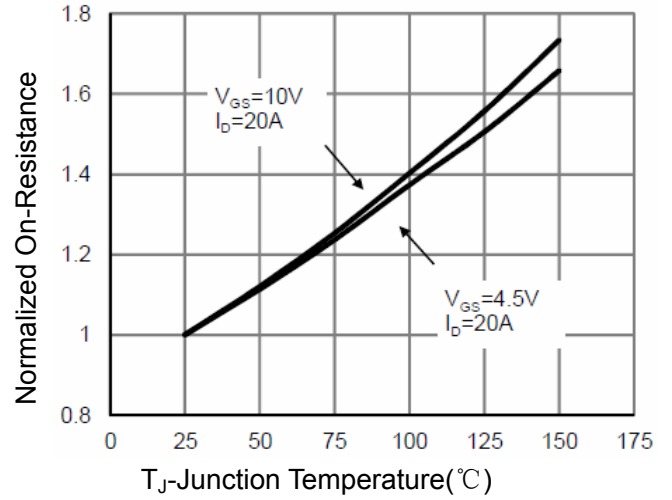


Figure 4 Rdson-Junction Temperature

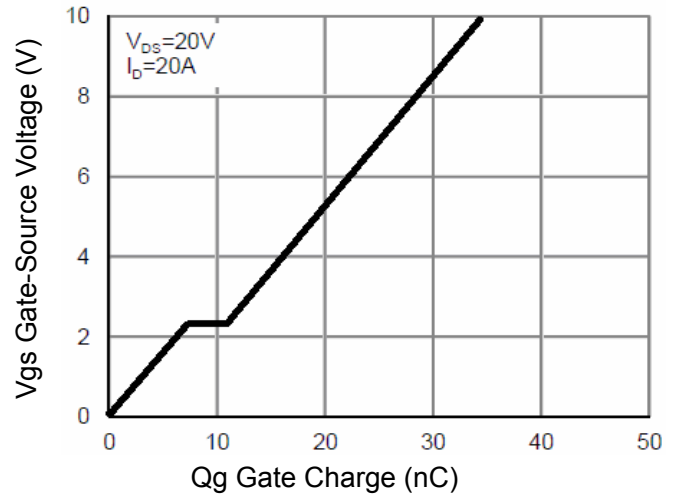


Figure 5 Gate Charge

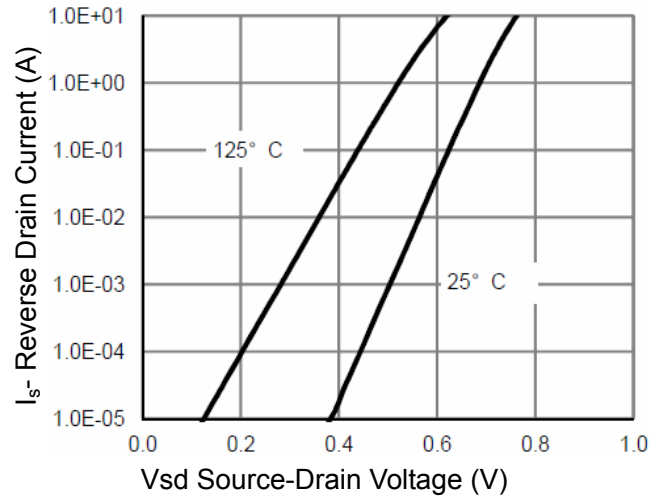


Figure 6 Source- Drain Diode Forward

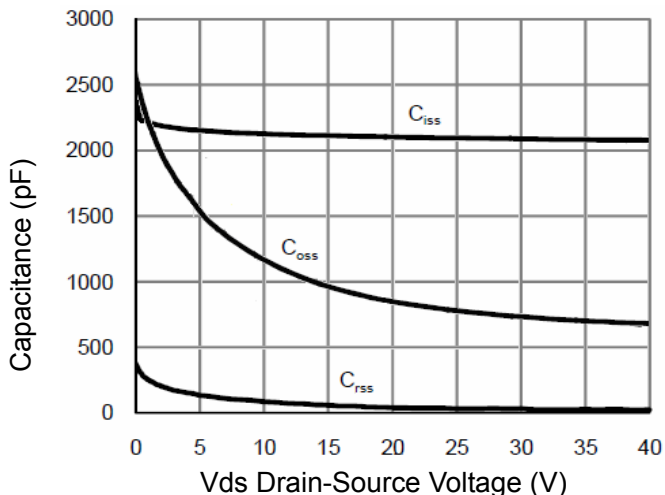


Figure 7 Capacitance vs Vds

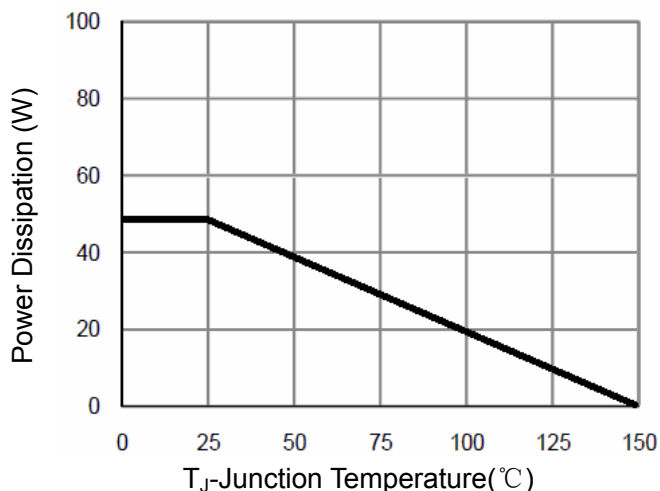


Figure 9 Power De-rating

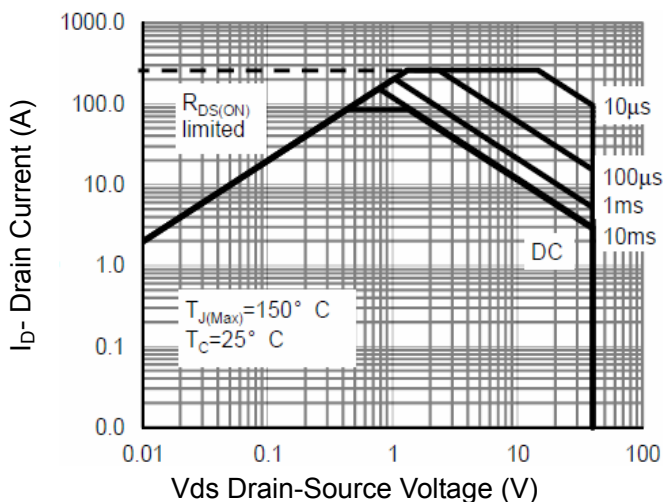


Figure 8 Safe Operation Area

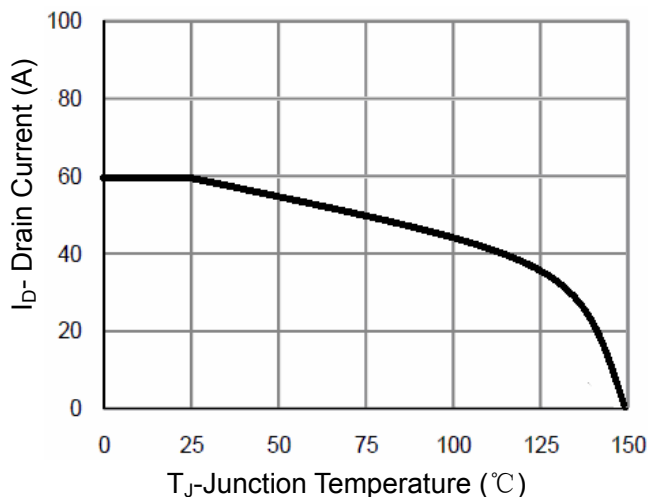


Figure 10 Current De-rating

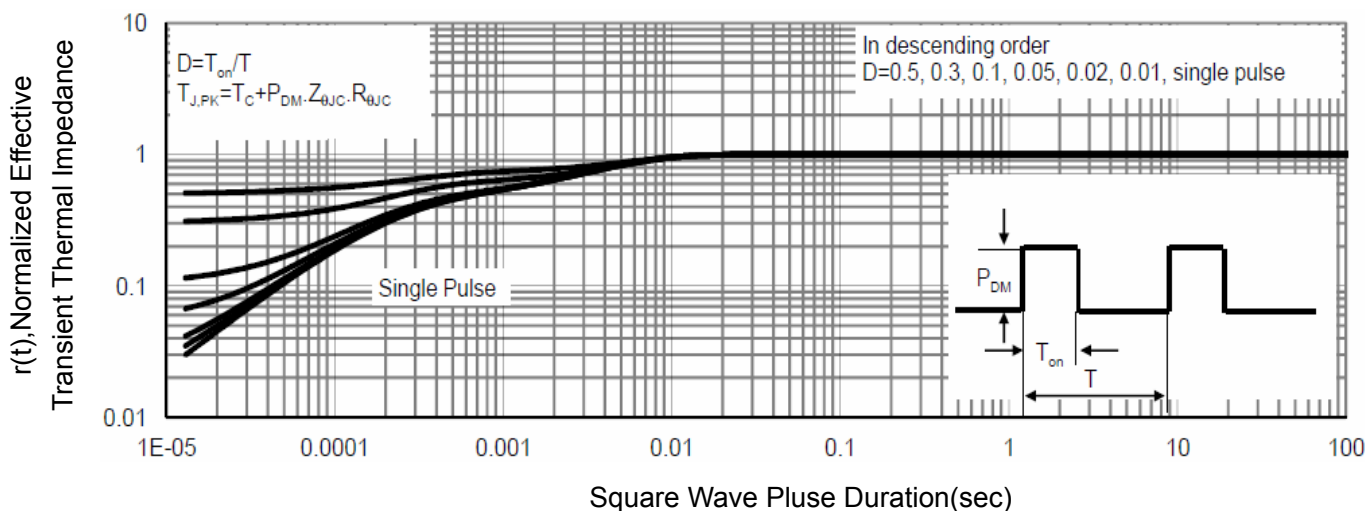
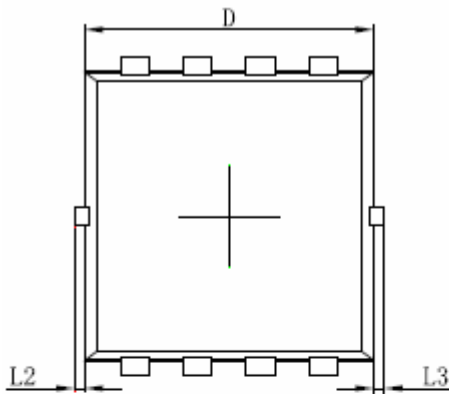
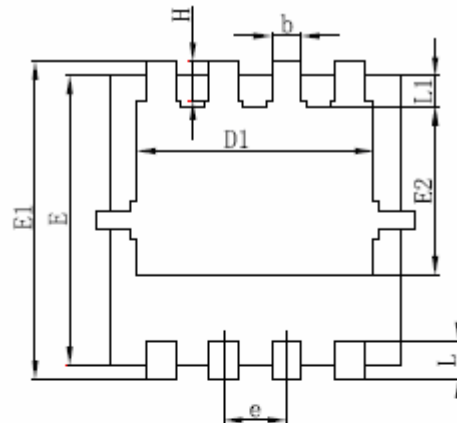


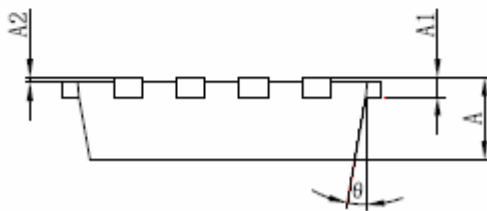
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information


Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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